FEATURES

GENERAL FEATURES

- **Three independent 3/1.5Gbps SATA ports.**
- **Connects 2 host ports to 1 device port.**
- **Supports 3/1.5Gbps rate detection/speed negotiation.**
- **Supports power down modes - Active, partial, slumber and power down.**
- **Advanced features configurable through MDIO bus.**

PORT MULTIPLIER/SELECTOR LOGIC FEATURES

- **Low latency architecture.**
- **Supports OOB signaling for SATA applications. Internal OOB detectors for COMRESET/ COMINIT and COMWAKE.**

HIGH SPEED I/O FEATURES

- **High speed outputs with programmable pre-emphasis to drive long interconnects.**
- **Selectable high speed input equalization for optimum reception.**
- **Compliant with SATA Gen-2i & Gen-2m specification.**
- **Enables reliable data transmission over 1 meter of FR-4 and 4 meters or more of unequalized copper cable.**
- **Supports spread spectrum clocking (SSC) to reduce EMI.**

PHYSICAL FEATURES

- **CMOS 0.13 Micron Technology**
- **Single 1.2 V Power Supply**
- **-40℃ to 85℃ Industrial Temperature Range**
- **No heatsink or airflow required**
- **64-QFN and 100-Pin LQFP Package**

1.0 INTRODUCTION

The XRS10L210 is a Serial ATA II Port Selector at 3.0 Gbps and 1.5 Gbps. It provides a failover path from two independent hosts to a single SATA drive and offers a leading solution for propagation of high data rate Serial ATA products in a wide variety of applications. The integration of Serial ATA PHY links, a variety of digital logic capabilities, rate adjust FIFOs, integrated low-cost clock oscillator support, test and loopback features is achieved in a low cost and lower power implementation.

The port selector function is used when dual hosts, such as I/O controllers, must access single-port disk drives in high availability storage subsystems where redundancy and load sharing are important. The outputs from the I/O controllers are multiplexed to a Serial ATA drive through the port selector block of the XRS10L210. Active/passive port selector in XRS10L210 allows two different host ports to connect to the same target in order to create a redundant path to that target. In combination with RAID, the XRS10L210 allows system providers to build fully redundant solutions. This avoids the presence of a single point of failure, and enables a fail-over path in the case of host failure.

The XRS10L210 includes enhanced features such as staggered HDD spin-up, power management control, hot plug capability and support for legacy software. The XRS10L210 acts as a retimer, maintaining independent signaling domains between the drives, hosts and the external interconnect.

The high-speed serial input feature: selectable equalization adjustment and the high-speed serial output feature: programmable pre-emphasis can be used to compensate for ISI (Inter-Symbol Interference) and increase maximum cable distances.

XRS10L210 meets tight jitter budgets in SATA applications. Exar's serial I/O technology enables reliable data transmission over 1 meter of FR-4 and 4 meters of unequalized copper cable.

Host and drive port speeds can be mixed and matched, based upon inherent data rate negotiation present in the SATA II specifications.

The MDIO bus allows simple configuration of the XRS10L210 when needed. Receive equalization, transmit amplitude and pre-emphasis and SSC control are all configurable via the 2-wire MDIO interface.

To summarize, the port selector functionality in the XRS10L210 allows replacement for expensive Fibre Channel drives with cost effective and high capacity SATA drives in enterprise class applications without compromising on redundancy or performance.

STANDARDS COMPLIANCE

The XRS10L210 is compliant with the following industry specifications:

- Serial ATA, Revision 1.0a
- Serial ATA II: Extensions to Serial ATA 1.0a, Revision 1.2
- Serial ATA II PHY Electrical Specifications, Revision 1.0
- Serial ATA II: Port Selector, Revision 1.0
- Serial ATA II: Revision 2.6

APPLICATIONS

- Serial ATA Enclosures
- Other Serial ATA link replicator applications
- Buffers for externally connected links
- High density storage boxes
- RAID Subsystems

APPLICATION EXAMPLE

The XRS10L210 is ideally suited for use within an external drive enclosure as a means of providing redundant host access to ensure system availability and reliability. This application is shown in **Figure 1**. The XRS10L210 can be used in a combined SAS and SATA storage system. The mux is required in Active/ Active or Active/Passive fail over systems. In enterprise storage applications, Fibre Channel and SAS drives are known for a dual port architecture where commands can be sent to either port by different hosts or the same host. The dual ported drive allows two different RAID controllers to access the same drive. The major advantage of this architecture is that it provides systems with fail-over capability. These storage systems allow components of the systems to be changed or serviced while the IO is running. SATA drives are being deployed in the enterprise systems where they lack dual port capability. The lack of dual port SATA drives can be compensated for by using the XRS10l210 in which single port SATA drives can be converted into dual ported drives.

Other applications for the XRS10L210 are in dual ported SAS/STP expanders, NAS servers, high availability, high density storage sub-systems and tape emulation market where SATA drives are used as the storage media.

FIGURE 1. SYSTEM BLOCK DIAGRAM FOR XRS10L210 IN A DRIVE ENCLOSURE APPLICATION

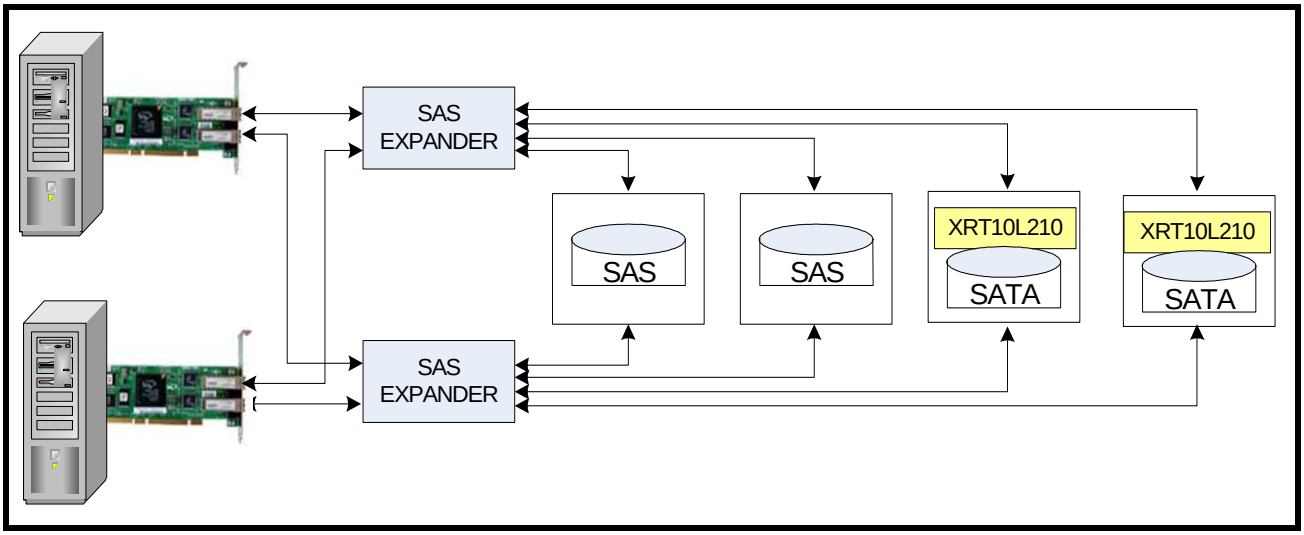
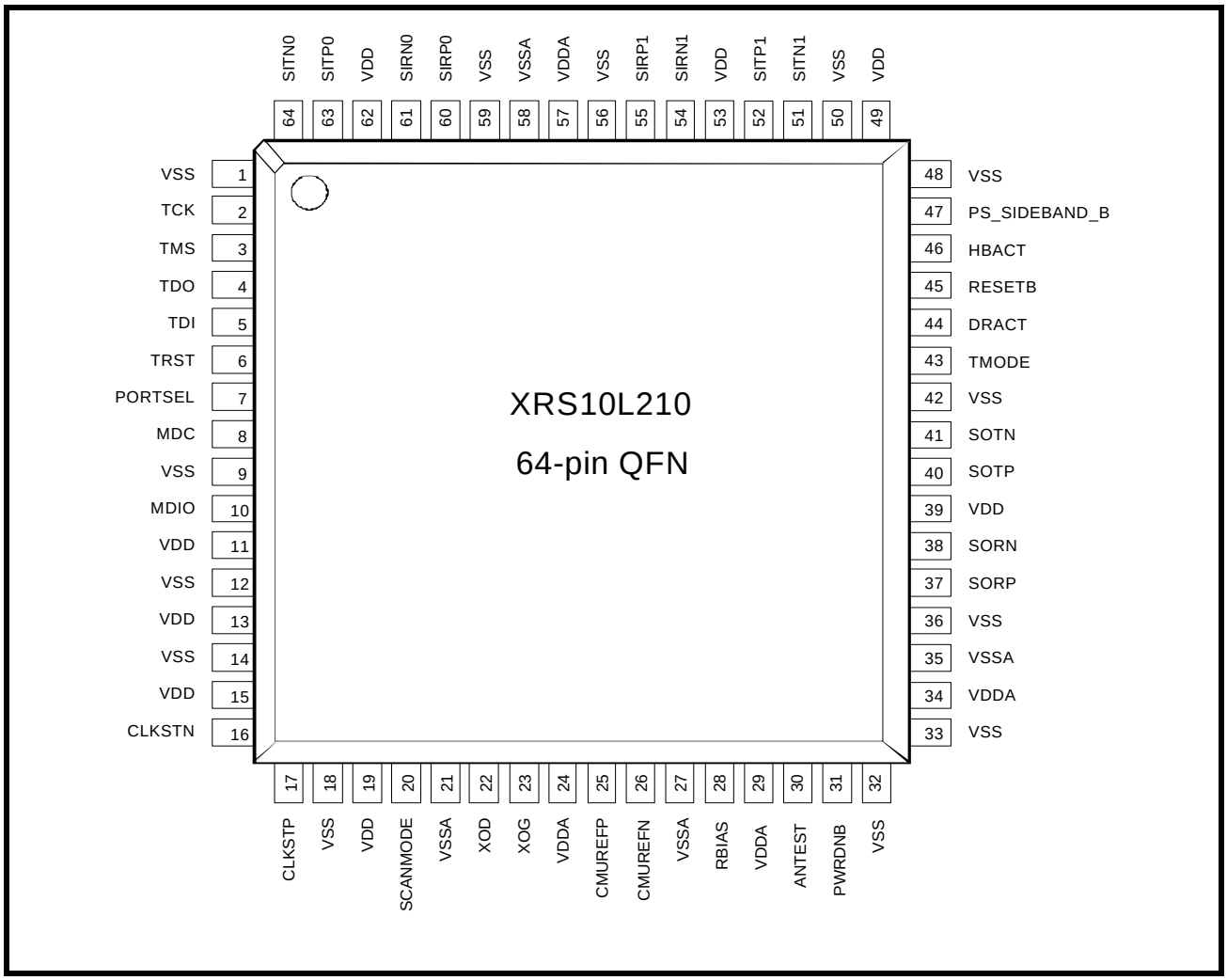
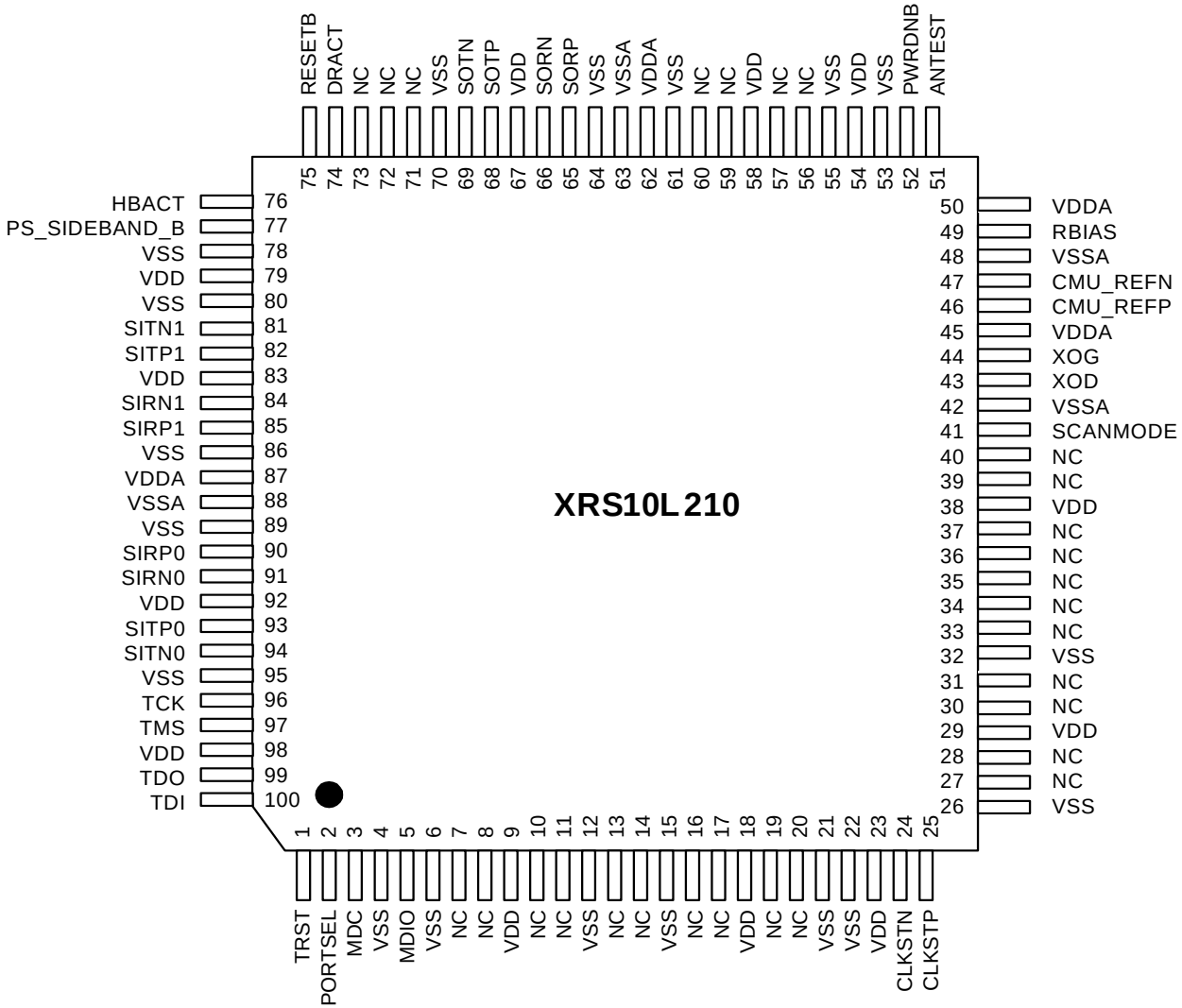


FIGURE 2. PINOUT OF THE XRS10L210 - 64 PIN QFN (NOTE 1)



NOTE: *1) 64 Pin QFN Pin out PRELIMINARY*

FIGURE 3. PINOUT OF THE XRS10L210 - 100 PIN LQFP



2.0 PIN DESCRIPTIONS

TABLE 1: XRS10L210 PIN DESCRIPTIONS

PIN NAME	LQFP 100 PIN NUMBER	QFN 64 PIN NUMBER (NOTE 1)	I/O	TYPE	DESCRIPTION
DATA INTERFACE					
SOTP/SOTN	68, 69	40. 41	O	CML AC Coupled	Serial ATA Output Transmitters. These ports communicate from the XRS10L210 to downstream devices
SORP/SORN	65, 66	37, 38	I		Serial ATA Input Receivers. These ports receive signals from downstream devices
SITP0/SITN0	93, 94	63, 64	O		Serial ATA Output Transmitters. These ports communicate from the XRS10L210 to upstream hosts.
SITP1/SITN1	82, 81	52, 51			
SIRP0/SIRN0	90, 91	60, 61	I		Serial ATA Input Receivers. These ports receive signals from upstream hosts.
SIRP1/SIRN1	85, 84	55, 54			
CLOCK INTERFACE					
CMU_REFP/ CMU_REFN	46, 47	25, 26	I	CML AC Coupled	Reference clock input
XOD	43	22	0	Analog	Crystal oscillator output
XOG	44	23	I	Analog	Crystal oscillator input, 1.26V max
MDIO INTERFACE SIGNALS					
MDC	3	8	I	LVCMOS	MDIO clock input, +3.3V LVCMOS
MDIO	5	10	I/O	LVCMOS	MDIO data port, +3.3V LVCMOS. Open drain
JTAG INTERFACE SIGNALS					
TCK	96	2	I	LVCMOS	JTAG test clock, +3.3V LVCMOS
TDI	100	5	I		JTAG test data in, +3.3V LVCMOS
TDO	99	4	O		JTAG test data out, +3.3V LVCMOS. Open drain If used to daisy chain JTAG devices, pull up externally using 3.3KOhm resistor.
TMS	97	3	I		JTAG mode select, +3.3V LVCMOS
TRST	1	6	I		JTAG test reset, +3.3V LVCMOS. Pull low externally using 3.3KOhm resistor for normal operation of the device.
GENERAL CONTROL AND CONFIGURATION SIGNALS (CMOS)					
RBIAS	49	28	I	Analog	Connection point for calibration termination resistor.
RESETB	75	45	I	LVCMOS	Active low reset pin, +3.3V LVCMOS.

TABLE 1: XRS10L210 PIN DESCRIPTIONS

PIN NAME	LQFP 100 PIN NUMBER	QFN 64 PIN NUMBER (NOTE 1)	I/O	TYPE	DESCRIPTION
PWRDNB	52	31	I	LVCMOS	Active low power down signal for chip, +3.3V LVCMOS.
DRACT	74	44	O	LVCMOS	Drive activity port for external LED. Active Low, 3.3V LVCMOS, open drain
HBACT	76	46	O	LVCMOS	0 = Host 0 selected (status) 1 = No host selected (status) 0-1-0-1 Toggle = Host 1 selected (1 sec stay at each state) 3.3V LVCMOS
PS_SIDEBAND_B	77	47	I	LVCMOS	+3.3V LVCMOS **Please refer to Table 2, "Host Port Selection," on page 8**
PORTSEL	2	7	I	LVCMOS	Port selector external input pin when this mode is set in the register. Low selects host port 0, otherwise port 1. +3.3V LVCMOS
TEST PIN					
ANTEST	51	30	O	Analog	Analog test pin
CLKSTN/ CLKSTP	24, 25	16, 17	O	CML AC Coupled	Output clock test pin
RESERVED PINS					
NC	7, 8, 10, 11, 13, 14, 16, 17, 19, 20, 27, 28, 30, 31, 33, 34, 35, 36, 37, 39, 40, 56, 57, 59, 60, 71, 72				No Connect - Do not connect this pin during operational use.
SCANMODE	41	20	I	LVCMOS	For factory use only, connect to ground.
TMODE	73	43			For factory use only, leave floating. Do not connect this pin during operational use.
POWER AND GROUND SIGNALS					

TABLE 1: XRS10L210 PIN DESCRIPTIONS

PIN NAME	LQFP 100 PIN NUMBER	QFN 64 PIN NUMBER (NOTE 1)	I/O	TYPE	DESCRIPTION
VDD	9, 18, 23, 29, 38, 54, 58, 67, 79, 83, 92, 98	11, 13, 15, 19, 39, 49, 53, 62	I		1.2V supply.
VDDA	45, 50, 62, 87	24, 29, 34, 57	I		1.2V Analog supply.
VSS	4, 6, 12, 15, 21, 22, 26, 32, 53, 55, 61, 64, 70, 78, 80, 86, 89, 95	1, 9, 12, 14, 18, 32, 33, 36, 42, 48, 50, 56, 59	I		Ground.
VSSA	42, 48, 63, 88	21, 27, 35, 58	I		Analog Ground.

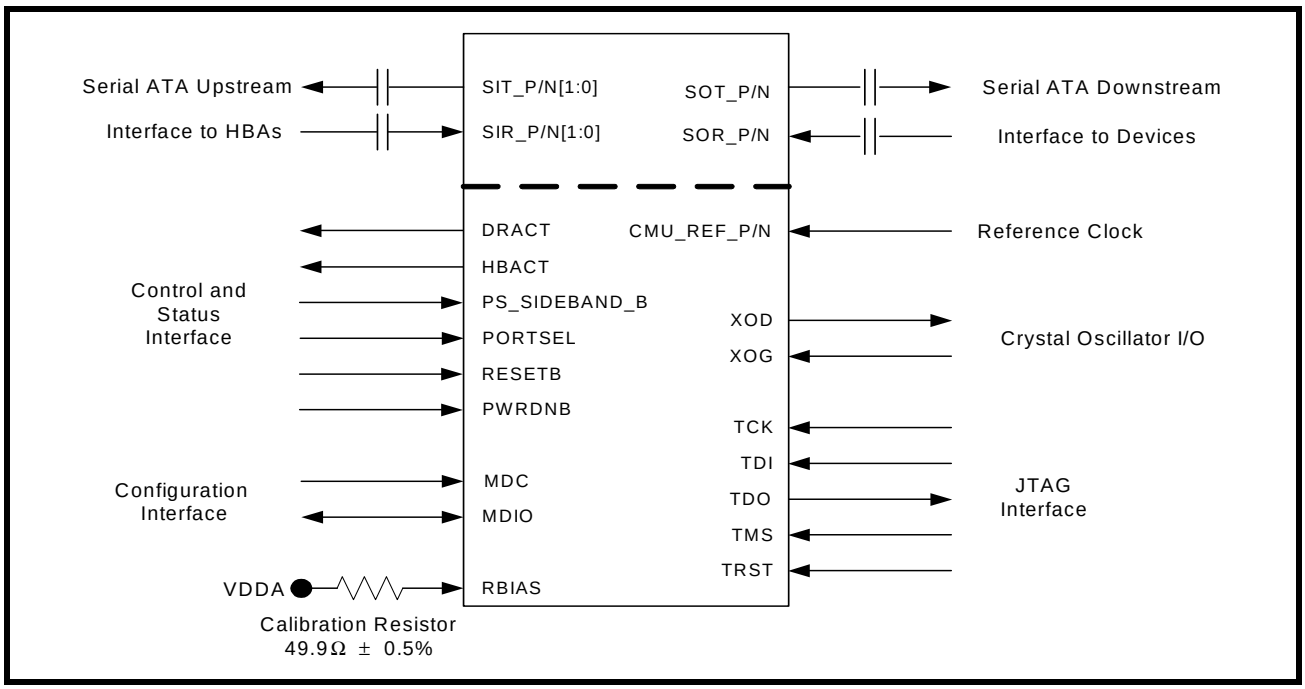
TABLE 2: HOST PORT SELECTION

HARDWARE PINS		REGISTER SETTINGS - REGISTER 0.009A			COMMENTS
PS_SIDEBAND_B PIN 77	PORTSEL PIN 2	P_SEL_MTHD BIT 0	P_SIDE_MTHD BIT 1	P_HOST_SEL BIT 2	3.3V LVCMOS
0	Selects host port 0 = Host port 0 1 = Host port 1	x	0	x	Host port is selected by hardware PORTSEL pin
x	Selects host port 0 = Host port 0 1 = Host port 1	1	0	x	Host port is selected by hardware PORTSEL pin
0	x	x	1	Selects host port 0 = Host port 0 1 = Host port 1	Host port is selected by register 0x0.009A bit 2
x	x	1	1	Selects host port 0 = Host port 0 1 = Host port 1	Host port is selected by register 0x0.009A bit 2
1	x	0	x	x	Host port is selected by protocol based selection

3.0 FUNCTIONAL DESCRIPTION

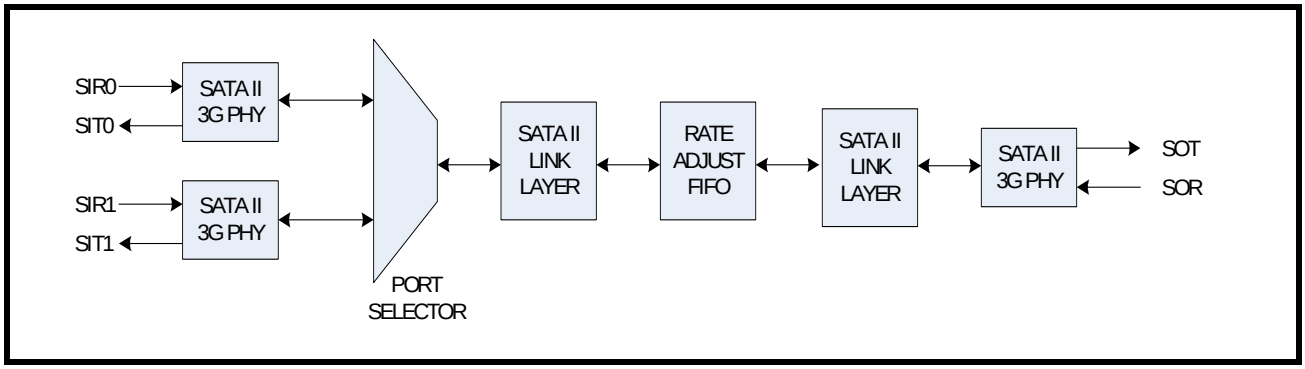
A top-level view of the XRS10L210 is shown in Figure 4 outlining the interfaces to the device and the required support components. The data path can be seen at the top of the device. This includes the two output transmit and input receive paths at the top left, providing the upstream interface to the host, and the two output transmit and input receive paths at the top right, providing the downstream interface to the target devices. The clocking, control, and configuration interfaces are shown below the dotted line.

FIGURE 4. XRS10L210 INTERFACES



The XRS10L210 incorporates identical instantiations of a dual-channel Serial ATA II 3 Gbps PHY macro. This common building block provides a uniform implementation with common characteristics and a common register map, but provides a functional implementation of independent PHY blocks. Digital logic implementations of Serial ATA link layer blocks along with port selector and port multiplier logic provide the remainder of the data path within the XRS10L210. In addition, management and control interfaces including an MDIO interface for register control, a JTAG interface for boundary scan purposes, and a resistor calibration circuit complete the device. A block diagram of the XRS10L210 is shown in Figure 5.

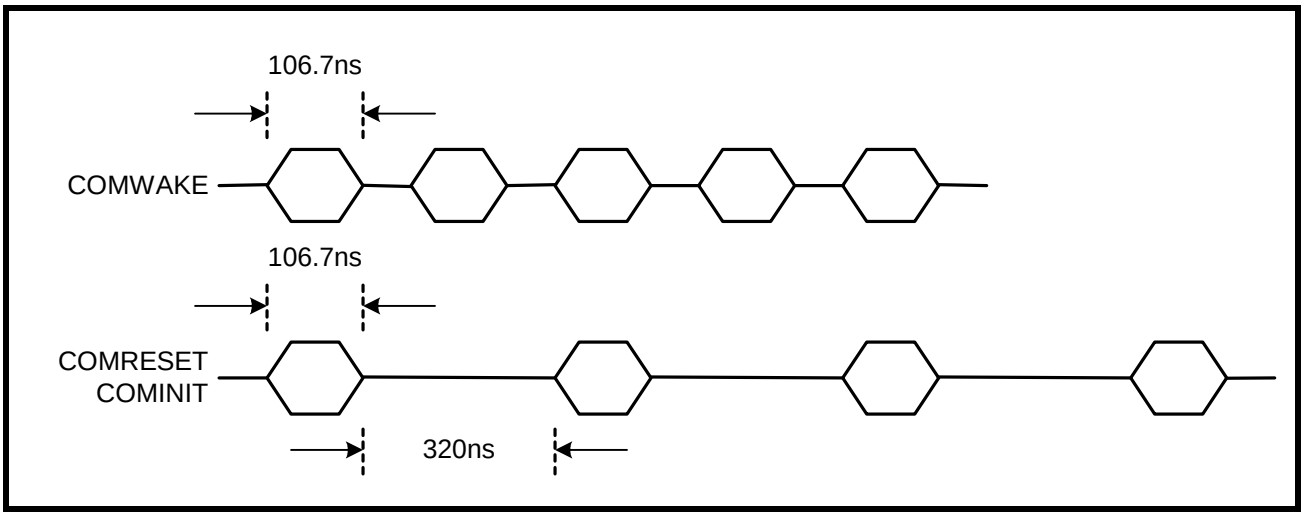
FIGURE 5. XRS10L210 BLOCK DIAGRAM



3.1 Out Of Band Feature

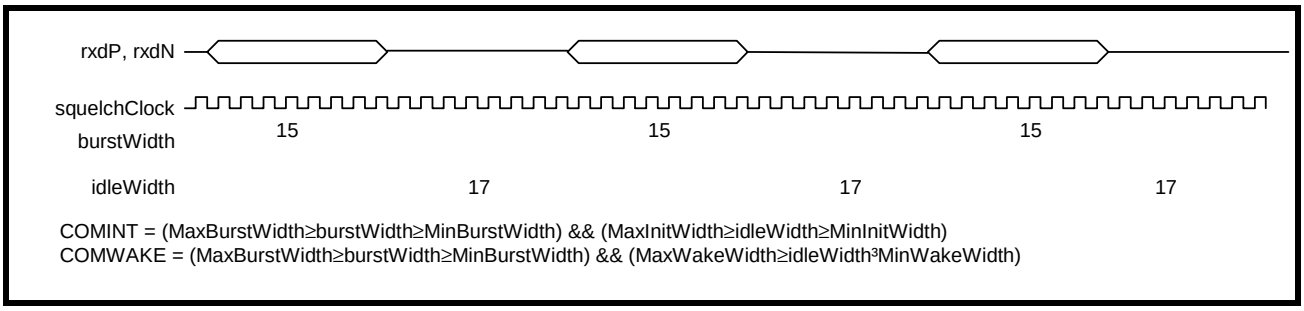
Each Serial ATA link provides full support for the three Out Of Band (OOB) signals supported by Serial ATA: COMRESET, COMINIT and COMWAKE. These sequences must be separated by idle periods as shown in Figure 6. The sequences are comprised of 106.7ns bursts of activity that are interleaved with varying length stretches of electrical idle. This alternating sequence must be repeated four times to be recognized.

FIGURE 6. COMWAKE AND COMRESET/COMINIT SEQUENCES



An example OOB sequence and the resulting burst and idle widths are shown in Figure 7. If the sequence of burstWidth and idleWidth counts falls within the range specified in the MDIO registers for four consecutive burst/idle sequences, then the link will assert COMINIT or COMWAKE. This OOB signal will remain asserted for as long as the corresponding sequence on the input pins continues.

FIGURE 7. EXAMPLE OOB SEQUENCE



3.2 Power Down Modes

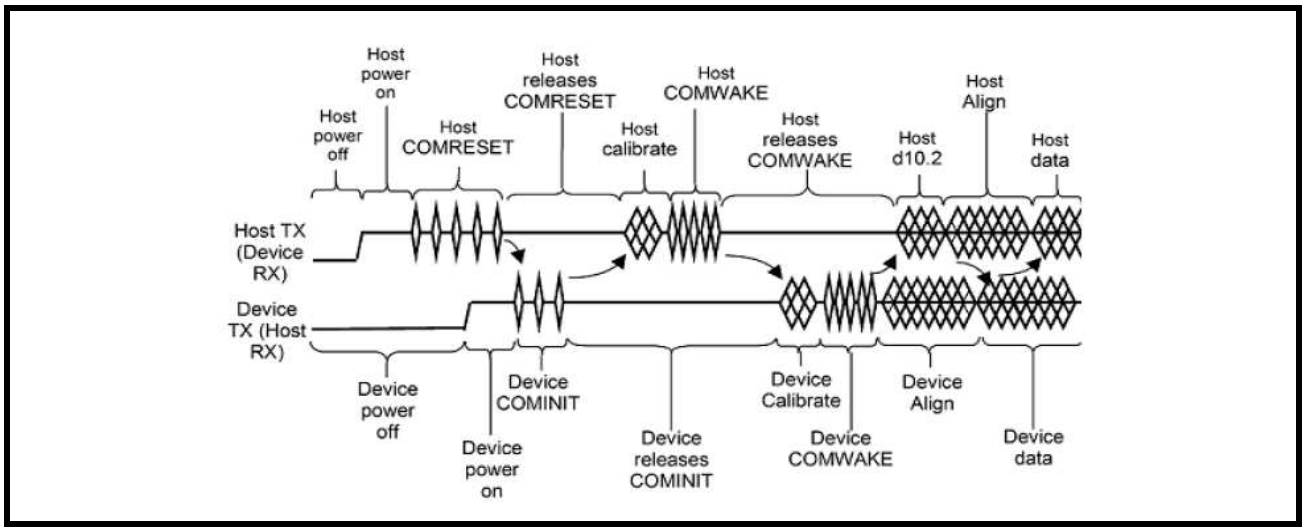
Each Serial ATA link within the XRS10L210 features independent support for 3 power modes via MDIO interface, as follows:

- Active: All parts of the link are active. All power-down signals are de-asserted.
- Partial: In partial mode, the input and output pipelines are shut down, but the PLL and the OOB generation circuits are active.
- Slumber: In slumber mode, the PLL is also shut down, saving additional power but adding latency on exit.

3.3 Speed Negotiation

The XRS10L210 will automatically perform speed negotiation with the host and devices in order to verify whether the second generation Serial ATA 3.0 Gbps data rate is available or whether the system will need to fall back upon the first generation Serial ATA 1.5 Gbps data rate. Speed negotiation is performed on an independent basis by each of the dual-channel macros. Speed negotiation is done independently on all host and device ports by default. MDIO configuration can request a common negotiated speed on the host and device ports if such a speed exists. To perform speed negotiation with a downstream device, the XRS10L210 will first perform a COMRESET/COMINIT handshake with the device and then performs a calibrate/ COMWAKE handshake. Following receipt of the device COMWAKE signal, the XRS10L210 will continually send out a D10.2 signal while awaiting receipt of the device ALIGN primitive. Depending on the speed of the ALIGN primitive, the XRS10L210 will be able to determine the PHY generation of the device, and provide the appropriate 1.5 Gbps or 3.0 Gbps ALIGN primitive in return to the device, thus completing speed negotiation. This process is outlined in **Figure 8**.

FIGURE 8. SERIAL ATA SPEED NEGOTIATION



For speed negotiation with an upstream host, after the COMRESET/COMINIT and COMWAKE handshake is complete, the XRS10L210 will initially send out an ALIGN primitive at the 2nd generation 3.0 Gbps data rate. If no confirming 3.0 Gbps ALIGN primitive is received from the host, the XRS10L210 will then step down and attempt negotiation at the lower 1.5 Gbps data rate.

3.4 Port selector Implementation

The XRS10L210 provides full support for the Serial ATA II Port Selector specification. A Serial ATA Port Selector is a mechanism that allows two different host ports to connect to the same device in order to create a redundant path to that device. Only one host connection to the device is active at a time.

The two host ports are responsible for coordination of access to the XRS10L210 by one of two separate means: protocol-based port selection or sideband port selection. Each method is described in detail in the next two sections.

3.4.1 Protocol Based Port Selection

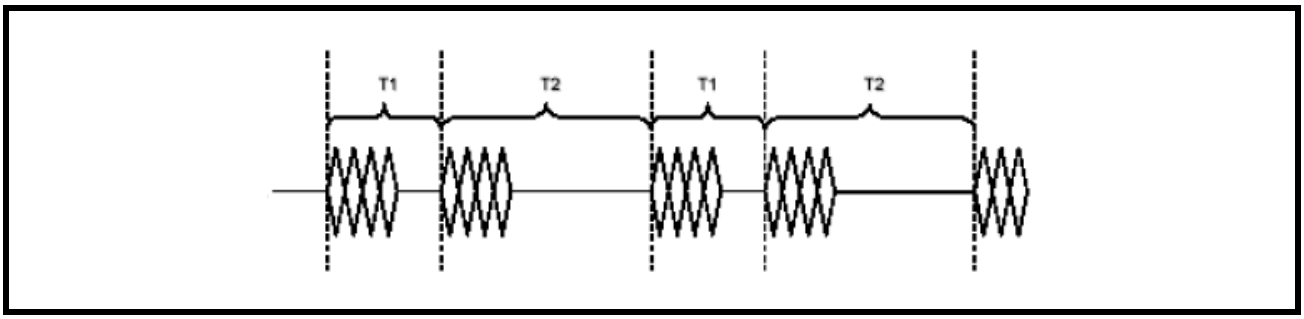
Protocol-based port selection makes use of a sequence of Serial ATA OOB signals to select the active host port. The port selection signal is based on a pattern of COMRESET OOB signals transmitted from the host to the XRS10L210. The port selection signal is composed of a series of COMRESET signals with the timing from one COMRESET signal to the next as shown in **Table 3** and **Figure 9**. The XRS10L210 selects the port, if inactive, on the de-assertion of COMRESET after receiving two complete back-to-back sequences with this defined inter-burst spacing. This can also be identified as two sequences of two COMRESET intervals comprising a total of five COMRESET bursts with four inter-burst delays. Once a port is designated as active, reception of additional COMRESET signals is propagated directly to the device, even if the COMRESET signals constitute a port selection signal.

Note that when protocol based selection mode has been enabled, following the initial hardware reset, a single COMRESET burst will select the active host port. After this intial host port selection, only COMRESET OOB observing the protocol timing given below will change the active host.

TABLE 3: PORT SELECTOR SIGNAL INTER-RESET TIMING REQUIREMENTS

	NOMINAL	MIN.	MAX	UNITS	COMMENTS
T1	2.0	1.6	2.4	ms	Inter-reset assertion delay for first event of the selection sequence
T2	8.0	7.6	8.4	ms	Inter-reset assertion delay for second event of the selection sequence

FIGURE 9. PORT SELECTION SIGNAL - TRANSMITTED COMRESET SIGNALS



3.4.2 Sideband Based Port Selection

The XRS10L210 also features support for a sideband port selection mechanism. This is implemented using a combination of the MDIO register settings and device pins including PS_SIDEBAND_B and PORTSEL. Refer to **Table 2** for sideband port selection settings.

3.5 Clocking

The XRS10L210 allows the use of either an external reference clock or of a low cost crystal oscillator to act as a reference clock. Separate device inputs are available for each approach, with full rate reference clock inputs provided on pins CMU_REFP and CMU_REFN, and crystal oscillator inputs provided on pins XOD and XOG. Supported data rates and their appropriate PLL divide factors are outlined in Table 4.

TABLE 4: PLL DIVIDE FACTORS

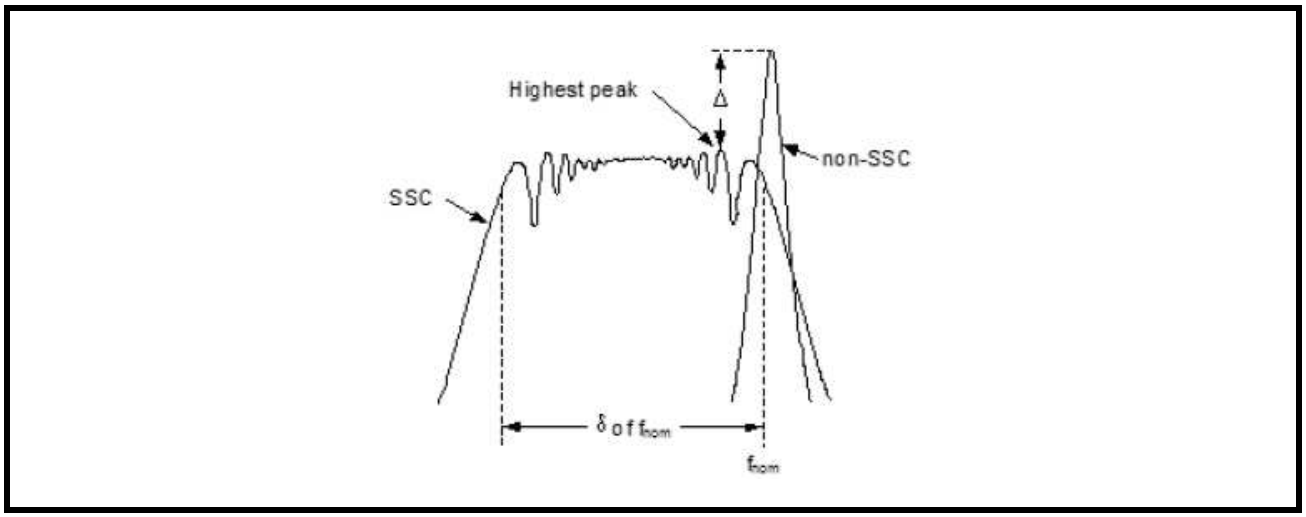
MODE	SYSCLK	/REF	/FB	DINCLK RXCLK	SERIAL CLOCK	DATA RATE
SATA Gen. 2	25MHz	1	60	300MHz	1.5GHz	3.0Gbps
SATA Gen. 2	50MHz	1	30	300MHz	1.5GHz	3.0Gbps
SATA Gen. 2	75MHz	1	20	300MHz	1.5GHz	3.0Gbps
SATA Gen. 2	100MHz	2	30	300MHz	1.5GHz	3.0Gbps
SATA Gen. 2	150MHz	1	10	300MHz	1.5GHz	3.0Gbps

NOTE: ** All link start with 3.0Gbps, then negotiate down to 1.5Gbps for SATA Generation 1 devices.*

3.5.1 Spread Spectrum Clocking

The XRS10L210 provides full support for receipt and generation of signals that have been configured for Spread Spectrum Clocking (SSC) support. The spread technique is implemented by down-spreading the data rate by 0.5% as a means of reducing EMI. Generation of the down-spread clock is performed within the XRS10L210. An example of the resultant spectral fundamental frequency before and after SSC can be seen in Figure 10.

FIGURE 10. SPREAD SPECTRUM CLOCKING



4.0 ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications for the XRS10L210.

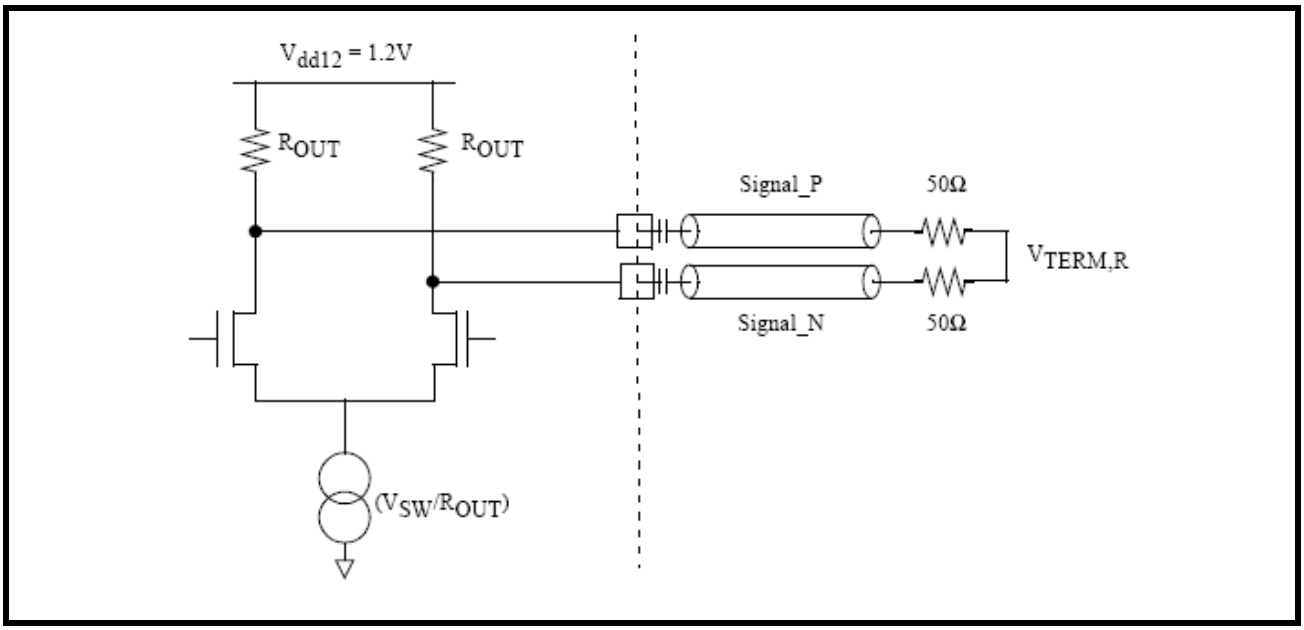
4.1 Serial ATA Specifications

The XRS10L210 electrical transmit and receive specifications are outlined in this section. The XRS10L210 is fully compliant to the Serial ATA II specification for Gen2i, Gen2x, Gen2m, Gen1i, Gen1x and Gen1m variations at 3.0 and 1.5 Gbps.

4.1.1 Serial ATA Transmitter

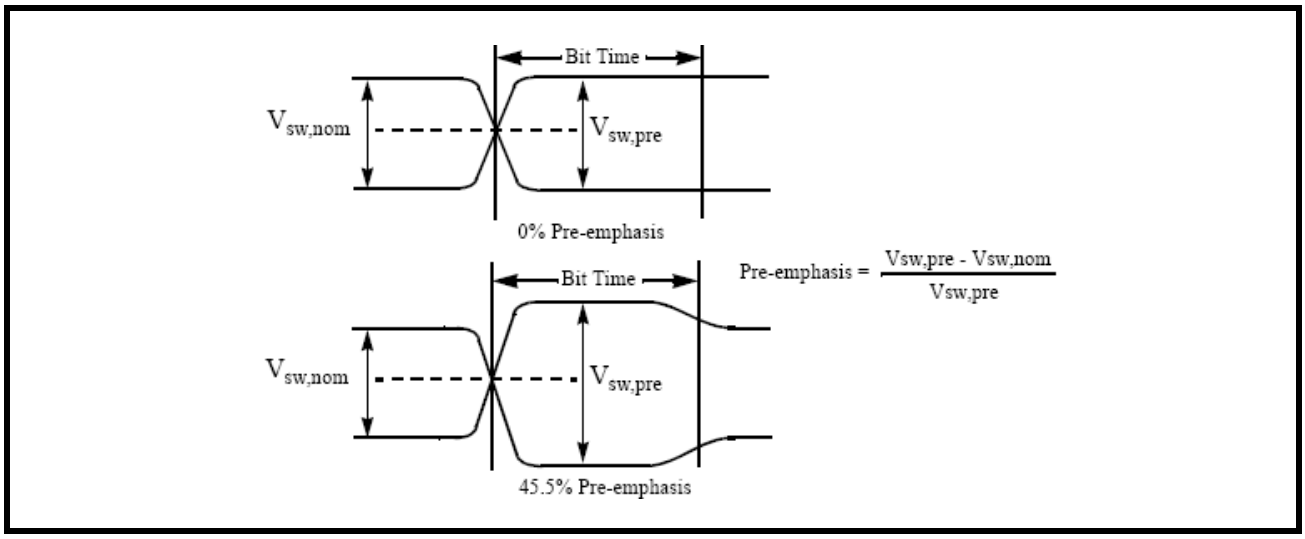
A simplified version of the output circuit and test fixture for each of the 3 Serial ATA transmit output pairs on the XRS10L210 is shown in **Figure 11**. The output differential pair is terminated to the supply VDD. The circuit is designed to be AC coupled.

FIGURE 11. SERIAL ATA EQUIVALENT OUTPUT CIRCUIT



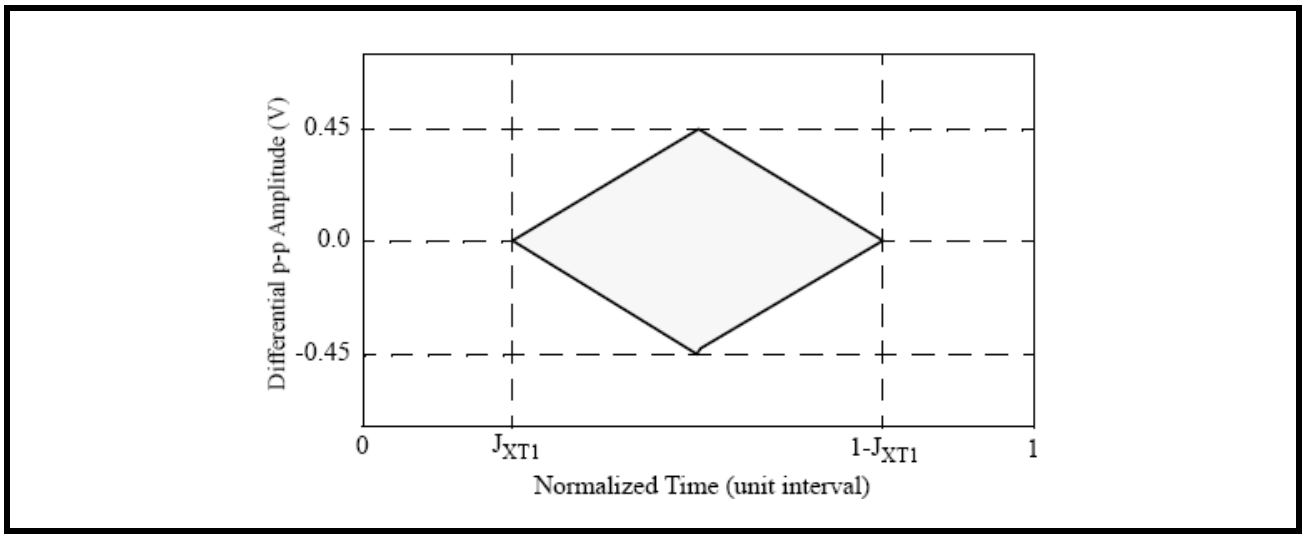
The XRS10L210 Serial ATA outputs include a simple one-tap equalizer, that is useful in driving longer printed circuit traces and is a required component in second generation Serial ATA PHYs. This equalizer pre-emphasizes the output signal whenever there is a data transition. The amount of pre-emphasis can vary between 0 and 45.5%, and is configured via MDIO register settings. Note that pre-emphasis doesn't increase the overall swing, but instead reduces the output amplitude when there is no transition.

FIGURE 12. EFFECTS OF TRANSMIT PRE-EMPHASIS



The overall swing level can also be modified via MDIO register settings. The XRS10L210 transmit mask is shown in **Figure 13**.

FIGURE 13. TRANSMIT EYE MASK FOR SERIAL ATA OUTPUT



4.1.2 Serial ATA Receiver

An equivalent circuit for the XRS10L210 Serial ATA inputs is shown in **Figure 14**. The device receiver mask is shown in **Figure 15**. This circuit is designed to be AC coupled. The termination resistors are not connected during power-up

FIGURE 14. SERIAL ATA EQUIVALENT INPUT CIRCUIT

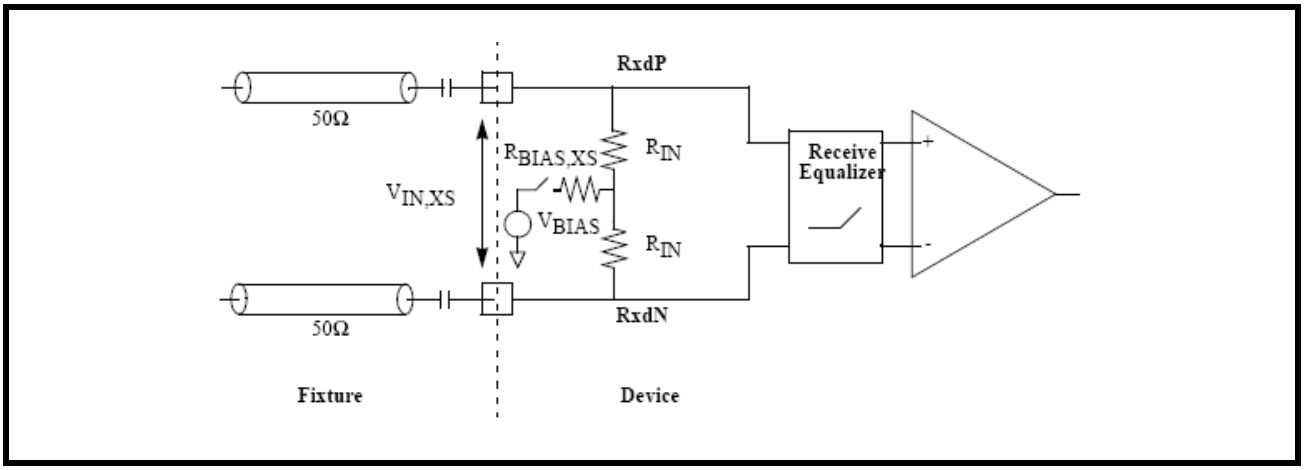


FIGURE 15. RECEIVE EYE MASK FOR SERIAL ATA INPUT

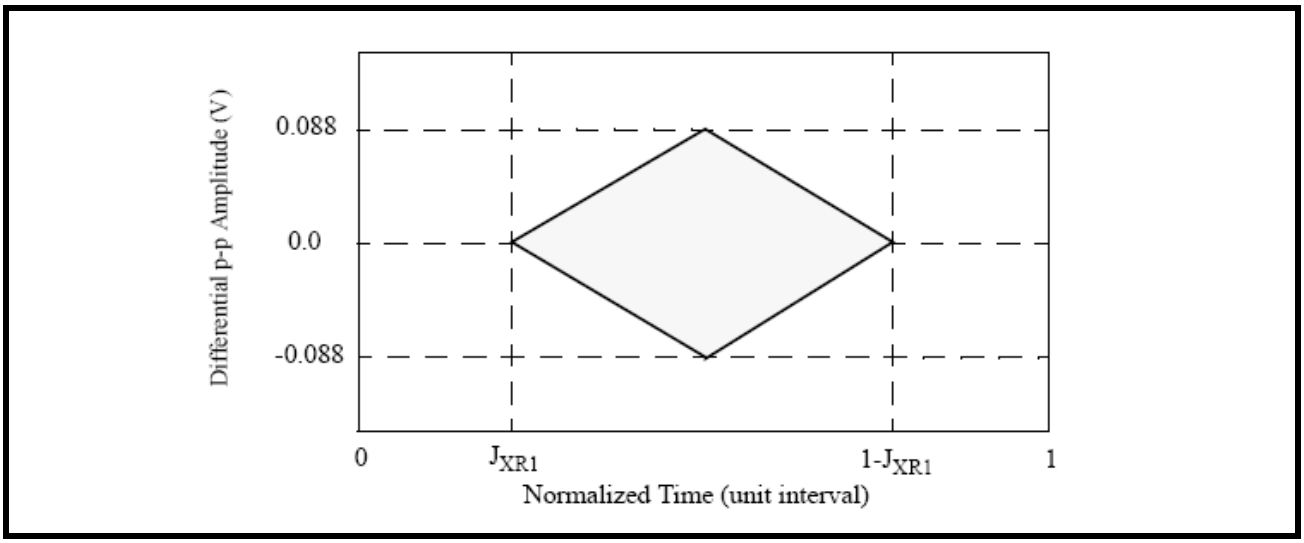


TABLE 5: SERIAL ATA LINK SPECIFICATIONS

NAME	DESCRIPTION	MIN.	NOM	MAX	UNITS
$t_{BIT,XS}$	Bit Time	670	-	333	ps
J_{XR1}	Input Jitter Tolerance Mask at signal crossover	0.32	-	-	UI
$J_{XR1,DJ}$	Deterministic jitter tolerance at signal crossover	0.18	-	-	UI
J_{XT1}	Output jitter mask at signal crossover	-	-	0.15	UI
$J_{XT1,DJ}$	Deterministic output jitter at signal crossover	-	-	0.07	UI
t_R/t_F	Input signal rise/fall times (20% - 80%)	0.2	-	0.46	UI
t_{QR}/t_{QF}	Output signal rise/fall times (20% - 80%)	0.2	-	0.41	UI
$t_{TOL,RX}$[1]	RX to sysclock frequency offset tolerance	-5350	0	350	ppm
V_{IN}	Input swing, differential peak-peak	175	-	1600	mV
V_{SW}[2]	Output swing, differential peak-peak	800	-	1200	mV
$V_{IN,IDLE}$	No swing detection threshold	65	120	155	mV
$R_{IN,DIFF}$	Differential mode input resistance	85	100	115	Ω
$R_{IN,CM}$[3]	Common mode input resistance	40	50	60	Ω
$R_{IN,OFF}$	Common mode input resistance, no power	200	-	-	kΩ
$R_{IN,XS}$	Output termination resistance	40	50	60	Ω
$S_{11,IN,DIFF}$	Differential input return loss, 50MHz - 1.5GHz	12	-	-	dB
$S_{11,IN,CM}$	Common mode input return loss 50MHz-1.5GHz	6	-	-	dB
$S_{22,OUT,DIFF}$	Differential output return loss 50MHz-1.5GHz	12	-	-	dB
$S_{22,OUT,CM}$	Common mode output return loss 50MHz-1.5GHz	6	-	-	dB
$t_{S,REG}$	Setup time for register port	1.5	-	-	ns
$t_{H,REG}$	Hold time for register port	1.5	-	-	ns
$t_{Q,REG}$	Clock to Q time for register port	0	-	2	ns
$t_{CYC,REG}$	Register port clock cycle time	10	-	-	ns
$t_{HI,REG}$	R register port clock high time	4	-	-	ns
$t_{LO,REG}$	Register port clock low time	4	-	-	ns
$t_{RF,REG}$	Register port input rise/fall time	-	-	0.5	ns

NOTES:

1. *This value includes 0.5% downspread Spread Spectrum clocking, plus 350ppm tolerance around the center frequency.*
2. *This is measured at the package ball and does not include any board or connector loss.*
3. *This value can be as low as 5Ω during power on.*

4.2 CMOS Interface

AC and DC specifications for the CMOS inputs and outputs are listed in Table 6. Since all these signals are asynchronous, there are no setup or hold times defined. The CMOS pins are defined in the General Control and Configuration portion of Table 1 in Section 3, "Pin Descriptions".

TABLE 6: CMOS I/O SPECIFICATIONS

NAME	DESCRIPTION	MIN	NOM	MAX	UNITS
$t_{DR}/t_{DF,CMOS}$	CMOS input signal rise/fall times (20% - 80%)	0.2	-	5	ns
$t_{QR}/t_{QF,CMOS}$**1**	CMOS output signal rise/fall times (20% - 80%)	0.2	-	5	ns
$V_{IL,CMOS}$	CMOS input low voltage	-0.3	0	0.8	V
$V_{IH,CMOS}$	CMOS input high voltage	1.7	3.3	3.6	V
$V_{OL,CMOS}$	CMOS output low voltage	-0.3	0	0.4	V
V_{PULLUP}	Open Drain Pull-up Voltage	2.3		3.6	V
$I_{OL,CMOS}$	Output current for VOL = 0.4V	10	-	20	mA
$dI_{OL}/dt_{,CMOS}$	Output current rate of change	-10	-	10	mA/ns
$L_{I,CMOS}$	CMOS I/O inductance	-	-	8	nH
$C_{I,CMOS}$	CMOS I/O capacitance	-	-	5	pF
$I_{LEAKAGE}$**2**	CMOS I/O Leakage Current			150	uA

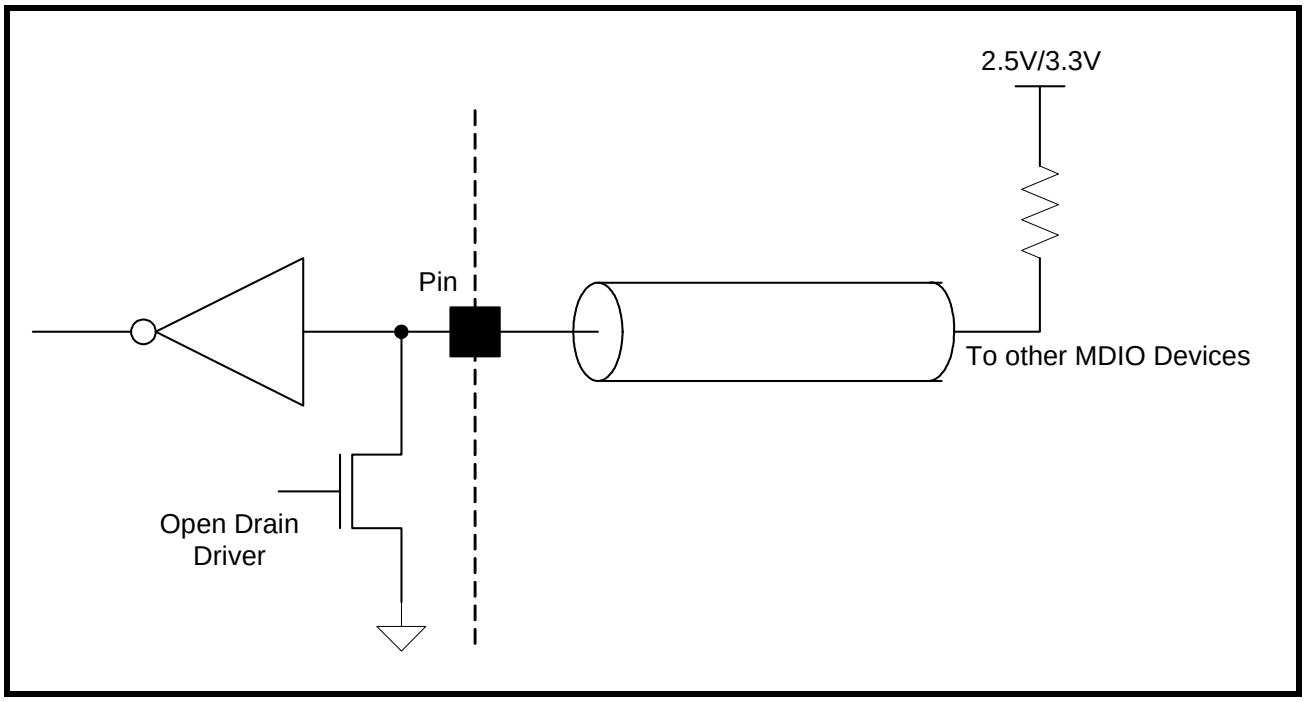
NOTE: *.1. This value is measured driving a load of 20pF.*

NOTE: *.2. This value is measured at 2.5 VDC.*

4.3 MDIO Interface

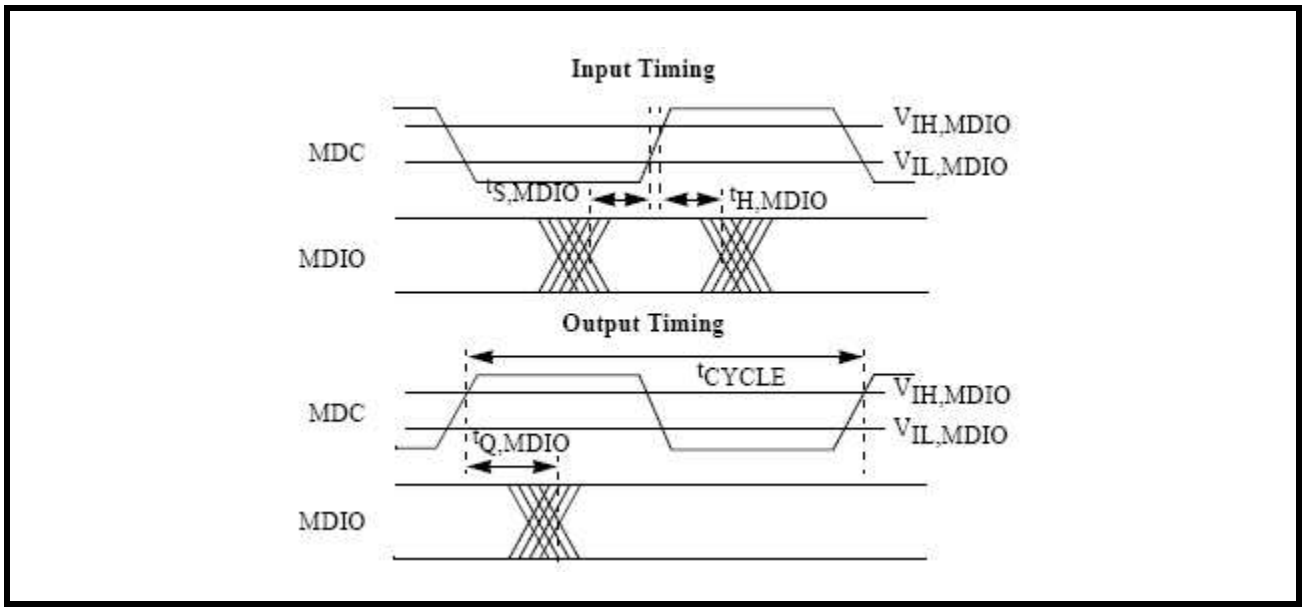
The Management Data Input/Output (MDIO) port complies with Clause 45 of the IEEE 802.3ae specification. A representative MDIO driver/receiver is shown in Figure 16. MDIO uses an open drain driver with a pullup resistor.

FIGURE 16. REPRESENTATIVE MDIO CIRCUIT



Representative MDIO Read and Write waveforms are shown in **Figure 17**. The XRS10L210 samples MDIO on the rising edge of MDC for input and drives MDIO after the rising edge of MDC for output. Note that setup, hold, and output timings are defined from the maximum V_{IL} and minimum V_{IH} levels.

FIGURE 17. MDIO INPUT AND OUTPUT WAVEFORMS



Values for MDIO parameters are shown in **Table 7**

TABLE 7: MDIO DC AND AC CHARACTERISTICS

NAME	DESCRIPTION	MIN	NOM	MAX	UNITS
$t_{CYCLE,MDIO}$	MDC cycle time	400	-	-	ns
$t_{LOW,MDC}$	MDC low time	160	-	-	ns
$t_{HIGH,MDC}$	MDC high time	160	-	-	ns
$t_{S,MDIO}$[1]	MDIO input to MDC setup time	10	-	-	ns
$t_{H,MDIO}$[2]	MDC to MDIO input hold time	10	-	-	ns
$t_{Q,MDIO}$[3]	MDC to MDIO output time	0	-	150	ns
$t_{DR}/t_{DF,MDIO}$	MDIO input signal rise/fall times (20% - 80%)	0.2	-	100	ns
$t_{QR}/t_{QF,MDIO}$[4]	MDIO output signal rise/fall times (20% - 80%)	0.2	-	80	ns
$V_{IL,MDIO}$	MDIO input low voltage	-0.3	0	0.8	V
$V_{IH,MDIO}$	MDIO input high voltage	1.7	3.3	3.6	V
$V_{OL,MDIO}$[4]	MDIO output low voltage	-0.3	0	0.4	V
V_{PULLUP}	Open Drain Pull-up Voltage	2.3		3.6	V
$I_{OL,MDIO}$	MDIO Output current for VOL = 0.4V	10	-	20	mA
$dI_{OL}/dt_{,MDIO}$	MDIO Output current rate of change	-10	-	10	mA/ns
$L_{I,MDIO}$	MDIO input inductance	-	-	8	nH
$C_{I,MDIO}$	MDIO input capacitance	-	-	5	pF

NOTES:

1. *Measured from minimum MDIO VIH to maximum MDC VIL for MDIO rising edge.*
   Measured from maximum MDIO VIL to maximum MDC VIL for MDIO falling edge.
2. *Measured from minimum MDC VIH to maximum MDIO VIL for MDIO rising edge.*
   Measured from minimum MDC VIH to minimum MDIO VIH for MDIO falling edge.
3. *Measured from minimum MDC VIH to maximum MDIO VIL for MDIO rising edge and MDC rising edge.*
   Measured from minimum MDC VIH to minimum MDIO VIH for MDIO falling edge and MDC rising edge.
   Measured from maximum MDC VIL to maximum MDIO VIL for MDIO rising edge and MDC falling edge.
   Measured from maximum MDC VIL to minimum MDIO VIH for MDIO falling edge and MDC falling edge.
4. *Measured driving a load of 470pF.*

TABLE 8: OPERATING CONDITIONS

Name	Description	Min	Nom	Max	Units
T_A	Ambient temperature under bias	-40	25	85	℃
V_{DD}	Core power supply voltage	1.14	1.2	1.26	V
I_{DD}	Core power supply current	-	300	400	mA

TABLE 8: OPERATING CONDITIONS

Name	Description	Min	Nom	Max	Units
V_{ESD1}	Electrostatic discharge tolerance, Human Body Model - Any pin with respect to any other pin except VDDA pins (pins 14, 34, 45, 50, 62, and 87)	-1400		1400	V
V_{ESD2}	Electrostatic discharge tolerance, Human Body Model - Any pin with respect to VDDA pins (pins 14, 34, 45, 50, 62, and 87)	-300		300	V
V_{ESD3}	Electrostatic discharge tolerance, Human Body Model - High speed IO pins (65, 66, 68, 69, 81, 82, 84, 85, 90, 91, 93, 94) with respect to VSS and VSSA pins when AC coupled to VDDA pins.	-2000		2000	V
θJA	Junction-to-ambient thermal resistance		38.5		^{0}C/W

5.0 REGISTER DESCRIPTIONS

The XRS10L210 provides a variety of registers for the purpose of device configuration, testing and monitoring. These registers are accessed through the MDIO interface, outlined in **"Section 4.3, MDIO Interface" on page 18**. Operational registers available to the customer are given below. Note that all other address space should be left unmodified in order to ensure proper behaviour of the device.

5.1 Register Overview

The XRS10L210 port address is hardwired to 0; this field should be set to 0 in all packets.The XRS10L210 contains two identical instantiations of a dual Serial ATA PHY macro. A common set of registers exists within each of these macros, and are outlined in **"Section 5.2, Macro Registers" on page 23**. MDIO device designations 1-2 are used for each of these macros as shown in **Table 9**. Registers relating to the XRS10L210 as a whole are outlined in **"Section 5.3, XRS10L210 Device Generic Registers" on page 28** and make use of MDIO device 0.

TABLE 9: MDIO DEVICE DESIGNATIONS

MDIO DEVICE DESIGNATION	MACRO	RELEVANT PINS
0	XRS10L210 Device Generic Registers	N/A
1	Serial ATA Input Macro	SI0, SI1
2	Serial ATA Output Macro 0	SO

The XRS10L210 registers are arranged as 8-bit fields with 8-bit addresses. These are mapped into the 16-bit MDIO address and data fields by setting the most significant byte of each to be 0. An example mapping from a macro address/data combination to an MDIO address & data combination is shown in **Table 10**.

TABLE 10: MDIO ADDRESSING

MACRO ADDRESS	MACRO DATA	MDIO ADDRESS	MDIO DATA
0x40	abcde	0x0040	00000000000abcde

NOTE: *The unused upper 3 bits in FBDIV are also set to 0 during MDIO writes and are undefined during MDIO reads.*

In the description of each register field, there is an entry describing its read/write status. This may fall into one of the following categories:

- RW- register field is read/write
- RO - register field is read only
- LL - Latching Low - Used with bits that monitor some state internal to the XRS10L210. When the condition for the bit to go low is reached, the bit stays low until the next time it is read. Once it is read, its value reverts to the cur-rent state of the condition it monitors.
- LH - Latching High - When the condition for the bit to go high is reached, the bit stays high until the next time it is read. Once it is read, its value reverts to the current state of the condition it monitors.
- SC - When an SC bit is set, some action is initiated; once the action is complete, the bit is cleared.

5.2 Macro Registers

The registers outlined in this section are common to each of the two Serial ATA dual PHY macros as described in the previous section. As such, each listed register is present in each of the 1, and 2 MDIO register spaces, and will perform the stated function on the specified Serial ATA lane.

The registers within each dual PHY macro are split into the following sections:

Transmit/Receive lane 0 registers:	Address range 000*****
Transmit/Receive lane 1 registers:	Address range 001*****
PLL registers:	Address range 010*****
Bias generator registers:	Address range 011*****

TABLE 11: TRANSMIT/RECEIVE LANE REGISTERS (MDIO DEVICE 1, 2)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRPTION
N.0000 N.0020	7	Reserved	RW	0	DO NOT MODIFY
	6	SATAPCIEXB_G1	RW	0	Tx output swing booster bit (Gen 1) 0 = boost swing by 15% 1 = nominal swing
	5:1	Reserved	RW	00001	DO NOT MODIFY
	0	SATAPCIEXB_G2	RW	0	Tx output swing booster bit (Gen 2) 0 = boost swing by 15% 1 = nominal swing
N.0001 N.0021	7:3	Reserved	RW	00000	DO NOT MODIFY
	2:0	Transmit_Eq0[2:0] Transmit_Eq1[2:0]	RW	011	Transmit pre-emphasis control 000 = 0% transmit preemphasis 001 = 6.5% transmit preemphasis 010 = 13% transmit preemphasis 011 = 19.5% transmit preemphasis 100 = 26% transmit preemphasis 101 = 32.5% transmit preemphasis 110 = 39% transmit preemphasis 111 = 45.5% transmit preemphasis

TABLE 11: TRANSMIT/RECEIVE LANE REGISTERS (MDIO DEVICE 1, 2)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRPTION
N.0002 N.0022	7:6 7:6	mscProg0[1:0] mscProg1[1:0]	RW	01	Receive equalization control – boost at 1.5GHz 00 = Lowest boost level 01 = 2nd boost level 10 = 3rd boost level 11 = Highest boost level
	5:3 5:3	Beacon_Swing0[2:0] Beacon_Swing1[2:0]	RW	100	Transmit swing size for OOB Signals 000 = 800mV 001 = 700mV 010 = 600mV 011 = 500mV 100 = 400mV 101 = 300mV 110 = 200mV 111 = 0mV
	2:0 2:0	Output_Swing0[2:0] Output_Swing1[2:0]	RW	100	Transmit swing size in normal operation 000 = 800mV 001 = 700mV 010 = 600mV 011 = 500mV 100 = 400mV 101 = 300mV 110 =200mV 111 = 0mV
N.0003 N.0023	7	enEqB	RW	0	Enable receive equalization 0 = enable equalization 1 = disable equalization
	6:0	Reserved	RW	0010000	DO NOT MODIFY
N.0015 N.0035	7	Reserved	RO	-	Reserved
	6:4	sysclk25divsel0[2:0] sysclk25divsel1[2:0]	RW	000	Divider selection for sysclk-> sysclk25 000 = divide by 1 (sysclk is 25MHz) 001 = divide by 2 (sysclk is 50MHz) 010 = divide by 3 (sysclk is 75MHz) 011 = divide by 4 (sysclk is 100MHz) 100 = divide by 5 (sysclk is 125MHz) 101 = divide by 6 (sysclk is 150MHz) 110 = divide by 10 (sysclk is 250MHz) 111 = divide by 12 (sysclk is 300MHz)
	3:0	Reserved	RW	0101	DO NOT MODIFY

TABLE 11: TRANSMIT/RECEIVE LANE REGISTERS (MDIO DEVICE 1, 2)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRPTION
N.0018 N.0038	7:3	Reserved	RW	00100	DO NOT MODIFY
	2:0	txbiasbuffsela0[2:0] txbiasbuffsela1[2:0]	RW	100	Tx Predriver swing size in normal operation 000 = 800mV 001 = 700mV 010 = 600mV 011 = 500mV 100 = 400mV (sata default) 101 = 300mV

TABLE 12: PLL CONFIGURATION (MDIO DEVICE 1, 2)

ADDRESS HEX	BIT(S)	NAME	TYPE	DEFAULT	DESCRIPTION
N.0040	7:6	Reserved	RO	-	Reserved
	5:0	FBDIV[5:0]	RW	101101	Divide value for feedback clock 110000 = divide by 5 100000 = divide by 10 100001 = divide by 15 100010 = divide by 20 100011 = divide by 25 100101 = divide by 30 100111 = divide by 50 101101 = divide by 60 (default for 25MHz Ref)) Other - reserved
N.0041	7:6	Reserved	RO	-	Reserved
	5:0	REFDIV[5:0]	RW	010000	Divide values for system clock 010000 = divide by 1 (default for 25MHz Ref)) 000000 = divide by 2 000001 = divide by 3 000010 = divide by 4 000011 = divide by 5 000101 = divide by 6 000110 = divide by 8 000111 = divide by 10 001101 = divide by 12 001110 = divide by 16 001111 = divide by 20 Others - reserved
N.0044	7:6	Reserved	RO	-	Reserved
	5:0	SSCMax	RW	00000	Maximum value for spread (set to 45, 0x2D when SSCBypass is set to '0')

TABLE 12: PLL CONFIGURATION (MDIO DEVICE 1, 2)

ADDRESS HEX	BIT(S)	NAME	TYPE	DEFAULT	DESCRIPTION
N.0045 NOTE 1	7:5		RO	-	Reserved
	4	SSCmode	RW	0	Selects position of spreading interpolator 0 = Interpolator in feedback path 1 = Interpolator in feedforward path (Set to '1' when SSCBypass = '0')
	3	Reserved	RW	0	DO NOT MODIFY
	2	SSCInvert	RW	0	Inverting SSC profile - Setting for downspread per SATA spec Set to '0' when SSCmode = '0' Set to '1' when SSCmode = '1'
	1	Reserved	RW	0	DO NOT MODIFY
	0	SSCBypass	RW	1	Bypass the saw generator and pulse density modulator and get increment from SSCMax (set SSCMax to 45 [0x2D] when SSCBypass is set to 0)

NOTE: *1) In order to enable SSC generation, set register N.0044 to 0x2D, N.0045 to 0x14 and then reset the PLL by writing register 0.0004 to 0x0 then 0xF.*

TABLE 13: POWERDOWN REGISTERS (MDIO DEVICES 1, 2)

ADDRESS HEX	BIT(S)	NAME	TYPE	RESET VALUE	DESCRIPTION
1.0080 2.0080	7:6	SIpwrdnDetB[1:0] SO01pwrdnDetB[1:0]	RW	11	Powers down the signal detector and COM* circuits 1 = normal operation 0 = power down
	5:4	SIpwrdnRxB[1:0] SO01pwrdnRxB[1:0]	RW	11	Powers down the receivers and CDR 1 = normal operation 0 = power down
	3:2	SIpwrdnTxDrvB[1:0] SO01pwrdnTxDrvB[1:0]	RW	11	Powers down the transmitter 1 = normal operation 0 = power down
	1:0	SIpwrdnTxB[1:0] SO01pwrdnTxB[1:0]	RW	11	Powers down the transmit pipes and clock 1 = normal operation 0 = power down
1.0081 2.0081	7:2	Reserved	RO	-	Reserved
	1	SIpwrdnBiasGen SO01pwrdnBiasGen	RW	0	Powers down the bandgap. 1 = power down 0 = normal operation
	0	SIpwrdnPLLB SO01pwrdnPLLB	RW	1	Powers down the PLL 1 = normal operation 0 = power down

TABLE 14: BIAS GENERATOR CONFIGURATION (MDIO DEVICE 1, 2)

ADDRESS HEX	BIT(S)	NAME	TYPE	RESET VALUE	DESCRIPTION
N.0064	7:4	pr100Tx[3:0]	RW	0x0	Transmit pre-driver current bias 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA 0111=175uA 1111=200uA
	3:0	Reserved[3:0]	RW	0x0	DO NOT MODIFY
N.0065	7:4	Reserved	RW	0x0	DO NOT MODIFY
	3:0	prcal100Tx[3:0]	RW	0x0	Transmit driver current bias 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA 0111=175uA 1111=200uA

5.3 XRS10L210 Device Generic Registers

This section outlines generic registers relating to the XRS10L210 as a whole. These registers are accessed through MDIO device 0.

TABLE 15: RESET CONTROL SIGNALS

ADDRESS HEX	BIT(S)	NAME	TYPE	RESET VALUE	DESCRIPTION
0.0004	3:0	resetPLLB_reg[3:0]	RW	0x0F	Resets the PLL portion of the macros 0x00 = PLL reset 0x0F = clears PLL reset
0.0030	7:0	revision_id[7:0]	R/O	0x01	Deivice Revision ID
0.0031	7:0	device_id [15:8]	R/O	0x83	Device ID MSB
0.0032	7:0	device_id [7:0	R/O	0x07	Device ID LSB

TABLE 16: SATA PORT SELECTOR REGISTERS

ADDRESS HEX	BIT(S)	NAME	TYPE	RESET VALUE	DESCRIPTION
0.009A	7:3	Reserved	RW	00100	DO NOT MODIFY
	2	p_host_sel	RW	0	Side band port selection 1 = Select Host port 1 0 = Select Host port 0
	1	p_side_mthd	RW	0	1 = p_host_sel based sideband selection 0 = external pin based sideband selection
	0	p_sel_mthd	RW	0	**Please refer to Table 2, "Host Port Selection," on page 8**

TABLE 17: PORT MULTIPLIER SATA STANDARD REGISTERS

REGISTER	BIT(S)	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
GSCR(0) Product Identifier	31 - 16	Device ID	R/O	0x8307	Device ID allocated by the vendor.
	15 - 0	Vendor ID	R/O	0x13A8	Vendor ID allocated by the PCI-SIG of the vendor that produced the Port Multiplier.
GSCR(1) Revision Information	31 - 16	Reserved	R/O	0x0000	31-16 Reserved
	15 - 8	REV_LEV	R/O	0x01	15-8 Revision level of the Port Multiplier.
	7:4	Reserved	R/O	0x0	7-4 Reserved
	3	PM_1,2	R/O	1	1=Supports Port Multiplier specification 1.2.
	2	PM_1.1	R/O	1	1=Supports Port Multiplier specification 1.1.
	1	PM_1.0	R/O	1	1=Supports Port Multiplier specification 1.0.
	0	Reserved	R/O	0	Reserved
GSCR(2) Port Information	7:4	Reserved	R/O	0x0	Reserved
	3 - 0	DEV_FAN_OUT_ PORTS	R/O	0x1	Number of exposed device fan-out ports.

TABLE 17: PORT MULTIPLIER SATA STANDARD REGISTERS

REGISTER	BIT(S)	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
GSCR(32) Error Information	31 - 15	Reserved	R/O	0x0	
	14	Reserved	R/O	0	Unused
	13	Reserved	R/O	0	Unused
	12	Reserved	R/O	0	Unused
	11	Reserved	R/O	0	Unused
	10	Reserved	R/O	0	Unused
	9	Reserved	R/O	0	Unused
	8	Reserved	R/O	0	Unused
	7	Reserved	R/O	0	Unused
	6	Reserved	R/O	0	Unused
	5	Reserved	R/O	0	Unused
	4	Reserved	R/O	0	Unused
	3	OR_PORT-3	R/O	0	OR of selectable bits in Port 3 PSCR[1] (SError)
	2	OR_PORT-2	R/O	0	OR of selectable bits in Port 2 PSCR[1] (SError)
	1	OR_PORT-1	R/O	0	OR of selectable bits in Port 1 PSCR[1] (SError)
	0	OR_PORT-0	R/O	0	OR of selectable bits in Port 0 PSCR[1] (SError)
GSCR(33) Error Information Bit Enable	31 - 0	ERR_INFO_EN	R/O	0x400FFFF	If set, bit is enabled for use in GSCR[32]
GSCR(64) Port Multiplier Revision 1.X Features Support	31 - 5	Reserved	R/O	0x0	Reserved
	4	PHY_EVENT	R/O	0	1 = Supports Phy event counters
	3	ASYNC	R/O	1	1 = Supports asynchronous notification
	2	SSC	R/O	0	1 = Supports dynamic SSC transmit enable
	1	$PMREQ_P$	R/O	1	1 = Supports issuing $PMREQ_P$ to host
	0	BIST	R/O	0	1 = Supports BIST
GSCR(96) Port Multiplier Revision 1.X Features Enable	31 - 4	Reserved	R/O	0x0	Reserved
	3	ASYNC_EN	R/W	0	1 = Asynchronous notification enabled
	2	SSC_EN	R/W	0	1 = Dynamic SSC transmit is enabled
	1	$PMREQ_P$_EN	R/W	0	1 = Issuing $PMREQ_P$ to host is enabled
	0	BIST_EN	R/W	0	1 = BIST support is enabled

TABLE 18: SATA STANDARD REGISTERS - DEVICE PORT (0 TO 1) - STATUS AND CONTROL

NOTE: *Registers designated as WC are write clear. In order to clear a particular bit or bit field within a WC designated register, write a '1' to that bit or bit field.*

REGISTER	BIT(S)	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
PSCR(0) (SStatus)	31 - 12	Reserved	R/O	0x0	Reserved
	11 - 8	IPM	R/O	0x0	The IPM value indicates the current interface power management state 0000b = Device not present or communication not established 0001b = Interface in active state 0010b= Interface in Partial power management state 0110b = Interface in Slumber power management state All other values reserved
	7 -4	SPD	R/O	0x0	The SPD value indicates the negotiated interface communication speed established 0000b = No negotiated speed (device not present or communication not established) 0001b = Generation 1 communication rate negotiated 0010b = Generation 2 communication rate negotiated All other values reserved
	3 - 0	DET	R/O	0x0	The DET value indicates the interface device detection and Phy state. 0000b = No device detected and Phy communication not established 0001b = Device presence detected but Phy communication not established 0011b = Device presence detected and Phy communication established 0100b = Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved
PSCR(1) (SError)	31 - 16	DIAG	R/WC	0x40	See description below
	15 - 0	ERR	R/WC	0x0	See description below
PSCR(2) (SControl)	31 - 19	Reserved	R/O	0x0	Reserved All reserved fields shall be cleared to zero.
	20 - 16	Reserved	R/W	0x0	Reserved All reserved fields shall be cleared to zero
	15 - 12	SPM	R/W	0x0	See description below
	11 - 8	IPM	R/W	0x0	See description below
	7 - 4	SPD	R/W	0x0	See description below
	3 - 0	DET	R/W	0x4	See description below

SError register SCR(1) -

The Serial ATA interface Error register - SError - is a 32-bit register that conveys supplemental Interface error information to complement the error information available in the Shadow Register Block Error register. The register represents all the detected errors accumulated since the last time the SError register was cleared (whether recovered by the interface of not). Set bits in the error register are explicitly cleared by a write operation to the SError register, or a reset operation. The value written to clear set error bits shall have 1's encoded in the bit positions corresponding to the bits that are to be cleared. Host software should clear the Interface SError register at appropriate checkpoints in order to best isolate error conditions and the commands they impact.

Bits [31:16] DIAG

The DIAG field contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. The field is bit significant as defined in the following figure.

DIAG	R	R	R	R	A	X	F	T	S	H	C	D	B	W	I	N

A Port Selector presence detected: This bit is set to one when COMWAKE is received while the host is in state HP2: HR_AwaitCOMINIT. On power-up reset this bit is cleared to zero. The bit is cleared to zero when the host writes a one to this bit location.

B 10b to 8b Decode error: When set to a one, this bit indicates that one or more 10b to 8b decoding errors occurred since the bit was last cleared to zero.

C CRC Error: When set to one, this bit indicates that one or more CRC errors occurred with the Link layer since the bit was last cleared to zero.

D Disparity Error: When set to one, this bit indicates that incorrect disparity was detected one or more times since the last time the bit was cleared to zero.

F Unrecognized FIS type: When set to one, this bit indicates that since the bit was last cleared one or more FISes were received by the Transport layer with good CRC, but had atype field that was not recognized.

I Phy Internal Error: When set to one, this bit indicates that the Phy detected some internal error since the last time this bit was cleared to zero.

N PHYRDY change: When set to one, this bit indicates that the PHYRDY signal changed state since the last time this bit was cleared to zero.

H Handshake error: When set to one, this bit indicates that one or more R_ERRPhandshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 10b/8b decoding error, or other error condition leading to a negative handshake on a transmitted frame.

R Reserved bit for future use: Shall be cleared to zero.

S Link Sequence Error: When set to one, this bit indicates that one or more Link state machine error conditions was encountered since the last time this bit was cleared to zero. The Link layer state machine defines the conditions under which the link layer detects an erroneous transition.

T Transport state transition error: When set to one, this bit indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared to zero.

W COMWAKE Detected: When set to one this bit indicates that a COMWAKE signal was detected by the Phy since the last time this bit was cleared to zero.

X Exchanged: When set to one this bit indicates that device presence has changed since the last time this bit was cleared to zero. The means by which the implementation determines that the device presence has changed is vendor specific. This bit may be set to one anytime a Phy reset initialization sequence occurs as determined by reception of the COMINIT signal whether in response to a new device being inserted, in response to a COMRESET having been issued, or in response to power-up.

Bits [15:0] ERR

The ERR field contains error information for use by host software in determining the appropriate response to the error condition. The field is bit significant as defined in the following figure.

ERR	R	R	R	R	E	P	C	T	R	R	R	R	R	R	M	I

C Non-recovered persistent communication or data integrity error: A communication error that was not recovered occurred that is expected to be persistent. Since the error condition is expected to be persistent the operation need not be retried by host software. Persistent communications errors may arise from faulty interconnect with the device, from adevice that has been removed or has failed, or a number of other causes.

E Internal error: The host bus adapter experienced an internal error that caused the operation to fail and may have put the host bus adapter into an error state. Host software should reset the interface before re-trying the operation. If the condition persists, the host bus adapter may suffer from a design issue rendering it incompatible with the attached device.

I Recovered data integrity error: A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action. This may arise from a noise burst in the transmission, a voltage supply variation, or from other causes. No action is required by host software since the operation ultimately succeeded, however, host software may elect to track such recovered errors in order to gauge overall communications integrity and potentially step down the negotiated communication speed.

M Recovered communications error: Communications between the device and host was temporarily lost but was re-established. This may arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PHYRDYn signal between the Phy and Link layers. No action is required by the host software since the operation ultimately succeeded, however, host software may elect to track such recovered errors in order to gauge overall communications integrity and potentially step down the negotiated communication speed.

P Protocol error: A violation of the Serial ATA protocol was detected. This may arise from invalid or poorly formed FISes being received, from invalid state transitions, or from other causes. Host software should reset the interface and retry the corresponding operation. If such an error persists, the attached device may have a design issue rendering it incompatible with the host bus adapter.

R Reserved bit for future use: Shall be cleared to zero.

T Non-recovered transient data integrity error: A data integrity error occurred that was not recovered by the interface. Since the error condition is not expected to be persistent the operation should be retried by host software.

SControl register SCR(2)

The Serial ATA interface Control register - SControl - is a 32-bit read-write register that provides the interface by which software controls Serial ATA interface capabilities. Writes to the SControl register result in an action being taken by the host adapter or interface. Reads from the register return the last value written to it.

Bits [19:16] PMP

The Port Multiplier Port (PMP) field represents the 4-bit value to be placed in the PM Port field of all transmitted FISes. This field is ‘0000’ upon power-up. This field is optional and an HBA implementation may choose to ignore this field if the FIS to be transmitted is constructed via an alternative method.

Bits [15:12] SPM

The Select Power Management (SPM) field is used to select a power management state. Anon-zero value written to this field shall cause the power management state specified to be initiated. A value written to this field is treated as a one-shot. This field shall be read as 0000b.

- 0000b = No power management state transition requested

- 0001b = Transition to the Partial power management state initiated
- 0010b = Transition to the Slumber power management state initiated
- 0100b = Transition to the active power management state initiated
- All other values reserved

Bits [11:8] IPM

The IPM field represents the enabled interface power management states that may be invoked via the Serial ATA interface power management capabilities

- 0000b = No interface power management state restrictions
- 0001b = Transitions to the Partial power management state disabled
- 0010b = Transitions to the Slumber power management state disabled
- 0011b = Transitions to both the Partial and Slumber power management states disabled
- All other values reserved

Bits [7:4]SPD

The SPD field represents the highest allowed communication speed the interface is allowed to negotiate when interface communication speed is established

- 0000b = No speed negotiation restrictions
- 0001b = Limit speed negotiation to a rate not greater than Gen 1 communication rate
- 0010b = Limit speed negotiation to a rate not greater than Gen 2 communication rate
- All other values reserved

Bits [3:0] DET

The DET field controls the host adapter device detection and interface initialization.

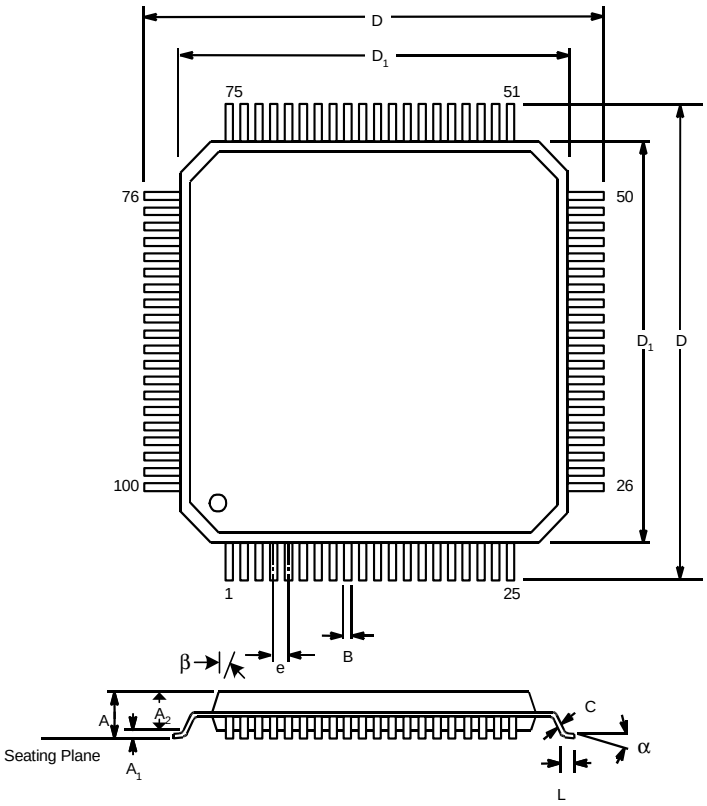
- 0000b = No device detection or initialization action requested
- 0001b = Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. Upon a write to the SControl register that sets the DET field to 0001b, the host interface shall transition to the HP1: HR_Reset state and shall remain in that state until the DET field is set to a value other than 0001b, by a subsequent write to the SControl register.
- 0100b = Disable the Serial ATA interface and put Phy in offline mode.
- All other values reserved

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRS10L210IV-F	100 Pin LQFP (Lead Free)	-40℃ to +85℃
XRS10L210IV	100 Pin LQFP	-40℃ to +85℃
XRS10L210IL-F	64 Pin QFN (Lead Free)	-40℃ to +85℃
XRS10L210IL	64 Pin QFN	-40℃ to +85℃

100 LEAD LOW-PROFILE QUAD FLAT PACK

(14 x 14 x 1.4 mm LQFP, 1.0 mm FORM)

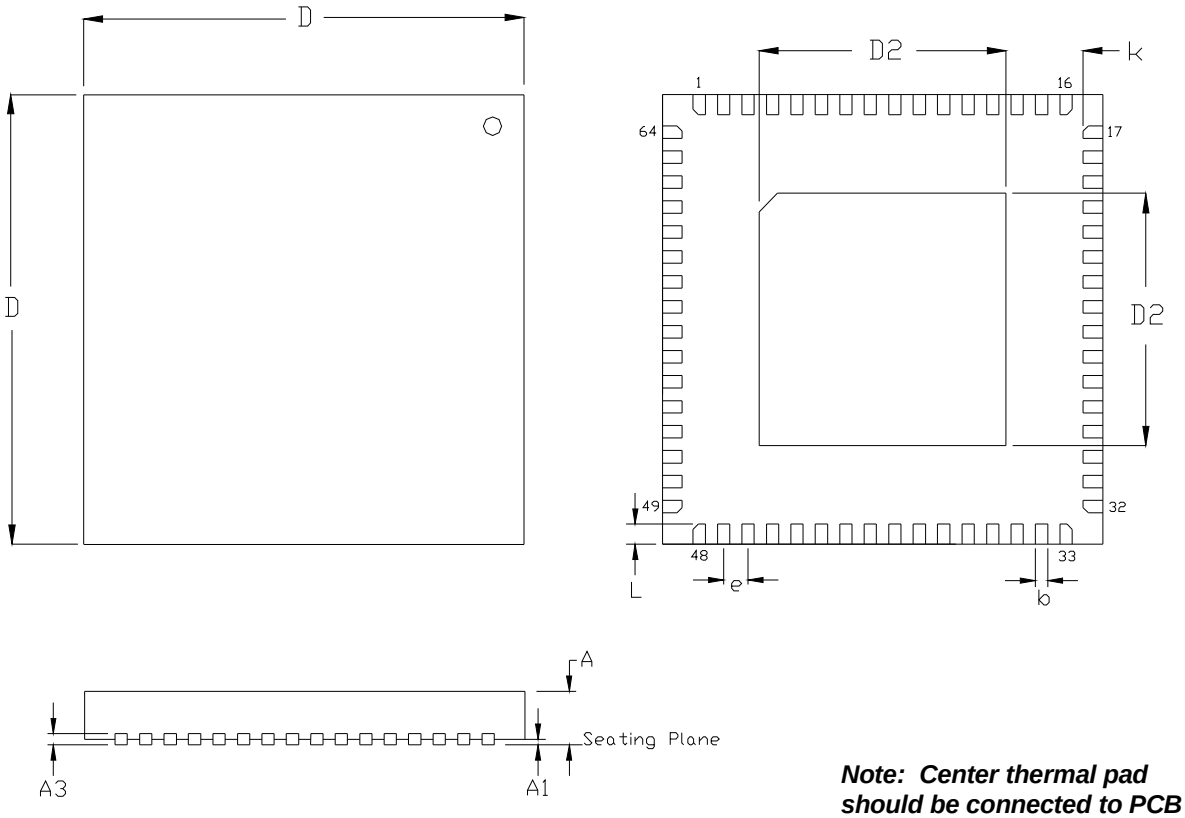


NOTE: *The control dimension is in millimeters*

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.010	0.014	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.622	0.638	15.80	16.20
D_1	0.390	0.555	13.90	14.10
e	0.0197 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°
β	7°typ		7°typ	

64 LEAD QUAD FLAT NO LEAD
(9 mm x 9 mm x 0.9mm, 0.50 pitch QFN, Small Thermal Pad)

Rev. 1.00



Note: Center thermal pad should be connected to PCB Ground Plane.

Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A3	0.006	0.010	0.15	0.25
D	0.350	0.358	8.90	9.10
D2	0.187	0.199	4.75	5.05
b	0.007	0.012	0.18	0.30
e	0.0197 BSC		0.50 BSC	
L	0.014	0.018	0.35	0.45
k	0.008	-	0.20	-

REVISIONS

REV #	DATE	DESCRIPTION OF CHANGES
1.00	January 2008	Released.
1.01	March 2008	Revised to operational registers.
1.02	August 2008	.Updated ESD Data
1.03	September 2008	Added 64 QFN Package.
1.04	December 2008	Pin-out correction for 64 QFN Package

NOTICE

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Datasheet December 2008.