CADEKA
Amplify the Human Experience

SPT9691

WIDE INPUT VOLTAGE, JFET COMPARATOR

FEATURES

- Common Mode Range -4.0 to +8.0 V
- Low Input Bias Current <100 pA
- Propagation Delay 2.5 ns (max)
- Low Offset ±25 mV
- Low Feedthrough and Crosstalk
- Differential Latch Control

APPLICATIONS

- Automated Test Equipment
- High-Speed Instrumentation
- Window Comparators
- High-Speed Timing
- Line Receivers
- High-Speed Triggers
- Threshold Detection
- Peak Detection

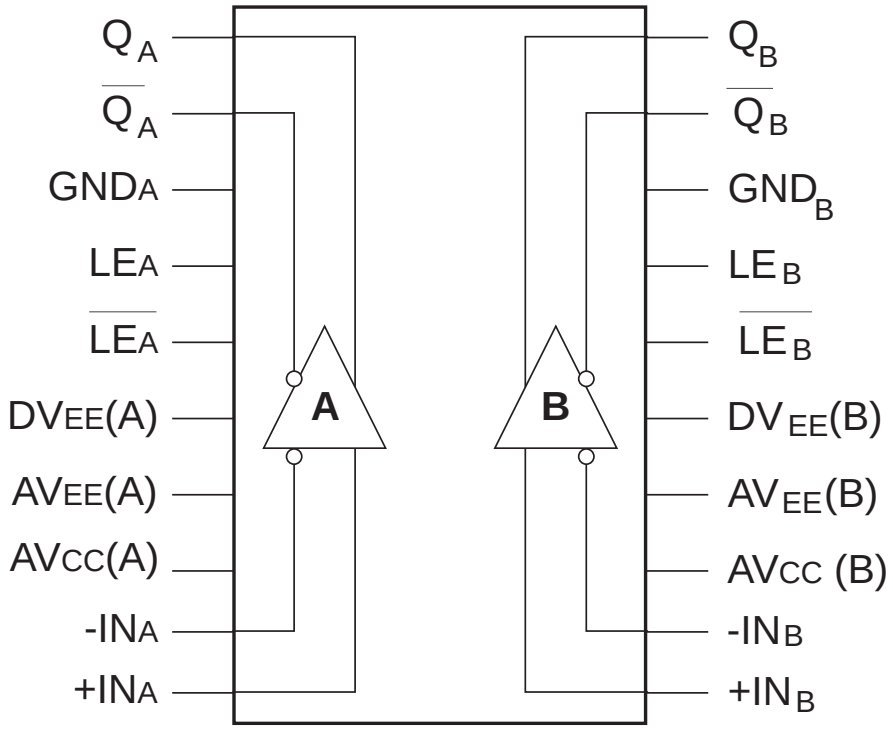
GENERAL DESCRIPTION

The SPT9691 is a high-speed, wide common mode voltage, JFET input, dual comparator. It is designed for applications that measure critical timing parameters in which wide common mode input voltages of -4.0 to +8.0 V are required. Propagation delays are constant for overdrives greater than 200 mV.

JFET inputs reduce the input bias currents to the nanoamp level, eliminating the need for input drivers and buffers in most applications. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. Each comparator has a complementary latch enable control that can be driven by standard ECL logic.

The SPT9691 is available in 20-lead PLCC, 20-lead plastic DIP and 20-contact LCC packages over the commercial temperature range. It is also available in die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages (Measured to GND)

Positive Supply Voltage (AV_{CC}) ..... -0.5 to +11.0 V
Negative Supply Voltage (AV_{EE}) ..... -11.0 to +0.5 V
Negative Supply Voltage (DV_{EE}) ..... -6.0 to +0.5 V

Input Voltages

Input Common Mode Voltage ..... DV_{EE}-1 to +AV_{CC}+1
Differential Input Voltage ..... -12.0 to +12.0 V
Input Voltage, Latch Controls ..... DV_{EE} to 0.5 V
V_{IN} to AV_{CC} Differential Voltage ..... -16 to +1.0 V
V_{IN} to AV_{EE} Differential Voltage ..... +4 to +21.0 V

Output

Output Current ..... 30 mA

Temperature

Operating Temperature, ambient ..... 0 to +70 °C
junction ..... +150 °C
Lead Temperature, (soldering 60 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, AV_{CC} = +10 V, AV_{EE}=-10.0 V, DV_{EE}=-5.2 V, RL = 50 Ohm to -2V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	$V_{IN,CM}$=0	I	-25	0.0	+25	mV
	$T_{MIN} < T_A < T_{MAX}$	IV	-25	0.0	+25	mV
Offset Voltage Tempco		V		50		µV/°C
Input Bias Current		I		±0.1	±10	nA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		±2.0	±100	nA
Input Offset Current		V		±1.0		nA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	V		±10		nA
Positive Supply Current (Dual)	AVcc=10 V	I		25	33	mA
Negative Supply Current (Dual)	AV_{EE}=-10.0 V	I		15	20	mA
Negative Supply Current (Dual)	DV_{EE}=-5.2 V	I		55	70	mA
Positive Supply Voltage, AV_{CC}		IV	9.75	10.0	10.25	V
Negative Supply Voltage, AV_{EE}		IV	-9.75	-10.0	-10.25	V
Negative Supply Voltage, DV_{EE}		IV	-4.95	-5.2	-5.45	V
Input Common Mode Range		I	-4.0		+8.0	V
Latch Enable Common Mode Range		IV	-2.0		0	V
Differential Voltage Range		I			±10	V
Open Loop Gain		V		60		dB
Differential Input Resistance		V		2		GΩ
Input Capacitance	LCC Package			1.0		pF
	PLCC Package			1.0		pF
	PDIP			2.9		pF
Power Supply Sensitivity		V		60		dB
Common Mode Rejection Ratio		I	50	60		dB
	$T_{MIN} < T_A < T_{MAX}$	IV	45	55		dB

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, AV_{CC} = +10 V, AV_{EE}=-10.0 V, DV_{EE}=-5.2 V, RL = 50 Ohm to -2V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Power Dissipation	Dual	I		700	895	mW
Output High Level	ECL 50 Ohms to -2V	I	-.98		-.70	V
Output Low Level	ECL 50 Ohms to -2V	I	-1.95		-1.65	V
AC ELECTRICAL CHARACTERISTICS						
Propagation Delay[1]	150 mV O.D.	IV	1.5	2.0	2.5	ns
Propagation Delay TEMPCO		V		2		ps/ °C
Propagation Delay Skew (A vs B)		V		100		ps
Propagation Delay Dispersion[2]	150 mV Overdrive Min.	V		200		ps
Latch Set-up Time		V		1.7		ns
Latch to Output Delay	150 mV O.D.	V		0.8		ns
Latch Pulse Width		V		2		ns
Latch Hold Time		V		-1.9		ns
Rise Time	20% to 80%	V		0.4		ns
Fall Time	20% to 80%	V		0.4		ns
Slew Rate		V		3		V/ns

NOTES:

[1] Valid for both high-to-low and low-to-high transitions.

[2] Dispersion is the change in propagation delay due to changes in slew rate, overdrive, and common mode level.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

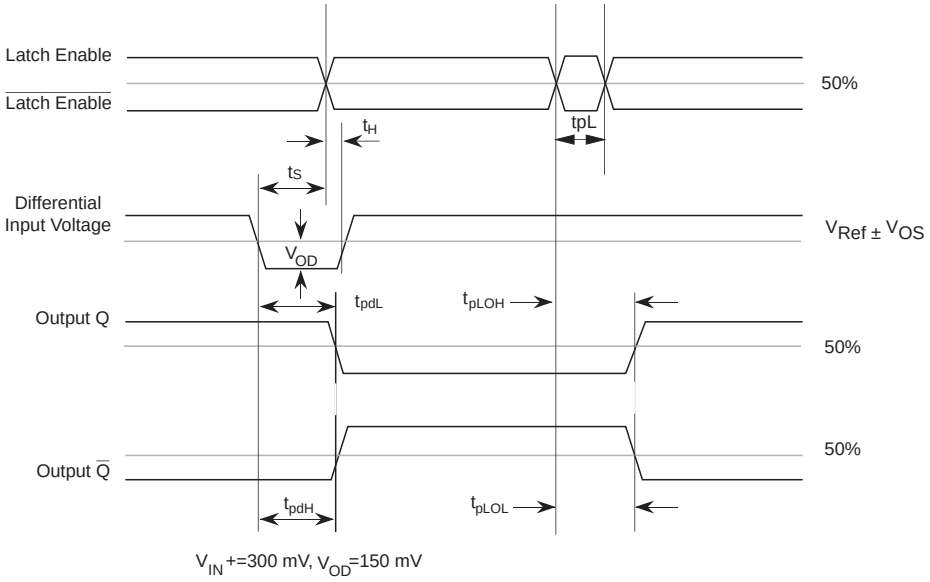
TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

TIMING INFORMATION

The timing diagram for the comparator is shown in figure 1. If LE is high and $\overline{LE}$ low in the SPT9691, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of a 150 mV overdrive voltage) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the LE falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H , the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Figure 1 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may not be detected.

SWITCHING TERMS (Refer to figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the reference voltage (± the input offset voltage) to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the reference voltage (± the input offset voltage) to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

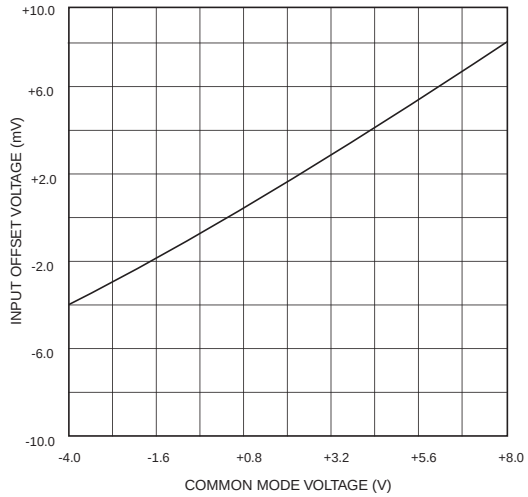
t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

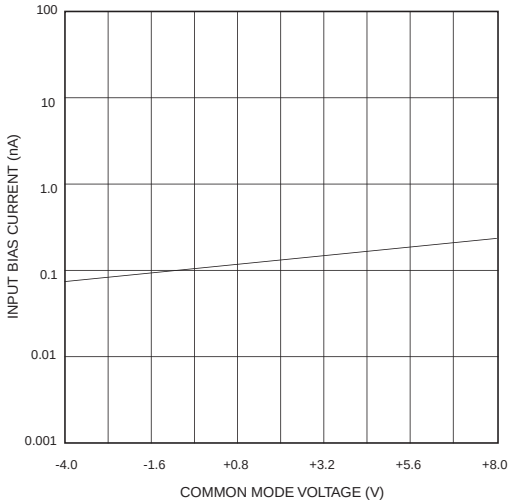
V_{OD} VOLTAGE OVERDRIVE - The difference between the differential input and reference input voltages.

TYPICAL PERFORMANCE CURVES

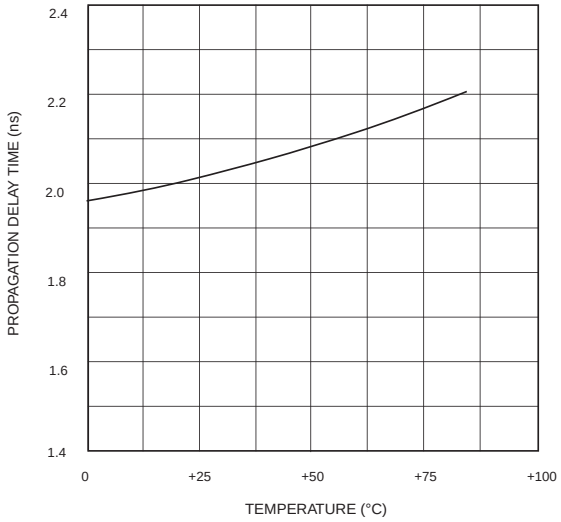
INPUT OFFSET VOLTAGE VS COMMON MODE VOLTAGE (T=+25 °C)



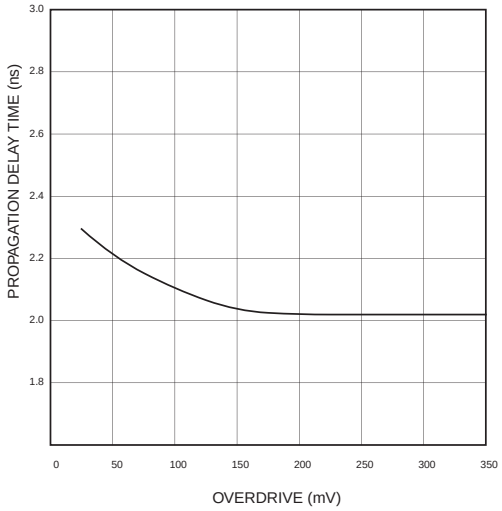
INPUT BIAS CURRENT VS COMMON MODE VOLTAGE (+25 °C)



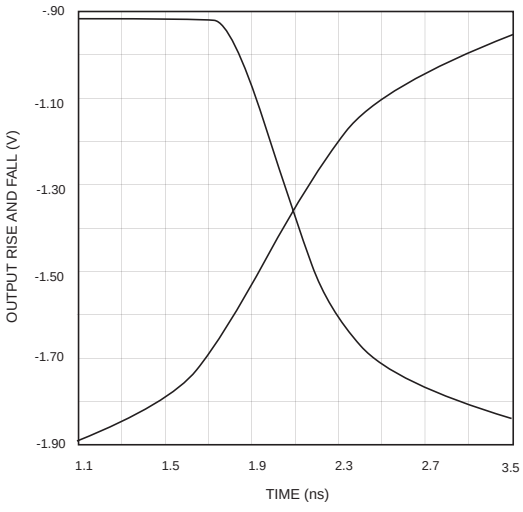
PROPOGATION DELAY TIME VS TEMPERATURE (V_{OD}=150 mV)



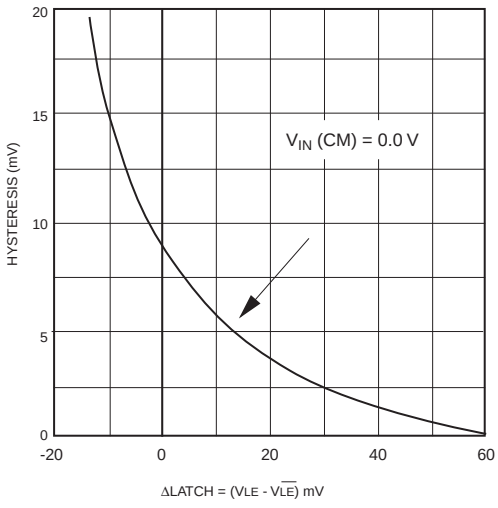
PROPAGATION DELAY TIME VS OVERDRIVE (mV)



RISE AND FALL OF OUTPUTS VS TIME CROSSOVER



HYSTERESIS VS ΔLATCH



GENERAL INFORMATION

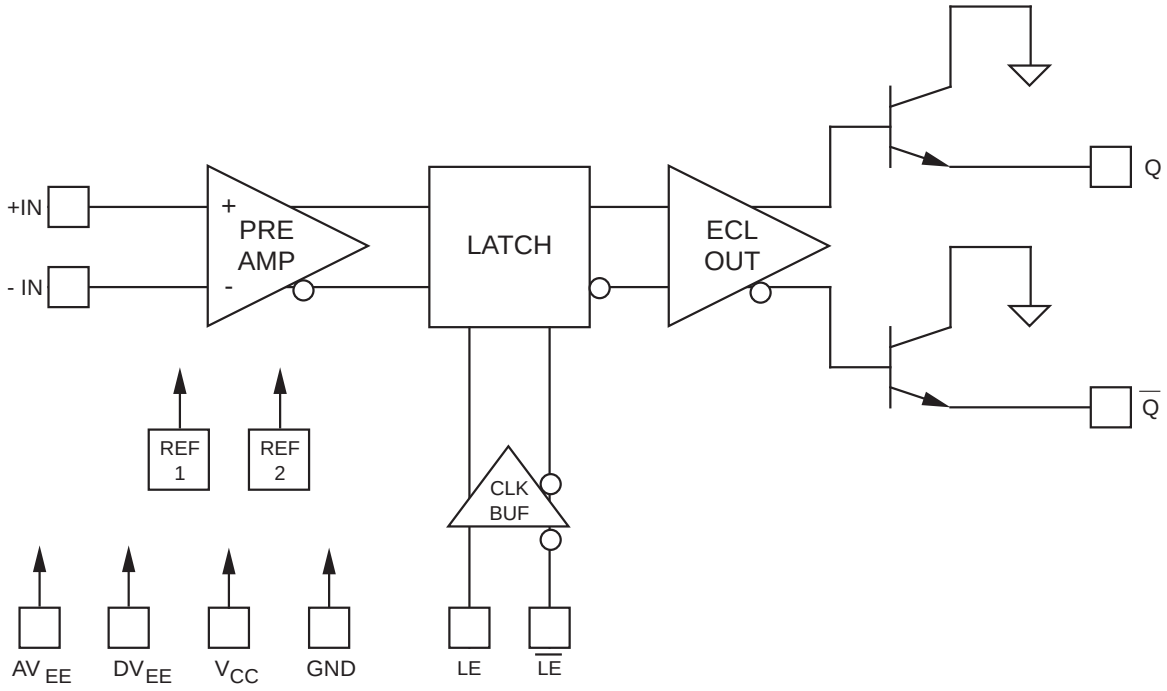
The SPT9691 is an ultrahigh-speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9691 has a complementary latch enable control for each comparator. Both should be driven by standard ECL logic levels.

A common mode voltage range of -4 V to +8 V is achieved by a proprietary JFET input design which requires a separate negative power supply (AV_{EE}).

The dual comparators have separate $AV_{CC,}$ $AV_{EE,}$ $DV_{EE,}$ and grounds for each comparator to achieve high crosstalk rejection. Single channel operation can be accomplished by floating all pins (including the ground and supply pins) of the unused comparator. Power dissipation during single channel operation is 50% of the dissipation during dual channel operation.

Figure 2 - Internal Function Diagram



TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in figure 3. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the SPT9691 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. All supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible. All ground pins should be connected to the same ground plane to further improve noise immunity and shielding. If using the SPT9691 as a single comparator, the outputs of the inactive comparator can be grounded, left open or terminated with 50 Ohms to -2 V. All outputs on the active comparator, whether used or unused, should have identical terminations to minimize ground current switching transients.

Diode D1 connected between AV_{CC} and GND is recommended to prevent possible damage to the device in case the AV_{CC} supply is disconnected. The diode should be a 1N914 or equivalent. If AV_{CC} is disconnected with this diode in place, there will be approximately a 6 mA current draw from both AV_{EE} and DV_{EE}. Diode D2 connected between AV_{EE} and DV_{EE} is necessary to avoid power supply sequence latch-up. This diode keeps AV_{EE} (also the substrate) less than a silicon diode drop away from the most negative circuit potential if DV_{EE} is powered up first. This diode should be a 1N5817 (Schottky) or equivalent.

Note: At no time should <u>both</u> inputs be allowed to float with power applied to the device. At least one of the inputs should be tied to a voltage within the common mode range (-4.0 to +8.0 V) to prevent possible damage to the device. To prevent possible latch-up during initial power up, the input voltages should not exceed ±1 V. Additional protection diodes D3-D6 should be used on the inputs if there is the possibility of exceeding the absolute maximum ratings of the inputs with respect to AV_{CC} and DV_{EE} (1N914 or equivalent). NOTE: For ease of implementation, all diodes (D1 - D6) can be 1N5817 (Schottky) or equivalent.

Figure 3 - SPT9691 Typical Interface Circuit

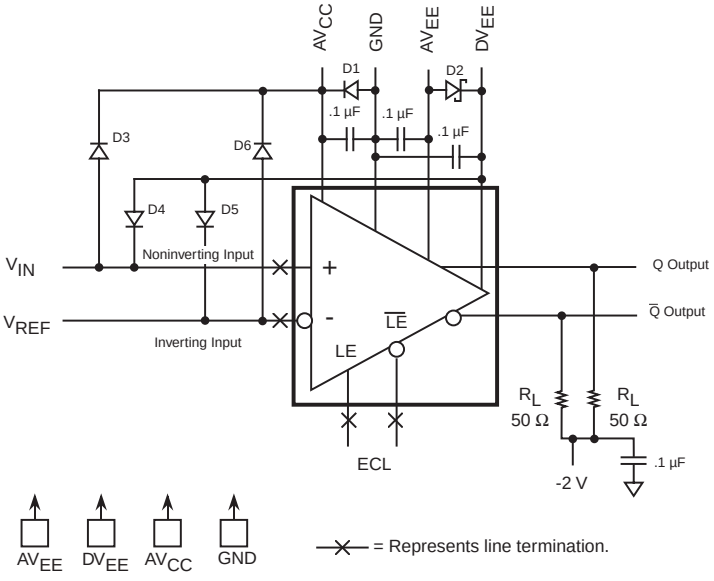
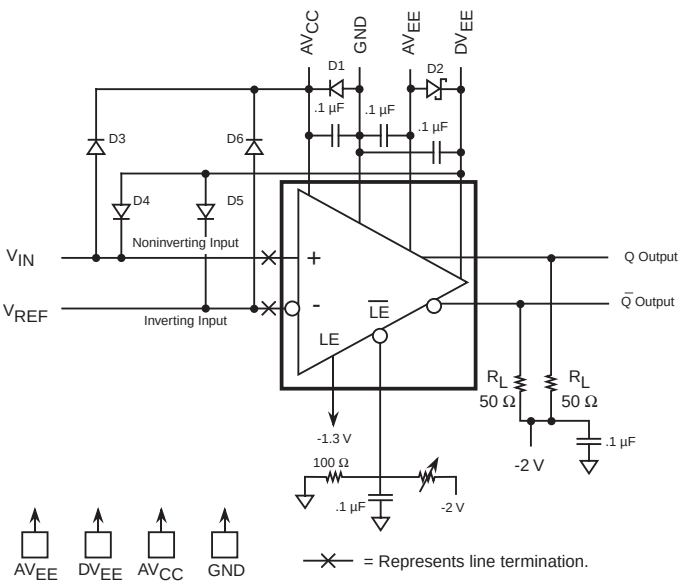
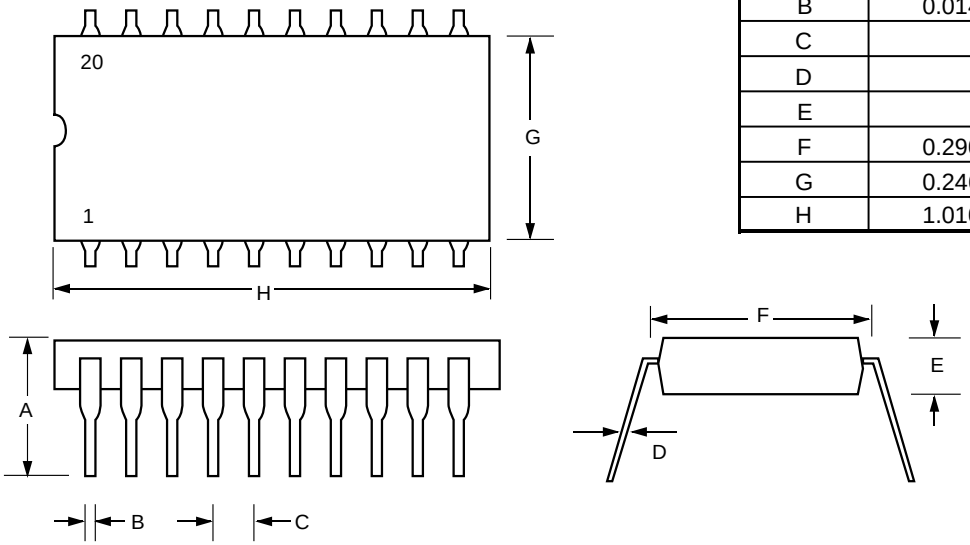


Figure 4 - SPT9691 Typical Interface Circuit With Hysteresis



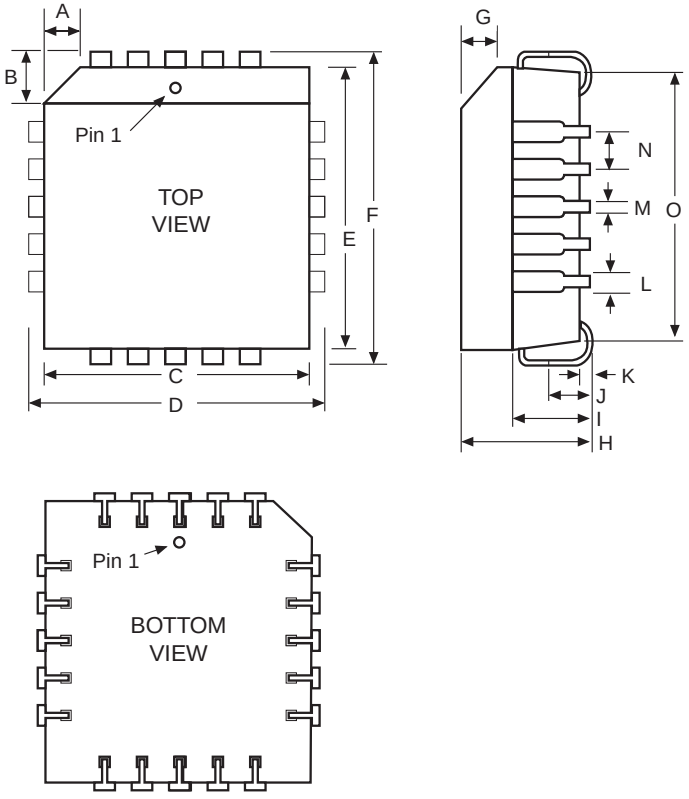
PACKAGE OUTLINES

20-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.300		7.62
B	0.014	0.026	0.36	0.66
C		.100 typ		2.54
D		.010 typ		0.25
E		1.20 typ		30.48
F	0.290	0.330	7.37	8.38
G	0.246	0.254	6.25	6.45
H	1.010	1.030	25.65	26.16

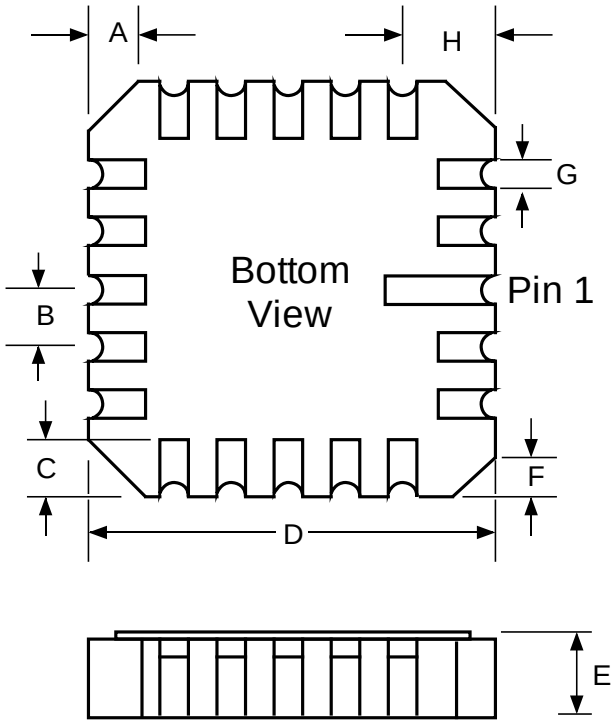
20-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.045 typ		1.14
B				
C	0.350	0.356	8.89	9.04
D	0.385	0.395	9.78	10.03
E	0.350	0.356	8.89	9.04
F	0.385	0.395	9.78	10.03
G	0.042	0.056	1.07	1.42
H	0.165	0.180	4.19	4.57
I	0.085	0.110	2.16	2.79
J	0.025	0.040	0.64	1.02
K	0.015	0.025	0.38	0.64
L	0.026	0.032	0.66	0.81
M	0.013	0.021	0.33	0.53
N		0.050		1.27
O	0.290	0.330	7.37	8.38

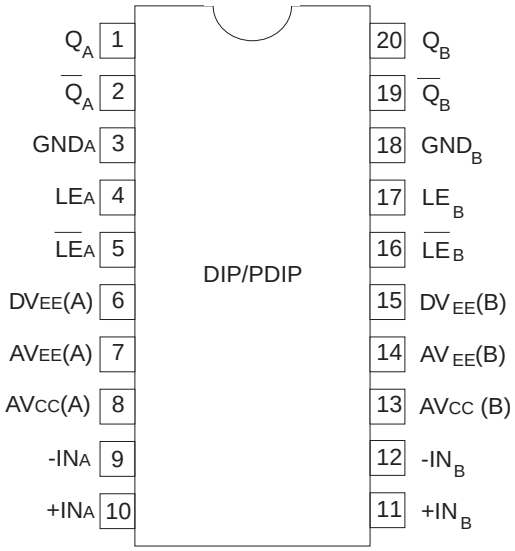
PACKAGE OUTLINES

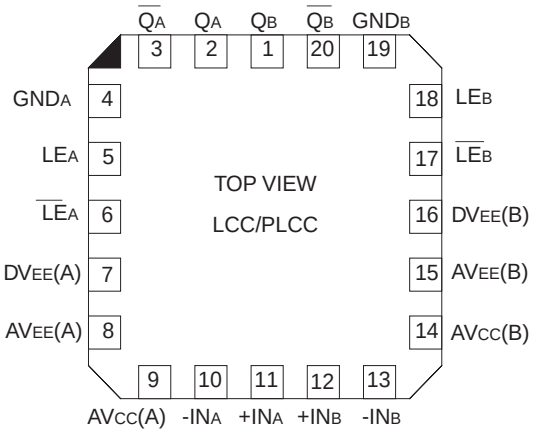
20-Contact Leadless Chip Carrier (LCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.040 typ		1.02
B		.050 typ		1.27
C	0.045	0.055	1.14	1.40
D	0.345	0.360	8.76	9.14
E	0.054	0.066	1.37	1.68
F		.020 typ		0.51
G	0.022	0.028	0.56	0.71
H		0.075		1.91

PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
$\overline{LE}_A$	Inverted Latch Enable A
LE_A	Latch Enable A
$AV_{CC}(A)$	Positive Supply Voltage (+10 V)
$AV_{EE}(A)$	Negative Supply Voltage (-10 V)
$DV_{EE}(A)$	Negative Supply Voltage (-5.2 V)
$AV_{CC}(B)$	Positive Supply Voltage (+10 V)
$AV_{EE}(B)$	Negative Supply Voltage (-10 V)
$DV_{EE}(B)$	Negative Supply Voltage (-5.2 V)
$-IN_A$	Inverting Input A
$+IN_A$	Noninverting Input A
$+IN_B$	Noninverting Input B
$-IN_B$	Inverting Input B
$\overline{LE}_B$	Inverted Latch Enabled B
LE_B	Latch Enable B
GND_B	Ground B
$\overline{Q}_B$	Inverted Output B
Q_B	Output B

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT9691SCC	0 to +70 °C	20C LCC
SPT9691SCN	0 to +70 °C	20L Plastic DIP
SPT9691SCP	0 to +70 °C	20L Plastic Leaded Chip Carrier (PLCC)
SPT9691SCU	+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.