

64-common X 160-segment + 1-icon common Bitmap LCD Driver

■ GENERAL DESCRIPTION

The **NJU6655B** is a bitmap LCD driver to display graphics or characters.

It contains 10,400 bits display data RAM, microprocessor interface circuits, instruction decoder, 64-common and 160-segment + 1-icon-common drivers.

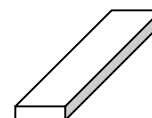
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel interface.

65 x 160 dots graphics or 10-character 4-line by 16 x 16 dots character with icon are displayed by **NJU6655B** itself.

The wide operating voltage from 2.4 to 5.5V and low operating current are suitable for battery-powered applications.

The build-in Electrical Variable Resistance is very precision, furthermore the rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE OUTLINE



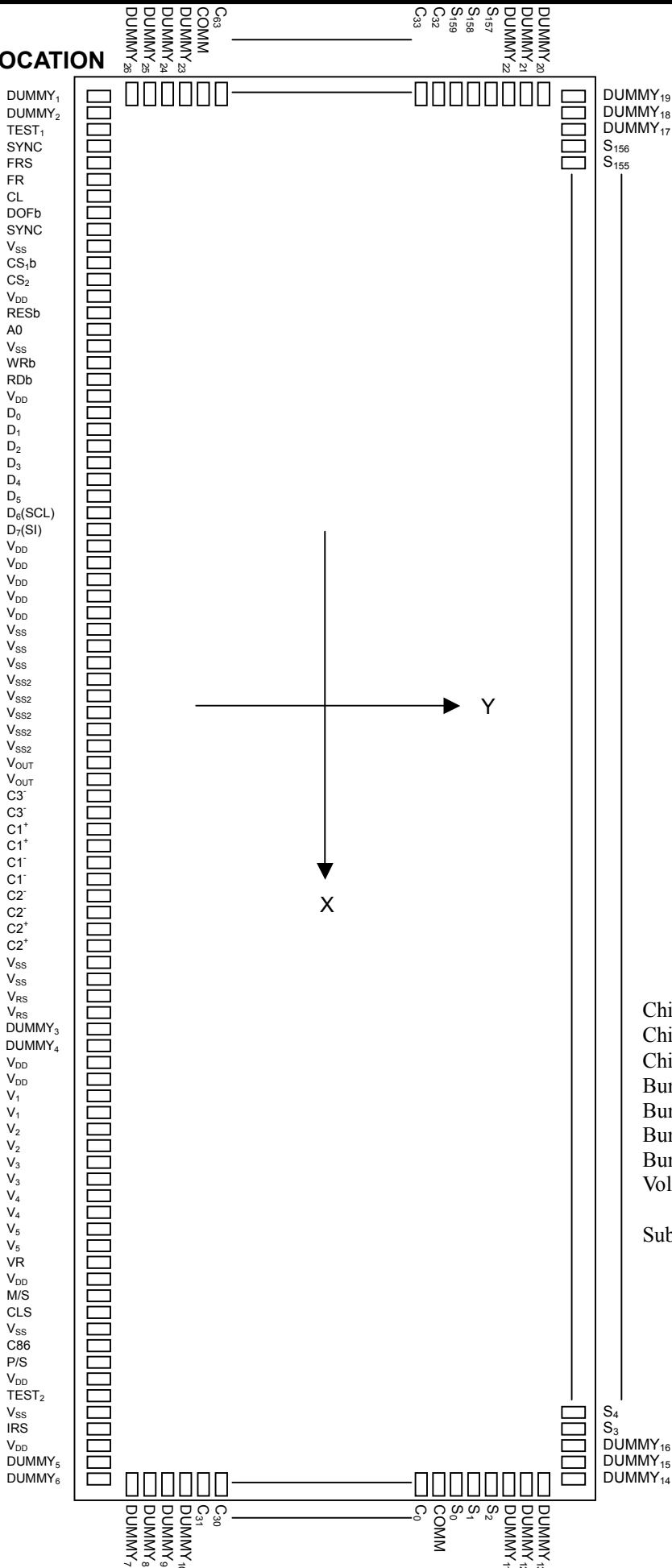
NJU6655BCJ

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 10,400 bits
- 225 LCD Drivers - 64-common and 160-segment + 1-icon common
- Direct Microprocessor Interface for both of 68 and 80 type MPU
- Serial Interface (SI, SCL, A0, CS_{1b}, CS₂)
- Programmable Bias selection : 1/5, 1/7, 1/9 bias
- Useful Instruction Set
 - Display On/Off Cont, Initial Display Line Set, Page Address Set, Column Address Set, Status Read,
 - Display Data Read/Write, ADC Select, Inverse Display, Entire Display On/Off, Bias Select, Read Modify Write,
 - End, Reset, Common Direction Register Set, Power control set, Feedback Resistor Ratio Set,
 - EVR Mode Set, EVR Register Set, Static Indicator On/Off, Static Indicator Register Set, Power Save,
 - Power Save Reset, n-line Inverse Drive Register Set, n-line Inverse Drive Reset, Partial Select,
 - Internal Oscillation Circuit ON.
- Power Supply Circuits for LCD Incorporated
 - Voltage Booster Circuits (4-time Maximum),
 - Voltage Adjust Circuits, Voltage Follower x 4
- Voltage Regulator Incorporated ($V_{REF} = \pm 3\%$)
- Precision Electrical Variable Resistance (64-step)
- Low Power Consumption 130uA(Typ.).
- Operating Voltage (All the voltages are based on $V_{DD}=0V$.)
 - Logic Operating Voltage : -2.4V to -5.5V
 - Voltage Booster Operating Voltage : -2.4V to -6.0V
 - LCD Driving Voltage : -4.5V to -18.0V
- Rectangle outlook for COG
- Package Outline : Bump-chip
- C-MOS Technology (Substrate : N)

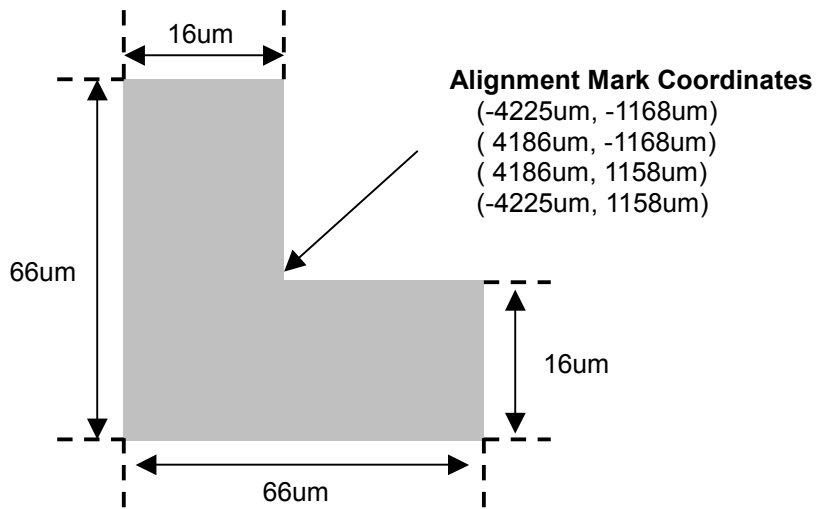
NJU6655B

■ PAD LOCATION

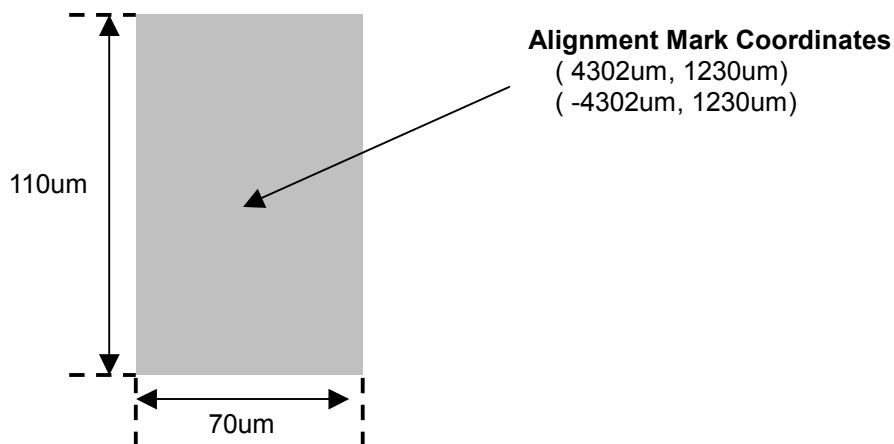


Chip Center : X=0um, Y=0um
 Chip Size : X=8.88mm, Y=2.77mm
 Chip Thickness : 675um ± 30um
 Bump Size : 130um x 31um
 Bump Pitch : 50um(Min.)
 Bump Height : 17.5um(Typ.)
 Bump Material : Au
 Voltage Boosting Polarity : Negative Voltage (V_{DD} common)
 Substrate : N

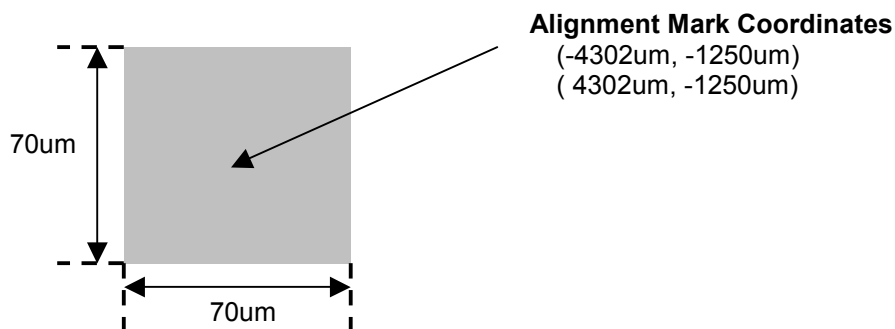
Alignment Mark 1



Alignment Mark 2



Alignment Mark 3



■ PAD COORDINATES

PAD No.	Terminal	X= um	Y= um
1	DUMMY ₁	-4092	-1213
2	DUMMY ₂	-4042	-1213
3	TEST ₁	-3919	-1213
4	SYNC	-3796	-1213
5	FRS	-3637	-1213
6	FR	-3417	-1213
7	CL	-3197	-1213
8	DOFb	-2976	-1213
9	SYNC	-2756	-1213
10	V _{SS}	-2598	-1213
11	CS _{1b}	-2474	-1213
12	CS ₂	-2317	-1213
13	V _{DD}	-2194	-1213
14	RESb	-2071	-1213
15	A0	-1914	-1213
16	V _{SS}	-1790	-1213
17	WRb	-1667	-1213
18	RD _b	-1510	-1213
19	V _{DD}	-1387	-1213
20	D ₀	-1229	-1213
21	D ₁	-1008	-1213
22	D ₂	-788	-1213
23	D ₃	-567	-1213
24	D ₄	-347	-1213
25	D ₅	-127	-1213
26	D ₆ (SCL)	94	-1213
27	D ₇ (SI)	314	-1213
28	V _{DD}	472	-1213
29	V _{DD}	522	-1213
30	V _{DD}	572	-1213
31	V _{DD}	622	-1213
32	V _{DD}	672	-1213
33	V _{SS}	722	-1213
34	V _{SS}	772	-1213
35	V _{SS}	822	-1213
36	V _{SS2}	872	-1213
37	V _{SS2}	922	-1213
38	V _{SS2}	972	-1213
39	V _{SS2}	1022	-1213
40	V _{SS2}	1072	-1213
41	V _{OUT}	1122	-1213
42	V _{OUT}	1172	-1213
43	C3 ⁻	1222	-1213
44	C3 ⁻	1272	-1213
45	C1 ⁺	1322	-1213
46	C1 ⁺	1372	-1213
47	C1 ⁻	1422	-1213
48	C1 ⁻	1472	-1213
49	C2 ⁻	1522	-1213
50	C2 ⁻	1572	-1213

Chip Size 8.88 x 2.77mm(Chip Center X=0um, Y=0um)

PAD No.	Terminal	X= um	Y= um
51	C2 ⁺	1622	-1213
52	C2 ⁺	1672	-1213
53	V _{SS}	1722	-1213
54	V _{SS}	1772	-1213
55	V _{RS}	1822	-1213
56	V _{RS}	1872	-1213
57	DUMMY ₃	1922	-1213
58	DUMMY ₄	1972	-1213
59	V _{DD}	2022	-1213
60	V _{DD}	2072	-1213
61	V ₁	2122	-1213
62	V ₁	2172	-1213
63	V ₂	2222	-1213
64	V ₂	2272	-1213
65	V ₃	2322	-1213
66	V ₃	2372	-1213
67	V ₄	2422	-1213
68	V ₄	2472	-1213
69	V ₅	2522	-1213
70	V ₅	2572	-1213
71	VR	2622	-1213
72	V _{DD}	2672	-1213
73	M/S	2796	-1213
74	CLS	2953	-1213
75	V _{SS}	3076	-1213
76	C86	3199	-1213
77	P/S	3356	-1213
78	V _{DD}	3480	-1213
79	TEST ₂	3603	-1213
80	V _{SS}	3726	-1213
81	IRS	3849	-1213
82	V _{DD}	3972	-1213
83	DUMMY ₅	4022	-1213
84	DUMMY ₆	4072	-1213
85	DUMMY ₇	4265	-1037
86	DUMMY ₈	4265	-987
87	DUMMY ₉	4265	-937
88	DUMMY ₁₀	4265	-887
89	C ₃₁	4265	-837
90	C ₃₀	4265	-787
91	C ₂₉	4265	-737
92	C ₂₈	4265	-687
93	C ₂₇	4265	-637
94	C ₂₆	4265	-587
95	C ₂₅	4265	-537
96	C ₂₄	4265	-487
97	C ₂₃	4265	-437
98	C ₂₂	4265	-387
99	C ₂₁	4265	-337
100	C ₂₀	4265	-287

PAD No.	Terminal	X= um	Y= um
101	C ₁₉	4265	-237
102	C ₁₈	4265	-187
103	C ₁₇	4265	-137
104	C ₁₆	4265	-87
105	C ₁₅	4265	-37
106	C ₁₄	4265	13
107	C ₁₃	4265	63
108	C ₁₂	4265	113
109	C ₁₁	4265	163
110	C ₁₀	4265	213
111	C ₉	4265	263
112	C ₈	4265	313
113	C ₇	4265	363
114	C ₆	4265	413
115	C ₅	4265	463
116	C ₄	4265	513
117	C ₃	4265	563
118	C ₂	4265	613
119	C ₁	4265	663
120	C ₀	4265	713
121	COMM	4265	763
122	S ₀	4265	813
123	S ₁	4265	863
124	S ₂	4265	913
125	DUMMY ₁₁	4265	963
126	DUMMY ₁₂	4265	1013
127	DUMMY ₁₃	4265	1063
128	DUMMY ₁₄	4115	1213
129	DUMMY ₁₅	4065	1213
130	DUMMY ₁₆	4015	1213
131	S ₃	3965	1213
132	S ₄	3915	1213
133	S ₅	3865	1213
134	S ₆	3815	1213
135	S ₇	3765	1213
136	S ₈	3715	1213
137	S ₉	3665	1213
138	S ₁₀	3615	1213
139	S ₁₁	3565	1213
140	S ₁₂	3515	1213
141	S ₁₃	3465	1213
142	S ₁₄	3415	1213
143	S ₁₅	3365	1213
144	S ₁₆	3315	1213
145	S ₁₇	3265	1213
146	S ₁₈	3215	1213
147	S ₁₉	3165	1213
148	S ₂₀	3115	1213
149	S ₂₁	3065	1213
150	S ₂₂	3015	1213

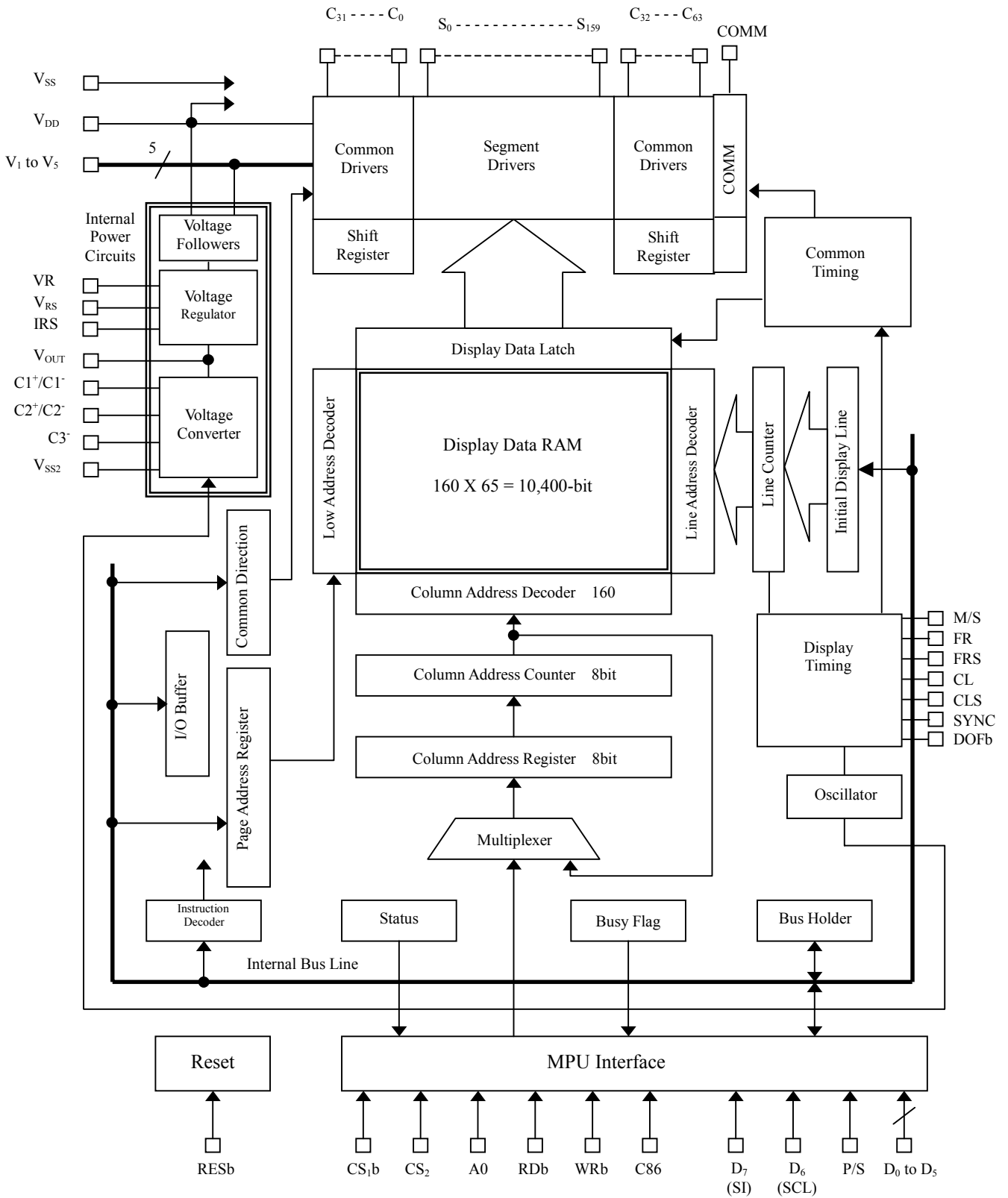
PAD No.	Terminal	X= um	Y= um
151	S ₂₃	2965	1213
152	S ₂₄	2915	1213
153	S ₂₅	2865	1213
154	S ₂₆	2815	1213
155	S ₂₇	2765	1213
156	S ₂₈	2715	1213
157	S ₂₉	2665	1213
158	S ₃₀	2615	1213
159	S ₃₁	2565	1213
160	S ₃₂	2515	1213
161	S ₃₃	2465	1213
162	S ₃₄	2415	1213
163	S ₃₅	2365	1213
164	S ₃₆	2315	1213
165	S ₃₇	2265	1213
166	S ₃₈	2215	1213
167	S ₃₉	2165	1213
168	S ₄₀	2115	1213
169	S ₄₁	2065	1213
170	S ₄₂	2015	1213
171	S ₄₃	1965	1213
172	S ₄₄	1915	1213
173	S ₄₅	1865	1213
174	S ₄₆	1815	1213
175	S ₄₇	1765	1213
176	S ₄₈	1715	1213
177	S ₄₉	1665	1213
178	S ₅₀	1615	1213
179	S ₅₁	1565	1213
180	S ₅₂	1515	1213
181	S ₅₃	1465	1213
182	S ₅₄	1415	1213
183	S ₅₅	1365	1213
184	S ₅₆	1315	1213
185	S ₅₇	1265	1213
186	S ₅₈	1215	1213
187	S ₅₉	1165	1213
188	S ₆₀	1115	1213
189	S ₆₁	1065	1213
190	S ₆₂	1015	1213
191	S ₆₃	965	1213
192	S ₆₄	915	1213
193	S ₆₅	865	1213
194	S ₆₆	815	1213
195	S ₆₇	765	1213
196	S ₆₈	715	1213
197	S ₆₉	665	1213
198	S ₇₀	615	1213
199	S ₇₁	565	1213
200	S ₇₂	515	1213

PAD No.	Terminal	X= um	Y= um
201	S ₇₃	465	1213
202	S ₇₄	415	1213
203	S ₇₅	365	1213
204	S ₇₆	315	1213
205	S ₇₇	265	1213
206	S ₇₈	215	1213
207	S ₇₉	165	1213
208	S ₈₀	115	1213
209	S ₈₁	65	1213
210	S ₈₂	15	1213
211	S ₈₃	-35	1213
212	S ₈₄	-85	1213
213	S ₈₅	-135	1213
214	S ₈₆	-185	1213
215	S ₈₇	-235	1213
216	S ₈₈	-285	1213
217	S ₈₉	-335	1213
218	S ₉₀	-385	1213
219	S ₉₁	-435	1213
220	S ₉₂	-485	1213
221	S ₉₃	-535	1213
222	S ₉₄	-585	1213
223	S ₉₅	-635	1213
224	S ₉₆	-685	1213
225	S ₉₇	-735	1213
226	S ₉₈	-785	1213
227	S ₉₉	-835	1213
228	S ₁₀₀	-885	1213
229	S ₁₀₁	-935	1213
230	S ₁₀₂	-985	1213
231	S ₁₀₃	-1035	1213
232	S ₁₀₄	-1085	1213
233	S ₁₀₅	-1135	1213
234	S ₁₀₆	-1185	1213
235	S ₁₀₇	-1235	1213
236	S ₁₀₈	-1285	1213
237	S ₁₀₉	-1335	1213
238	S ₁₁₀	-1385	1213
239	S ₁₁₁	-1435	1213
240	S ₁₁₂	-1485	1213
241	S ₁₁₃	-1535	1213
242	S ₁₁₄	-1585	1213
243	S ₁₁₅	-1635	1213
244	S ₁₁₆	-1685	1213
245	S ₁₁₇	-1735	1213
246	S ₁₁₈	-1785	1213
247	S ₁₁₉	-1835	1213
248	S ₁₂₀	-1885	1213
249	S ₁₂₁	-1935	1213
250	S ₁₂₂	-1985	1213

PAD No.	Terminal	X= um	Y= um
251	S ₁₂₃	-2035	1213
252	S ₁₂₄	-2085	1213
253	S ₁₂₅	-2135	1213
254	S ₁₂₆	-2185	1213
255	S ₁₂₇	-2235	1213
256	S ₁₂₈	-2285	1213
257	S ₁₂₉	-2335	1213
258	S ₁₃₀	-2385	1213
259	S ₁₃₁	-2435	1213
260	S ₁₃₂	-2485	1213
261	S ₁₃₃	-2535	1213
262	S ₁₃₄	-2585	1213
263	S ₁₃₅	-2635	1213
264	S ₁₃₆	-2685	1213
265	S ₁₃₇	-2735	1213
266	S ₁₃₈	-2785	1213
267	S ₁₃₉	-2835	1213
268	S ₁₄₀	-2885	1213
269	S ₁₄₁	-2935	1213
270	S ₁₄₂	-2985	1213
271	S ₁₄₃	-3035	1213
272	S ₁₄₄	-3085	1213
273	S ₁₄₅	-3135	1213
274	S ₁₄₆	-3185	1213
275	S ₁₄₇	-3235	1213
276	S ₁₄₈	-3285	1213
277	S ₁₄₉	-3335	1213
278	S ₁₅₀	-3385	1213
279	S ₁₅₁	-3435	1213
280	S ₁₅₂	-3485	1213
281	S ₁₅₃	-3535	1213
282	S ₁₅₄	-3585	1213
283	S ₁₅₅	-3635	1213
284	S ₁₅₆	-3685	1213
285	DUMMY ₁₇	-4015	1213
286	DUMMY ₁₈	-4065	1213
287	DUMMY ₁₉	-4115	1213
288	DUMMY ₂₀	-4265	1063
289	DUMMY ₂₁	-4265	1013
290	DUMMY ₂₂	-4265	963
291	S ₁₅₇	-4265	913
292	S ₁₅₈	-4265	863
293	S ₁₅₉	-4265	813
294	C ₃₂	-4265	763
295	C ₃₃	-4265	713
296	C ₃₄	-4265	663
297	C ₃₅	-4265	613
298	C ₃₆	-4265	563
299	C ₃₇	-4265	513
300	C ₃₈	-4265	463

NJU6655B

■ BLOCK DIAGRAM



■ TERMINAL DISCRPTION

No.	SYMBOL	I/O	FUNCTION																				
1,2,57,58, 83 to 88, 125 to 130, 285 to 290, 327 to 330	DUMMY ₁ to DUMMY ₂₆		Dummy terminals. These are open terminals electrically.																				
13,19, 28 to 32 59,60,72, 78,82	V _{DD}	Power	Power supply terminal.																				
10,16, 33 to 35 53,54,75, 80	V _{SS}	GND	Ground terminal.																				
36 to 40	V _{SS2}	Power	Reference voltage for voltage booster.																				
55,56	V _{RS}	Power	External reference voltage input terminal. Normally open.																				
61,62 63,64 65,66 67,68 69,70	V ₁ V ₂ V ₃ V ₄ V ₅	Power	LCD driving voltage supplying terminal. When the internal voltage booster is not used, supply each level of LCD driving voltage from outside with following relation. $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{OUT}$ When the internal power supply is on, the internal circuits generate and supply following LCD bias voltage from V ₁ to V ₄ terminal. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Bias</th> <th>V₁</th> <th>V₂</th> <th>V₃</th> <th>V₄</th> </tr> </thead> <tbody> <tr> <td>1/5 Bias</td> <td>$V_5 + 4/5V_{LCD}$</td> <td>$V_5 + 3/5V_{LCD}$</td> <td>$V_5 + 2/5V_{LCD}$</td> <td>$V_5 + 1/5V_{LCD}$</td> </tr> <tr> <td>1/7 Bias</td> <td>$V_5 + 6/7V_{LCD}$</td> <td>$V_5 + 5/7V_{LCD}$</td> <td>$V_5 + 2/7V_{LCD}$</td> <td>$V_5 + 1/7V_{LCD}$</td> </tr> <tr> <td>1/9 Bias</td> <td>$V_5 + 8/9V_{LCD}$</td> <td>$V_5 + 7/9V_{LCD}$</td> <td>$V_5 + 2/9V_{LCD}$</td> <td>$V_5 + 1/9V_{LCD}$</td> </tr> </tbody> </table> (V _{LCD} =V _{DD} -V ₅)	Bias	V ₁	V ₂	V ₃	V ₄	1/5 Bias	$V_5 + 4/5V_{LCD}$	$V_5 + 3/5V_{LCD}$	$V_5 + 2/5V_{LCD}$	$V_5 + 1/5V_{LCD}$	1/7 Bias	$V_5 + 6/7V_{LCD}$	$V_5 + 5/7V_{LCD}$	$V_5 + 2/7V_{LCD}$	$V_5 + 1/7V_{LCD}$	1/9 Bias	$V_5 + 8/9V_{LCD}$	$V_5 + 7/9V_{LCD}$	$V_5 + 2/9V_{LCD}$	$V_5 + 1/9V_{LCD}$
Bias	V ₁	V ₂	V ₃	V ₄																			
1/5 Bias	$V_5 + 4/5V_{LCD}$	$V_5 + 3/5V_{LCD}$	$V_5 + 2/5V_{LCD}$	$V_5 + 1/5V_{LCD}$																			
1/7 Bias	$V_5 + 6/7V_{LCD}$	$V_5 + 5/7V_{LCD}$	$V_5 + 2/7V_{LCD}$	$V_5 + 1/7V_{LCD}$																			
1/9 Bias	$V_5 + 8/9V_{LCD}$	$V_5 + 7/9V_{LCD}$	$V_5 + 2/9V_{LCD}$	$V_5 + 1/9V_{LCD}$																			
45,46 47,48 51,52 49,50 43,44	C1 ⁺ C1 ⁻ C2 ⁺ C2 ⁻ C3 ⁻	O	Boosted capacitor connecting terminals used for voltage booster.																				
41,42	V _{OUT}	O	Voltage booster output terminal. Connect the boosted capacitor between this terminal and V _{SS2} .																				
71	VR	I	Voltage adjustment terminal Connect external feedback resistor to control the LCD driving voltage V ₅ . This terminal is effective when IRS="L".																				
20 to 27 (26, 27)	D ₀ to D ₇ (SCL, SI)	I/O	Data input/output terminals. P/S="H" : Tri-state bi-directional Data I/O terminal in 8-bit parallel operation. P/S="L" : D ₇ =Serial data input terminal. D ₆ =Serial data clock signal input terminal. D ₀ to D ₅ terminals are Hi-impedance. Data from SI is loaded at the rising edge of SCL and latched as the parallel data at 8th rising edge of SCL. When CS ₁ b="H", D ₀ to D ₇ terminals are Hi-impedance.																				
15	A0	I	Data discrimination signal input terminal. Connect to the Address bus of MPU. The data on the D ₀ to D ₇ is distinguished between Display data and Instruction by status of A0. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A0</th> <th>H</th> <th>L</th> </tr> </thead> <tbody> <tr> <td>Distinction</td> <td>Display Data</td> <td>Instruction</td> </tr> </tbody> </table>	A0	H	L	Distinction	Display Data	Instruction														
A0	H	L																					
Distinction	Display Data	Instruction																					
14	RESb	I	Reset terminal. When the RESb terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of RESb.																				

No.	SYMBOL	I/O	FUNCTION																															
11	CS _{1b}	I	Chip select terminal.																															
12	CS ₂	I	Data Input/Output are available during CS _{1b} ="L" and CS ₂ ="H".																															
18	RDb (E)	I	<p><In case of 80 Type MPU> RDb signal of 80 type MPU input terminal. Active "L" During this signal is "L", D₀ to D₇ terminals are output.</p> <p><In case of 68 Type MPU> Enable signal of 68 type MPU input terminal. Active "H"</p>																															
17	WRb (R/W)	I	<p><In case of 80 Type MPU> Connect to the 80 type MPU WRb signal. Active "L". The data on the data bus input synchronizing the rise edge of this signal.</p> <p><In case of 68 Type MPU> The read/write control signal of 68 type MPU input terminal.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>R/W</td> <td>H</td> <td>L</td> </tr> <tr> <td>State</td> <td>Read</td> <td>Write</td> </tr> </table>	R/W	H	L	State	Read	Write																									
R/W	H	L																																
State	Read	Write																																
76	C86	I	<p>MPU interface type selection terminal. This terminal must connect to V_{DD} or V_{SS}.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>C86</td> <td>H</td> <td>L</td> </tr> <tr> <td>State</td> <td>68 Type</td> <td>80 Type</td> </tr> </table>	C86	H	L	State	68 Type	80 Type																									
C86	H	L																																
State	68 Type	80 Type																																
77	P/S	I	<p>Serial or parallel interface selection terminal.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>P/S</th> <th>Chip Select</th> <th>Data/Instruction</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> <tr> <td>"H"</td> <td>CS_{1b},CS₂</td> <td>A0</td> <td>D₀toD₇</td> <td>RDb,WRb</td> <td>-</td> </tr> <tr> <td>"L"</td> <td>CS_{1b},CS₂</td> <td>A0</td> <td>SI(D₇)</td> <td>-</td> <td>SCL(D₆)</td> </tr> </table> <p>In case of the serial interface (P/S="L") RAM data and status read operation do not work in mode of the serial interface. RDb and WRb must be fixed "H" or "L", and D₀ to D₅ are high impedance.</p>	P/S	Chip Select	Data/Instruction	Data	Read/Write	Serial Clock	"H"	CS _{1b} ,CS ₂	A0	D ₀ toD ₇	RDb,WRb	-	"L"	CS _{1b} ,CS ₂	A0	SI(D ₇)	-	SCL(D ₆)													
P/S	Chip Select	Data/Instruction	Data	Read/Write	Serial Clock																													
"H"	CS _{1b} ,CS ₂	A0	D ₀ toD ₇	RDb,WRb	-																													
"L"	CS _{1b} ,CS ₂	A0	SI(D ₇)	-	SCL(D ₆)																													
74	CLS	I	<p>Terminal to select whether or enable or disable the display clock internal oscillator circuit.</p> <p>CLS="H" : Internal oscillator circuit is enable CLS="L" : Internal oscillator circuit is disabled (requires external input) When CLS="L", input the display clock through the CL terminal.</p>																															
73	M/S	I	<p>This terminal selects the master/slave operation for the NJU6655. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the LCD, synchronizing the LCD system.</p> <p>M/S = "H" : Master operation M/S = "L" : Slave operation</p> <p>The following is true depending on the M/S and CLS status:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>M/S</th> <th>CLS</th> <th>OSC.</th> <th>Power Supply Circuit</th> <th>CL</th> <th>FR</th> <th>FRS</th> <th>DOFb</th> </tr> <tr> <td rowspan="2">"H"</td> <td>"H"</td> <td>Available</td> <td>Available</td> <td>Output</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>"L"</td> <td>Not Avail.</td> <td>Available</td> <td>Input</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>"L"</td> <td>*</td> <td>Not Avail.</td> <td>Not Avail.</td> <td>Input</td> <td>Input</td> <td>Output</td> <td>Input</td> </tr> </table> <p style="text-align: right;">*:Don't Care</p>	M/S	CLS	OSC.	Power Supply Circuit	CL	FR	FRS	DOFb	"H"	"H"	Available	Available	Output	Output	Output	Output	"L"	Not Avail.	Available	Input	Output	Output	Output	"L"	*	Not Avail.	Not Avail.	Input	Input	Output	Input
M/S	CLS	OSC.	Power Supply Circuit	CL	FR	FRS	DOFb																											
"H"	"H"	Available	Available	Output	Output	Output	Output																											
	"L"	Not Avail.	Available	Input	Output	Output	Output																											
"L"	*	Not Avail.	Not Avail.	Input	Input	Output	Input																											
7	CL	I/O	<p>Display clock input/output terminal. The following is true depending on the M/S and CLS status.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>M/S</th> <th>CLS</th> <th>CL</th> </tr> <tr> <td rowspan="2">"H"</td> <td>"H"</td> <td>Output</td> </tr> <tr> <td>"L"</td> <td>Input</td> </tr> <tr> <td>"L"</td> <td>*</td> <td>Input</td> </tr> </table> <p style="text-align: right;">*:Don't Care</p>	M/S	CLS	CL	"H"	"H"	Output	"L"	Input	"L"	*	Input																				
M/S	CLS	CL																																
"H"	"H"	Output																																
	"L"	Input																																
"L"	*	Input																																

No.	SYMBOL	I/O	FUNCTION																				
6	FR	I/O	LCD alternating current signal I/O terminal. M/S="H" : Output M/S="L" : Input																				
4,9	SYNC	I/O	LCD synchronizing current signal I/O terminal. M/S="H" : Output M/S="L" : Input																				
8	DOFb	I/O	LCD Display blanking control terminal. M/S="H" : Output terminal. Display "On" = "H", Display "Off" = "L" M/S="L" : Input terminal. External control. Refer to the following table. <div style="margin-left: 20px; border: 1px solid black; padding: 5px; width: fit-content;"> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th rowspan="2">Instruction</th> <th colspan="2">DOFb</th> </tr> <tr> <th>H</th> <th>L</th> </tr> </thead> <tbody> <tr> <td>Display On</td> <td>On</td> <td>Off</td> </tr> <tr> <td>Display Off</td> <td>Off</td> <td>Off</td> </tr> </tbody> </table> </div>	Instruction	DOFb		H	L	Display On	On	Off	Display Off	Off	Off									
Instruction	DOFb																						
	H	L																					
Display On	On	Off																					
Display Off	Off	Off																					
81	IRS	I	Internal Feedback Resistor Select IRS="H" : Internal feedback IRS="L" : External feedback resistor This setting is effective in the master operation. It is ineffective in the slave operation but should be fixed to "H" or "L".																				
5	FRS	O	The output terminal for the static drive. This terminal is used in conjunction with the SYNC terminal.																				
89 to 120	C ₃₁ to C ₀	O	LCD driving signal output terminals. -Common output terminals : C ₀ to C ₆₃ -Segment output terminals : S ₀ to S ₁₅₉ Common output terminals The following output voltages are selected by the combination of alternating (FR) signal and Common scanning data.																				
122 to 124, 131 to 284, 291 to 293	S ₀ to S ₁₅₉	O	<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Scan Data</th> <th>FR</th> <th>Output Voltage</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>V₅</td> </tr> <tr> <td>L</td> <td>V_{DD}</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>V₁</td> </tr> <tr> <td>L</td> <td>V₄</td> </tr> </tbody> </table>	Scan Data	FR	Output Voltage	H	H	V ₅	L	V _{DD}	L	H	V ₁	L	V ₄							
Scan Data	FR	Output Voltage																					
H	H	V ₅																					
	L	V _{DD}																					
L	H	V ₁																					
	L	V ₄																					
294 to 325	C ₃₂ to C ₆₃	O	Segment output terminals The following output voltages are selected by the combination of alternating (FR) signal and display data in the RAM. <div style="margin-left: 20px; border: 1px solid black; padding: 5px; width: fit-content;"> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th rowspan="2">RAM Data</th> <th rowspan="2">FR</th> <th colspan="2">Output Voltage</th> </tr> <tr> <th>Normal</th> <th>Reverse</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>V_{DD}</td> <td>V₂</td> </tr> <tr> <td>L</td> <td>V₅</td> <td>V₃</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>V₂</td> <td>V_{DD}</td> </tr> <tr> <td>L</td> <td>V₃</td> <td>V₅</td> </tr> </tbody> </table> </div>	RAM Data	FR	Output Voltage		Normal	Reverse	H	H	V _{DD}	V ₂	L	V ₅	V ₃	L	H	V ₂	V _{DD}	L	V ₃	V ₅
RAM Data	FR	Output Voltage																					
		Normal	Reverse																				
H	H	V _{DD}	V ₂																				
	L	V ₅	V ₃																				
L	H	V ₂	V _{DD}																				
	L	V ₃	V ₅																				
121,326	COMM	O	COM output terminals for the indicator. Both terminals output the same signal. Leave these open if they are not used.																				
3	TEST ₁	O	Maker test only. Normally open.																				
79	TEST ₂	I	Maker test only. This terminal must connect to V _{SS} .																				

■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1-1) Busy Flag (BF)

During internal operation, the LSI is being busy and can't accept any instructions except "status read". The BF data is output through D₇ terminal by the "status read" instruction.

When the cycle time (tcyc) mentioned in the "AC characteristics" is satisfied, the BF check isn't required after each instruction, so that MPU processing performance can be improved.

(1-2) Initial display line register

The initial display line register assigns a DDRAM line address, which corresponds to COM₀ by "initial display line set" instruction. It is used for not only normal display but also vertical display scrolling and page switching without changing the contents of the DDRAM.

However, the 65th address for icon display can't be assigned for initial display line address.

(1-3) Line counter

The line counter provides a DDRAM line address. It initializes its contents at the switching of frame timing signal (FR), and also counts-up in synchronization with common timing signal.

(1-4) Column address counter

The column address counter is an 8-bit preset counter, which provides a DDRAM column address, and it is independent of below-mentioned page address register.

It will increment (+1) the column address whenever "display data read" or "display data write" instructions are issued. However, the counter will be locked when no-existing address above A0_H are addressed. The count-lock will be able to be released by the "column address set" instruction again. The counter can invert the correspondence between the column address and segment driver direction by means of "ADC set" instruction.

(1-5) Page address register

The page address register provides a DDRAM page address.

The last page address "8" should be used for icon display because the only D₀ is valid.

(1-6) Display data RAM (DDRAM)

The DDRAM contains 10,400-bit, and stores display data, which are 1-to-1 correspondents to LCD panel pixels.

When normal display mode, the display data "1" turns on and "0" turns off LCD pixels. When inverse display mode, "1" turns off and "0" turns on.

Page Address	Data	Display Pattern	Line Address	Common Driver
D3,D2,D1,D0 (0,0,0,0)	D0	PAGE 0	00 _H	C56
	D1		01	C57
	D2		02	C58
	D3		03	C59
	D4		04	C60
	D5		05	C61
	D6		06	C62
	D7		07	C63
D3,D2,D1,D0 (0,0,0,1)	D0	PAGE 1	08	C0
	D1		09	C1
	D2		0A	C2
	D3		0B	C3
	D4		0C	C4
	D5		0D	C5
	D6		0E	C6
	D7		0F	C7
D3,D2,D1,D0 (0,0,1,0)	D0	PAGE 2	10	C8
	D1		11	C9
	D2		12	C10
	D3		13	C11
	D4		14	C12
	D5		15	C13
	D6		16	C14
	D7		17	C15
⋮ ⋮ ⋮ ⋮	D0	⋮	18	C16
	D1		19	C17
	⋮		1A	C18
	⋮		⋮	⋮
	⋮		⋮	⋮
	⋮		⋮	⋮
	⋮		⋮	⋮
	⋮		⋮	⋮
D3,D2,D1,D0 (0,1,1,1)	D0	PAGE 7	36	C46
	D1		37	C47
	D2		38	C48
	D3		39	C49
	D4		3A	C50
	D5		3B	C51
	D6		3C	C52
	D7		3D	C53
(1,0,0,0)	D0	PAGE 8	3E	C54
	D1		3F	C55
	D2			
	D3			
	D4			
	D5			
	D6			
	D7			

Column Address	ADC	D0="0"	00	01	02	03	04	05	06		9E	9F
		D0="1"	9F	9E	9D	9C	9B	9A	99	←	01	00
		Segment Drivers	0	1	2	3	4	5	6	-----	158	159

Fig.1 Display data RAM (DDRAM) Map

For example the Initial display is 08_H.

* : COMM is independent of the “Initial display line set” instruction and always corresponds to the 65th line.

(1-7) Common direction register

The common direction register is selected by the "Partial Select" and "Common Direction Register Set" instructions as shown in Table 1. When using the partial display function, the COM₀ - COM₁₅ and COM₄₈ - COM₆₃ terminals cannot be used.

Table 1. Common direction

Partial Select	Common Direction Register Set	Common drivers				
D ₀	D ₃	PAD No.	114	83	309	278
0	0	Pin name	C ₀	C ₃₁	C ₆₃	C ₃₂
0	1		COM ₀ →	COM ₃₁	COM ₆₃ ←	COM ₃₂
			COM ₆₃ ←	COM ₃₂	COM ₀ →	COM ₃₁
		PAD No.	98	83	293	278
1	0	Pin name	C ₁₆	C ₃₁	C ₄₇	C ₃₂
1	1		COM ₁₆ →	COM ₃₁	COM ₄₇ ←	COM ₃₂
			COM ₄₇ ←	COM ₃₂	COM ₁₆ →	COM ₃₁

(1-8) Reset circuit

The reset circuit initializes the LSI to the following status by using of the reset signal into the RESb terminal.

-Reset status using the RESb terminal:

1. Display off
2. Normal display (Non-inverse display)
3. ADC select : Normal mode (D₀="0")
4. Power control register clear : D₂,D₁,D₀="0,0,0"
5. Serial interface register clear
6. LCD bias select : D₁,D₀="0,0"(1/9 bias)
7. Power save reset
8. Entire display off : Normal mode
9. Internal oscillation circuit stop
10. Partial select : D₀="0"(1/65 duty)
11. Static indicator off
Static indicator register : D₁,D₂="0,0"
12. Read modify write off
13. Initial display line address : 00_H
14. Column address : 00_H
15. Page address : 0 page
16. Common direction register : D₃="0"(Normal)
17. Feedback resistors ratio : D₂,D₁,D₀="0,0,0"
18. EVR mode off and EVR register: D₅,D₄,D₃,D₂,D₁,D₀="1,0,0,0,0,0"
19. n-line inverse drive register : D₃,D₂,D₁,D₀="0,0,0,0"(n-line inverse reset)
20. Test mode reset (Test mode 1 and Test mode 2)

The RES terminal should be connected to MPU's reset terminal, and the reset operation should be executed at the same timing of the MPU reset. As described in the "BUS TIMING CHARACTERISTICS", it is necessary to input 1.5us(min.) or over "L" level signal into the RES terminal in order to carry out the reset operation. The LSI will return to normal operation after about 1.5us(max.) from the rising edge of the reset signal.

The reset operation by RESb="L" initializes each register setting as above reset status, but the internal oscillation circuit and output terminals (D₀ to D₇) are not affected.

The reset operation is necessary to avoid malfunctions.

Note 1) The "Reset" instruction in Table.4 can't be substituted for the reset operation by using of the RES terminal. It executes above-mentioned only 11 to 20 items.

Note 2) The reset terminal is susceptible to external noise, so design PCB layout in consideration for the noise.

Note 3) In case of using external power supply for LCD driving voltage, the RESb terminal is required to be being "L" level when the external power supply is turned-on.

(1-9) LCD driving circuits

(a) Common and segment drivers

LCD drivers consist of 64-common drivers, 160-segment drivers and 1-icon-common driver.

As shown in “■ LCD driving waveform”, LCD driving waveforms are generated by the combination of display data, common timing signal and internal FR timing signal.

(b) Display data latch circuit

The display data latch circuit temporally stores 160-bit display data transferred from the DDRAM in the synchronization with the common timing signal, and then it transfers these stored data to the segment drivers.

“Display on/off”, “inverse display on/off” and “entire display on/off” instructions control only the contents of this latch circuit, they can’t change the contents of the DDRAM.

In addition, the LCD display isn’t affected by the DDRAM access during its displaying because the data read-out timing from this latch circuit to the segment drivers is independent of accessing timing to the DDRAM.

(c) Line counter and latch signal or latch Circuits

The clock line counter and latch signal to the latch circuits are generated from the internal display clock (CL). The line address of display data RAM is renewed synchronizing with display clock (CL).

160bits display data are latched in display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display timing generator

The display timing generates the timing signal for the display system by combination of the master clock CL and driving signal FR (refer to Fig.2) The frame signal FR and LCD alternative signal generate LCD driving waveform on the 2-frame alternative driving method or the n-line inverse driving method.

(e) Common timing generation

The common timing is generated by display clock CL (refer to Fig.2)

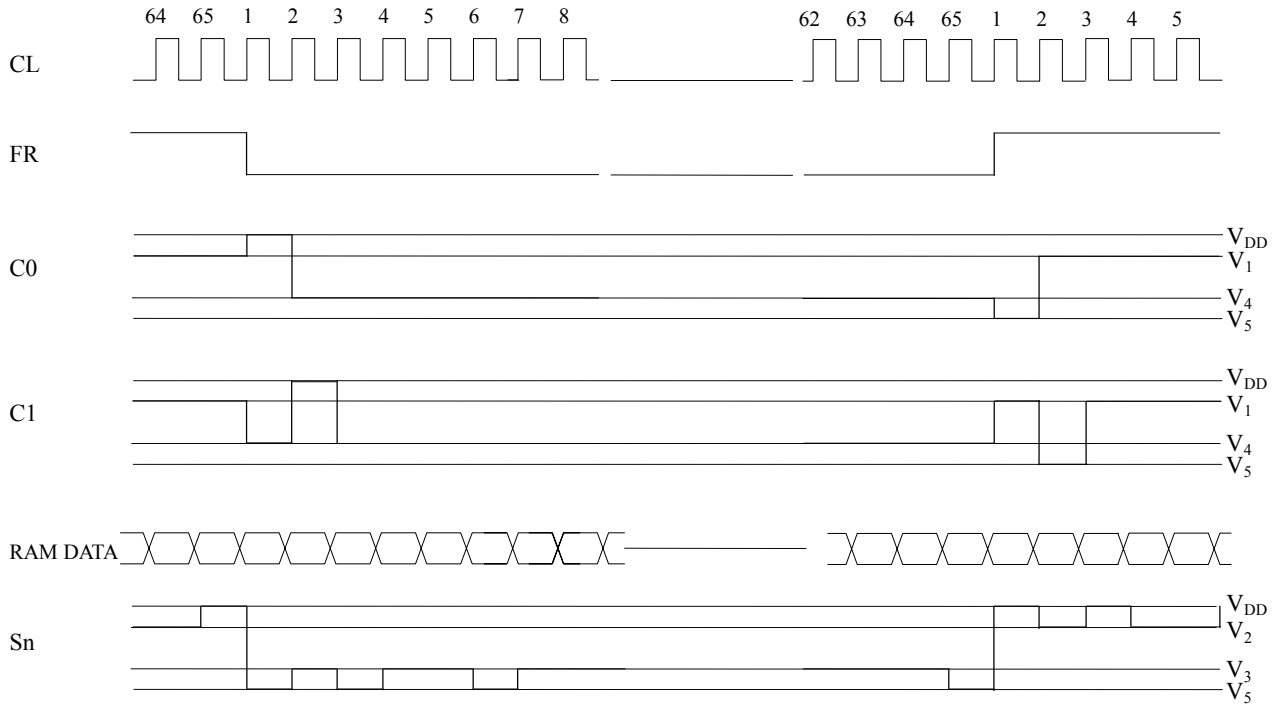


Fig.2-1 2-frame alternating drive mode

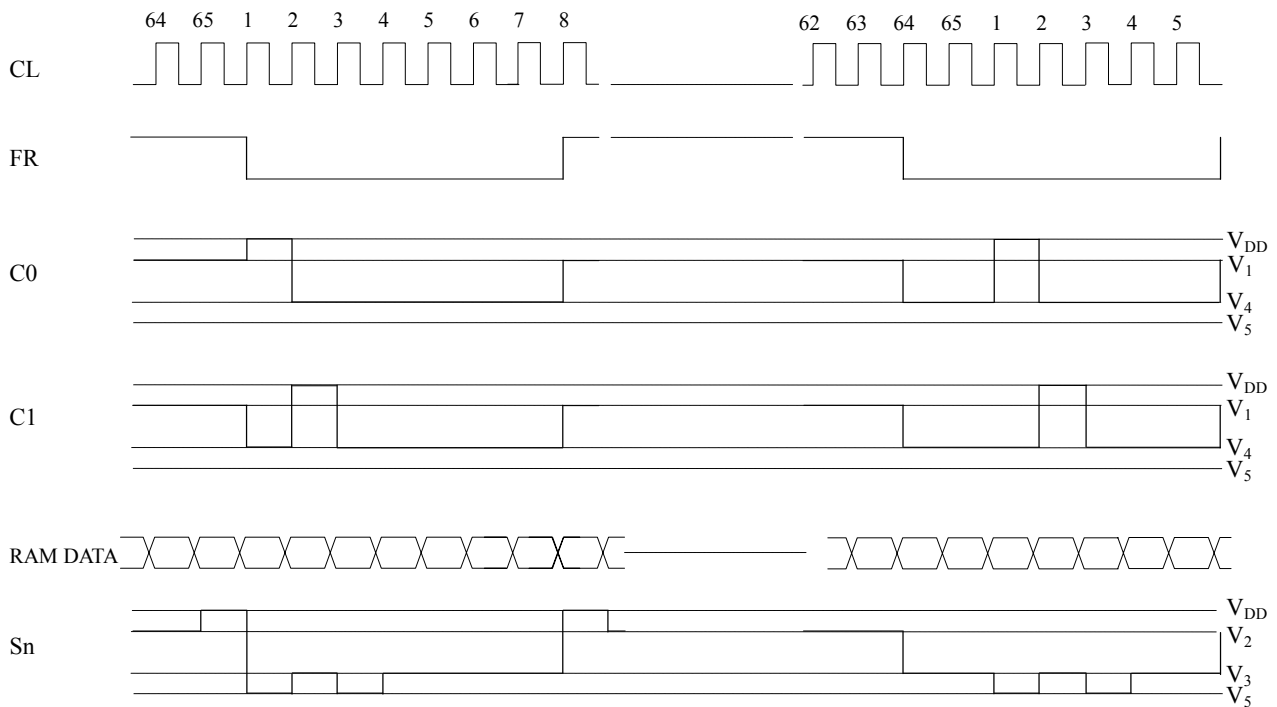


Fig.2-2 n-line inverse drive mode (n=7, line inverting register sets to 6)

(f) Oscillator

This is the low power consumption CR oscillator which provides the display clock and voltage converter timing clock.

(g) Internal power circuits

The internal power circuits are composed of x4 boost voltage converter, output voltage regulator including 64-step EVR and voltage followers.

The optimum values of the external passive components for the internal power circuits, such as capacitors for V_1 to V_5 terminals and feed back resistors for VR terminal, depend on LCD panel size. Therefore, it is necessary to evaluate the actual LCD module with these external components in order to determine the optimum values.

Each portion of the internal power circuits is controlled by “power control set” instruction as shown in Table.2. In addition, the combination of power supply circuits is described in Table.3.

Table.2 Power control set

Portions		Status	
		“1”	“0”
D ₂	Voltage converter	ON	OFF
D ₁	Voltage regulator	ON	OFF
D ₀	Voltage followers	ON	OFF

Table.3 Power supply combinations

Status	D ₂	D ₁	D ₀	Voltage converter	Voltage regulator	Voltage followers	External voltage	Capacitor terminals
1) Using all internal power circuits	1	1	1	ON	ON	ON	V _{SS2}	Use
2) Using voltage regulator and Voltage followers	0	1	1	OFF	ON	ON	V _{OUT} , V _{SS2}	Open
3) Using voltage followers	0	0	1	OFF	OFF	ON	V _{OUT} , V ₅ , V _{SS2}	Open
4) Using only external power supply	0	0	0	OFF	OFF	OFF	V _{OUT} , V ₁ ~V ₅	Open

* Capacitor input terminals: C1+, C1-, C2+, C2-, C3-

* Do not use other combinations except examples in Table.3.

The internal LCD power supply is designed to drive small LCD panels such as cellular phones. Thus, if the IC is used to drive a large panel, make sure whether it works with the internal power supply or needs an external power supply.

The selections of external components for the LCD bias circuit, the voltage booster and the feedback loop depend on panel sizes, so make sure what are the best values in the particular application.

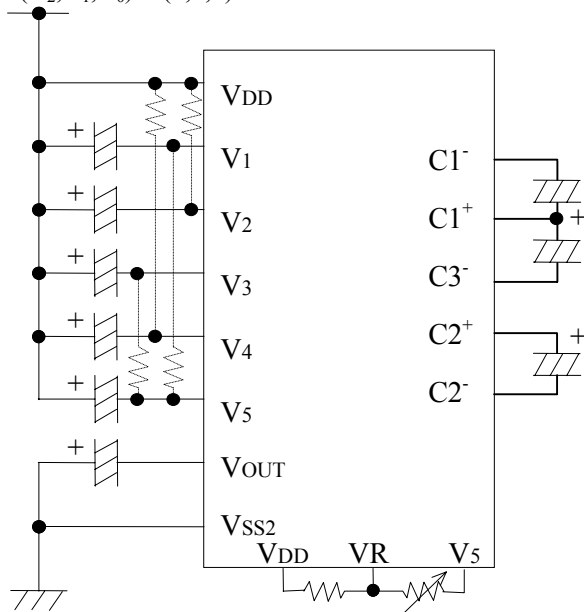
○Power Supply applications

Power Control Instruction

- D₂ : Boost Circuit
- D₁ : Voltage Regulator
- D₀ : Voltage Follower

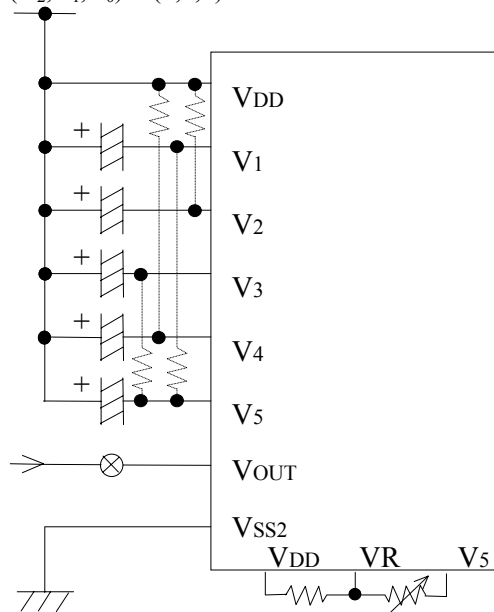
(1) Internal power supply Example.

All of the Internal Booster, Voltage Regulator, Voltage Follower using
(D₂,D₁,D₀) = (1,1,1)



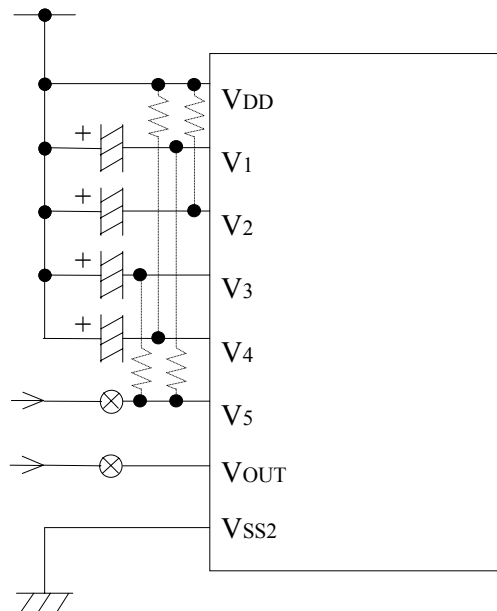
(2) Only V_{OUT} Supply from outside Example.

Internal Voltage Regulator, Voltage Follower using.
(D₂,D₁,D₀) = (0,1,1)



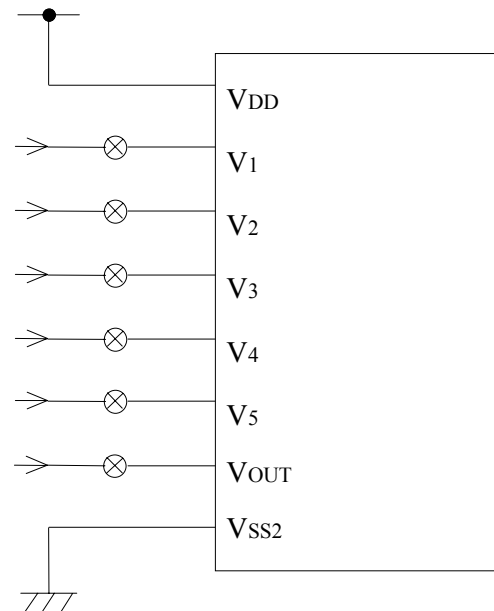
(3) V_{OUT} and V₅ Supply from outside Example.

Internal Voltage Follower using.
(D₂,D₁,D₀) = (0,0,1)



(4) External Power Supply Example.

All of V₁ to V₅ and V_{OUT} supply from outside
(D₂,D₁,D₀) = (0,0,0)



⊗ : These switches should be open during the power save mode.

Note) : When using the voltage follower circuit, external resistors may be necessary to stabilize V₁, V₂, V₃ and V₄ voltages.

(2) Instruction set

The **NJU6655B** distinguishes the signal on the data bus D_0 to D_7 as an Instruction by combination of A_0 , RDb and $WRb(R/W)$. The decode of the instruction and execution performs with only high speed Internal timing without relation to the external clock. Therefore no busy flag check required normally. In case of serial interface, the data input as $MSB(D_7)$ first serially. The Table. 4-1,4-2 shows the instruction codes of the **NJU6655B**.

Table. 4-1 Instruction table

(*: Don't Care)

Instruction		Instruction code										Description	
		A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁		D ₀
(a)	Display On/Off	0	1	0	1	0	1	0	1	1	1	0/1	LCD Display On/Off $D_0=0$:Off $D_0=1$:On
(b)	Initial Display Line Set	0	1	0	0	1	Line Address					Determine the Display Line of RAM to COM_0	
(c)	Page Address Set	0	1	0	1	0	1	1	Page Address			Set the page of DD RAM to the Page Address Register	
(d)	Column Address Set Upper Order 4bits	0	1	0	0	0	0	1	Upper Order Column Address			Set the Upper order 4 bits Column Address to the Register	
	Column Address Set Lower Order 4bits	0	1	0	0	0	0	0	Lower Order Column Address			Set the Lower order 4 bits Column Address to the Register	
(e)	Status Read	0	0	1	Status			0	0	0	0	Read out the internal Status	
(f)	Write Display Data	1	1	0	Write Data						Write the data into the Display Data RAM		
(g)	Read Display Data	1	0	1	Read Data						Read the data from the Display Data RAM		
(h)	ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	Set the DD RAM vs Segment $D_0=0$:Normal $D_0=1$:Inverse
(i)	Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0/1	Inverse the On and Off Display $D_0=0$:Normal $D_0=1$:Inverse
(j)	Whole Display On/Off	0	1	0	1	0	1	0	0	1	0	0/1	Whole Display Turns On $D_0=0$: Normal $D_0=1$: Whole Disp. On
(k)	LCD Bias Select	0	1	0	1	0	0	1	0	0	Bias		Select the Bias
(l)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Address Register when writing but no-change when reading
(m)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify write Mode
(n)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the Internal Circuits
(o)	Common Direction Select	0	1	0	1	1	0	0	0/1	*	*	*	Set the scanning order of common drivers to the Register $D_3=0$: Normal, $D_3=1$: Inverse
(p)	Power Control Set	0	1	0	0	0	1	0	1	Operating Mode		Set the status of internal power circuits	
(q)	Feedback Resistor Ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio		Set the status of internal resistors ratio (Rb/Ra)	

Table. 4-2 Instruction table

(*: Don't Care)

Instruction		Instruction code											Description
		A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
(r)	EVR Mode Set	0	1	0	1	0	0	0	0	0	0	1	Set EVR mode
	EVR Register Set	0	1	0	*	*	Setting Data					0	Set the V ₅ output level to the EVR register
(s)	Static Indicator On/Off	0	1	0	1	0	1	0	1	1	0	0/1	D ₀ =0 : Off, D ₀ =1 : On
	Static Indicator Register Set	0	1	0	*	*	*	*	*	*	Mode		Set static indicator register
(t)	Power Save	0	1	0	1	0	1	0	1	0	0	0/1	D ₀ =0 : Standby mode D ₀ =1 : Sleep mode
(u)	Power Save Reset	0	1	0	1	1	1	0	0	0	0	1	Release from the Power Save Mode
(v)	n-line Inverse Drive Register Set	0	1	0	0	0	1	1	Number of Inverse Lines			0	Set the number of inverse drive line
(w)	n-line Inverse Drive Reset	0	1	0	1	1	1	0	0	1	0	0	Release the line inverse drive
(x)	Partial Select	0	1	0	1	0	1	0	0	0	1	0/1	D ₀ =0 : Off (1/65 Duty) D ₀ =1 : On (1/33 Duty)
(y)	Internal Oscillation Circuit On	0	1	0	1	0	1	0	1	0	1	1	Start the operation of the Internal Oscillation circuit
(z)	NOP	0	1	0	1	1	1	0	0	0	1	1	

(2-1) Explanation of Instruction Code

(a) Display On/Off

This instruction selects display turn-on or turn-off regardless of the contents of the DDRAM.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off

 1: Display On

(b) Initial Display Line Set

This instruction specifies the DDRAM line address which corresponds to the COM₀ position.

By means of repeating this instruction, the initial display line address will be dynamically changed; it means smooth display scrolling will be enabled.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	1	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀

A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Line Address (HEX)
0	0	0	0	0	0	00
0	0	0	0	0	1	01
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	1	3F

(c) Page Address Set

In order to access to the DDRAM for writing or reading display data, both “page address set” and “column address set” instructions are required before accessing.

The last page address “8” should be used for icon display because the only D₀ is valid.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	1	A ₃	A ₂	A ₁	A ₀

A ₃	A ₂	A ₁	A ₀	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
:	:	:	:	:
1	0	0	0	8

(d) Column Address Set

As above-mentioned, in order to access to the DDRAM for writing or reading display data, it is necessary to execute both “page address set” and “column address set” before accessing. The 8-bit column address data will be valid when both upper 4-bit and lower 4-bit data are set into the column address register.

Once the column address is set, it will automatically increment (+1) whenever the DDRAM will be accessed, so that the DDRAM will be able to be continuously accessed without “column address set” instruction.

The column address will stop increment and the page address will not be changed when the last address 9F_H is addressed.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
0	1	0	0	0	0	1	A ₇	A ₆	A ₅	A ₄	Upper 4-bit
0	1	0	0	0	0	0	A ₃	A ₂	A ₁	A ₀	Lower 4-bit

A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Column Address (HEX)	
0	0	0	0	0	0	0	0	00	
0	0	0	0	0	0	0	1	01	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
1	0	0	1	1	1	1	1	9F	

(e) Status Read

This instruction reads out the internal status regarding “busy flag”, “ADC select”, “display on/off” and “reset”.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : When D₇ is “1”, the LSI is being busy and can’t accept any instructions.

ADC : It shows the correspondence between the column address and segment drivers.
 When D₆ is “0”, the column address (159-n) corresponds to segment driver n.
 When D₆ is “1”, the column address (n) corresponds to segment driver n.
 Please be careful that read out data is opposite of “ADC select” instruction data.

ON/OFF : It shows display on or off status.
 When D₅ is “0”, the LSI is in display-on status.
 When D₅ is “1”, the LSI is in display-off status.
 Please be careful that read out data is opposite of “Display On/Off” instruction data.

RESET : It shows reset status.
 When D₄ is “0”, the LSI is in normal operation.
 When D₄ is “1”, the LSI is during reset operation.

(f) Display Data Write

This instruction writes display data into the selected column address on the DDRAM.

The column address automatically increments (+1) whenever the display data is written by this instruction, so that this instruction can be continuously issued without “column address set” instruction.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	Write Data							

(g) Display Data Read

This instruction reads out the display data stored in the selected column address on the DDRAM. The column address automatically increments (+1) whenever the display data is read out by this instruction, so that this instruction can be continuously issued without "column address set" instruction. After the "column address set" instruction, a dummy read will be required, please refer to the (4-4). In case of using serial interface mode, this instruction can't be used.

A0	RD _b	WR _b	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	Read Data							

(h) ADC Select

This instruction selects segment driver direction. The correspondence between the column address and segment driver direction is shown in Fig.1. This function reduces the restrictions on the IC position of an LCD module.

A0	RD _b	WR _b	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	0	0	0	D

- D 0: Clockwise Output (Normal) Segment Driver S₀ to S₁₅₉
 1: Counterclockwise Output (Inverse) Segment Driver S₁₅₉ to S₀

(i) Inverse Display On/Off

This instruction inverses the status of turn-on or turn-off of entire LCD pixels. It doesn't change the contents of the DDRAM.

A0	RD _b	WR _b	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	0	1	1	D

- D 0: Normal RAM data "1" correspond to "On"
 1: Inverse RAM data "0" correspond to "On"

(j) Whole Display On/Off

This instruction turns on entire LCD pixels regardless the contents of the DDRAM. It doesn't change the contents of DDRAM. This instruction should be performed prior to the "Inverse display On/Off" instruction.

A0	RD _b	WR _b	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	0	1	0	D

- D 0: Normal Display (Whole Display Off)
 1: Whole Display Turns On (Whole Display On)

(k) Bias Select

This instruction selects LCD bias value.

A0	RD _b	WR _b	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	0	1	0	0	A ₁	A ₀

A ₁	A ₀	LCD Bias
0	0	1/9
0	1	1/7
1	0	1/5
1	1	Prohibited*

* : Because it may malfunction-operate, do not set (D₁,D₀) = (1,1).

(l) Read Modify Write

This instruction controls column address increment.

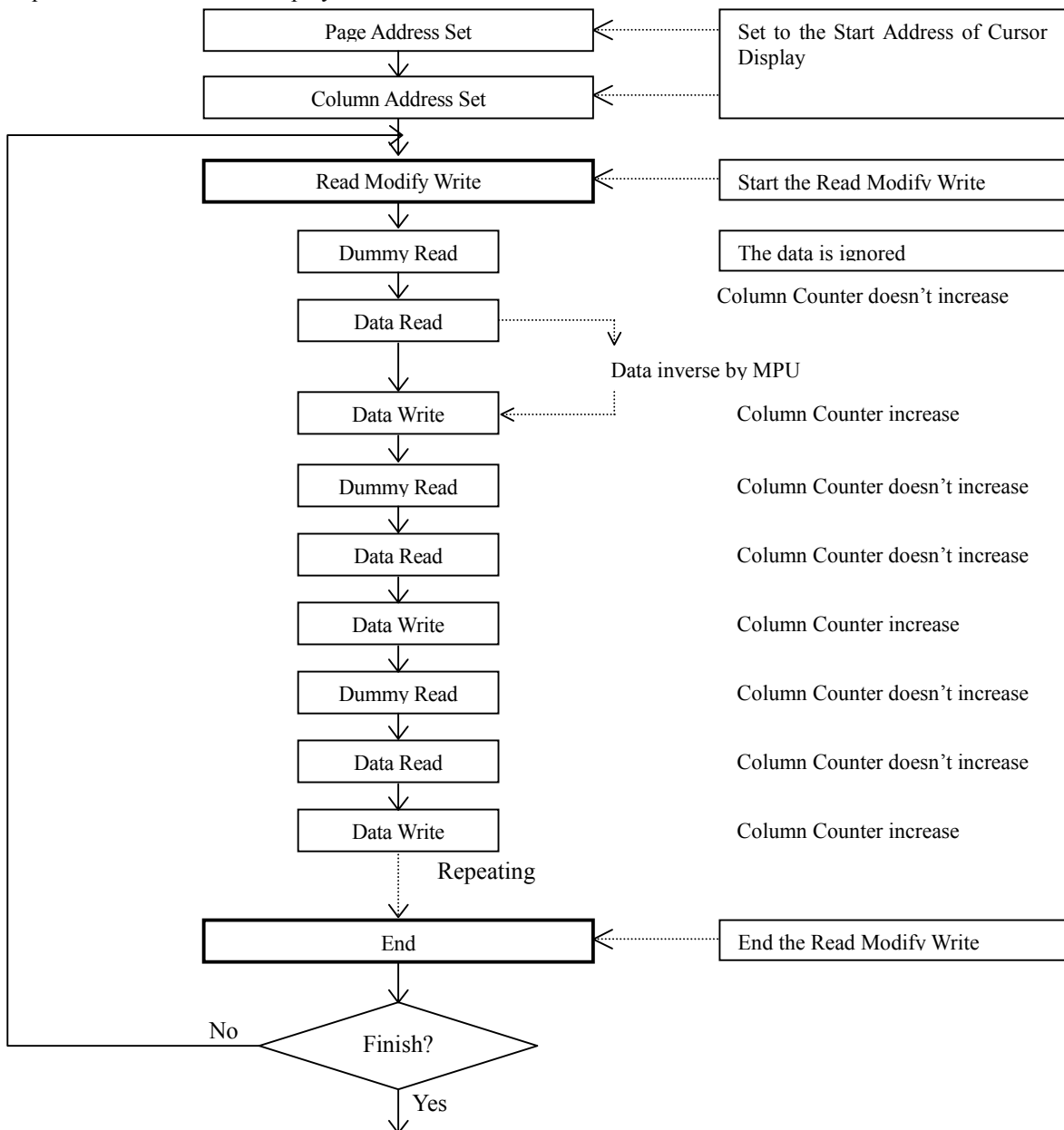
By using of this instruction, the column address can't increment when read operation but it can increment when write operation. This status will be continued until the below-mentioned "end" instruction will be issued.

This instruction can reduce the load of MPU, during the display data in specific DDRAM area is repeatedly changed for cursor blink or others.

A0	RDb	WRb	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note) In this "Read Modify Write" mode, out of display data "Read" / "Write", any instructions except "Column Address Set" can be executed.

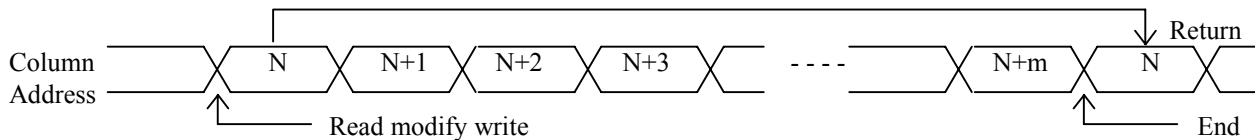
- The Sequence of Cursor Blink Display



(m) End

The “end” instruction cancels the read modify write mode and makes the column address return to the initial value just before “read modify write” is started.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	1	0	1	1	1	0



(n) Reset

This instruction reset the LSI to the following status, however it doesn't change the contents of the DDRAM. Please be careful that it can't be substituted for the reset operation by using of the RESb terminal.

Reset status by “reset” instruction:

- 1: Static indicator register : D₁,D₀ = “0,0”
- 2: Read modify write off
- 3: Initial display line address : 00_H
- 4: Column address : 00_H
- 5: Page address : 0 page
- 6: Common direction register : D₃=”0”(Normal mode)
- 7: Feedback resistors ratio : D₂,D₁,D₀ = “0,0,0”
- 8: EVR mode off and EVR register : D₅,D₄,D₃,D₂,D₁,D₀ = “1,0,0,0,0,0”
- 9: n-line inverse drive register : D₃,D₂,D₁,D₀ = “0,0,0,0”
- 10: Test mode reset (Test mode 1 and Test mode 2)

The DD RAM is not affected of this initialization.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	1	0	0	0	1	0

(o) Common Driver Direction Select

This instruction selects common driver direction.
Please refer to (1-7) common driver direction for more detail.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	0	0	D ₃	*	*	*

(*: Don't Care)

- D₃ 0: Normal Common driver direction (C₀ to C₆₃) or (C₁₆ to C₄₇)
- 1: Inverse Common driver direction (C₆₃ to C₀) or (C₄₇ to C₁₆)

(p) Power Control Set

This instruction controls the status of internal power circuits. Please refer to the (1-9) LCD Driving Circuits (g) internal power circuits for more detail.

A0	RDb	WRb	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A ₂	A ₁	A ₀

- A₂ 0: Voltage Converter Off
1: Voltage Converter On
- A₁ 0: Voltage Regulator Off
1: Voltage Regulator On
- A₀ 0: Voltage Followers Off
1: Voltage Followers On

Note) The internal power supply must be Off when external power supply using.

* The wait time depends on the C₄ to C₈, C_{OUT} capacitors, and V_{DD} and V_{LCD} Voltage.
Therefore it requires the actual evaluation using the LCD module to get the correct time.

(q) Feedback Resistor Ratio Set

This instruction is used to determine the internal feedback resistor ratio.
Please refer to the (3-2) Voltage Adjust Circuits for more detail.

A0	RDb	WRb	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	A ₂	A ₁	A ₀

A ₂	A ₁	A ₁	Internal resistor ratio 1+(Rb/Ra)	V _{LCD} 1+(Rb/Ra)
0	0	0	4.5	Minimum
0	0	1	5.0	:
0	1	0	5.5	:
0	1	1	6.0	:
1	0	0	6.5	:
1	0	1	7.0	:
1	1	0	7.6	:
1	1	1	8.1	Maximum

(r) EVR Set

1) EVR mode set

This instruction sets the LSI into the EVR mode, and it is always used by the combination with “EVR register set”. The LSI can't accept any instructions except the “EVR register set” during the EVR set mode. This mode will be released after the “EVR register set” instruction.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	0	0	0	0	0	1

2) EVR Register Set

This instruction sets 6-bit data into the EVR register to determine the output voltage “V₅” of the internal voltage regulator.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀

(*: Don't Care)

A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	V _{LCD}
0	0	0	0	0	0	Minimum
0	0	0	0	0	1	:
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	1	Maximum

(s) Static Indicator

1) Static Indicator On/Off

This instruction selects static indicator turn-on or turn-off, and it is always used by the combination with the “static indicator register set”.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	1	1	0	D

D 0: Static Indicator Off
 1: Static Indicator On

2) Static Indicator Register Set

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	*	*	*	*	*	*	A ₁	A ₀

(*: Don't Care)

A ₁	A ₀	Indicator display Status
0	0	Off
0	1	On (Blink at 1.0s intervals)
1	0	On (Blink at 0.5s intervals)
1	1	On (Turn on at all time)

(t) Power Save

This instruction sets the LSI into the power save mode. This instruction is reducing operating current as well as static operations.

The internal status and the contents of the DDRAM will be remained just before the “Power save” instruction. In addition, the DDRAM can be accessed during the power save mode.

There are two power save modes, sleep mode and standby mode.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	1	0	0	D

D 0: Standby Mode
 1: Sleep Mode

<Sleep Mode>

All functions are halted so that its operating current is reduced as low as standby current.

All LCD system stops as follows,

- 1) Oscillator and internal power circuits stop.
- 2) All common and segment drivers output V_{DD} level.

<Standby Mode>

A part of functions are halted. The only static drive system as the indicator operates.

The LCD system except the static indicator stops as follows,

- 1) Internal power circuits stop. (Oscillator is operating.)
- 2) LCD driving is stopped. All common and segment drivers output V_{DD} level.
- 3) The only static indicator is working.

(u) Power Save Reset

This instruction releases the power save mode.

A0	RDb	WRb	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	1	0	0	0	0	1

(v) n-line Inverse Drive Register Set

This instruction specifies the number of n-line. Please refer to the (1-9)LCD Driving Circuits (e)Common timing generation Fig.2-1, Fig.2-2 for more detail.

A0	RDb	WRb	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	A ₃	A ₂	A ₁	A ₀

A ₃	A ₂	A ₁	A ₀	Inverse Lines
0	0	0	0	-(*)
0	0	0	1	2
0	0	1	0	3
⋮	⋮	⋮	⋮	⋮
1	1	1	0	15
1	1	1	1	16

(*) 2-frame alternating drive mode.

(w) n-line Inverse Drive Reset

This instruction releases n-line inversion, but does not change the contents of the n-line register.

A0	RDb	WRb	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	0	0

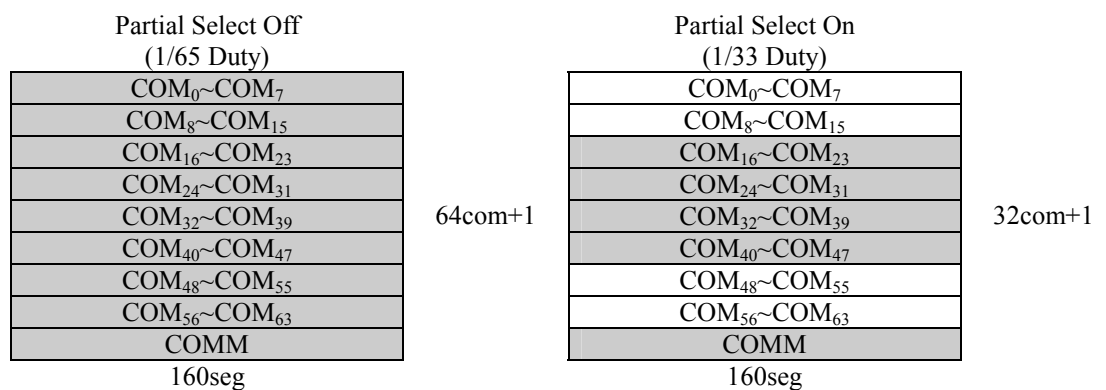
(x) Patial Select

This instruction starts the partial mode operation.

A0	RDb	WRb	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

- D 0: 1/65 Duty (Partial Select Off)
 1: 1/33 Duty (Partial Select On)

Display structure by Partial Select On / Off



Active Display-block

(y) Internal Oscillation Circuit On

This setting is effective when M/S="1" and CLS="1".

A0	RDb	WRb	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	1

(z)NOP

Non Operation.

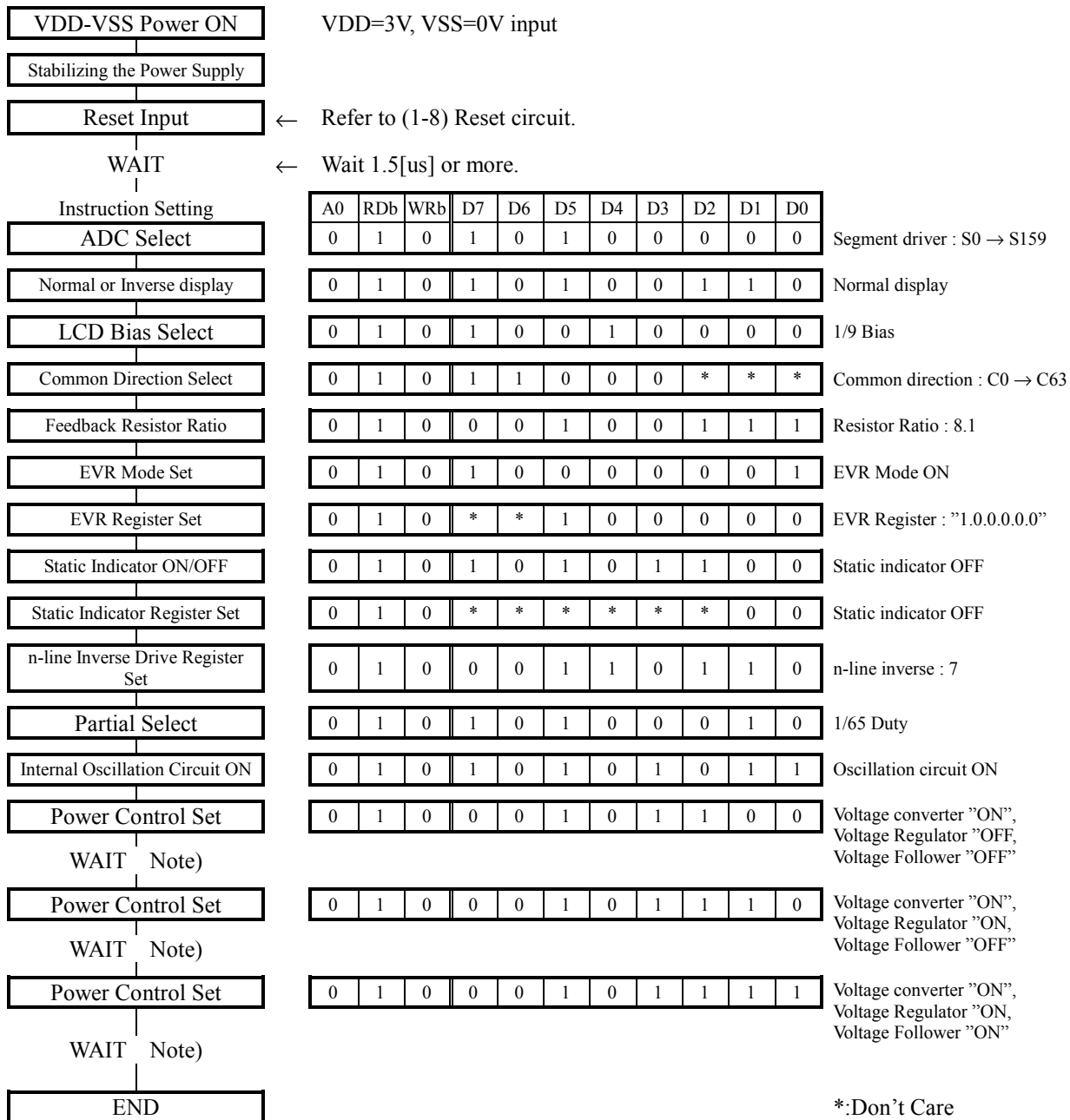
A0	RDb	WRb	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

- Example for Instruction Setting (Reference)

<Conditions>

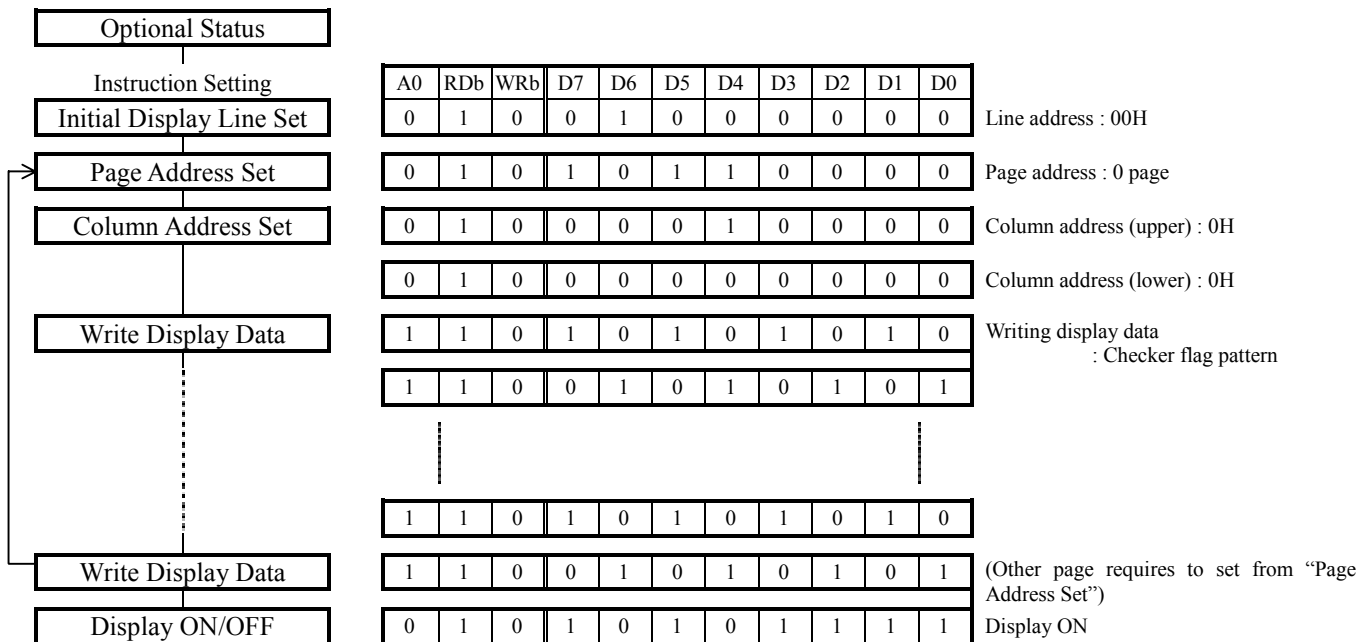
VDD=3V, 4-time booster, Using the internal feedback resistor, Using the internal oscillator, Using the n-line inverse drive, Using the 80-type I/F.

Example for Initialize Sequence

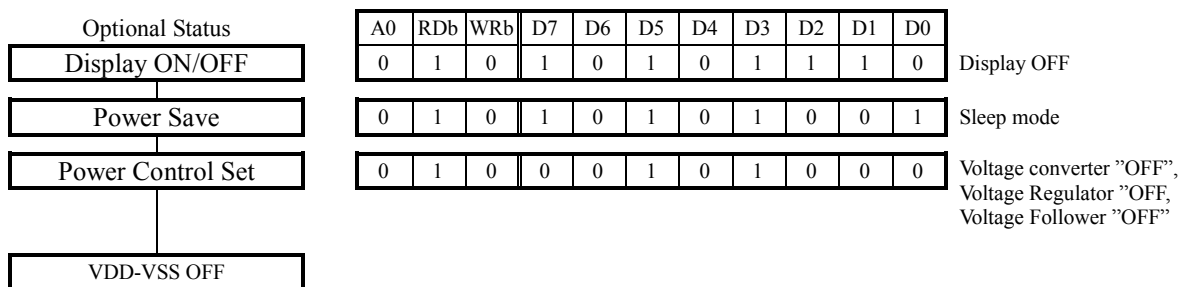


Note) Wait time for stabilizing internal power supply differs by external components (Cout, C1~C8), VDD, and VLCD. Make sure what is the wait time in the particular application.

Example for Display Data Write Sequence



Example for Power Supply OFF Sequence



(3) Internal power circuits

(3-1) Voltage converter

The voltage converter generates maximum 4x boosted negative-voltage from the voltage between V_{DD} and V_{SS2} . The boosted voltage is output from the V_{OUT} terminal.

The internal oscillator is required to be operating when using this converter, because the divided signal provided from the oscillator is used for the internal timing of this circuit.

The boosted voltage between V_{DD} and V_{OUT} must not exceed 18.0V.

The voltage converter requires external capacitors for boosting as shown in below.

● The boosted voltage and V_{DD} , V_{SS2}

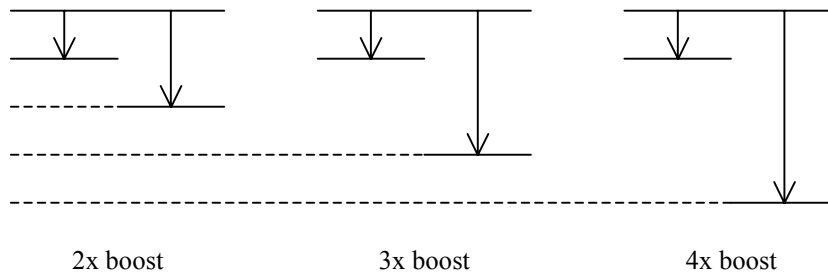
$V_{DD}=+3V$

$V_{SS2}=0V$

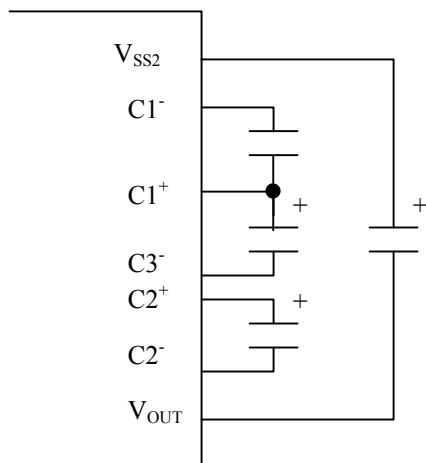
$V_{OUT}=-3V$

$V_{OUT}=-6V$

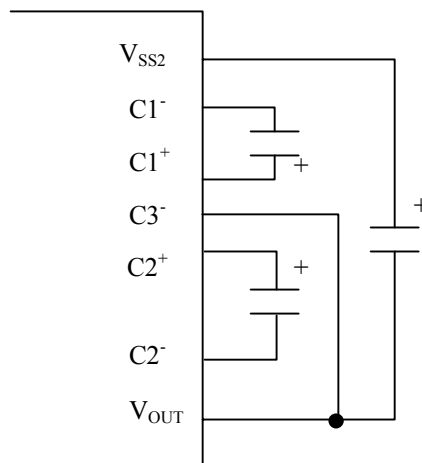
$V_{OUT}=-9V$



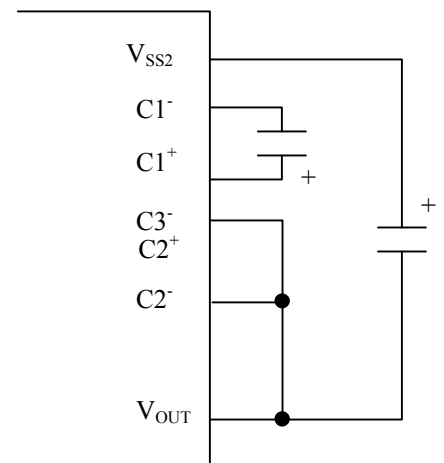
● Example for connecting the capacitors
4x boost



3x boost



2x boost



(3-2) Voltage Adjust Circuits

The voltage adjust circuits is composed of the reference voltage circuit, 64-step E.V.R. and feedback resistors. The adjust circuits produces the LCD driving voltage V_5 on the V_5 terminal, using the V_{OUT} voltage supplied from the internal booster.

(a) Using Internal Feedback Resistors

LCD contrast can be fine-tuned by adjusting the V_5 voltage through setting the internal feedback resistors and the E.V.R. And the V_5 voltage is calculated from the foemula (1), where $|V_5| < |V_{OUT}|$.

$$\begin{aligned}
 V_{LCD} &= V_{DD} - V_5 && \text{----- (1)} \\
 &= (1 + (R_b/R_a)) \times V_{CON} && [V_{CON} = (EVR) \times (V_{REG})] \\
 &= (1 + (R_b/R_a)) \times (EVR) \times V_{REG} && [EVR = (n+99) / 162]
 \end{aligned}$$

V_{LCD} : LCD Driving Voltage V_{CON} : Contrast Control Voltage V_{REG} : Reference Voltage
 R_a, R_b : Feedback Resistors n : E.V.R. Setting Value

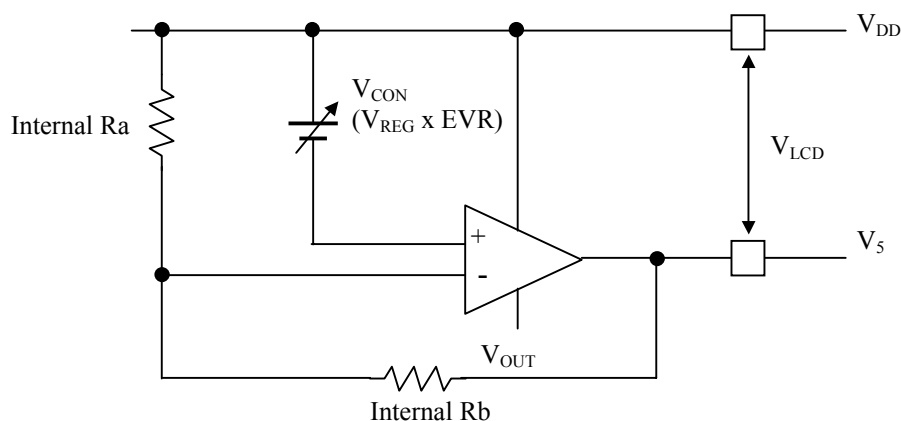


Fig.3-1 Voltage adjust circuits (Using internal feedback resistors)

The V_{REG} is the regulated voltage with temperature coefficient, as follows.

	Temperature Coefficient	V_{REG}
Internal Power Supply	0.05[%/°C] (Typ.)	2.15[V] (Typ.)

*: The temperature coefficient has dispersion.

The V_5 is adjusted in 64-step by setting 6-bit data into the E.V.R. register, as follows.

E.V.R. Register		E.V.R. Value	V_{LCD}
00 _H	(0,0,0,0,0,0)	(99/162)	Minimum
01 _H	(0,0,0,0,0,1)	(100/162)	:
02 _H	(0,0,0,0,1,0)	(101/162)	:
:	:	:	:
:	:	:	:
:	:	:	:
3D _H	(1,1,1,1,0,1)	(160/162)	:
3E _H	(1,1,1,1,1,0)	(161/162)	:
3F _H	(1,1,1,1,1,1)	(162/162)	Maximum

The ratio of the Ra and Rb (Ra/Rb) is selected out of 8 options by the "Feedback Resistor set" instruction.

The Register of Feedback Resistor		1+(Rb/Ra)	V _{LCD}
00 _H	(0,0,0)	4.5	Minimum
01 _H	(0,0,1)	5.0	:
02 _H	(0,1,0)	5.5	:
03 _H	(0,1,1)	6.0	:
04 _H	(1,0,0)	6.5	:
05 _H	(1,0,1)	7.0	:
06 _H	(1,1,0)	7.6	:
07 _H	(1,1,1)	8.1	Maximum

* : The resistance of the feedback resistors has a certain amount of error. If it may impact on the LCD contrast external feedback resistors should be considered.

(b) Using External Feedback Resistors

When IRS="L", the V₅ voltage can be adjusted by the external feedback resistors. And the E.V.R. function is applied in combination, and fine-tunes the LCD contrast through software. The V₅ voltage is calculated from the formula (2), where |V₅| < |V_{OUT}|.

$$\begin{aligned}
 V_{LCD} &= V_{DD} - V_5 && \text{----- (2)} \\
 &= (1 + (R_b/R_a)) \times V_{CON} && [V_{CON} = (EVR) \times (V_{REG})] \\
 &= (1 + (R_b/R_a)) \times (EVR) \times V_{REG} && [EVR = (n+99) / 162]
 \end{aligned}$$

V_{LCD} : LCD Driving Voltage V_{CON} : Contrast Control Voltage V_{REG} : Reference Voltage
 Ra,Rb : Feedback Resistors n : E.V.R. Setting Value

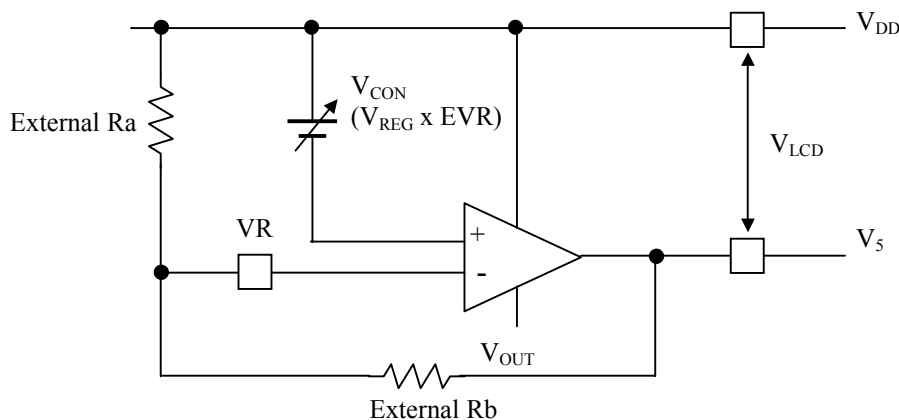


Fig.3-2 Voltage adjust circuits (Using external feedback resistors)

- * : When using either the internal feedback resistors or E.V.R. or both, the LCD voltage generator and the buffer amplifiers must be activated.
- * : The VR terminal is only used for the external feedback resistors. This must be open when using the internal feedback resistors.

<Design example for the adjustable range / Reference> Using external resistors(Not using variable resistor), $V_{LCD}=7V$

Power supply $V_{DD}=3.0V$, $V_{SS}=0V$

E.V.R. register = (D₅,D₄,D₃,D₂,D₁,D₀) : (1,0,0,0,0,0)

By formula (2)

$$\begin{aligned} V_{LCD} &= V_{DD}-V_5 \\ &= (1+(Rb/Ra)) \times (EVR) \times V_{REG} \\ 7[V] &= (1+(Rb/Ra)) \times (131/162) \times 2.15 \end{aligned}$$

$$Rb/Ra = 3.03 \quad \text{----- (3)}$$

In case of the current value sets 5uA, which flows to Ra and Rb

$$Ra+Rb = 1.4M\Omega \quad \text{----- (4)}$$

By formula (3), (4)

$$\begin{aligned} Ra+3.03Ra &= 1.4M\Omega \\ Ra &= 347k\Omega \quad \text{----- (5)} \end{aligned}$$

Therefore,

$$\begin{aligned} Rb &= 1.4M\Omega - 347k\Omega \\ &= 1053k\Omega \quad \text{----- (6)} \end{aligned}$$

The adjustable range and the step voltage are calculated as follows in the formula (2).

- In case of setting 00_H in the E.V.R. register,

$$\begin{aligned} V_{LCD} &= (1+(Rb/Ra)) \times (EVR) \times V_{REG} \\ &= (1+3.03) \times [(99/162) \times 2.15] \\ &= 5.29V \end{aligned}$$

- In case of setting 3F_H in the E.V.R. register,

$$\begin{aligned} V_{LCD} &= (1+(Rb/Ra)) \times (EVR) \times V_{REG} \\ &= (1+3.03) \times [(162/162) \times 2.15] \\ &= 8.66V \end{aligned}$$

	(min.) 00 _H	(max.) 3F _H
V _{LCD} Adjustable Range	5.29	8.66[V]
V _{LCD} Step Voltage	53	[mV]

*: In case of $V_{DD}=3V$

(3-3) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally by dividing the V_{LCD} ($V_{LCD}=V_{DD}-V_5$) voltage with the internal bleeder resistance. And it is supplied to the LCD driving circuits after the impedance conversion with voltage follower circuit.

As shown in Fig 4, Five capacitors are required to connect to each LCD driving voltage terminal for voltage stabilizing. And the value of capacitors $C_4, C_5, C_6, C_7,$ and C_8 are determined depending on the actual LCD panel display evaluation.

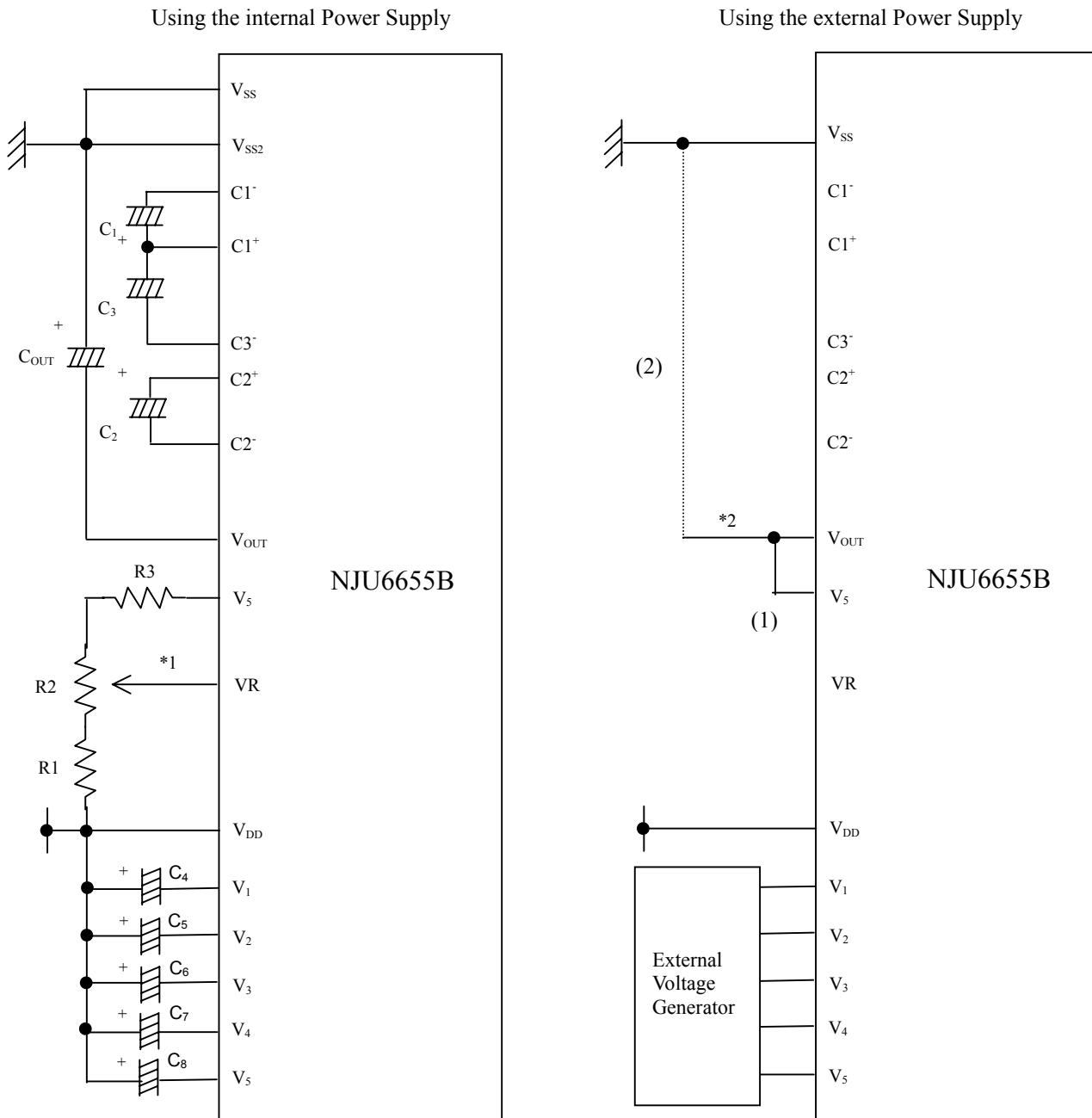


Fig.4 LCD Driving Voltage Generation Circuits

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.

*2 Following connection of V_{OUT} is required when external power supply using.

(1): When $V_{SS} > V_5$ --- $V_{OUT}=V_5$

(2): When $V_{SS} < V_5$ --- $V_{OUT}=V_{SS}$

Reference set up value
 $V_{LCD}=V_{DD}-V_5=7.0$ to $10.5V$

C_{OUT}	~1.0uF
$C_1 \sim C_3, C_8$	~1.0uF
$C_4 \sim C_7$	0.1 ~ 0.47uF
R1	232kΩ
R2	115kΩ
R3	1.053MΩ

(4) MPU interface

(4-1) Interface type selection

NJU6655B interfaces with MPU by 8-bit bidirectional data bus (D₇ to D₀) or serial (SI:D₇). The 8 bit parallel or serial interface is determined by a condition of the P/S terminal connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out operation is impossible.

Table.5 Relation between P/S terminal and each I/O terminal

P/S	Type	CS ₁ b	A0	RDb	WRb	C86	SI(D ₇)	SCL(D ₆)	D ₀ ~D ₅
H	Parallel	CS ₁ b	A0	RDb	WRb	C86	D ₇	D ₆	D ₀ ~D ₅
L	Serial	CS ₁ b	A0	-	-	-	SI	SCL	Hi-Z

"Hi-Z" : Hi-impedance "-" : They should be fixed to "H" or "L".

Parallel Interface

The **NJU6655B** interfaces to 68 or 80 type MPU directly when the parallel interface (P/S="H") is selected. 68 type MPU or 80 is determined by the condition of C86 terminal connecting to "H" or "L" as shown in Table 6.

Table.6 Relation between C86 terminal and each I/O terminal

C86	Type	CS ₁ b	A0	RDb	WRb	D ₀ ~D ₇
H	68 type MPU	CS ₁ b	A0	E	R/W	D ₀ ~D ₇
L	80 type MPU	CS ₁ b	A0	RDb	WRb	D ₀ ~D ₇

(4-2) Discrimination of Data Bus Signal

The **NJU6655B** discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and (RDb,WRb) signals as shown in Table 7.

Table.7 Relation between A0 terminal and 68/80 type terminal

Common	68 type	80 type		Function
	R/W	RDb	WRb	
A0	H	L	H	Read Display Data
H	L	H	L	Write Display Data
L	H	L	H	Status Read
L	L	H	L	Write into the Register(Instruction)

(4-3) Serial Interface (P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminal CS_{1b} set to "L", CS₂ set to "H" and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition when the chip is not selected.

The data input from SI terminal is MSB first like as the order of D₇, D₆, - - - D₀, and the data are entered into the shift register synchronizing with the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input.

Discrimination of the display data or instruction of the serial input data is executed by the condition of A0 at the 8th serial clock rise edge. A0="H" is display data and A0="L" is instruction. When RESb terminal becomes "L" or CS_{1b} terminal becomes "H" (CS₂ terminal becomes "L") before 8th serial clock rise edge, NJU6655A recognizes them as a instruction data incorrectly. Therefore a unit of serial data must be structured by 8-bit.

The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface.

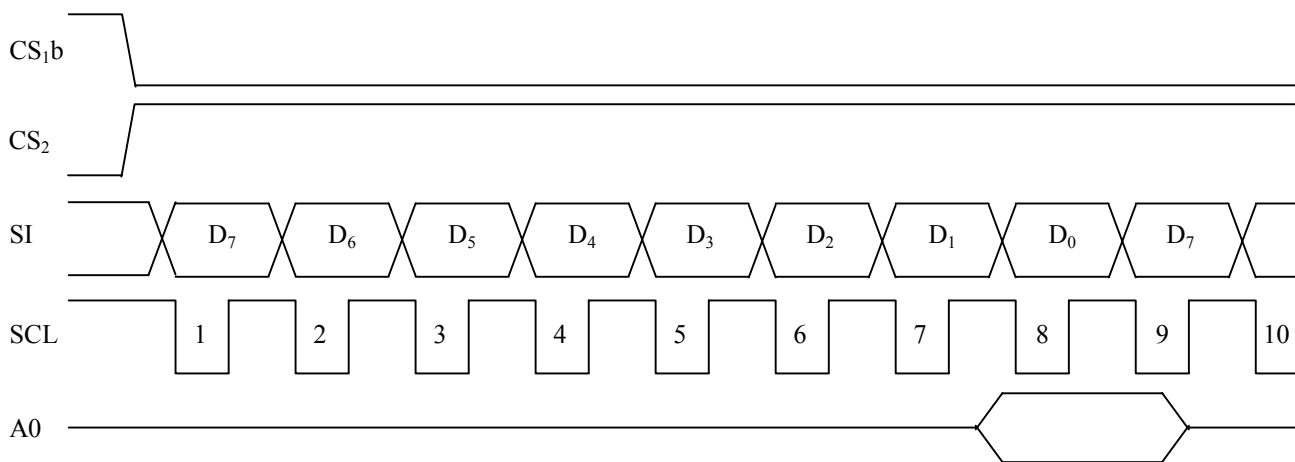


Fig.5 Signal chart of serial interface

(4-4) Access to the Display Data RAM and Internal Register

The NJU6655B is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU reads out the data from the Display Data RAM, the read out data in the data read cycle (dummy read) is held in the bus-holder, then it is read out from the bus-holder to the system bus at the next data read cycle. When the MPU writes the data into the Display Data RAM, the data is held in the bus-holder, then it is written into the Display Data RAM by the next data write cycle.

Therefore high speed data transmission between MPU and NJU6655B is available because of it is not limited by the tACC and tDS as display data RAM access time and is limited by the system cycle time (R) or (W).

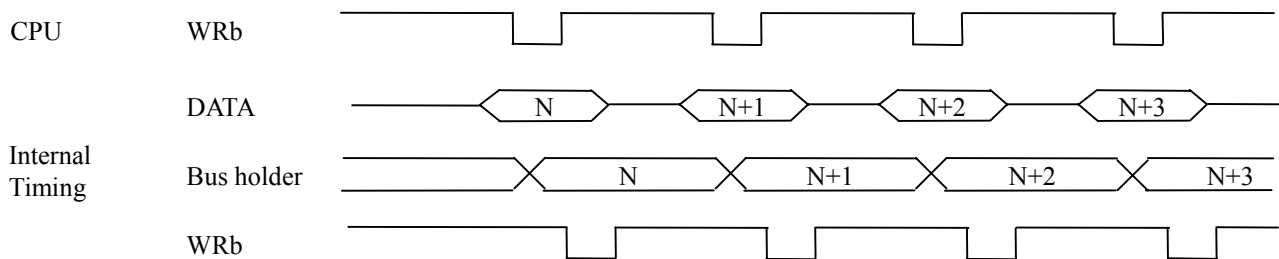
If the cycle time is not be kept in the MPU operation, NOP should be inserted to the system instead of the waiting operation.

The read out operation does not read out the data in the pointed address just after the address set operation. And second read out operation can read out the data correctly from the pointed address.

Therefore, one dummy read operation is required after address setting or write cycle as shown in Fig. 6.

The example of Read Modify Write operation is mentioned in (2-1) Instruction (1)The sequence of inverse display.

● Write Operation



● Read Operation

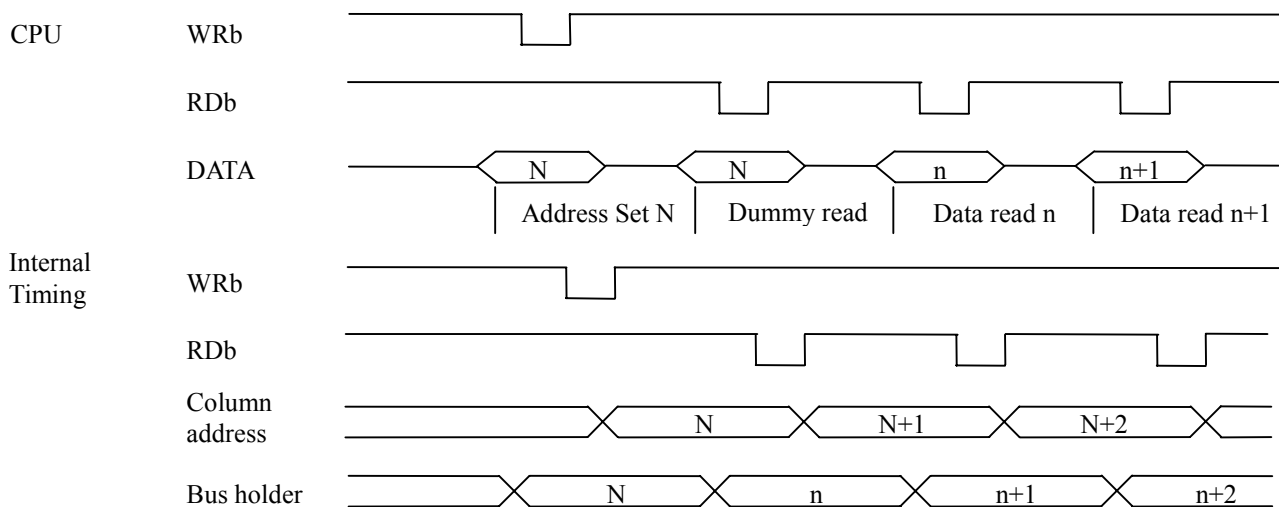


Fig.6 Relation between display data write/read and internal timing

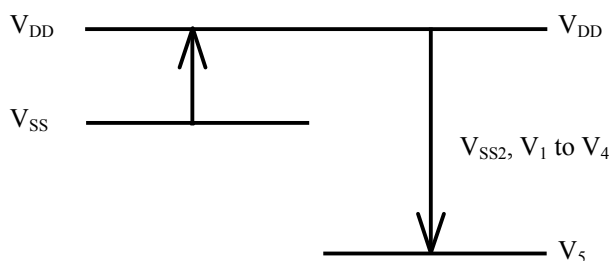
(4-5) Chip select

CS_{1b}, CS₂ are Chip Select terminals. In case of CS_{1b}="L" and CS₂="H", the interface with MPU is available. In case of CS_{1b}="H" or CS₂="L", the D₀ to D₇ are high impedance and A₀, RDb, WRb, D₇(SI) and D₆(SCL) inputs are ignored. If the serial interface is selected when CS_{1b}="H" or CS₂="L", the shift register and the counter are reset. However, the reset is always operated in any conditions of CS_{1b} and CS₂.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V _{DD}	-0.3 to +7.0	V
Supply Voltage (2) (When using 3x voltage converter) (When using 4x voltage converter)	V _{SS2}	-7.0 to +0.3 -6.0 to +0.3 -4.5 to +0.3	V
Supply Voltage (3)	V ₅ , V _{OUT}	-18.0 to +0.3	V
Supply Voltage (4)	V ₁ , V ₂ , V ₃ , V ₄	V ₅ to +0.3	V
Input Voltage	V _{IN}	-0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT}	-0.3 to V _{DD} + 0.3	V
Operating Temperature	T _{opr}	-40 to +85	°C
Storage Temperature (Chip)	T _{stg}	-55 to +125	°C



Note 1) V_{SS2}, V₁ to V₅, V_{OUT} voltage values are specified as V_{DD} = 0V.

Note 2) The relation of V_{DD} ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V₅ > V_{OUT} ; V_{DD} > V_{SS} ≥ V_{OUT} must be maintained.

In case of inputting external LCD driving voltage, LCD drive voltage should start supplying to NJU6655B at the mean time of turning on V_{DD} power supply or after turned on V_{DD}.

In use of the voltage boost circuit, the condition that the supply voltage : 18V ≥ V_{DD} - V_{OUT} is necessary.

Note 3) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ DC Electrical Characteristics

($V_{DD}=2.4$ to $3.6V$, $V_{SS}=0V$, $T_a= -40$ to $85^{\circ}C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE	
Power Supply (1)	V_{DD}	Recommend→ Possible→	2.4	-	3.6	V	5	
			2.4	-	5.5	V		
Power Supply (2)	V_{SS2}	V_{DD} common	-6.0	-	-2.4	V		
Power Supply (3)	V_5	V_{DD} common	-18	-	-4.5	V		
	V_1, V_2	V_{DD} common	$0.4V_5$	-	V_{DD}			
	V_3, V_4		V_5	-	$0.6V_5$			
“H” Level Input Voltage	V_{IHC1}		$0.8V_{DD}$	-	V_{DD}	V		
“L” Level Input Voltage	V_{ILC1}		V_{SS}	-	$0.2V_{DD}$	V		
“H” Level Output Voltage	V_{OHC1}	$I_{OH}=-0.5mA$	$0.8V_{DD}$	-	V_{DD}	V		
“L” Level Output Voltage	V_{OLC1}	$I_{OL}=0.5mA$	V_{SS}	-	$0.2V_{DD}$	V		
Leakage Current	I_{LI}	All input terminals	-1.0	-	1.0	μA		
	I_{LO}	D_0 to D_7 terminals, Hi-Z state	-3.0	-	3.0	μA		
Driver On-resistance	R_{ON1}	$T_a=25^{\circ}C$	$V_5=-14.0V$	-	2.0	3.5	$k\Omega$	6
	R_{ON2}			$V_5=-8.0V$	-	3.2	5.4	
Stand-by Current	I_{SSQ}		-	0.01	5	μA		
Output Leakage Current	I_{5Q}	$V_5=-18.0V$ (V_{DD} common)	-	0.01	15	μA		
Input Terminal Capacitance	C_{IN}	$T_a=25^{\circ}C$	-	5	8	pF	7	
Oscillation Frequency	f_{OSC}	$V_{DD}=3V, T_a=25^{\circ}C$	17.0	20.8	24.6	kHz		
Display Clock Frequency	f_{CL}	External input	4.25	5.20	6.15	kHz		

Note 5) Although the **NJU6655B** can operate in wide range of the operating voltage, it shall not be guaranteed in a sudden voltage fluctuation during the access with MPU.

Note 6) R_{ON} is the resistance values in supplying 0.1V voltage-difference between power supply terminals (V_1, V_2, V_3, V_4) and each output terminals (common / segment). This is specified within the range of Operating Voltage (2).

Note 7) Apply to A_0, D_7 to $D_0, RD_b, WR_b, CS_1_b, CS_2, RES_b, C86$ and P/S terminals.

(V_{DD}=2.4 to 3.6V, V_{SS}=0V, Ta= -40 to 85°C)

Voltage Booster	Input Voltage	V _{SS2}	V _{DD} common, 3-times boost	-6.0	-	-2.4	V		
			V _{DD} common, 4-times boost	-4.5	-	-2.4			
	Output Voltage	V _{OUT}	V _{DD} common	-18.0	-	-	V		
	On-resistance	R _{QUAD}	4-times boost, C ₁ -C ₃ , C _{OUT} =1uF V _{DD} =3V, V _{SS} =V _{SS2}		2.5	3.5	kΩ		
	Adjustment Range LCD Driving Voltage	V _{OUT2}	Voltage boost operation off External power supply	-18.0	-	-6.0	V	8	
	Voltage Follower Operating Voltage	V ₅	Voltage adjustment circuit off External power supply	-18.0	-	-4.5	V		
	Operating current	I _{DDQ1}	Power save mode (Sleep mode)		0.01	5.0	uA		
			Power save mode (Standby mode)		4	10			
		I _{DD2}	V _{DD} =3V, V ₅ =-11V		130	200	uA	9	
			All COM/SEG open, Without MPU access, Checker flag display		20	50			
	LCD driving Voltage	V _{LCD}	Ext. Resistance (EVR=3F _H)	Ra=Rb=910kΩ	-4.43	-4.30	-4.17	V	10
			Int. Resistance (EVR=3F _H)	1+(Rb/Ra)=4.5	-10.16	-9.68	-9.19		
				1+(Rb/Ra)=5	-11.29	-10.75	-10.21		
				1+(Rb/Ra)=5.5	-12.42	-11.83	-11.23		
				1+(Rb/Ra)=6	-13.55	-12.90	-12.26		
1+(Rb/Ra)=6.5				-14.67	-13.98	-13.28			
1+(Rb/Ra)=7				-15.80	-15.05	-14.30			
1+(Rb/Ra)=7.6				-17.16	-16.34	-15.52			
1+(Rb/Ra)=8.1	-18.29	-17.42	-16.54						
Reference Voltage	V _{REF}	Ta=25°C		2.150		V			
Temperature Coefficient	TC	V _{DD} =3V		-0.05		%/°C			

Note 8) The voltage adjustment circuit controls V₅ within the range of the voltage follower operating voltage.

Note 9) Each operating current shall be defined as being measured in the following condition.

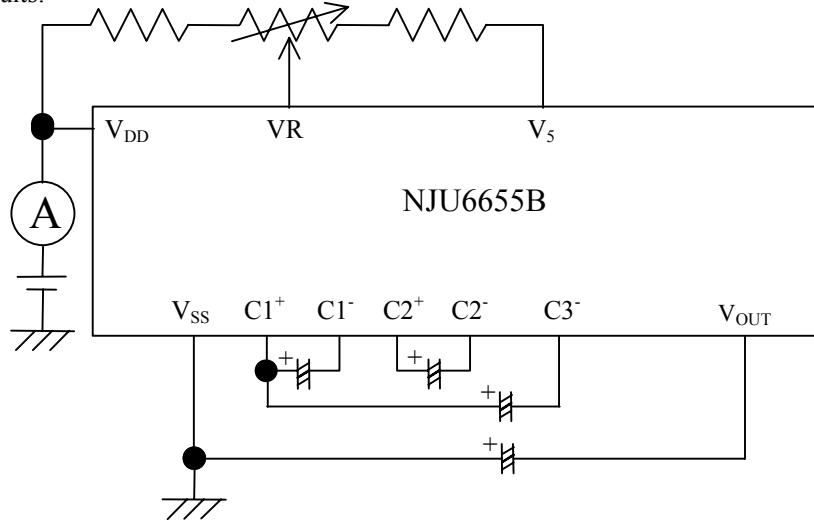
Note10) The LCD driving voltage spec: V_{LCD}± 3% (Using to External resistance) / V_{LCD}± 5 % (Using to Internal resistance).

NJU6655B

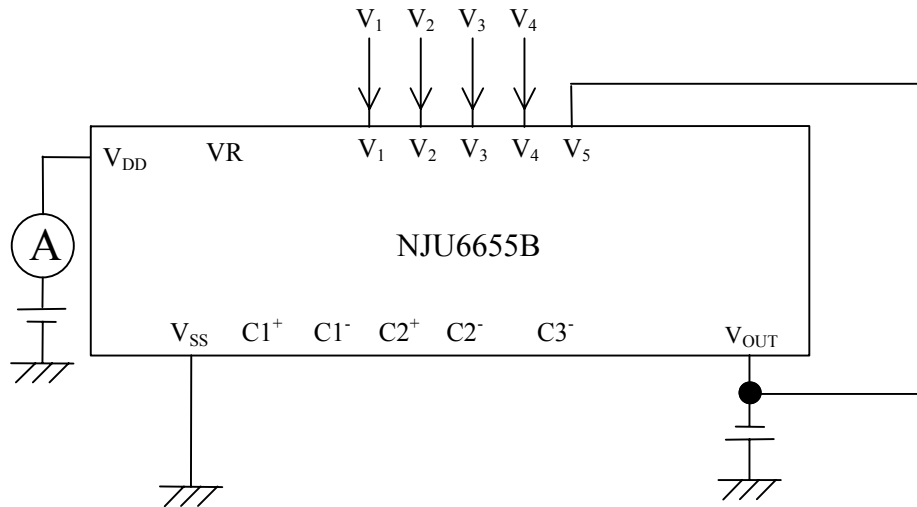
Symbol	Power Control			Operating Condition			External Voltage Supply (Input Terminal)
	D ₂	D ₁	D ₀	Voltage converter	Voltage regulator	Voltage followers	
I _{DD1}	1	1	1	On	On	On	Use(V _{SS2})
I _{DD2}	0	0	0	Off	Off	Off	Use(V _{OUT} , V ₁ ~V ₅)

IDD 1,2 measurement circuits:

:I_{DD1}

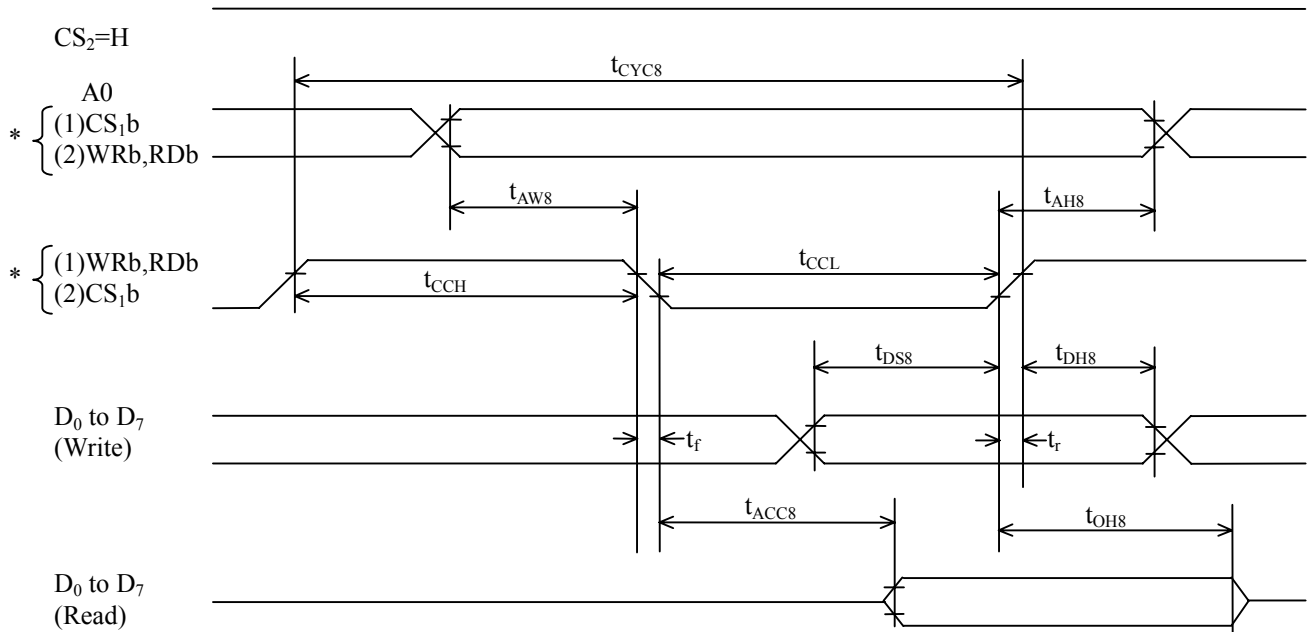


:I_{DD2}



■ BUS TIMING CHARACTERISTICS

- Read and Write characteristics (80 type MPU)



($V_{SS}=0V$, $V_{DD}=2.4$ to $3.6V$, $T_a=-40$ to $85^\circ C$)

PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	MAX	UNIT
Address Hold Time	A0,CS ₁ b	t _{AH8}		0	-	ns
Address Set Up Time	CS ₂	t _{AW8}		0	-	ns
System Cycle Time		t _{CYC8}		800	-	ns
Control "L" Pulse Width (WRb)	WRb RDb	t _{CCLW}		120	-	ns
Control "L" Pulse Width (RDb)		t _{CCLR}		240	-	ns
Control "H" Pulse Width (WRb)		t _{CCHW}		120	-	ns
Control "H" Pulse Width (RDb)		t _{CCHR}		120	-	ns
Data Set Up Time	D ₀ to D ₇	t _{DS8}		80	-	ns
Data Hold Time		t _{DH8}		30	-	ns
RDb Access Time		t _{ACC8}	CL=100pF	-	280	ns
Output Disable Time		t _{OH8}		10	200	ns
Input Signal Rising, Falling Edge	CS ₁ b,CS ₂ , WRb,RDb, A0,D ₀ to D ₇	t _r , t _f			15	ns

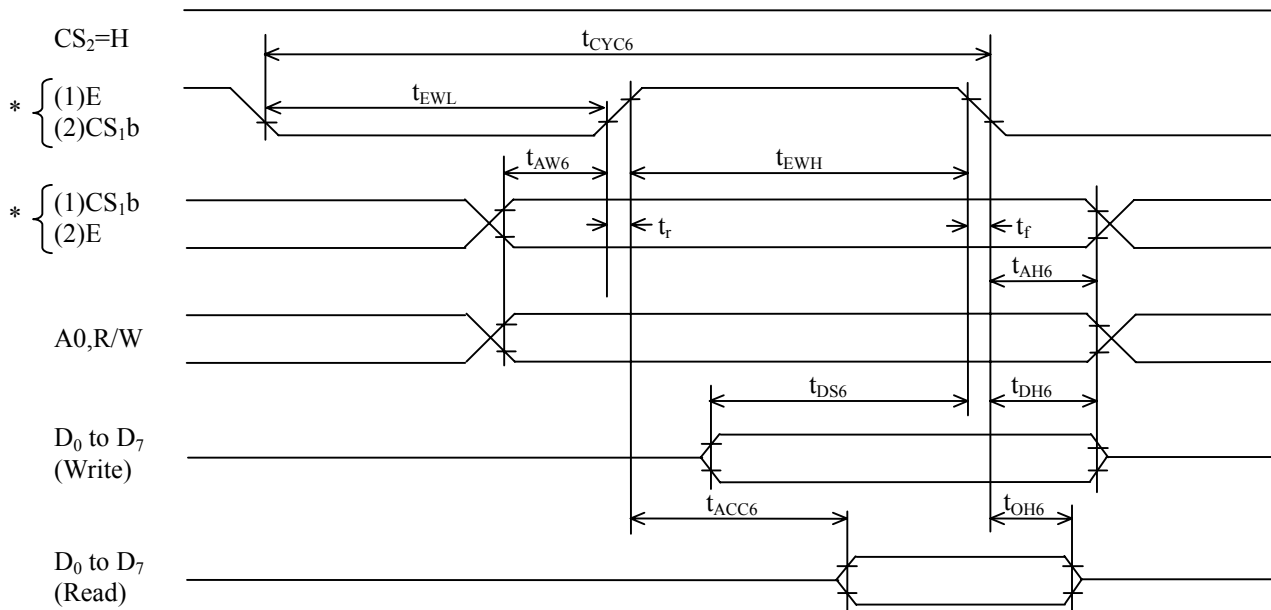
($V_{SS}=0V$, $V_{DD}=4.5$ to $5.5V$, $T_a=-40$ to $85^{\circ}C$)

PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	MAX	UNIT
Address Hold Time	A0,CS _{1b}	tAH8		0	-	ns
Address Set Up Time	CS ₂	tAW8		0	-	ns
System Cycle Time		tCYC8		250	-	ns
Control "L" Pulse Width (WRb)	WRb RDb	tCCLW		30	-	ns
Control "L" Pulse Width (RDb)		tCCLR		70	-	ns
Control "H" Pulse Width (WRb)		tCCHW		30	-	ns
Control "H" Pulse Width (RDb)		tCCHR		30	-	ns
Data Set Up Time	D ₀ to D ₇	tDS8		30	-	ns
Data Hold Time		tDH8		10	-	ns
RDb Access Time		tACC8	CL=100pF	-	70	ns
Output Disable Time		tOH8		5	50	ns
Input Signal Rising, Falling Edge	CS _{1b} ,CS ₂ , WRb,RDb, A0,D ₀ to D ₇	tr, tf			15	ns

Note 10) Each timing is specified based on $0.2xV_{DD}$ and $0.8xV_{DD}$.

* : (1) Accessed by WRb and RDb signal when CS_{1b}="L". (2) Accessed by CS_{1b} signal when WRb and RDb ="L".

- Read and Write characteristics (68 type MPU)



(V_{SS}=0V, V_{DD}=2.4 to 3.6V, Ta=-40 to 85°C)

PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	MAX	UNIT	
Address Hold Time	A0,CS _{1b}	t _{AH6}		0	-	ns	
Address Set Up Time	CS ₂	t _{AW6}		0	-	ns	
System Cycle Time		t _{CYC6}		800	-	ns	
Enable "H" Pulse Width (Read)	E(RDb)	t _{EWHR}		240	-	ns	
Enable "H" Pulse Width (Write)		t _{EWHW}		120	-	ns	
Enable "L" Pulse Width (Read)		t _{EWLR}		120	-	ns	
Enable "L" Pulse Width (Write)		t _{EWLW}		120	-	ns	
Data Set Up Time	D ₀ to D ₇	t _{DS6}		80	-	ns	
Data Hold Time		t _{DH6}		30	-	ns	
RDb Access Time		t _{ACC6}	CL=100pF		-	280	ns
Output Disable Time		t _{OH6}			10	200	ns
Input Signal Rising, Falling Edge	E(RDb), R/W(WRb), A0,D ₀ to D ₇	t _r , t _f			15	ns	

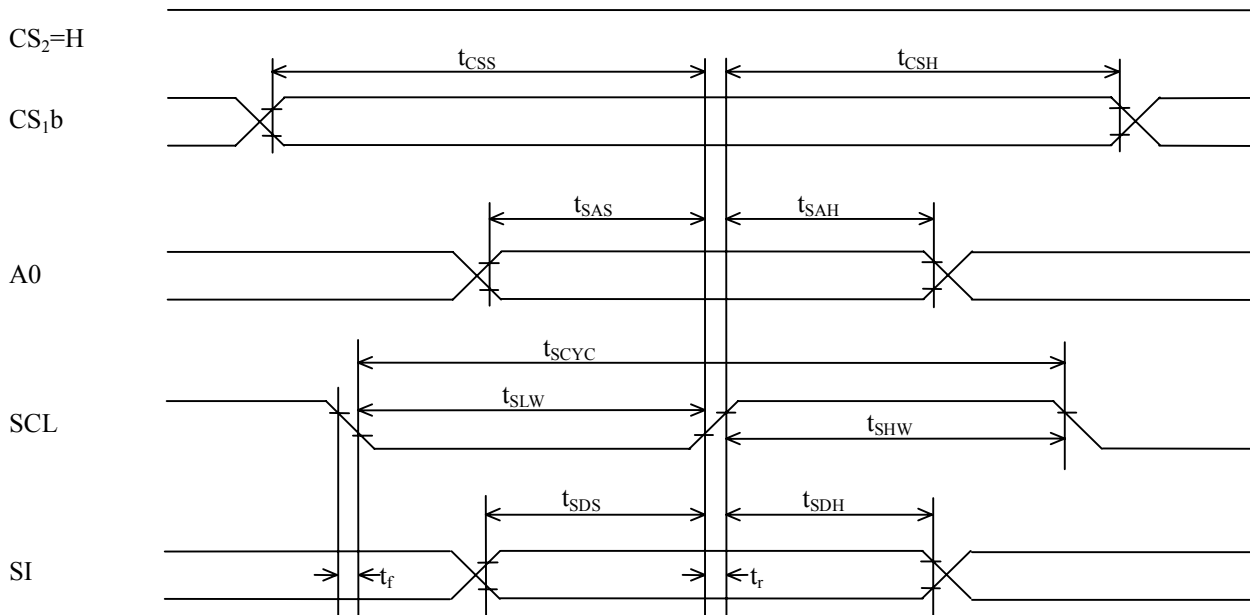
($V_{SS}=0V$, $V_{DD}=4.5$ to $5.5V$, $T_a=-40$ to $85^{\circ}C$)

PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	MAX	UNIT
Address Hold Time	A0,CS _{1b}	tAH6		0	-	ns
Address Set Up Time	CS ₂	tAW6		0	-	ns
System Cycle Time		tCYC6		250	-	ns
Enable "H" Pulse Width (Read)	E(RDb)	tEWHR		70	-	ns
Enable "H" Pulse Width (Write)		tEWHW		30	-	ns
Enable "L" Pulse Width (Read)		tEWLR		30	-	ns
Enable "L" Pulse Width (Write)		tEWLW		30	-	ns
Data Set Up Time	D ₀ to D ₇	tDS6		30	-	ns
Data Hold Time		tDH6		10	-	ns
RDb Access Time		tACC6	CL=100pF	-	70	ns
Output Disable Time		tOH6		5	50	ns
Input Signal Rising, Falling Edge	E(RDb), R/W(WRb), A0,D ₀ to D ₇	tr, tf			15	ns

Note 11) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

* : (1) Accessed by WRb and RDb signal when CS_{1b}="L". (2) Accessed by CS_{1b} signal when WRb and RDb ="L".

- Write characteristics (Serial interface)



($V_{SS}=0V$, $V_{DD}=2.4$ to $3.6V$, $T_a=-40$ to $85^{\circ}C$)

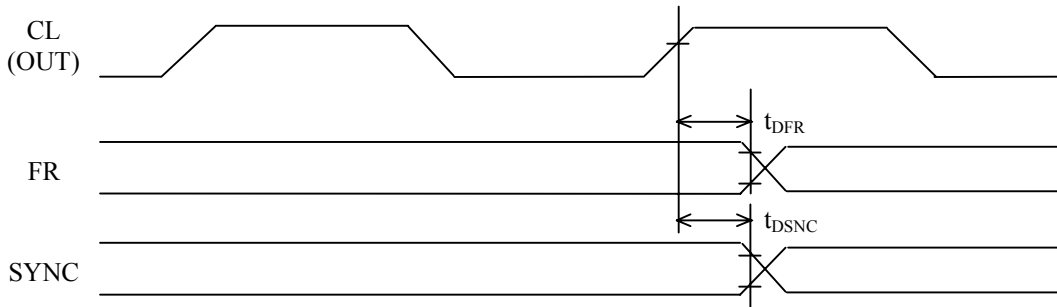
PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	MAX	UNIT
Serial Clock Cycle	SCL(D ₆)	tSCYC		400	-	ns
SCL "H" Pulse Width		tSHW		150	-	ns
SCL "L" Pulse Width		tSLW		150	-	ns
Address Set Up Time	A0	tSAS		250	-	ns
Address Hold Time		tSAH		250	-	ns
Data Set Up Time	SI(D ₇)	tSDS		150	-	ns
Data Hold Time		tSDH		150	-	ns
CS _{1b} -SCL Time	CS _{1b} ,CS ₂	tCSS		250	-	ns
		tCSH		250	-	ns
Input Signal Rising, Falling Edge	SCL(D ₆),A0, CS _{1b} ,CS ₂ , SI(D ₇)	tr, tf			15	ns

($V_{SS}=0V$, $V_{DD}=4.5$ to $5.5V$, $T_a=-40$ to $85^{\circ}C$)

PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	MAX	UNIT
Serial Clock Cycle	SCL(D ₆)	tSCYC		200	-	ns
SCL "H" Pulse Width		tSHW		75	-	ns
SCL "L" Pulse Width		tSLW		75	-	ns
Address Set Up Time	A0	tSAS		50	-	ns
Address Hold Time		tSAH		100	-	ns
Data Set Up Time	SI(D ₇)	tSDS		50	-	ns
Data Hold Time		tSDH		50	-	ns
CS _{1b} -SCL Time	CS _{1b} ,CS ₂	tCSS		100	-	ns
		tCSH		100	-	ns
Input Signal Rising, Falling Edge	SCL(D ₆),A0, CS _{1b} ,CS ₂ , SI(D ₇)	tr,, tf			15	ns

Note 12) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

- Display control timing characteristics



($V_{SS}=0V$, $V_{DD}=2.4$ to $3.6V$, $T_a=-40$ to $85^\circ C$)

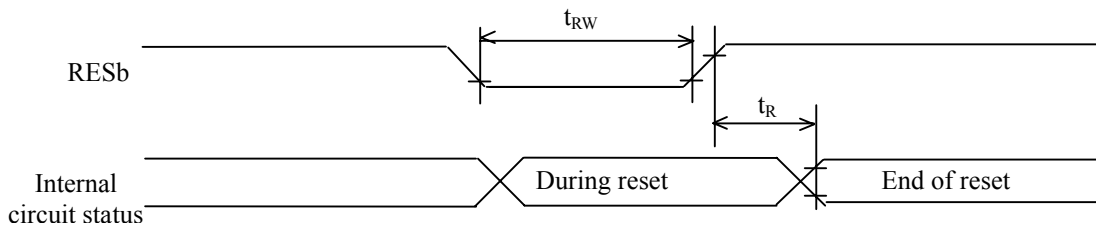
PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
FR Delay Time	FR	t_{DFR}	CL=50pF	-	50	200	ns
SYNC Delay Time	SYNC	t_{DSNC}	CL=50pF	-	50	200	ns

($V_{SS}=0V$, $V_{DD}=4.5$ to $5.5V$, $T_a=-40$ to $85^\circ C$)

PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
FR Delay Time	FR	t_{DFR}	CL=50pF	-	10	40	ns
SYNC Delay Time	SYNC	t_{DSNC}	CL=50pF	-	10	40	ns

Note 13) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.
(The delay time is applied to the master operation only.)

- Reset input timing



($V_{SS}=0V$, $V_{DD}=2.4$ to $3.6V$, $T_a=-40$ to $85^\circ C$)

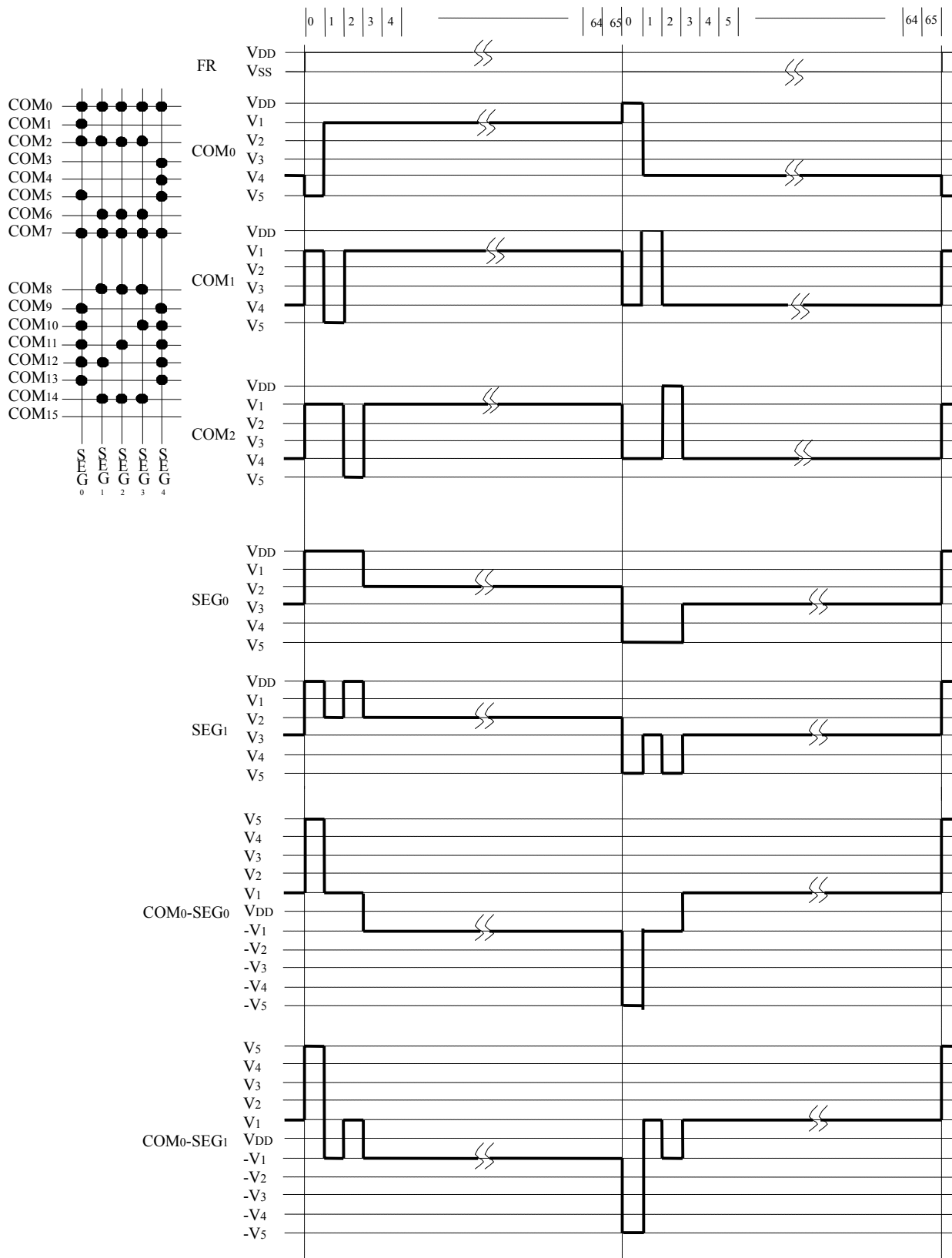
PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reset Time		t_R		-	-	1.5	us
Reset "L" Level Pulse Width	RESb	t_{rw}		1.5	-	-	us

($V_{SS}=0V$, $V_{DD}=4.5$ to $5.5V$, $T_a=-40$ to $85^\circ C$)

PARAMETER	TERMINAL	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reset Time		t_R		-	-	0.5	us
Reset "L" Level Pulse Width	RESb	t_{rw}		0.5	-	-	us

Note 14) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

■ LCD DRIVING WAVEFORM



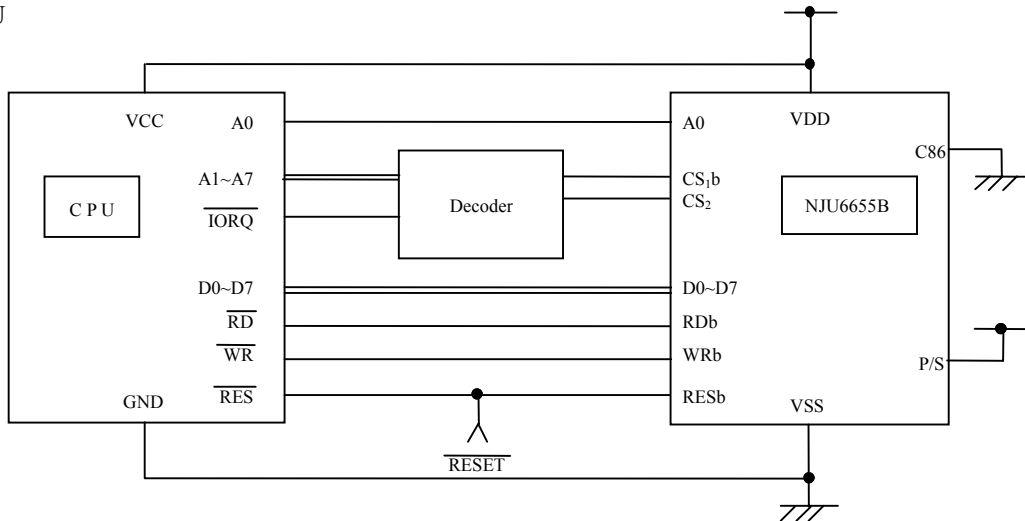
APPLICATION CIRCUIT

(1) Microprocessor Interface Example

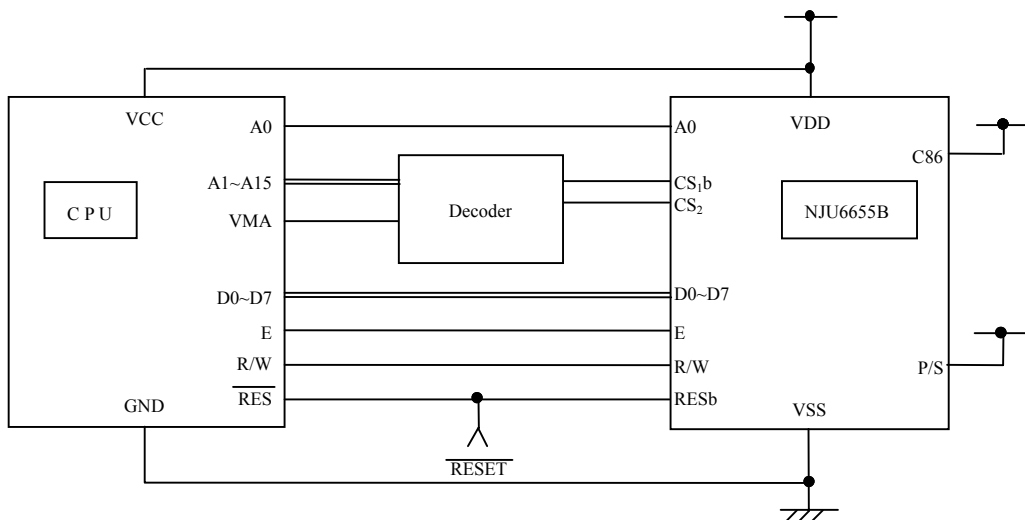
The NJU6655B interfaces to 80 type or 68 type MPU directly. And the serial interface also communicate with MPU.

* : C86 terminal must be fixed V_{DD} or V_{SS}.

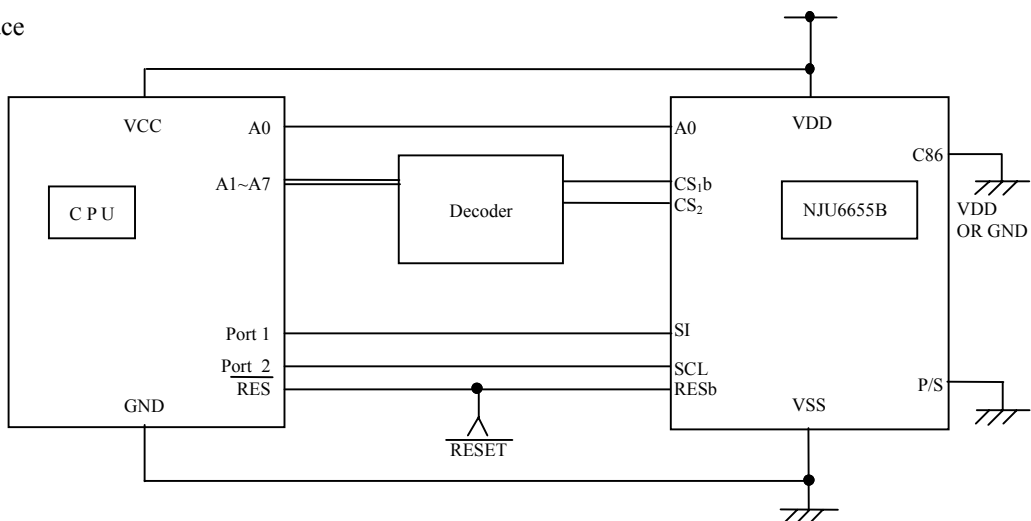
- 80 Type MPU



- 68 Type MPU

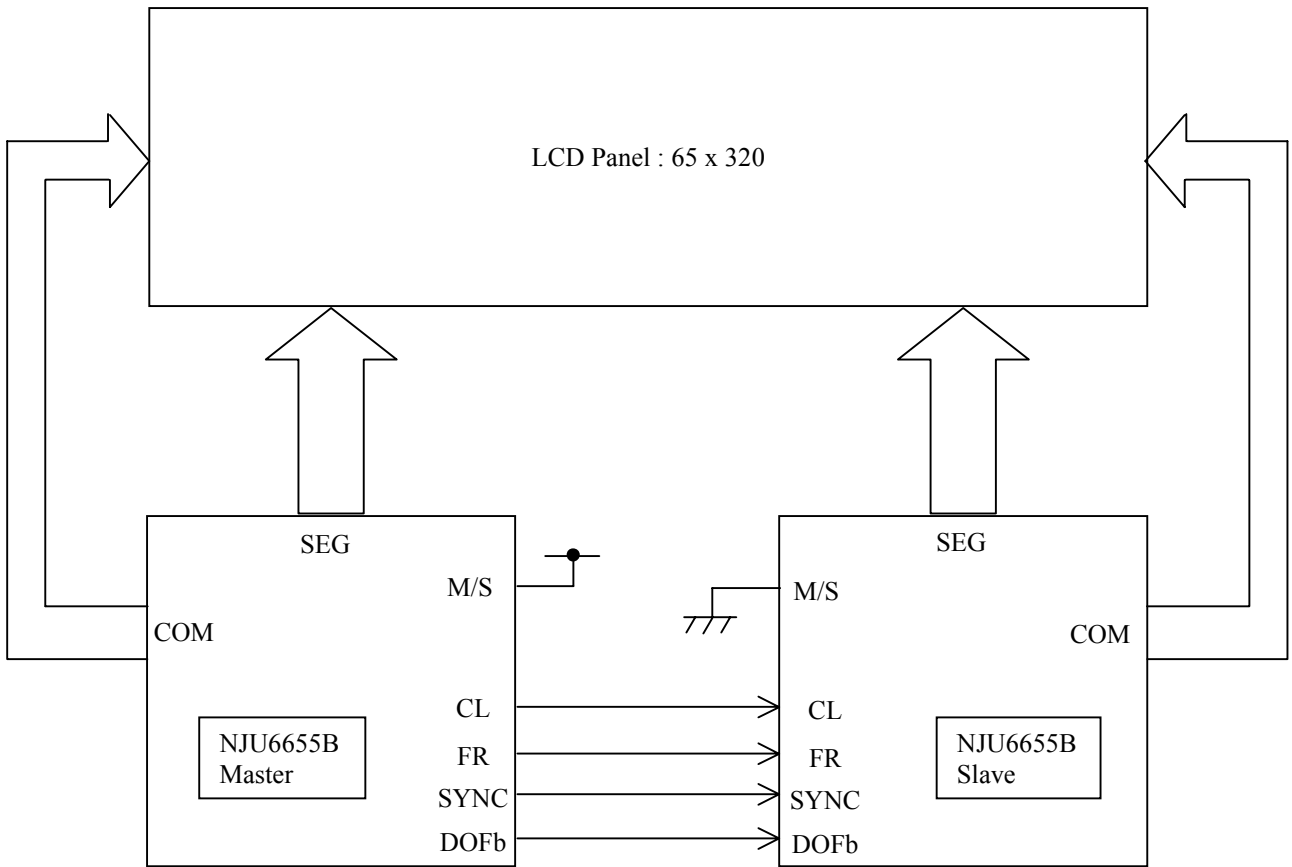


- Serial Interface



NJU6655B

(2) 65 x 320 dots Driving Application Circuits Example
(Common and Segment Drivers Extension by using two of NJU6655B)



[CAUTION]

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