

# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for CDMA base station applications with frequencies from 2500 to 2700 MHz. Suitable for WiMAX, WiBro, BWA, and OFDM multicarrier Class AB and Class C amplifier applications.

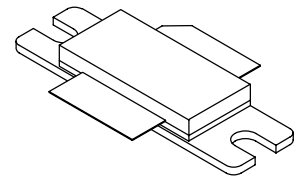
- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 500$  mA,  $P_{out} = 7$  Watts Avg., Full Frequency Band, Channel Bandwidth = 3.84 MHz. PAR = 8.5 dB @ 0.01% Probability on CCDF.  
 Power Gain — 16 dB  
 Drain Efficiency — 22.5%  
 ACPR @ 5 MHz Offset — -42.5 dBc @ 3.84 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2600 MHz, 50 Watts CW Output Power

### Features

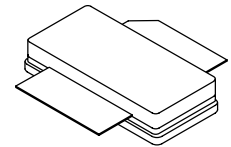
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32  $V_{DD}$  Operation
- Integrated ESD Protection
- Lower Thermal Resistance Package
- Designed for Lower Memory Effects and Wide Instantaneous Bandwidth Applications
- Low Gold Plating Thickness on Leads, 40 $\mu$ m Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

**MRF6S27050HR3**  
**MRF6S27050HSR3**

**2500-2700 MHz, 7 W AVG., 28 V**  
**SINGLE W-CDMA**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**CASE 465-06, STYLE 1**  
**NI-780**  
**MRF6S27050HR3**



**CASE 465A-06, STYLE 1**  
**NI-780S**  
**MRF6S27050HSR3**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +68	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +12	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 43 W CW Case Temperature 72°C, 7 W CW	$R_{\theta JC}$	0.85 0.98	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 68\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 250\ \mu\text{Adc}$ )	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 500\ \text{mA}$ , Measured in Functional Test)	$V_{GS(Q)}$	2	2.8	4	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2.2\ \text{Adc}$ )	$V_{DS(on)}$	—	0.21	0.3	Vdc

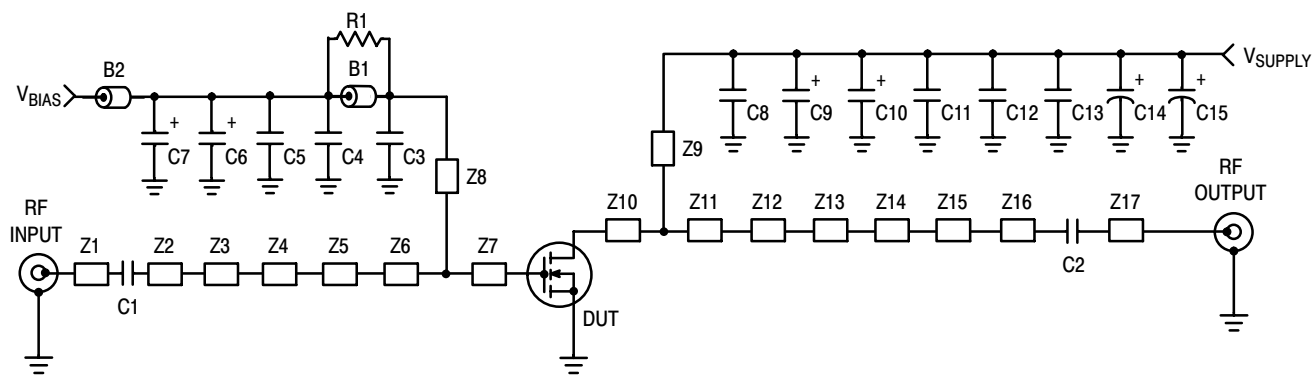
**Dynamic Characteristics** <sup>(1)</sup>

Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	0.83	—	pF
Output Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	232	—	pF

**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 500\ \text{mA}$ ,  $P_{out} = 7\ \text{W Avg. W-CDMA}$ ,  
 $f = 2585\ \text{MHz}$  and  $2615\ \text{MHz}$ , Single-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carrier. ACPR measured in 3.84 MHz Channel  
 Bandwidth @  $\pm 5\ \text{MHz}$  Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.

Power Gain	$G_{ps}$	15	16	18	dB
Drain Efficiency	$\eta_D$	20.5	22.5	—	%
Adjacent Channel Power Ratio	ACPR	-40	-42.5	—	dBc
Input Return Loss	IRL	—	-10	—	dB

1. Part internally matched both on input and output.



Z1	0.748" x 0.081" Microstrip	Z10	0.091" x 0.753" Microstrip
Z2	0.273" x 0.081" Microstrip	Z11	0.150" x 0.753" Microstrip
Z3	0.055" x 0.220" Microstrip	Z12	0.153" x 0.543" Microstrip
Z4	0.090" x 0.440" Microstrip	Z13	0.145" x 0.384" Microstrip
Z5	0.195" x 0.170" Microstrip	Z14	0.446" x 0.148" Microstrip
Z6	0.797" x 0.490" Microstrip	Z15	0.130" x 0.425" Microstrip
Z7	0.082" x 0.490" Microstrip	Z16	0.384" x 0.081" Microstrip
Z8	0.050" x 0.476" Microstrip	Z17	0.730" x 0.081" Microstrip
Z9	0.070" x 0.350" Microstrip	PCB	Arlon GX0300-55-22, 0.030", $\epsilon_r = 2.55$

**Figure 1. MRF6S27050HR3(SR3) Test Circuit Schematic**

**Table 5. MRF6S27050HR3(SR3) Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
B1	Ferrite Bead	2508051107Y0	Fair-Rite
B2	Ferrite Bead, Short	2743019447	Fair-Rite
C1, C2	4.3 pF Chip Capacitors	600B4R3BT250XT	ATC
C3, C8	3.6 pF Chip Capacitors	600B3R6BT250XT	ATC
C4, C11	2.2 $\mu$ F, 50 V Chip Capacitors	C1825C225J5RAC	Kemet
C5	0.01 $\mu$ F, 100 V Chip Capacitor	C1825C103J1RAC	Kemet
C6	22 $\mu$ F, 25 V Tantalum Capacitor	ECS-T1ED226R	Panasonic TE series
C7	47 $\mu$ F, 16 V Tantalum Capacitor	T491D476K016AT	Kemet
C9, C10	10 $\mu$ F, 50 V Tantalum Capacitors	522Z-050/100MTRE	Tecate
C12, C13	1.0 $\mu$ F, 50 V Chip Capacitors	GRM32RR71H105KA01B	Murata
C14	330 $\mu$ F, 63 V Electrolytic Capacitor	SME63V331M12X25LL	Nippon Chemi-Con
C15	47 $\mu$ F, 50 V Electrolytic Capacitor	MVK50VC47RM8X10TP	United Chemi-Con
R1	2.7 $\Omega$ , 1/4 W Chip Resistor	CRCW12062R7F100	Vishay

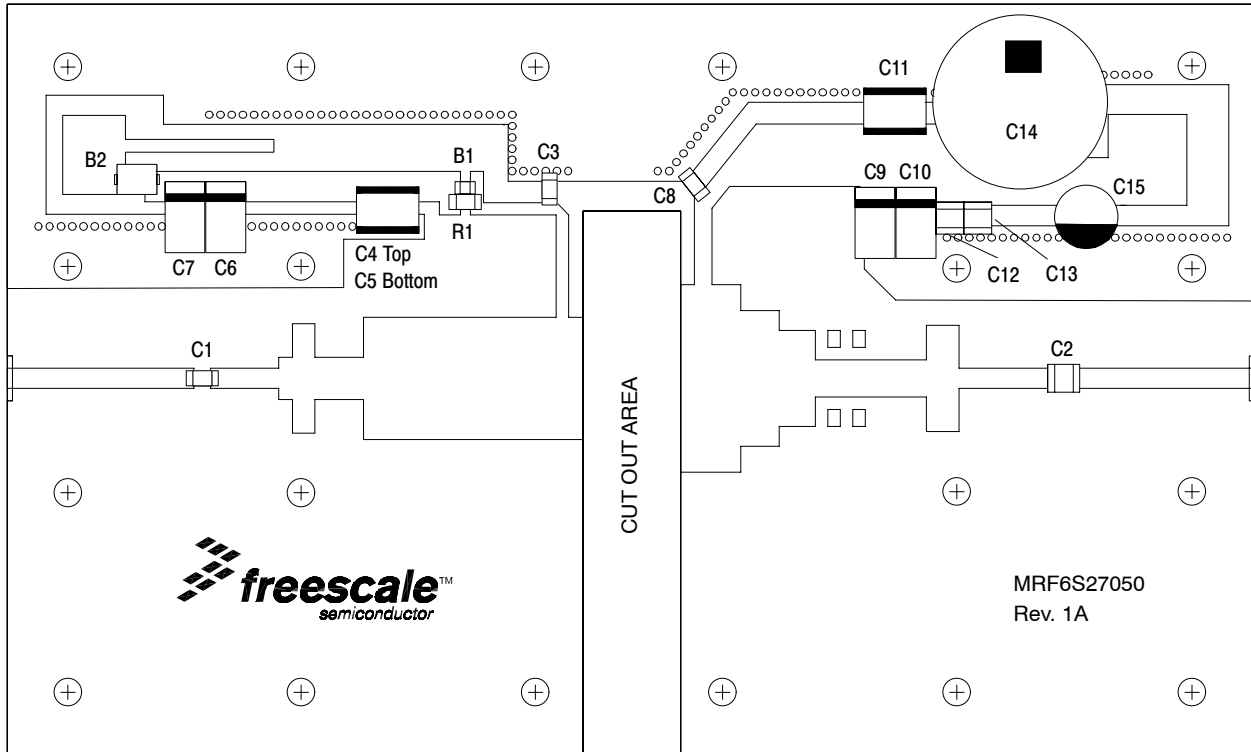
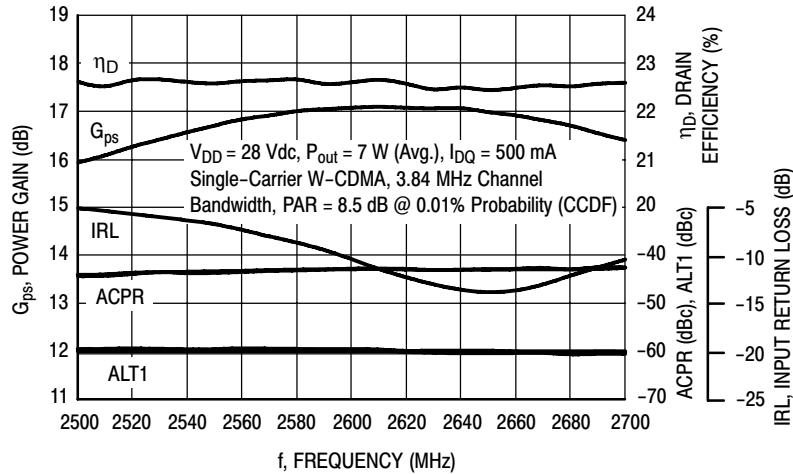
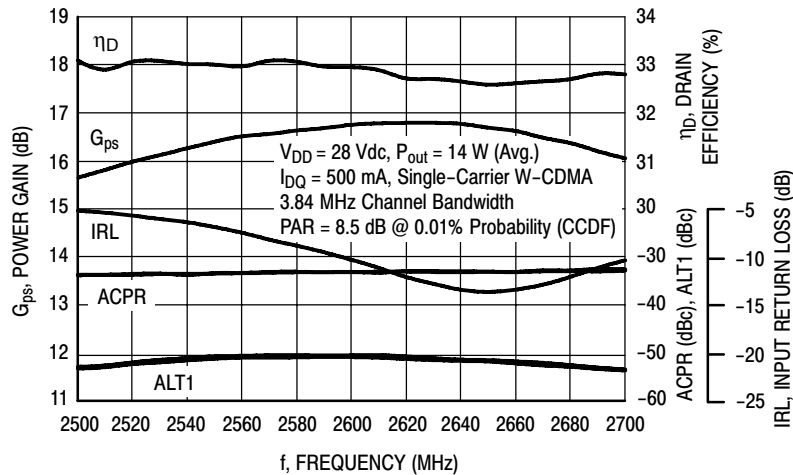


Figure 2. MRF6S27050HR3(SR3) Test Circuit Component Layout

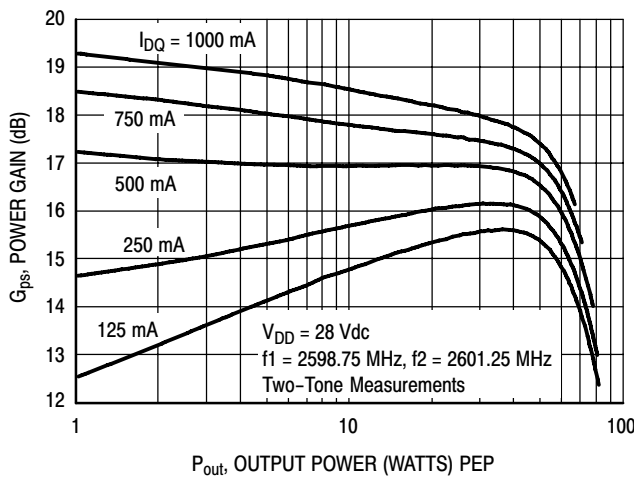
## TYPICAL CHARACTERISTICS



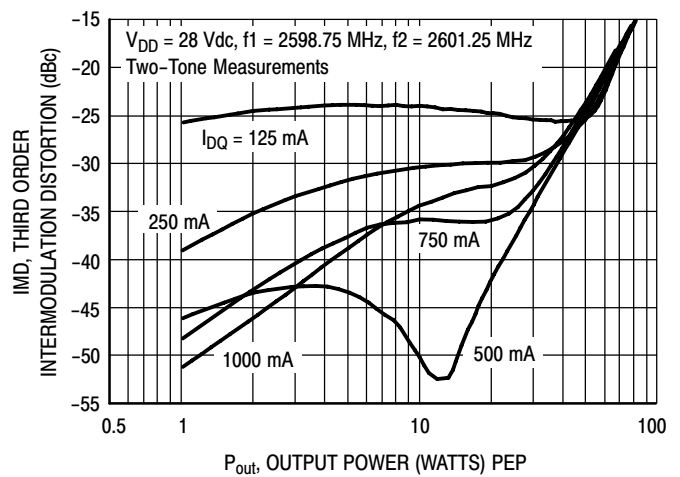
**Figure 3. Single-Carrier W-CDMA Broadband Performance @  $P_{out} = 7$  Watts Avg.**



**Figure 4. Single-Carrier W-CDMA Broadband Performance @  $P_{out} = 14$  Watts Avg.**

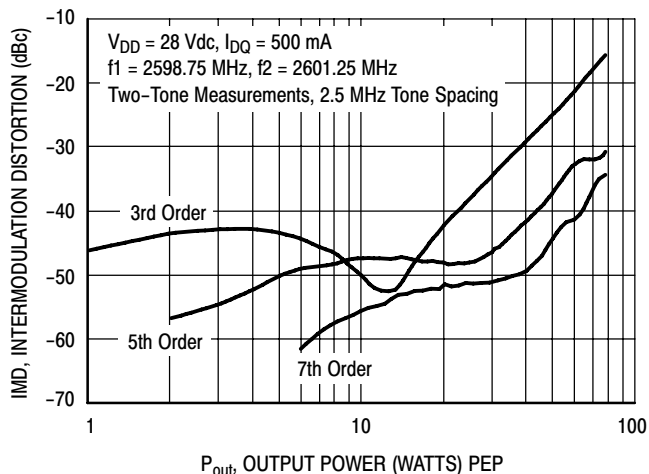


**Figure 5. Two-Tone Power Gain versus Output Power**

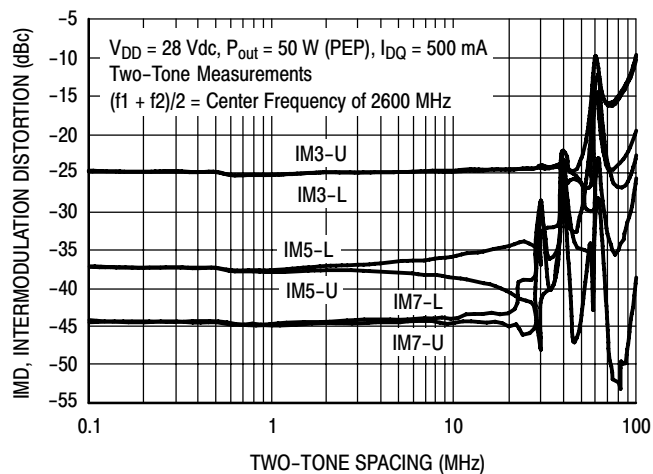


**Figure 6. Third Order Intermodulation Distortion versus Output Power**

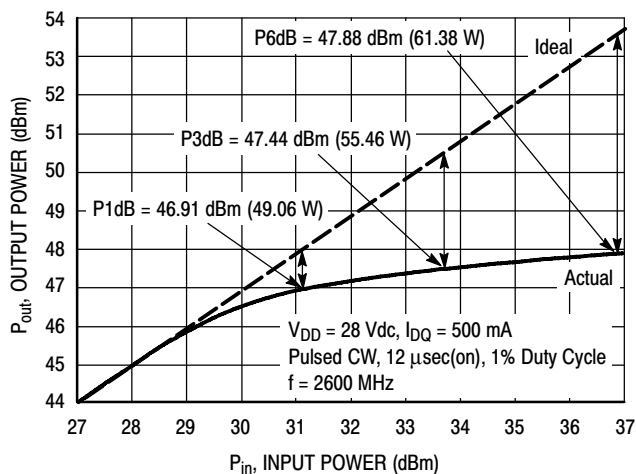
## TYPICAL CHARACTERISTICS



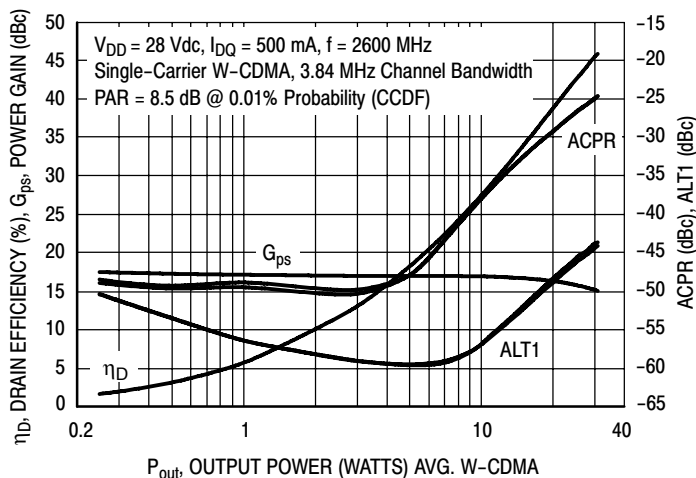
**Figure 7. Intermodulation Distortion Products versus Output Power**



**Figure 8. Intermodulation Distortion Products versus Tone Spacing**

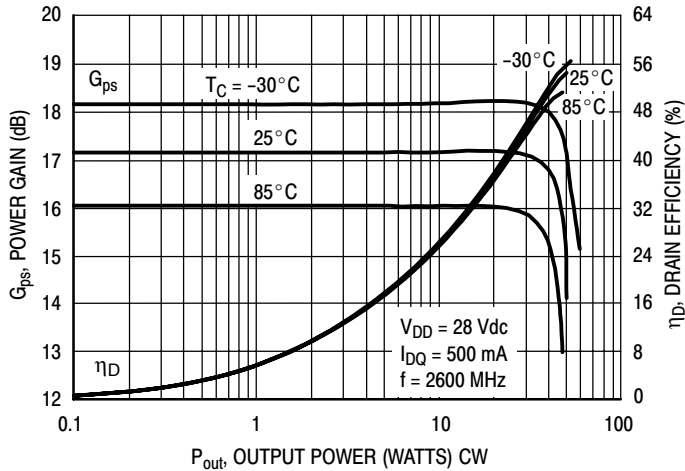


**Figure 9. Pulsed CW Output Power versus Input Power**

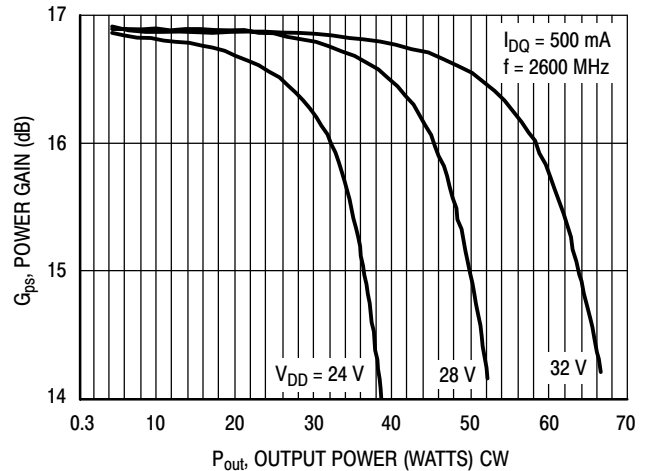


**Figure 10. Single-Carrier W-CDMA ACPR, ALT1, Power Gain and Drain Efficiency versus Output Power**

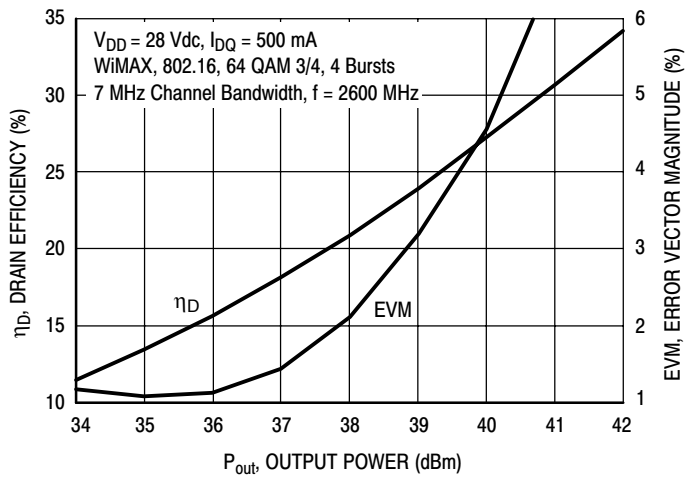
## TYPICAL CHARACTERISTICS



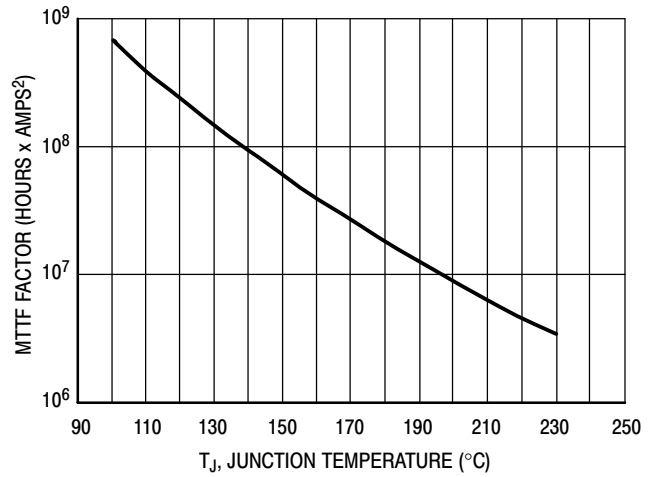
**Figure 11. Power Gain and Drain Efficiency versus CW Output Power**



**Figure 12. Power Gain versus Output Power**



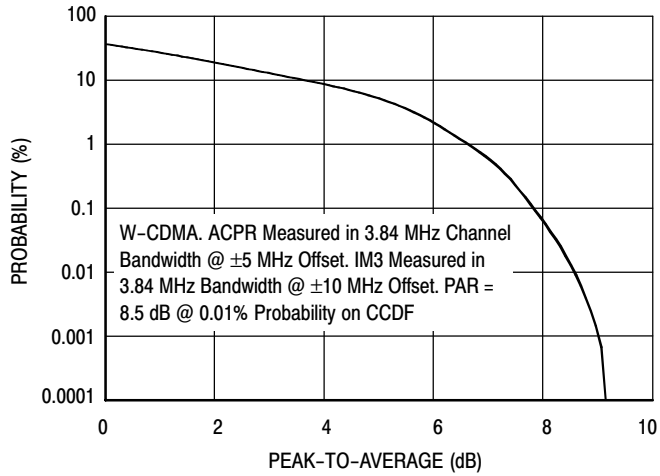
**Figure 13. Drain Efficiency and Error Vector Magnitude versus Output Power**



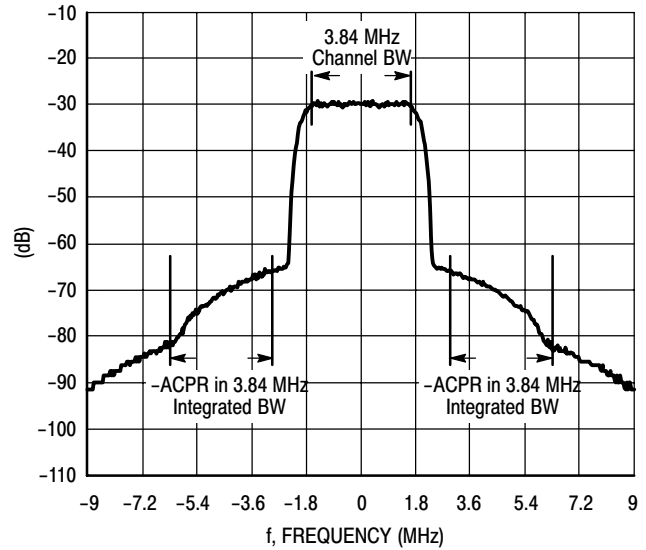
This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than  $\pm 10\%$  of the theoretical prediction for metal failure. Divide MTTF factor by  $I_{DQ}^2$  for MTTF in a particular application.

**Figure 14. MTTF Factor versus Junction Temperature**

## W-CDMA TEST SIGNAL

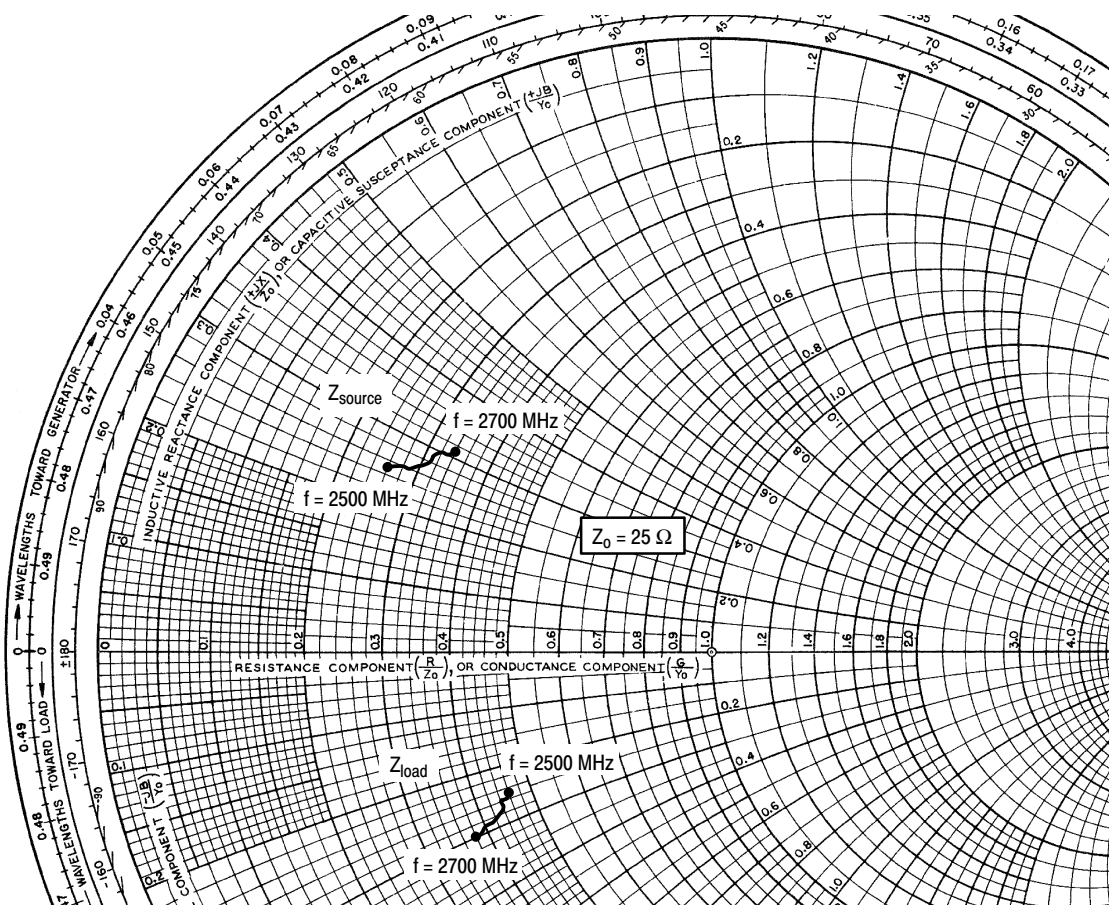


**Figure 15. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single-Carrier Test Signal**



**Figure 16. Single-Carrier W-CDMA Spectrum**





$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 500 \text{ mA}$ ,  $P_{out} = 7 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2500	$6.897 + j6.212$	$11.524 - j6.193$
2525	$7.062 + j6.412$	$11.325 - j6.396$
2550	$7.239 + j6.611$	$11.110 - j6.594$
2575	$7.428 + j6.808$	$10.880 - j6.783$
2600	$7.630 + j7.002$	$10.634 - j6.962$
2625	$7.846 + j7.193$	$10.373 - j7.130$
2650	$8.075 + j7.380$	$10.098 - j7.283$
2675	$8.320 + j7.561$	$9.810 - j7.420$
2700	$8.579 + j7.737$	$9.511 - j7.541$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

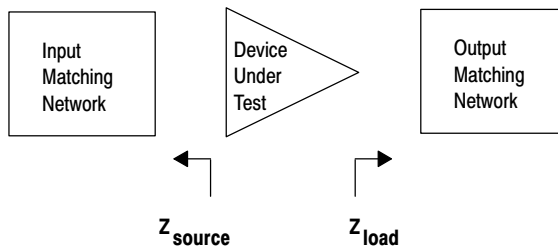
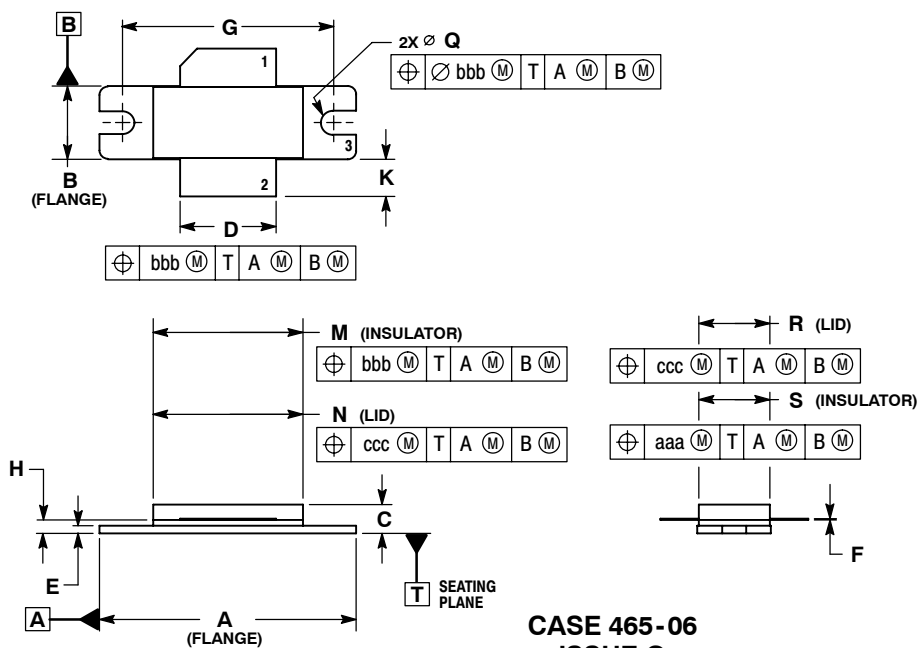


Figure 17. Series Equivalent Source and Load Impedance

## PACKAGE DIMENSIONS

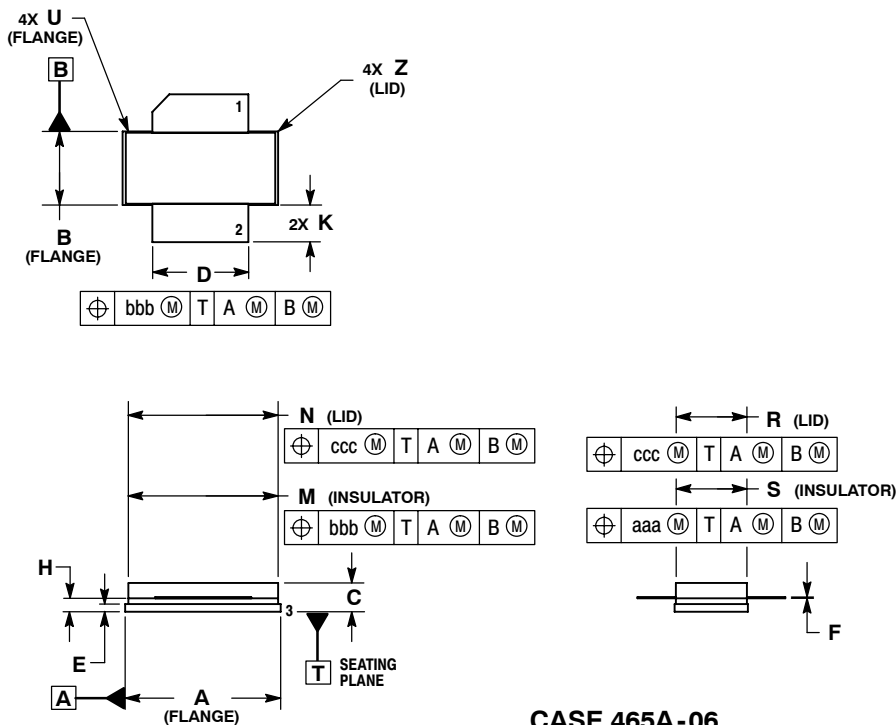


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DELETED
  4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	$\varnothing$ 0.118	$\varnothing$ 0.138	$\varnothing$ 3.00	$\varnothing$ 3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

**CASE 465-06  
 ISSUE G  
 NI-780  
 MRF6S27050HR3**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DELETED
  4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 5. SOURCE

**CASE 465A-06  
 ISSUE H  
 NI-780S  
 MRF6S27050HSR3**

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2006	<ul style="list-style-type: none"><li>• Initial Release of Data Sheet</li></ul>

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **Web Support:**

<http://www.freescale.com/support>

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
+1-800-521-6274 or +1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.  
© Freescale Semiconductor, Inc. 2006. All rights reserved.

