

BUV27

NPN Silicon Power Transistor

This device is designed for use in switching regulators and motor control.

Features

- Low Collector Emitter Saturation Voltage
- Fast Switching Speed
- Pb-Free Package is Available*

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-------------------|-------------|--------------------------|
| Collector-Emitter Sustaining Voltage | V_{CEO} | 120 | Vdc |
| Collector-Emitter Breakdown Voltage | V_{CBO} | 240 | Vdc |
| Emitter-Base Voltage | V_{EBO} | 7.0 | Vdc |
| Collector Current – Continuous – Peak (Note 1) | I_C I_{CM} | 12 20 | Adc |
| Base Current | I_B | 4.0 | Adc |
| Total Device Dissipation ($T_C = 25^\circ\text{C}$) Derate above 25°C | P_D | 70 0.56 | W W/ $^\circ\text{C}$ |
| Operating and Storage Temperature | T_J, T_{stg} | - 65 to 150 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Rating | Symbol | Max | Unit |
|---|------------------------------------|--------------|---------------------------|
| Thermal Resistance, Junction-to-Case Junction-to-Ambient | $R_{\theta JC}$ $R_{\theta JA}$ | 1.78 62.5 | $^\circ\text{C}/\text{W}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle \leq 10%.

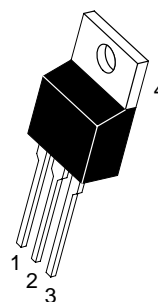


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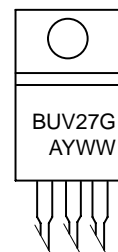
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POWER TRANSISTOR
12 AMPERES
120 VOLTS
70 WATTS

MARKING DIAGRAM



TO-220AB
CASE 221A
STYLE 1



BUV27 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping |
|--------|-----------------------|-------------|
| BUV27 | TO-220AB | 50 per Rail |
| BUV27G | TO-220AB (Pb-Free) | 50 per Rail |

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|----------------------------------|--|--|-----|-----|------------|------|
| I _{CER} | Collector Cut-off Current (R _{BE} = 50 Ω) | V _{CE} = 240 V, T _C = 125°C | | | 3.0 | mA |
| I _{CEX} | Collector Cut-off Current | V _{CE} = 240 V, V _{BE} = -1.5 V, T _C = 125°C | | | 1.0 | mA |
| I _{EBO} | Emitter Cut-off Current (I _C = 0) | V _{BE} = 5 V | | | 1.0 | mA |
| V _{CEO(sus)} | Collector-Emitter Sustaining Voltage | I _C = 0.2 A, L = 25 mH | 120 | | | V |
| V _{EBO} | Emitter-Base Voltage (I _C = 0) | I _E = 50 mA | 7.0 | | 30 | V |
| V _{CE(sat)} (Note 2) | Collector-Emitter Saturation Voltage | I _C = 4 A, I _B = 0.4 A I _C = 8 A, I _B = 0.8 A | | | 0.7 1.5 | V |
| V _{BE(sat)} (Note 2) | Base-Emitter Saturation Voltage | I _C = 8 A, I _B = 0.8 A | | | 2.0 | V |

Resistive Load

| | | | | | | |
|-----------------|--------------|---|--|------|------|----|
| t _{on} | Turn-on Time | V _{CC} = 90 V, I _C = 8 A V _{BE} = -6 V, I _{B1} = 0.8 A R _{BB} = 3.75 Ω | | 0.4 | 0.8 | ms |
| t _s | Storage Time | | | 0.5 | 1.2 | μs |
| t _f | Fall Time | | | 0.12 | 0.25 | μs |

Inductive Load

| | | | | | | |
|----------------|--------------|--|--|------|------|----|
| t _s | Storage Time | V _{CC} = 90 V, I _C = 8 A I _{B1} = 0.8 A, V _{BE} = -5 V L _B = 1 μH | | 0.6 | | μs |
| t _f | Fall Time | | | 0.04 | | |
| t _s | Storage Time | V _{CC} = 90 V, I _C = 8 A I _{B1} = 0.8 A, V _{BE} = -5 V L _B = 1 μH, T _J = 125°C | | | 2.0 | |
| t _f | Fall Time | | | | 0.15 | |

2. Pulsed: Pulse Duration = 300 μs, Duty Cycle = 2%

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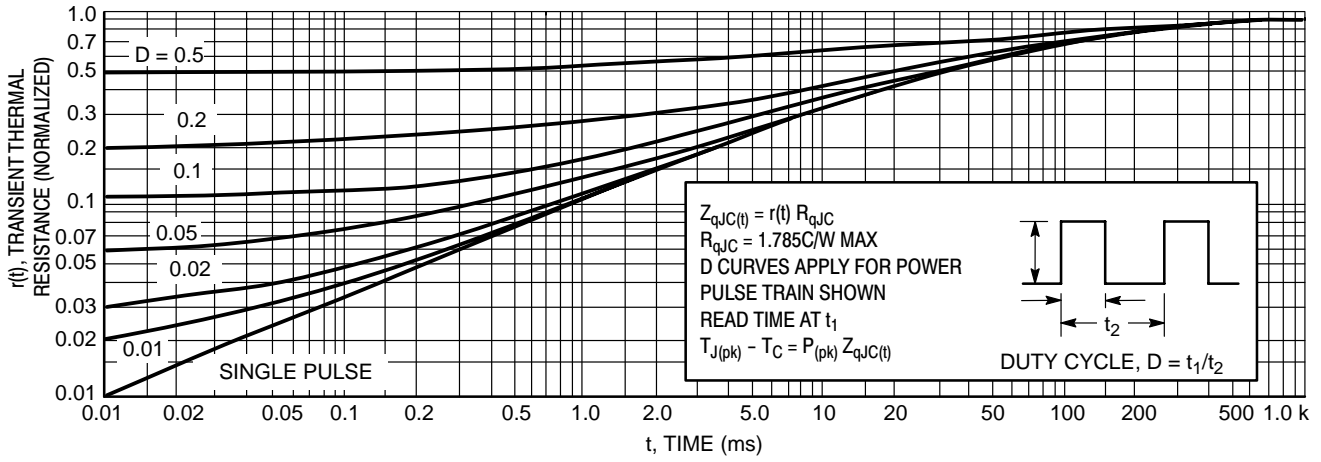


Figure 1. Thermal Response

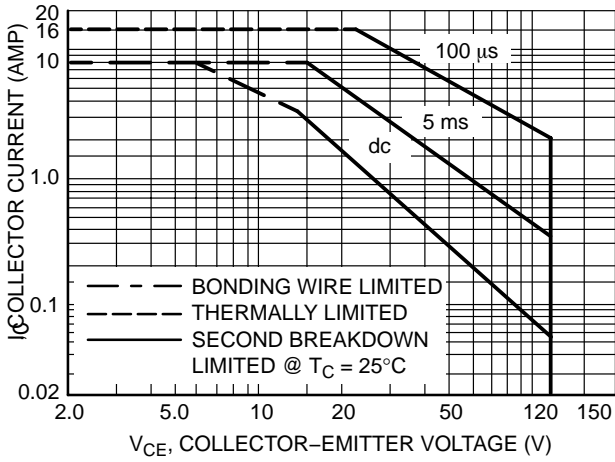


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 is based on $T_{J(pk)} = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

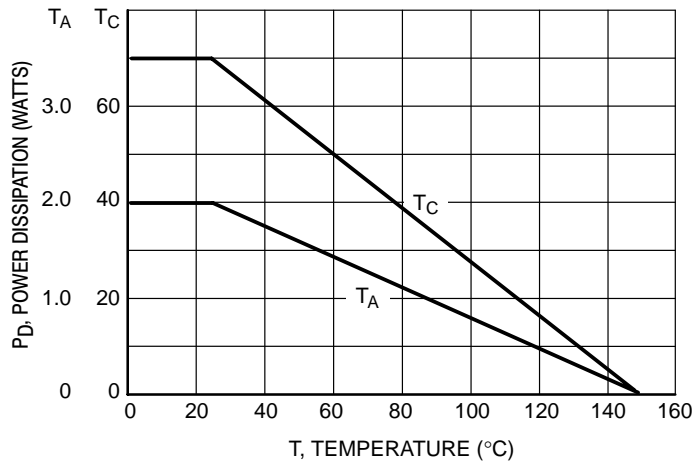
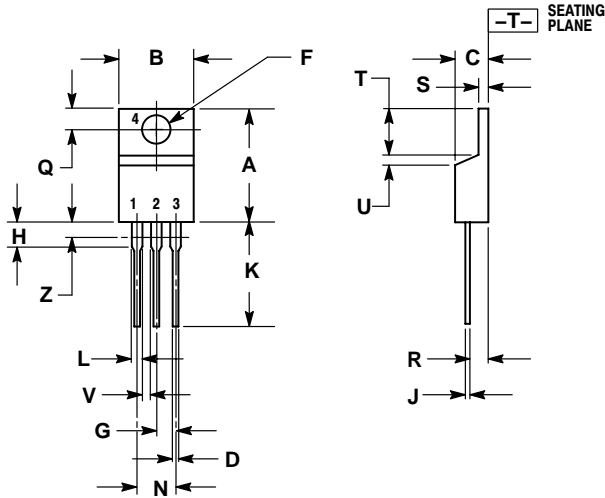


Figure 3. Power Derating

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PACKAGE DIMENSIONS

TO-220AB CASE 221A-09 ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.405 | 9.66 | 10.28 |
| C | 0.160 | 0.190 | 4.07 | 4.82 |
| D | 0.025 | 0.035 | 0.64 | 0.88 |
| F | 0.142 | 0.147 | 3.61 | 3.73 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.155 | 2.80 | 3.93 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.39 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | --- | 1.15 | --- |
| Z | --- | 0.080 | --- | 2.04 |

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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