BLA6G1011-200R

Power LDMOS transistor

Rev. 02 — 1 March 2010 Preliminary data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for avionics applications at frequencies from 1030 MHz to 1090 MHz.

Table 1. Test information

Typical RF performance at T_{case} = 25 °C in a class-AB production test circuit.

Mode of operation	f	V_{DS}	P_L	G_p	η_D	t_r	t_f
	(MHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed class-AB	1030 to 1090	28	200	20	65	10	6

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

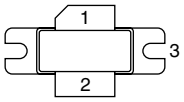
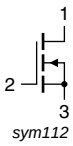
- Typical pulsed RF performance at frequencies of 1030 MHz and 1090 MHz, a supply voltage of 28 V and an I_{Dq} of 100 mA:
  - Output power = 200 W
  - Power gain = 20 dB
  - Efficiency = 65 %
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1030 MHz to 1090 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- Avionics transmitter applications in the 1030 MHz to 1090 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

sym112

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA6G1011-200R	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	49	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 25 °C; t_p = 50 μs; δ = 2 %	0.085	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.9 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 270 mA	1.4	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1620 mA	1.7	2.2	2.7	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	40	48	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9.45 A	11	18	26	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 9.45 A	0.012	0.07	0.093	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	3	-	pF

Table 7. RF characteristics

Mode of operation: Pulsed RF; t_p = 50 μs; δ = 2 %; V_{DS} = 28 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		200	-	-	W
G_p	power gain	P_L = 200 W	18	20	-	dB
RL_{in}	input return loss	P_L = 200 W	8	10	-	dB
η_D	drain efficiency	P_L = 200 W	58	65	-	%
t_r	rise time	P_L = 200 W	-	10	20	ns
t_f	fall time	P_L = 200 W	-	6	20	ns

6.1 Ruggedness in class-AB operation

The BLA6G1011-200R is an enhanced rugged device and is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: t_p = 50 μs; δ = 2 %; V_{DS} = 28 V; I_{Dq} = 100 mA; P_L = 200 W; f = 1030 MHz to 1090 MHz.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Typical values unless otherwise specified.

f	Z_S	Z_L
MHz	Ω	Ω
1030	0.57 – j0.94	0.80 – j0.68
1060	0.70 – j1.13	0.84 – j0.52
1090	0.80 – j1.53	0.86 – j0.35

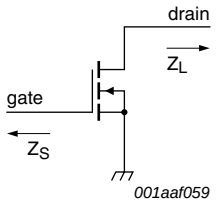
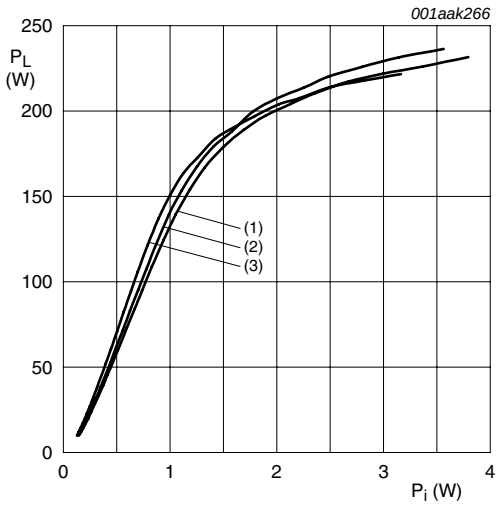


Fig 1. Definition of transistor impedance

7.2 RF performance



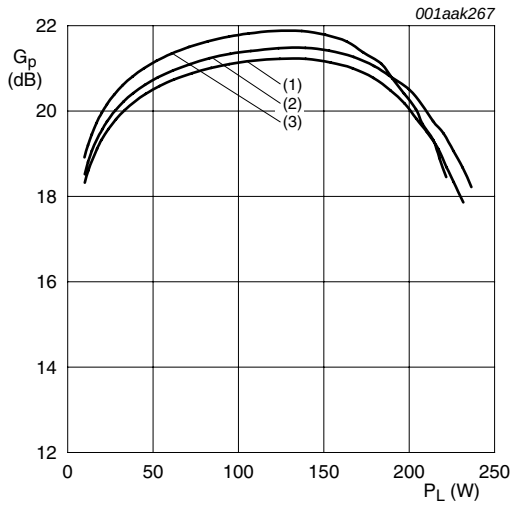
V_{DS} = 28 V; t_p = 50 µs; δ = 2 %; I_{Dq} = 100 mA.

(1) f = 1030 MHz

(2) f = 1060 MHz

(3) f = 1090 MHz

Fig 2. Output power as a function of input power; typical values



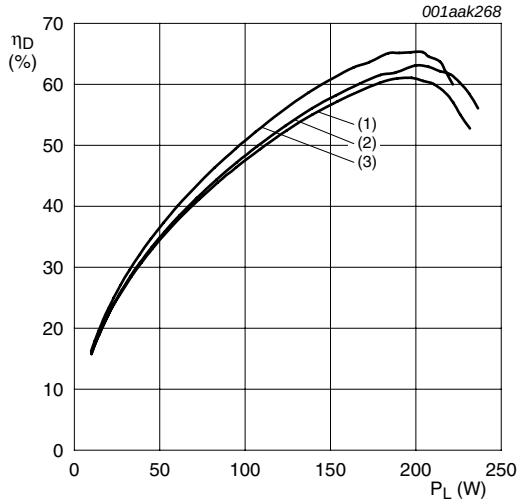
V_{DS} = 28 V; t_p = 50 µs; δ = 2 %; I_{Dq} = 100 mA.

(1) f = 1030 MHz

(2) f = 1060 MHz

(3) f = 1090 MHz

Fig 3. Power gain as a function of load power; typical values



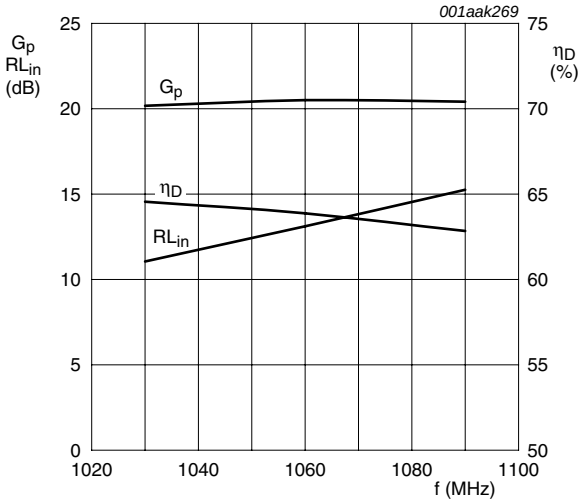
V_{DS} = 28 V; t_p = 50 μs; δ = 2 %; I_{Dq} = 100 mA.

(1) f = 1030 MHz

(2) f = 1060 MHz

(3) f = 1090 MHz

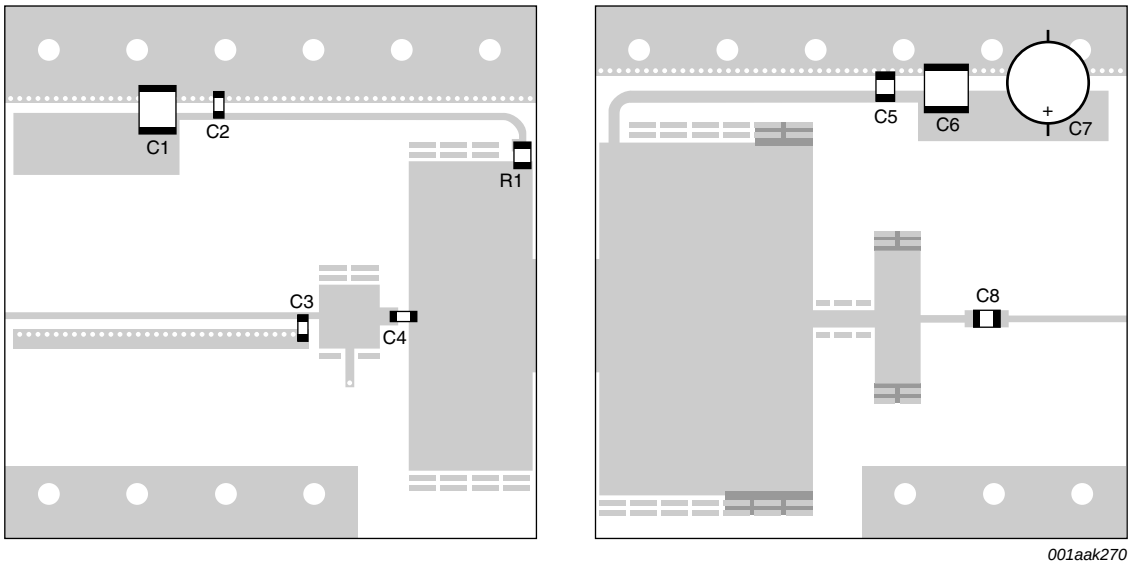
Fig 4. Drain efficiency as a function of load power; typical values



P_L = 200 W; V_{DS} = 28 V; t_p = 50 μs; δ = 2 %; I_{Dq} = 100 mA.

Fig 5. Power gain, input return loss and drain efficiency as function of frequency; typical values

7.3 Application circuit



See Table 9 for list of components.

Fig 6. Component layout for class-AB application circuit

Table 9. List of components

See Figure 6.

Striplines are on a Rogers Duroid 6010 Printed-Circuit Board (PCB); ε_r = 6.15 F/m; thickness = 0.64 mm

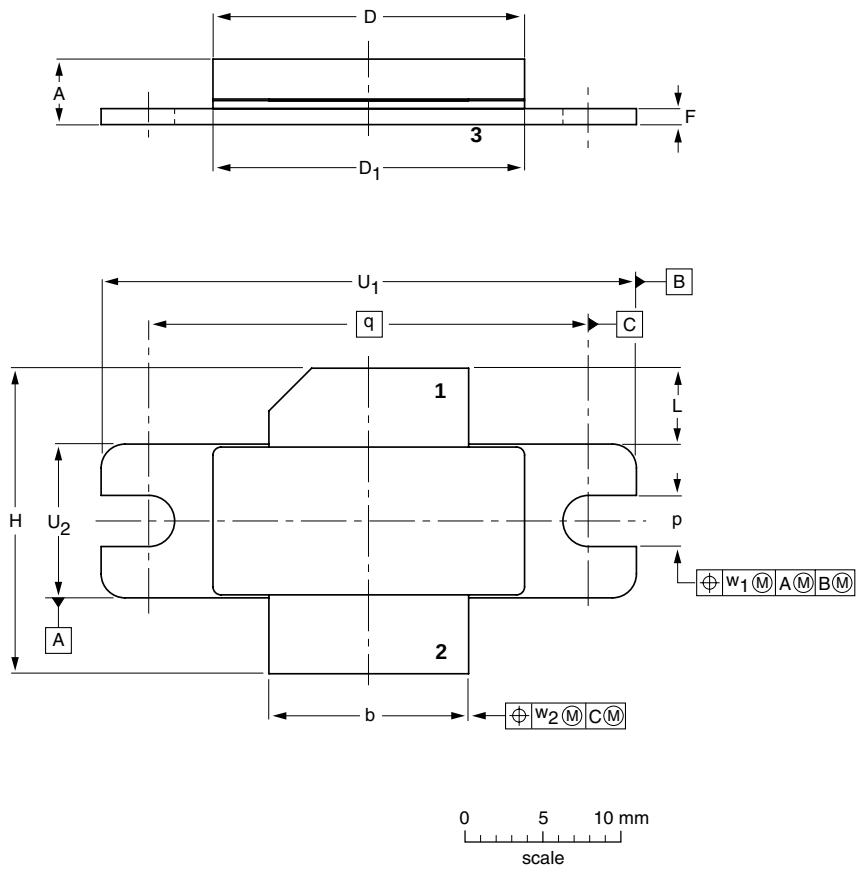
Component	Description	Value		Remarks
C1, C6	multilayer ceramic chip capacitor	10 μF		TDK
C2	multilayer ceramic chip capacitor	68 pF	[1]	
C3	multilayer ceramic chip capacitor	1.5 pF	[1]	
C4	multilayer ceramic chip capacitor	3.9 pF	[1]	
C5, C8	multilayer ceramic chip capacitor	30 pF	[2]	
C7	electrolytic capacitor	470 μF; 63 V		
R1	SMD resistor	12 Ω		1206

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Fig 7. Package outline SOT502A

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA6G1011-200R_2	20100301	Preliminary data sheet	-	BLA6G1011-200R_1
Modifications:	• The status of this document has been changed to “Preliminary data sheet”.			
BLA6G1011-200R_1	20090617	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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