8input-2output Video Switch with Isolation Amplifier & small AC-coupled Video Driver

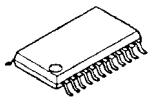
■ GENERAL DESCRIPTION

The **NJW1341** is 8-Input,2-Output Video Switch.

The **NJW1341** consists of switch and isolation amplifiers(2input) and Video Driver which features small AC-coupled(1output).

All of functions are controlled by I2C Bus.

■ PACKAGE OUTLINE



NJW1341VC3

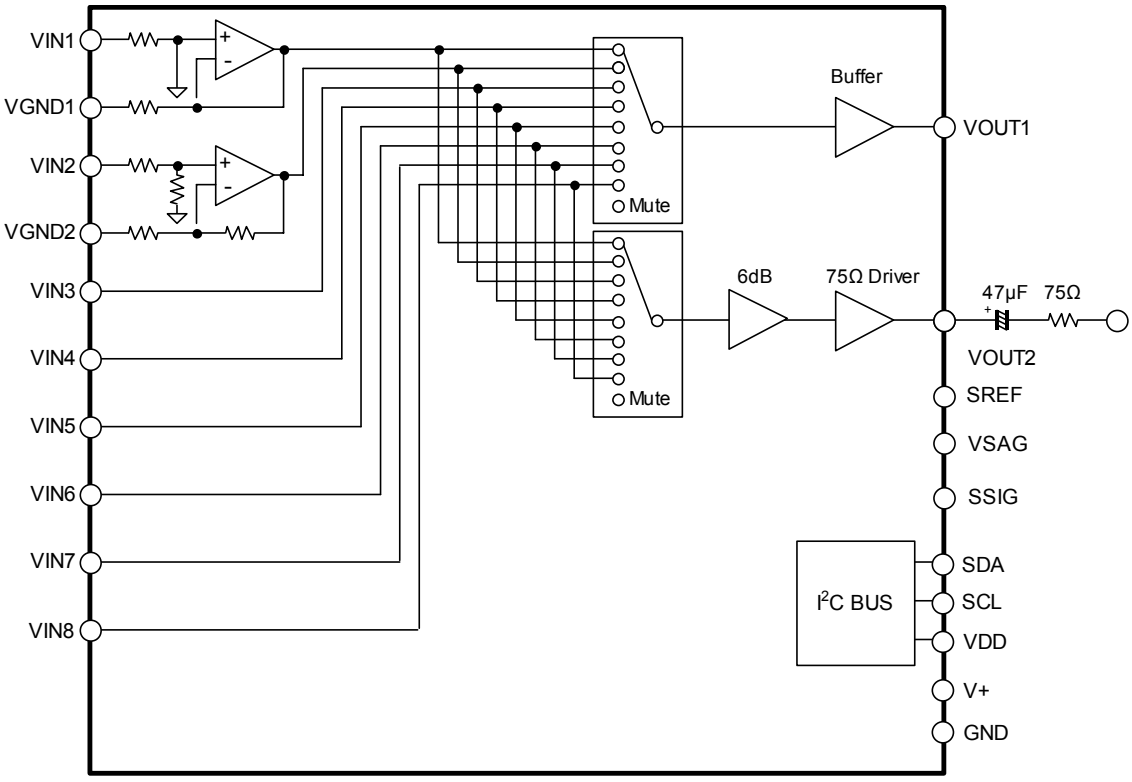
■APPLICATIONS

- ●Car AVN
- ●Any Video System

■ FEATURES

- ● Operating Voltage 4.5 to 9.5V
- ● Small AC-coupled video amplifier (VOUT2)
- ● Isolation Amplifiers(VIN1,2)
- ● 8in-2out Video Switch
- ● Common Mode Rejection Ratio -50dB typ
- ● Bi-CMOS Technology
- ● I^2C BUS interface
- ● Package Outline SSOP20-C3

■ BLOCK DIAGRAM



Ver.2

■ **ABSOLUTE MAXIMUM RATING** (Ta=25°C)

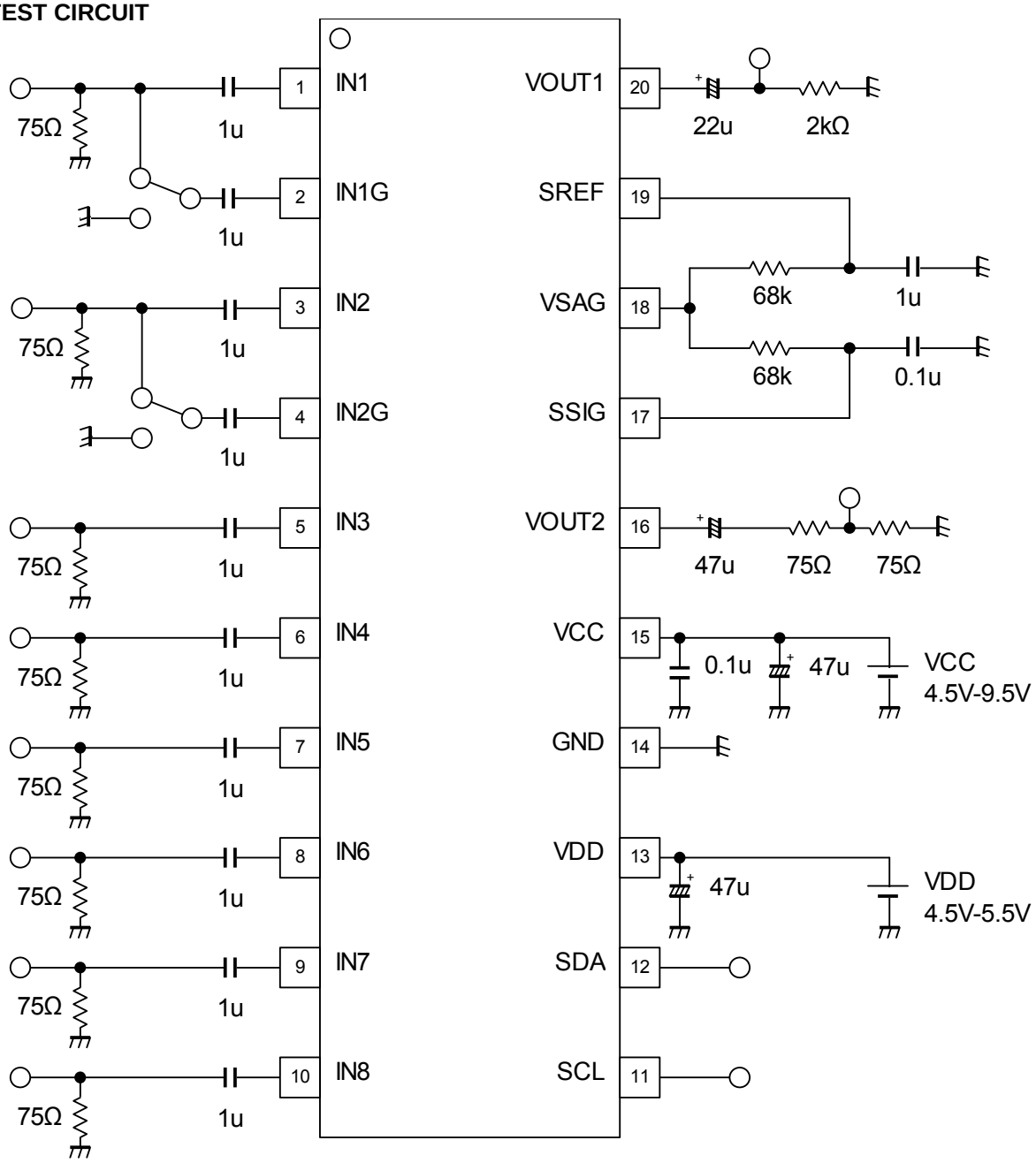
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	VCC:+13,VDD:+7	V
Power Dissipation	P_D	1,000(note1)	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +150	°C

(note1)At on a board of EIA/JEDEC specification. (114.3 x 76.2 x 1.6mm 2 layers, FR-4)

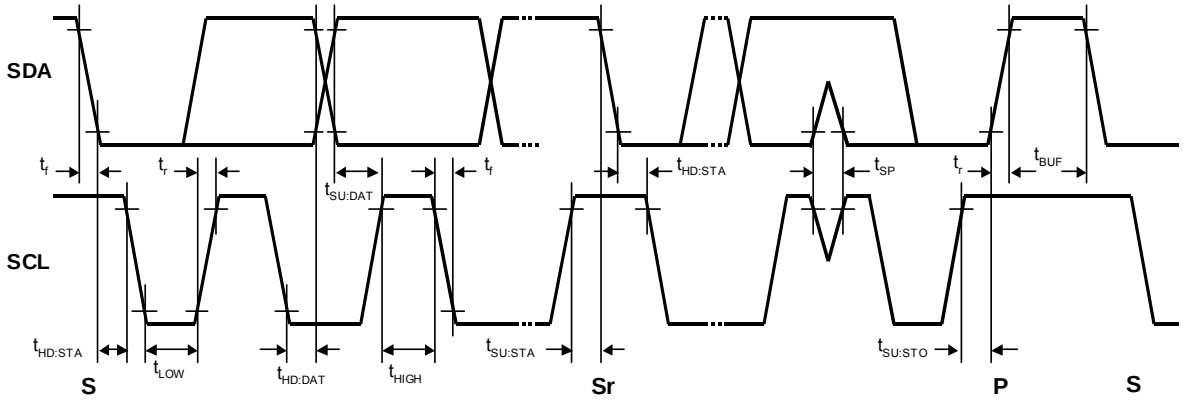
■ **ELECTRICAL CHARACTERISTICS(V^+=5V,Ta=25°C)**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage 1	V_{CC}		4.5	5	9.5	V
Operating Voltage 1	V_{DD}		4.5	5	5.5	V
Operating Current 1	I_{CC1}	No,signal	-	25	40	mA
Operating Current 2	I_{CC2}	OUT2 power save	-	10	15	mA
Operating Current 3	I_{CC3}	OUT1power save	-	20	35	mA
Operating Current 4	I_{save}	OUT1,OUT2 power save		2	4	mA
Maximum Output Voltage	Vvom	f=100kHz,THD=1%	2.4	-	-	Vp-p
Voltage Gain1	Gv1	OUT1,Vin=1MHz,1.0Vp-p,Sine Signal	-1.0	0	1.0	dB
Voltage Gain2	Gv2	OUT2,Vin=1MHz,1.0Vp-p,Sine Signal	5.5	6.0	6.5	dB
Low Pass Filter Characteristic 1	Gf	Vin=10MHz /1MHz, 1.0Vp-p sine wave	-1.0	0	1.0	dB
Differential Gain	DG	Vin=1.0Vp-p,10step Video Signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p,10step Video Signal	-	0.5	-	deg
S/N Ratio	SN	Vin=1.0Vp-p, 100% White video signal,RL=75Ω, 100KHz to 6MHz	-	60	-	dB
Common mode Rejection Ratio	CMR	Vin=20kHz, 1.0Vp-p Sine Signal	-	-55	-	dB
CrossTalk	CT	Vin=4.43MHz, 1.0Vp-p Sine Signal		-60		dB

■ **TEST CIRCUIT**



■TIMING on the I²C BUS (SDA, SCL)



■CHARACTERISTICS OF BUS LINES (SDA, SCL) FOR I²C BUS DEVICES

I²C BUS Load Conditions
STANDARD MODE : Pull up resistance 4kΩ (Connected to +3.3V), Load capacitance 200pF (Connected to GND)
FAST MODE : Pull up resistance 4kΩ (Connected to +3.3V), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V_{IL}	0.0	-	1.5	0.0	-	1.5	V
High Level Input Voltage	V_{IH}	2.7	-	5.0	2.7	-	5.0	V
Hysteresis of Schmitt Trigger Inputs	V_{hys}	-	-	-	0.25	-	-	V
Low level Output Voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	0	-	0.4	V
Output Fall Time From V_{IHmin} to V_{ILmax} with a Bus Capacitance from 10pF to 400pF	t_{of}	-	-	250	$20 +0.1C_b$	-	250	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	-	-	-	0	-	50	ns
Input Current each I/O pin with an Input Voltage between 0.1 and $0.9V_{DDmax}$	I_i	-10	-	10	-10	-	10	μA
Capacitance for each I/O pin	C_i	-	-	10	-	-	10	pF
SCL Clock Frequency	f_{SCL}	-	-	100	-	-	400	kHz
Data Transfer Start Minimum Waiting Time	$t_{HD:STA}$	4.0	-	-	0.6	-	-	μs
Low Level Clock Pulse Width	t_{LOW}	4.7	-	-	1.3	-	-	μs
High Level Clock Pulse Width	t_{HIGH}	4.0	-	-	0.6	-	-	μs
Minimum Start Preparation Waiting Time	$t_{SU:STA}$	4.7	-	-	0.6	-	-	μs
Minimum Data Hold Time NOTE)	$t_{HD:DAT}$	0.0	-	3.45	0.0	-	0.9	μs
Minimum Data Preparation Time	$t_{SU:DAT}$	250	-	-	100	-	-	ns
Rise Time	t_r	-	-	1000	-	-	300	ns
Fall Time	t_f	-	-	300	-	-	300	ns
Minimum Stop Preparation Waiting Time	$t_{SU:STO}$	4.0	-	-	0.6	-	-	μs
Data Change Minimum Waiting Time	t_{BUF}	4.7	-	-	1.3	-	-	μs
Capacitive load for each bus line	C_b	-	-	400	-	-	400	pF
Noise Margin at the Low Level	V_{nL}	0.5	-	-	0.5	-	-	V
Noise Margin at the High Level	V_{nH}	1	-	-	1	-	-	V

C_b ; total capacitance of one bus line in pF.

NOTE). Please hold the Data Hold Time ($t_{HD:DAT}$) to 300ns or more to avoid status of unstable at SCL falling edge.

■ DEFINITION OF I²C REGISTER

♦I²C BUS FORMAT

MSB		LSB	MSB		LSB	
S	Slave Address	A	Data		A	P
1bit	8bit	1bit	8bit		1bit	1bit

S: Starting Term
A: Acknowledge Bit
P: Ending Term

♦SLAVE ADDRESS

MSB							LSB
0	0	1	0	0	0	0	0

R/W=0: Receive Only
R/W=1: Data is not transmitted.

♦CONTROL REGISTER DEFAULT VALUE

Control register default values are as follows :

	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	0	0	0	0	0	0	0	0

♦INSTRUCTION CODE

	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	OUT1 MUTE	OUT1 Select			OUT2 MUTE	OUT2 Select		

♦MUTE TABLE

MUTE D7	OUT1
0	MUTE OFF
1	MUTE ON

MUTE D3	OUT2
0	MUTE OFF
1	MUTE ON

MUTE OFF: Active mode
MUTE ON: Power save mode

♦**VOUT SELECT TABLE**

OUT1 Select			OUT1
D6	D5	D4	
0	0	0	VIN1
0	0	1	VIN2
0	1	0	VIN3
0	1	1	VIN4
1	0	0	VIN5
1	0	1	VIN6
1	1	0	VIN7
1	1	1	VIN8

OUT2 Select			OUT2
D2	D1	D0	
0	0	0	VIN1
0	0	1	VIN2
0	1	0	VIN3
0	1	1	VIN4
1	0	0	VIN5
1	0	1	VIN6
1	1	0	VIN7
1	1	1	VIN8