

74ABT827

10-bit buffer/line driver; non-inverting; 3-state

Rev. 03 — 24 February 2010

Product data sheet

1. General description

The 74ABT827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT827 10-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE0}$, $\overline{OE1}$) for maximum control flexibility.

2. Features and benefits

- Ideal where high speed, light loading, or increased fan-in are required
- Flow-through pinout architecture for microprocessor oriented applications
- Output capability: +64 mA and –32 mA
- Power-up 3-state
- Inputs are disabled during 3-state mode
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

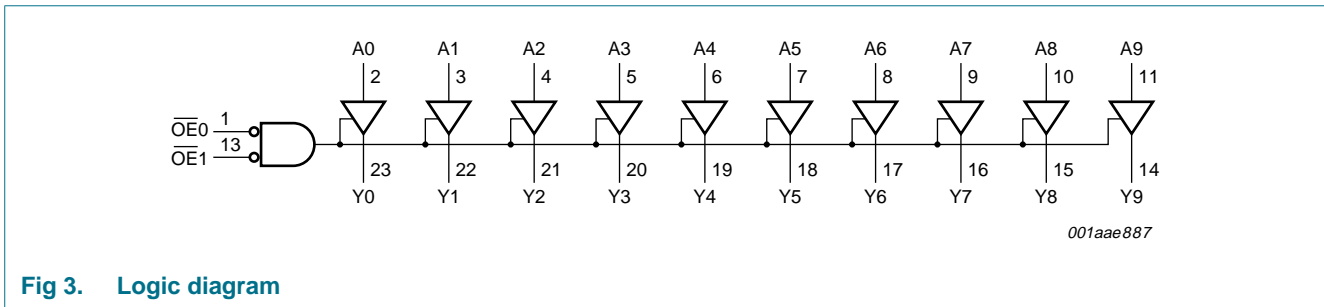
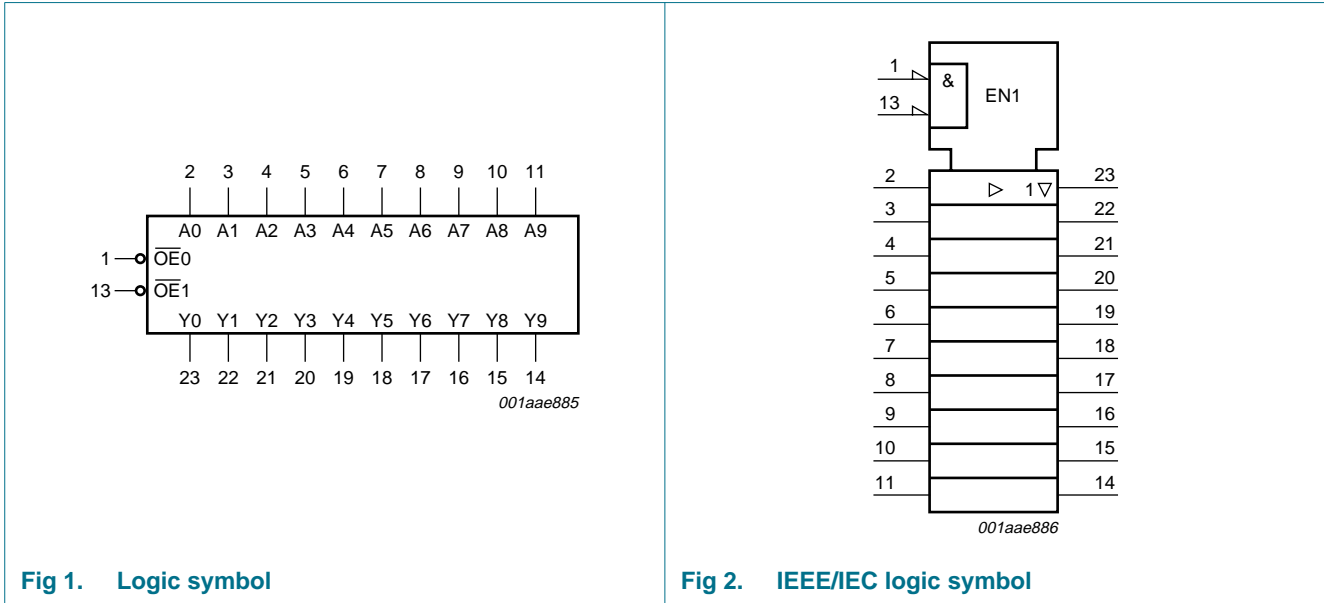
3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ABT827D	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT827DB	–40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT827PW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1



4. Functional diagram



5. Pinning information

5.1 Pinning

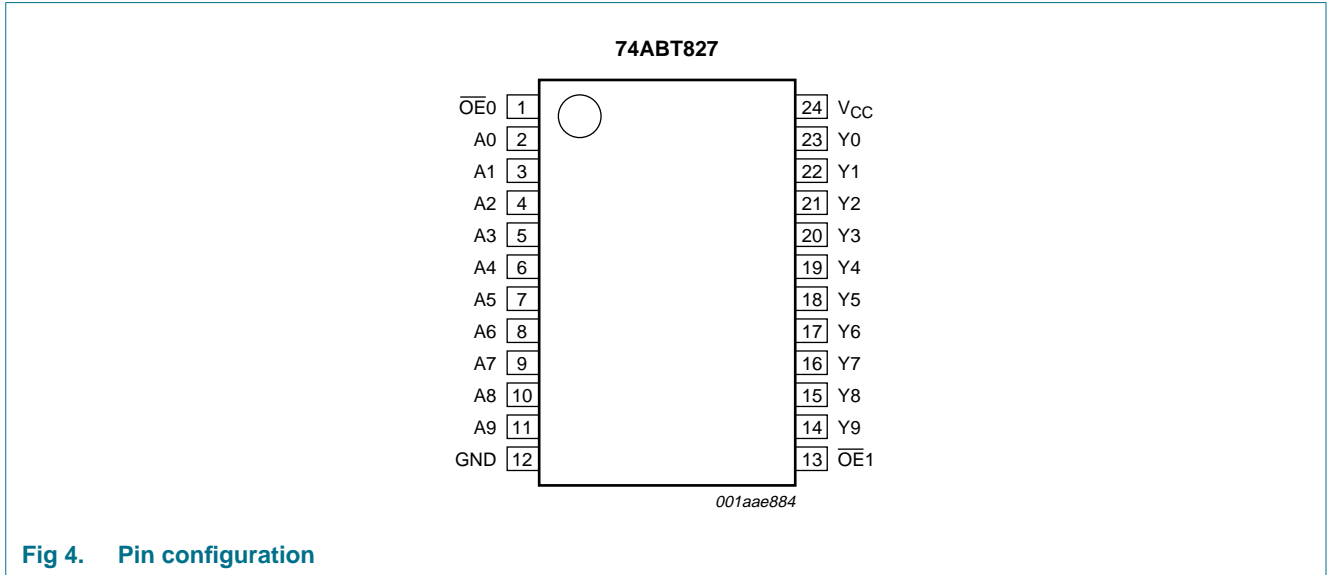


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}0$	1	output enable input (active LOW)
A0 to A9	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	data input
GND	12	ground (0 V)
$\overline{OE}1$	13	output enable input (active LOW)
Y0 to Y9	23, 22, 21, 20, 19, 18, 17, 16, 15, 14	data output
V _{CC}	24	supply voltage

6. Functional description

6.1 Function table

Table 3. Function table^[1]

Inputs		Output	Operating mode
$\overline{OE}n$	A _n	Y _n	
L	L	L	transparent
L	H	H	transparent
H	X	Z	high-impedance

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		[1] -1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
T_j	junction temperature		[2] -	150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit	
			Min	Typ	Max	Min	Max		
V_{IK}	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$	-1.2	-0.9	-	-1.2	-	V	
V_{OH}	HIGH-level output voltage	$V_I = V_{IL} \text{ or } V_{IH}$							
		$V_{CC} = 4.5 \text{ V}; I_{OH} = -3 \text{ mA}$	2.5	2.9	-	2.5	-	V	
		$V_{CC} = 5.0 \text{ V}; I_{OH} = -3 \text{ mA}$	3.0	3.4	-	3.0	-	V	
		$V_{CC} = 4.5 \text{ V}; I_{OH} = -32 \text{ mA}$	2.0	2.4	-	2.0	-	V	
V_{OL}	LOW-level output voltage	$V_{CC} = 4.5 \text{ V}; I_{OL} = 64 \text{ mA}; V_I = V_{IL} \text{ or } V_{IH}$	-	0.42	0.55	-	0.55	V	
I_I	input leakage current	$V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } 5.5 \text{ V}$	-	± 0.01	± 1.0	-	± 1.0	μA	
I_{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_I \text{ or } V_O \leq 4.5 \text{ V}$	-	± 5.0	± 100	-	± 100	μA	
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.0 \text{ V}; V_O = 0.5 \text{ V}; V_I = \text{GND or } V_{CC}; \overline{\text{OEn}} \text{ HIGH}$	[1]	± 5.0	± 50	-	± 50	μA	
I_{OZ}	OFF-state output current	$V_{CC} = 5.5 \text{ V}; V_I = V_{IL} \text{ or } V_{IH}$							
		$V_O = 2.7 \text{ V}$	-	5.0	50	-	50	μA	
		$V_O = 0.5 \text{ V}$	-	-5.0	-50	-	-50	μA	
I_{LO}	output leakage current	HIGH-state; $V_O = 5.5 \text{ V}; V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$	-	5.0	50	-	50	μA	
I_O	output current	$V_{CC} = 5.5 \text{ V}; V_O = 2.5 \text{ V}$	[2]	-180	-80	-50	-180	-50	mA
I_{CC}	supply current	$V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$							
		outputs HIGH-state	-	0.5	250	-	250	μA	
		outputs LOW-state	-	25	38	-	38	mA	
		outputs disabled	-	0.5	250	-	250	μA	
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 5.5 \text{ V};$ one input at 3.4 V; other inputs at V_{CC} or GND	[3]						
		outputs enabled	-	0.5	1.5	-	1.5	mA	
		outputs 3-state, one data input	-	0.01	50	-	50	mA	
		outputs 3-state; one enable input	-	0.5	1.5	-	1.5	mA	
C_I	input capacitance	$V_I = 0 \text{ V or } V_{CC}$	-	4	-	-	-	pF	
C_O	output capacitance	outputs disabled; $V_O = 0 \text{ V or } V_{CC}$	-	7	-	-	-	pF	

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 ms. For $V_{CC} = 2.1 \text{ V}$ to $V_{CC} = 5 \text{ V} \pm 10 \%$, a transition time of up to 100 μs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

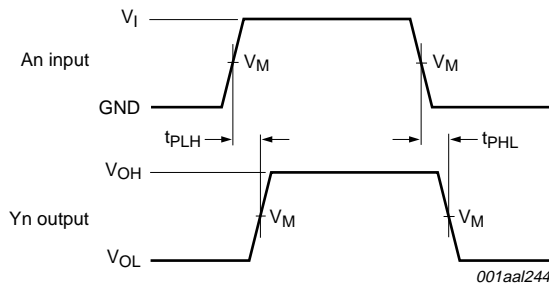
[3] This is the increase in supply current for each input at 3.4 V.

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V; for test circuit, see Figure 7.

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			-40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	A _n to Y _n ; see Figure 5	1.1	3.0	4.4	1.1	4.8	ns
t _{PHL}	HIGH to LOW propagation delay	A _n to Y _n ; see Figure 5	1.1	2.9	4.1	1.1	4.7	ns
t _{PZH}	OFF-state to HIGH propagation delay	\overline{OEn} to Y _n ; see Figure 6	1.6	3.7	5.1	1.6	5.9	ns
t _{PZL}	OFF-state to LOW propagation delay	\overline{OEn} to Y _n ; see Figure 6	2.6	4.6	5.9	2.6	6.9	ns
t _{PHZ}	HIGH to OFF-state propagation delay	\overline{OEn} to Y _n ; see Figure 6	2.0	4.8	6.3	2.0	6.8	ns
t _{PLZ}	LOW to OFF-state propagation delay	\overline{OEn} to Y _n ; see Figure 6	2.5	5.1	6.6	2.5	6.9	ns

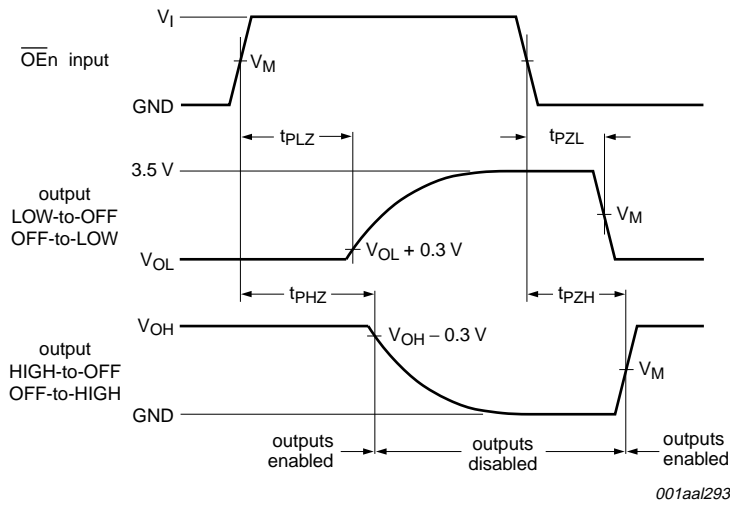
11. Waveforms



$V_M = 1.5\text{ V}$

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

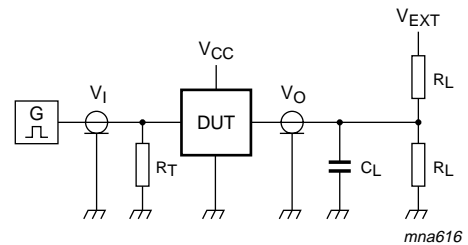
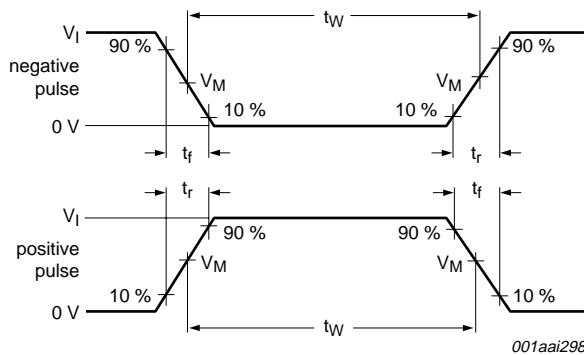
Fig 5. Propagation delay input (An) to output (Yn)



$V_M = 1.5\text{ V}$

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. 3-state enable and disable times



a. Input pulse definition

Test data and V_{EXT} levels are given in [Table 8](#).

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 7. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_w	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	$\leq 2.5\text{ ns}$	50 pF	500 Ω	open	open	7.0 V

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

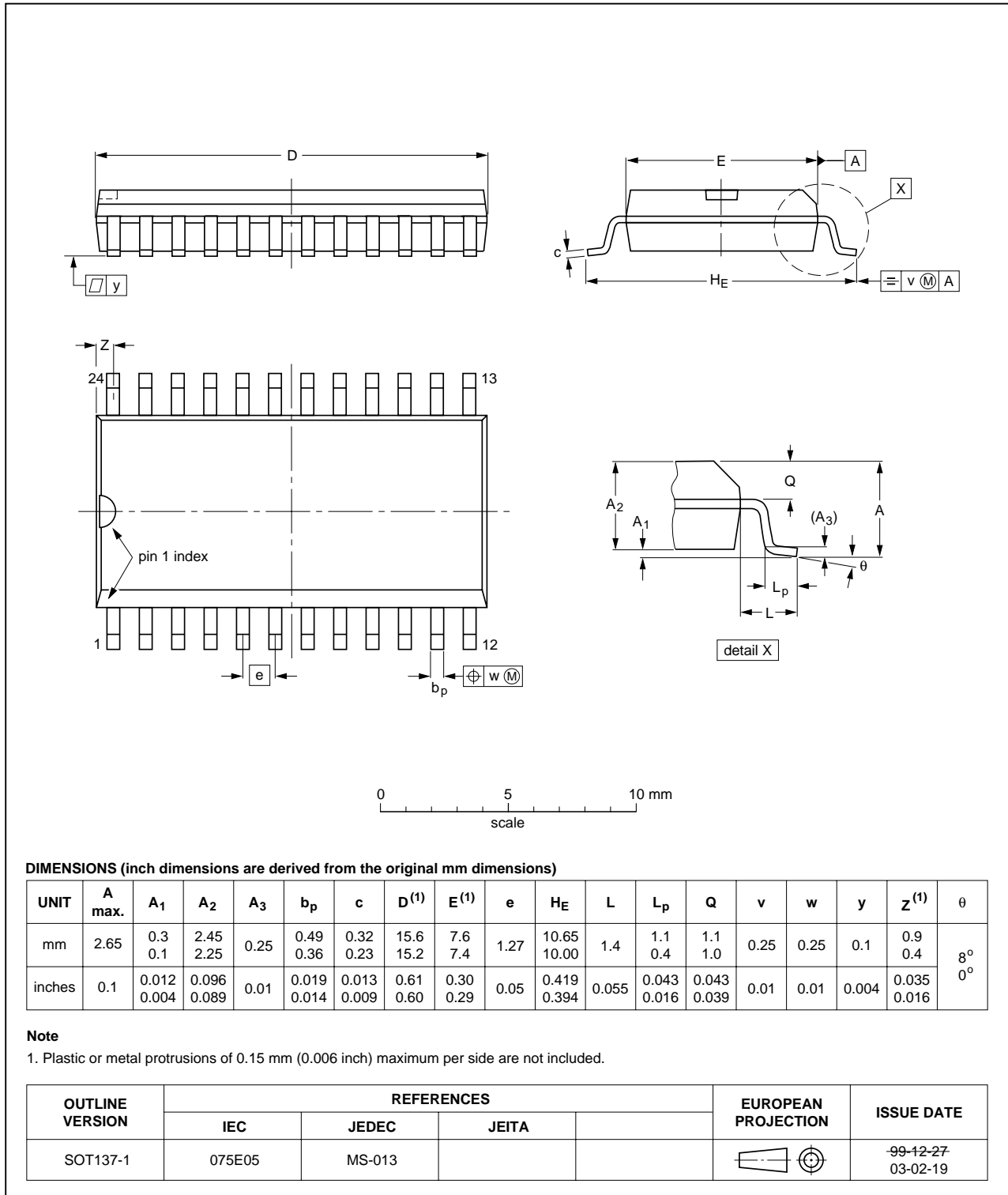


Fig 8. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

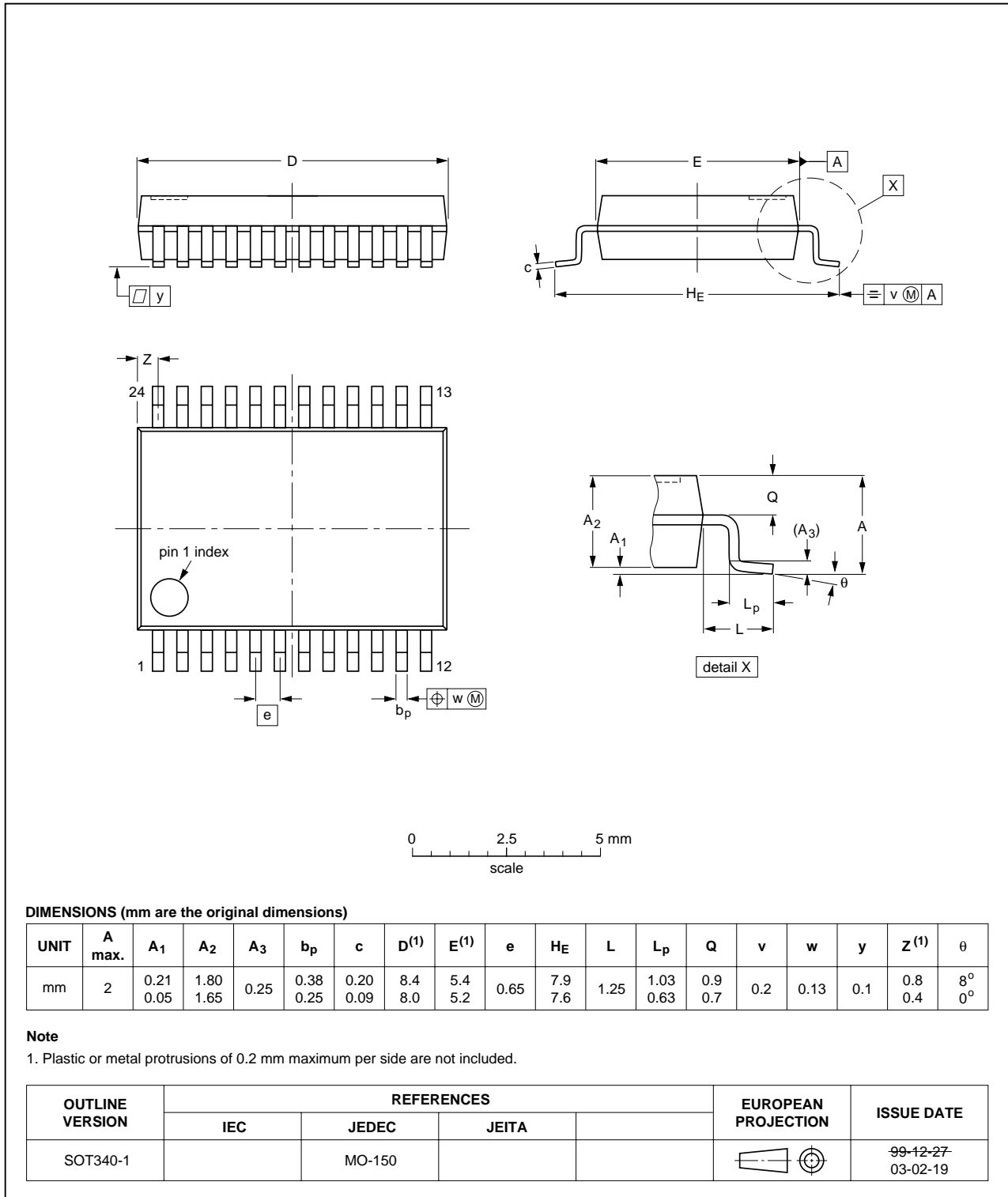


Fig 9. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

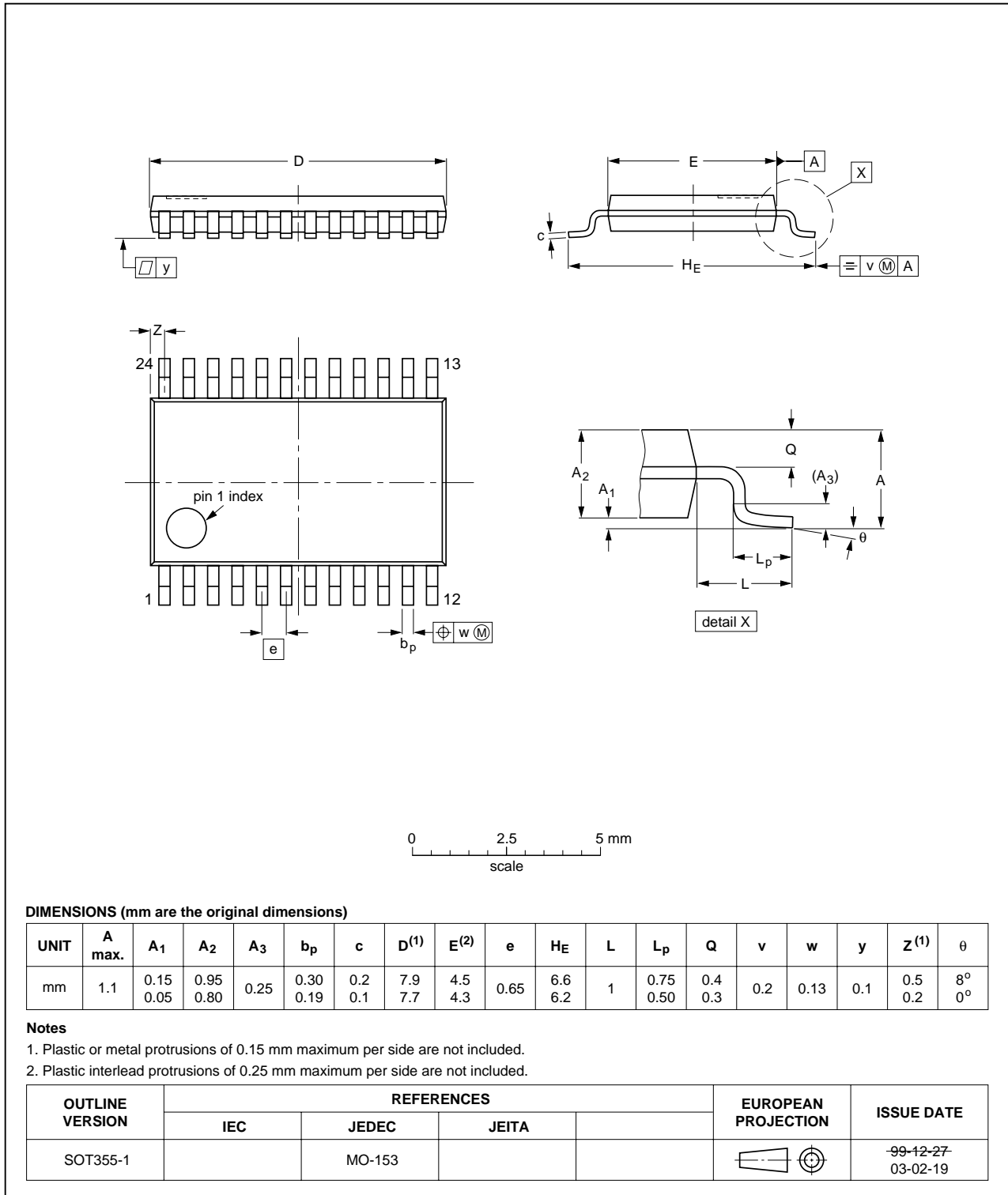


Fig 10. Package outline SOT355-1 (TSSOP24)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT827_3	20100224	Product data sheet	-	74ABT827_2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. DIP 24 (SOT222-1) package removed from Section 3 “Ordering information” and Section 12 “Package outline” 			
74ABT827_2	19980116	Product specification	-	74ABT827_1
74ABT827_1	19950906	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	3
6.1	Function table	3
7	Limiting values	4
8	Recommended operating conditions	4
9	Static characteristics	5
10	Dynamic characteristics	6
11	Waveforms	6
12	Package outline	8
13	Abbreviations	11
14	Revision history	11
15	Legal information	12
15.1	Data sheet status	12
15.2	Definitions	12
15.3	Disclaimers	12
15.4	Trademarks	13
16	Contact information	13
17	Contents	14

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