74F827

10-bit buffer/line driver; non-inverting; 3-state Rev. 04 — 29 January 2010

Product data sheet

General description 1.

The 74F827 10-bit buffer, provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The device has NOR output enables (OE0, OE1) for maximum control flexibility.

2. **Features**

- High impedance NPN base inputs for reduced loading (20 μA input current in HIGH and LOW states)
- I_{IL} = 20 μA compared to 600 μA in FAST family specification
- Ideal for high speed, light bus loading with increased fan-in
- Controlled rise and fall times to minimize ground bounce
- Glitch-free power-up in 3-state
- Flow-through pinout architecture for microprocessor oriented applications
- Output sink capability, I_{OL} = 64 mA

Ordering information 3.

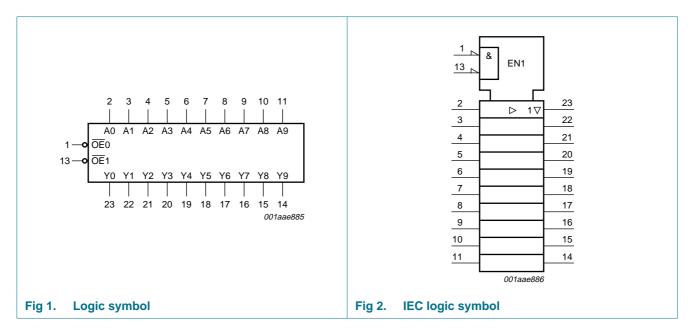
Table 1. **Ordering information**

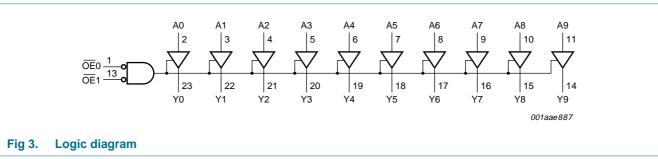
| Type number | Package | | | | | | | | |
|-------------|-------------------|--------|---|----------|--|--|--|--|--|
| | Temperature range | Name | Description | Version | | | | | |
| N74F827D | 0 °C to 70 °C | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 | | | | | |
| N74F827DB | 0 °C to 70 °C | SSOP24 | plastic shrink small outline package; 24 leads; body width 5.3 mm | SOT340-1 | | | | | |



10-bit buffer/line driver; non-inverting; 3-state

4. Functional diagram

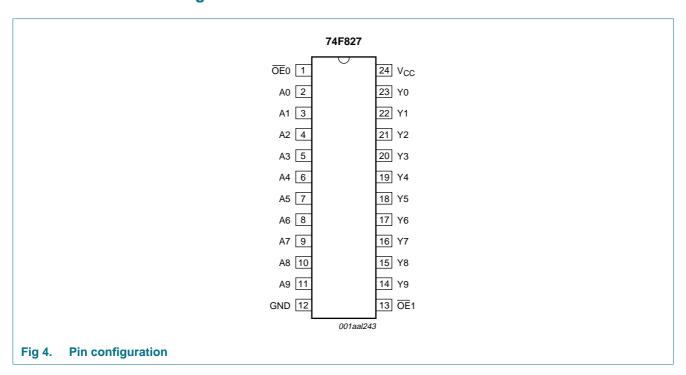




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5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description | Unit load HIGH/LOW | Load value[1] HIGH/LOW |
|----------|--|----------------------------------|-----------------------|---------------------------|
| ŌĒ0 | 1 | output enable input (active LOW) | 1.0/0.033 | 20 μΑ/20 μΑ |
| A0 to A9 | 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 | data input | 1.0/0.033 | 20 μΑ/20 μΑ |
| GND | 12 | ground (0 V) | - | - |
| ŌE1 | 13 | output enable input (active LOW) | 1.0/0.033 | 20 μΑ/20 μΑ |
| Y0 to Y9 | 23, 22, 21, 20, 19, 18, 17, 16, 15, 14 | data output | 1200/106.7 | 24 mA/64 mA |
| V_{CC} | 24 | supply voltage | - | - |

^[1] One FAST Unit Load (UL) is defined as 20 μA in HIGH state, 0.6 μA in LOW state.

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6. Functional description

6.1 Function table

Table 3. Function selection^[1]

| Input | | Output | Status |
|-----------------|----|--------|-------------|
| OE n | An | Yn | |
| L | L | L | transparent |
| L | Н | Н | |
| Н | X | Z | disabled |

^[1] H = HIGH voltage level;

L = LOW voltage level;

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|------------------------|----------------------|------------------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_{I} | input voltage | | [<u>1]</u> -0.5 | +7.0 | V |
| Vo | output voltage | output in HIGH-state | [<u>1]</u> -0.5 | +7.0 | V |
| I _{IK} | input clamping current | V _I < 0 V | -30 | +5 | mA |
| I _O | output current | output in LOW-state | - | 128 | mA |
| T _{amb} | ambient temperature | in free-air | [2] 0 | 70 | °C |
| T _{stg} | storage temperature | | -65 | +150 | °C |

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|-----------------|---------------------------|------------|-----|-----|-----|------|
| V_{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I _{IK} | input clamping current | | -18 | - | - | mA |
| I _{OH} | HIGH-level output current | | -24 | - | - | mA |
| I _{OL} | LOW-level output current | | - | - | 64 | mA |

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X = don't care;

Z = high-impedance OFF-state.

^[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

10-bit buffer/line driver; non-inverting; 3-state

9. Static characteristics

Table 6. Static characteristics

| Symbol | Parameter | Conditions | | | 25 °C | | 0 °C to | 70 °C | Unit |
|-----------------|--------------------------|--|-----|------|--------|-----|---------|-------|------|
| | | | | Min | Typ[1] | Max | Min | Max | |
| V _{IK} | input clamping voltage | $V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$ | · | -1.2 | -0.73 | - | -1.2 | - | ٧ |
| V _{OH} | HIGH-level output | $V_{CC} = 4.5 \text{ V}; V_{IL} = 0.8 \text{ V}; V_{IH} = 2.0 \text{ V}$ | | | | | | | |
| | voltage | $I_{OH} = -15 \text{ mA}$ | | | | | | | |
| | | V _{CC} = ±10 % | | - | - | - | 2.4 | - | V |
| | | V _{CC} = ±5 % | | - | 3.3 | - | 2.4 | - | V |
| | | $I_{OH} = -24 \text{ mA}$ | | | | | | | |
| | | V _{CC} = ±10 % | | - | - | - | 2.0 | - | V |
| | | V _{CC} = ±5 % | | - | - | - | 2.0 | - | V |
| V _{OL} | LOW-level output | $V_{CC} = 4.5 \text{ V}; V_{IL} = 0.8 \text{ V}; V_{IH} = 2.0 \text{ V}$ | | | | | | | |
| | voltage | I _{OL} = 64 mA | | | | | | | |
| | | V _{CC} = ±10 % | | - | - | - | - | 0.55 | V |
| | | V _{CC} = ±5 % | | - | 0.42 | - | - | 0.55 | V |
| l _l | input leakage current | $V_{CC} = 0 \text{ V}; V_{I} = 7.0 \text{ V}$ | | - | - | - | - | 100 | μΑ |
| l _{IH} | HIGH-level input current | $V_{CC} = 5.5 \text{ V}; V_I = 2.7 \text{ V}$ | | - | - | - | - | 20 | μΑ |
| I _{IL} | LOW-level input current | $V_{CC} = 5.5 \text{ V}; V_I = 0.5 \text{ V}$ | | - | - | - | - | -20 | μΑ |
| l _{oz} | OFF-state output current | V _{CC} = 5.5 V | | | | | | | |
| | | $V_0 = 2.7 \text{ V}$ | | - | - | - | - | 50 | μΑ |
| | | $V_0 = 0.5 \text{ V}$ | | - | - | - | - | -50 | μΑ |
| lo | output current | V _{CC} = 5.5 V | [2] | - | - | - | -100 | -225 | mΑ |
| Icc | supply current | V_{CC} = 5.5 V; V_I = GND or V_{CC} | | | | | | | |
| | | outputs HIGH-state | | - | 50 | - | - | 70 | mΑ |
| | | outputs LOW-state | | - | 70 | - | - | 100 | mΑ |
| | | outputs OFF-state | | - | 60 | - | - | 90 | mΑ |

^[1] All typical values are measured at $V_{CC} = 5 \text{ V}$.

10. Dynamic characteristics

Table 7. Dynamic characteristics *GND* = 0 *V; for test circuit, see Figure 7.*

| Symbol | Parameter | Conditions | 25 °C; | V _{CC} = | 5.0 V | 0 °C to V _{CC} = 5.0 | Unit | |
|-----------|-------------------|--|--------|-------------------|-------|----------------------------------|------|----|
| | | | Min | Тур | Max | Min | Max | |
| t_{PLH} | LOW to HIGH | An to Yn; see Figure 5 | | | | | | |
| | propagation delay | $C_L = 50 \text{ pF}$ | 2.0 | 5.5 | 8.5 | 2.0 | 9.0 | ns |
| | | $C_L = 300 \text{ pF}, 1 \text{ output switching}$ | - | 9.5 | 13.0 | - | 14.0 | ns |
| | | C _L = 300 pF, 10 outputs switching | - | 12.0 | 16.0 | - | 17.0 | ns |

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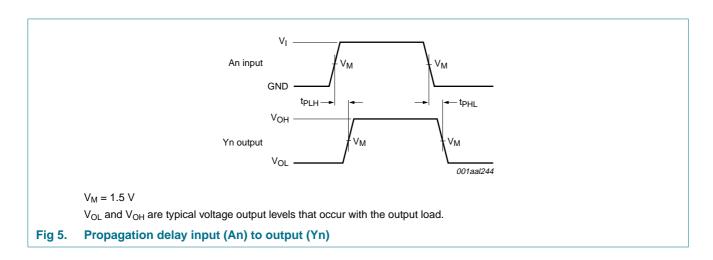
^[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

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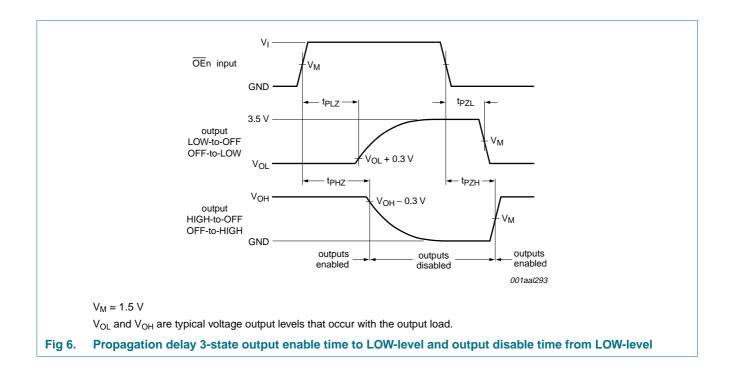
Table 7. Dynamic characteristics ...continued GND = 0 V; for test circuit, see Figure 7.

| Symbol | Parameter | Conditions | 25 °C | ; V _{CC} = | 5.0 V | | 70 °C; V ± 0.5 V | Unit |
|------------------|-------------------|--|-------|---------------------|-------|-----|---------------------|------|
| | | | Min | Тур | Max | Min | Max | |
| t _{PHL} | HIGH to LOW | An to Yn; see Figure 5 | | | | | | |
| | propagation delay | C _L = 50 pF | 2.0 | 4.5 | 8.5 | 2.0 | 9.0 | ns |
| | | C _L = 300 pF, 1 output switching | - | 7.5 | 10.0 | - | 11.0 | ns |
| | | $C_L = 300 \text{ pF}$, 10 outputs switching | - | 14.0 | 17.0 | - | 18.0 | ns |
| t_{PZH} | OFF-state to HIGH | OEn to Yn; see Figure 6 | | | | | | |
| | propagation delay | C _L = 50 pF | 5.0 | 8.0 | 12.0 | 4.5 | 14.0 | ns |
| | | C _L = 300 pF, 1 output switching | - | 15.0 | 20.0 | - | 21.0 | ns |
| | | $C_L = 300 \text{ pF}$, 10 outputs switching | - | 15.0 | 20.0 | - | 21.0 | ns |
| t _{PZL} | OFF-state to LOW | OEn to Yn; see Figure 6 | | | | | | |
| | propagation delay | C _L = 50 pF | 4.0 | 6.0 | 10.5 | 4.0 | 11.5 | ns |
| | | C _L = 300 pF, 1 output switching | - | 9.5 | 13.0 | - | 14.0 | ns |
| | | $C_L = 300 \text{ pF}$, 10 outputs switching | - | 17.0 | 21.0 | - | 21.5 | ns |
| t _{PHZ} | HIGH to OFF-state | OEn to Yn; see Figure 6 | | | | | | |
| | propagation delay | C _L = 50 pF | 2.5 | 5.0 | 8.0 | 2.0 | 8.5 | ns |
| | | C _L = 300 pF, 1 output switching | - | 15.0 | 19.0 | - | 20.0 | ns |
| | | $C_L = 300 \text{ pF}$, 10 outputs switching | - | 15.0 | 19.0 | - | 20.0 | ns |
| t _{PLZ} | LOW to OFF-state | OEn to Yn; see Figure 6 | | | | | | |
| | propagation delay | C _L = 50 pF | 2.5 | 5.0 | 8.0 | 2.0 | 8.5 | ns |
| | | C _L = 300 pF, 1 output switching | - | 9.5 | 13.5 | - | 14.0 | ns |
| | | $C_L = 300 \text{ pF}, 10 \text{ outputs switching}$ | - | 12.5 | 15.5 | - | 16.0 | ns |

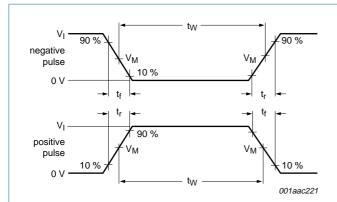
11. Waveforms

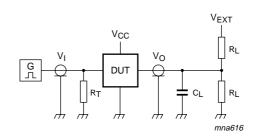


10-bit buffer/line driver; non-inverting; 3-state



10-bit buffer/line driver; non-inverting; 3-state





a. Input pulse definition

b. Test circuit

Test data and V_{EXT} levels are given in Table 8.

R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

 V_{EXT} = Test voltage for switching times.

Fig 7. Test circuit for measuring switching times

Table 8. Test data

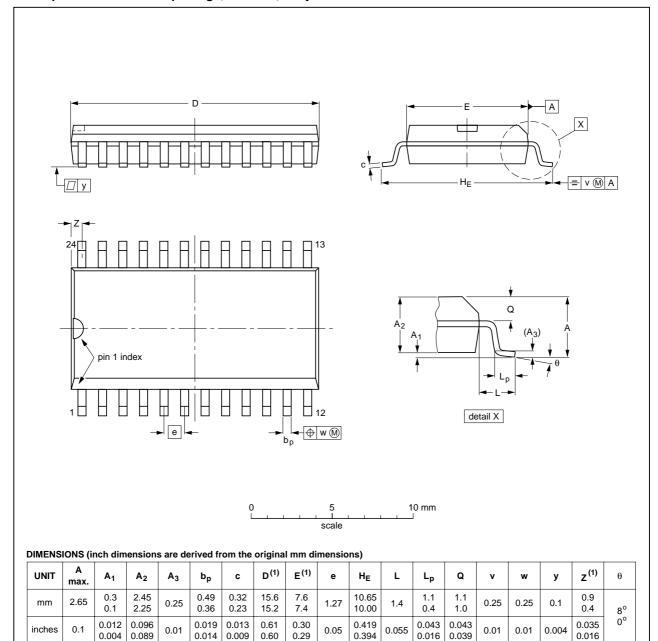
| Input | | | | Load | | V _{EXT} | | | |
|-------|--------------------------------|--------|----------------|----------------|-------------------------------------|------------------|-------------------------------------|-------|--|
| VI | f_{l} t_{W} t_{r}, t_{f} | | C _L | R _L | t _{PHL} , t _{PLH} | | t _{PZL} , t _{PLZ} | | |
| 3.0 V | 1 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | open | open | 7.0 V | |

10-bit buffer/line driver; non-inverting; 3-state

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE | | REFER | ENCES | | EUROPEAN | ISSUE DATE |
|----------|--------|--------|-------|--|------------|----------------------------------|
| VERSION | IEC | JEDEC | JEITA | | PROJECTION | ISSUE DATE |
| SOT137-1 | 075E05 | MS-013 | | | | -99-12-27 03-02-19 |

Fig 8. Package outline SOT137-1 (SO24)

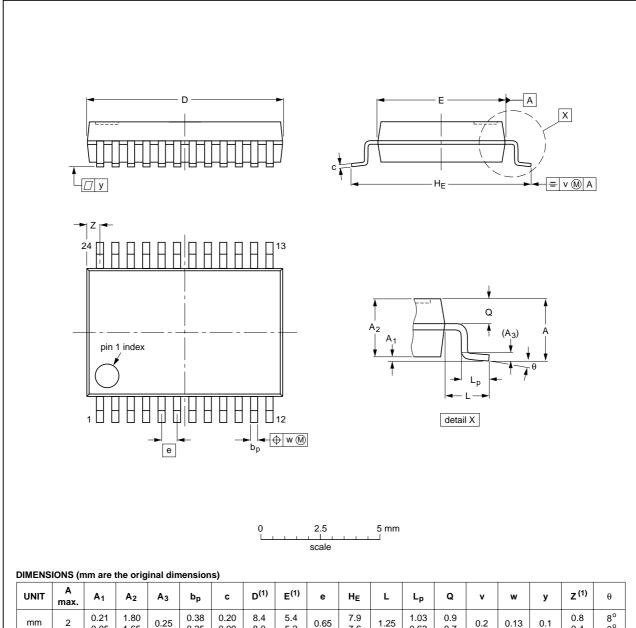
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74F827 **NXP Semiconductors**

10-bit buffer/line driver; non-inverting; 3-state

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



| UNIT | A max. | A ₁ | A ₂ | А3 | bp | С | D ⁽¹⁾ | E ⁽¹⁾ | е | HE | L | Lp | Q | v | w | у | Z ⁽¹⁾ | θ |
|------|-----------|-----------------------|----------------|------|--------------|--------------|------------------|------------------|------|------------|------|--------------|------------|-----|------|-----|------------------|----------|
| mm | 2 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 8.4 8.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 0.8 0.4 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

| OUTLINE | | EUROPEAN | ISSUE DATE | | |
|----------|-----|----------|------------|------------|---------------------------------|
| VERSION | IEC | JEDEC | JEITA | PROJECTION | ISSUE DATE |
| SOT340-1 | | MO-150 | | | 99-12-27 03-02-19 |

Fig 9. Package outline SOT340-1 (SSOP24)

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10-bit buffer/line driver; non-inverting; 3-state

13. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|-------------------------|
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| НВМ | Human Body Model |
| MM | Machine Model |

14. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes | | |
|-----------------|--|-----------------------|---------------|-----------------|--|--|
| 74F827_4 | 20100129 | Product data sheet | - | 74F827_3 | | |
| Modifications: | The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. | | | | | |
| | Legal texts have been adapted to the new company name where appropriate. | | | | | |
| | DIP 24 (SOT222-1) package removed from <u>Section 3 "Ordering information"</u> and <u>Section</u> 12 "Package outline" | | | | | |
| 74F827_3 | 20040121 | Product specification | - | 74F827_74F828_2 | | |
| 74F827_74F828_2 | 19941205 | Product specification | - | - | | |

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15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|--------------------------------|-------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

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10-bit buffer/line driver; non-inverting; 3-state

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