BLD6G22L-50; BLD6G22LS-50

W-CDMA 2110 MHz to 2170 MHz fully integrated Doherty transistor

Rev. 02 — 18 March 2010 Objective data sheet

1. Product profile

1.1 General description

The BLD6G22L-50 and BLD22LS-50 incorporate a fully integrated Doherty solution using NXP's state of the art GEN6 LDMOS technology. This device is perfectly suited for CDMA base station applications at frequencies from 2110 MHz to 2170 MHz. The main and peak device, input splitter and output combiner are integrated in a single package. This package consists of one gate and drain lead and two extra leads of which one is used for biasing the peak amplifier and the other is not connected. It only requires the proper input/output match and bias setting as with a normal class-AB transistor.

Table 1. Typical performance

RF performance at T_h = 25 °C.

Mode of operation	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)	$P_{L(3dB)}$ (W)
W-CDMA [1][2]	2110 to 2170	28	8	13.3	38	−30	52

[1] Test signal: 2-carrier W-CDMA; test model 1; 64 DPCH; PAR = 8.3 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

[2] I_{Dq} = 170 mA (main); $V_{GS(amp)peak}$ = 0 V.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- Typical W-CDMA performance at frequencies from 2110 MHz to 2170 MHz:
  - Average output power = 8 W
  - Power gain = 13.3 dB
  - Efficiency = 38 %
- Fully optimized integrated Doherty concept:
  - integrated asymmetrical power splitter at input
  - integrated power combiner
  - peak biasing down to 0 V
  - low junction temperature
  - high efficiency

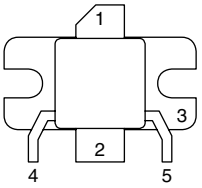
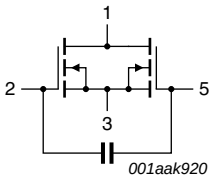
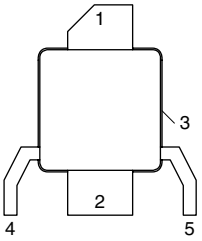
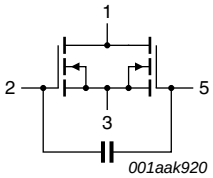
- Integrated ESD protection
- Good pair match (main and peak on the same chip)
- Independent control of main and peak bias
- Internally matched for ease of use
- Excellent ruggedness
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- High efficiency RF power amplifiers with digital pre-distortion for W-CDMA multi carrier applications in the 2110 MHz to 2170 MHz range.

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLD6G21L-50 (SOT1130A)				
1	drain			
2	gate + bias main			
3	source	[1]		
4	n.c.			
5	bias peak			
BLD6G21LS-50 (SOT1130B)				
1	drain			
2	gate + bias main			
3	source	[1]		
4	n.c.			
5	bias peak			

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLD6G22L-50	-	flanged ceramic package; 2 mounting holes; 4 leads	SOT1130A
BLD6G22LS-50	-	earless flanged ceramic package; 4 leads	SOT1130B

4. Block diagram

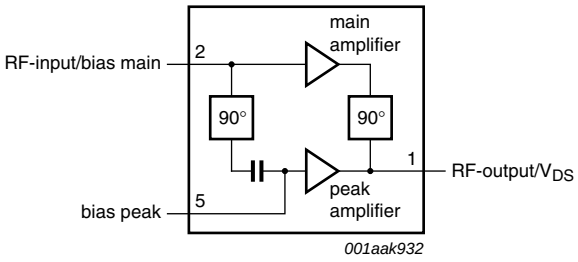


Fig 1. Block diagram of BLD6G22L-50 and BLD6G22LS-50

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Valid for both main and peak device.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–0.5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–0.5	+13	V
I_D	drain current		-	10.2	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 8 W	[1]	1.9	K/W

[1] When operated with a 2-carrier (W-CDMA) modulated signal with PAR = 8.3 dB at 0.01 % probability on the CCDF.

7. Characteristics

Table 6. Characteristics

Valid for both main and peak device.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.62 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 31 mA	1.4	1.8	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 170 mA	1.55	2.05	2.55	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	4.6	5.1	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 1.55 A	1.4	2.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.085 A	-	0.52	0.736	Ω

8. Application information

Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR 8.3 dB at 0.01 % probability on CCDF; carrier spacing = 5 MHz; f = 2140 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 170 mA; $V_{GS(amp)peak}$ = 0 V; T_{case} = 25 °C; unless otherwise specified; in a production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	8	-	W
G_p	power gain	$P_{L(AV)}$ = <tbd>	<tbd>	13.3	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = <tbd>	<tbd>	38	-	%
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = <tbd>	<tbd>	7.6	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = <tbd>	<tbd>	20	-	dB
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = <tbd>	-	–30	<tbd>	dBc

8.1 Ruggedness in Doherty operation

The BLD6G22L-50 and BLD6G22LS-50 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 170 mA; P_L = 8 W (W-CDMA); f = 2140 MHz.

8.2 Impedance information

Table 8. Typical impedance

Measured load-pull data; typical values unless otherwise specified.

f	Z_S	Z_L
MHz	Ω	Ω
2050	9.4 – 12.3j	5.5 – 7.6j
2110	11.4 – 11.2j	6.7 – 8.2j
2140	12.3 – 10.5j	7.0 – 7.5j
2170	12.2 – 9.3j	7.2 – 6.8j
2230	11.8 – 7.3j	5.4 – 5.5j

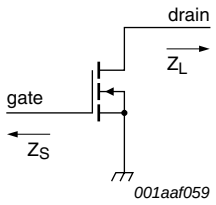
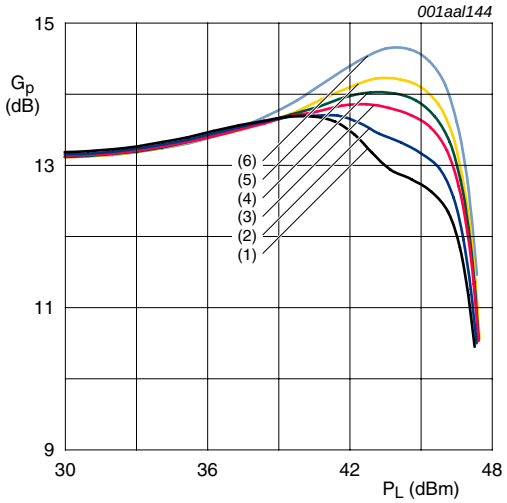


Fig 2. Definition of transistor impedance

8.3 Performance curves

Performance curves are measured in a BLD6G22L-50 application circuit.

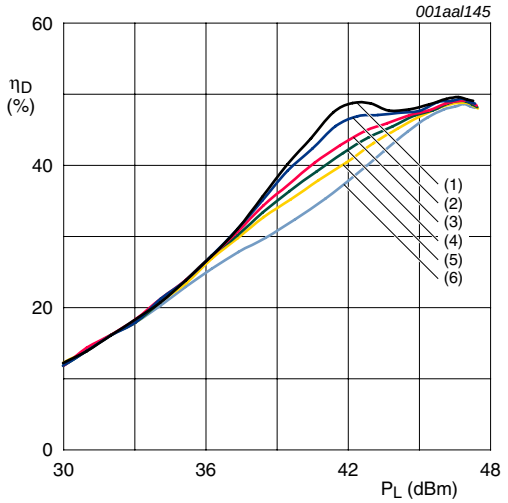
8.3.1 CW pulsed



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C;
f = 2140 MHz; δ = 10 %; t_p = 100 μs on 1 ms period.

(1) $V_{GS(amp)peak}$ = 0 V
(2) $V_{GS(amp)peak}$ = 0.2 V
(3) $V_{GS(amp)peak}$ = 0.4 V
(4) $V_{GS(amp)peak}$ = 0.5 V
(5) $V_{GS(amp)peak}$ = 0.6 V
(6) $V_{GS(amp)peak}$ = 0.8 V

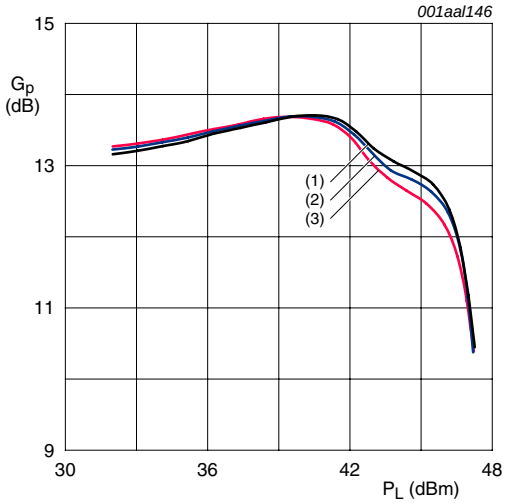
Fig 3. Power gain as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C;
f = 2140 MHz; δ = 10 %; t_p = 100 μs on 1 ms period.

(1) $V_{GS(amp)peak}$ = 0 V
(2) $V_{GS(amp)peak}$ = 0.2 V
(3) $V_{GS(amp)peak}$ = 0.4 V
(4) $V_{GS(amp)peak}$ = 0.5 V
(5) $V_{GS(amp)peak}$ = 0.6 V
(6) $V_{GS(amp)peak}$ = 0.8 V

Fig 4. Drain efficiency as a function of load power; typical values



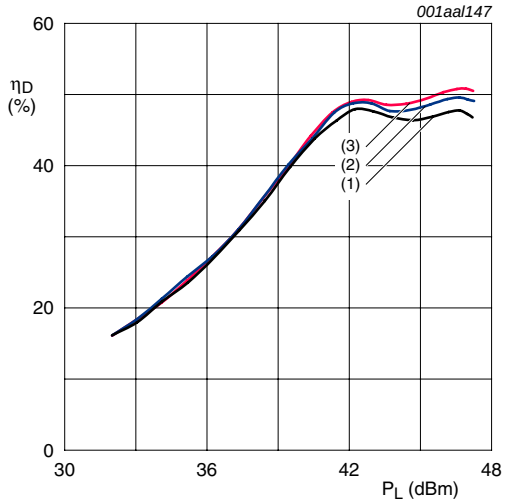
V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; δ = 10 %; t_p = 100 μs on 1 ms period.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 5. Power gain as a function of load power; typical values



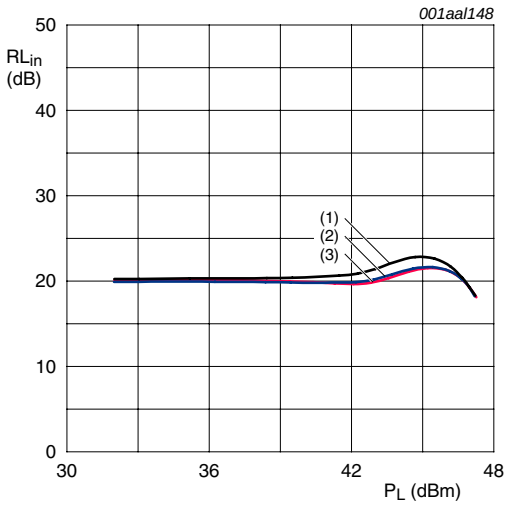
V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; δ = 10 %; t_p = 100 μs on 1 ms period.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 6. Drain efficiency as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; δ = 10 %; t_p = 100 μs on 1 ms period.

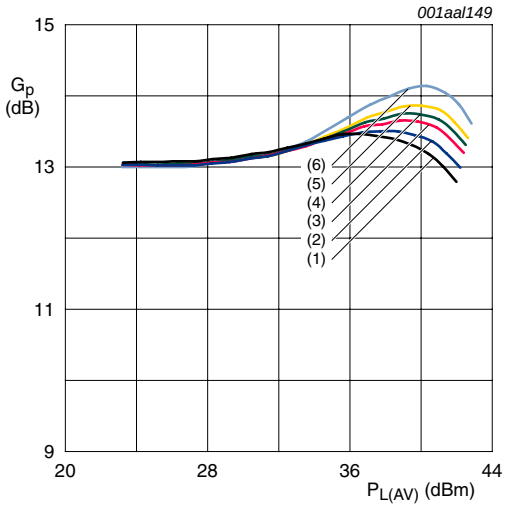
(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 7. Input return loss as a function of load power; typical values

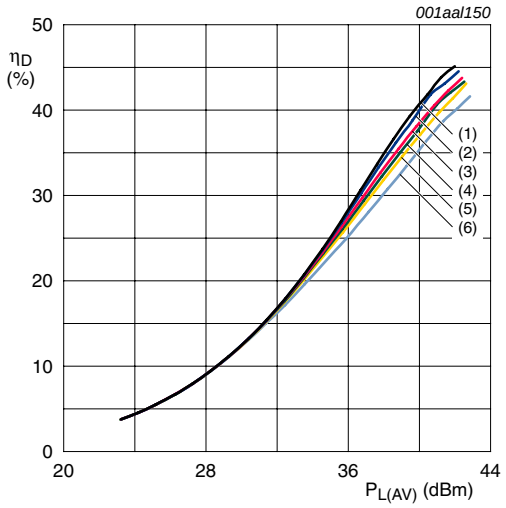
8.3.2 W-CDMA



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; f = 2140 MHz; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

(1) $V_{GS(amp)peak}$ = 0 V
(2) $V_{GS(amp)peak}$ = 0.2 V
(3) $V_{GS(amp)peak}$ = 0.4 V
(4) $V_{GS(amp)peak}$ = 0.5 V
(5) $V_{GS(amp)peak}$ = 0.6 V
(6) $V_{GS(amp)peak}$ = 0.8 V

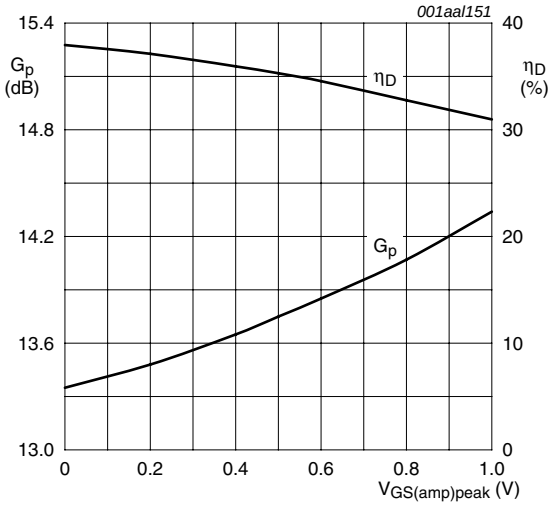
Fig 8. Power gain as a function of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; f = 2140 MHz; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

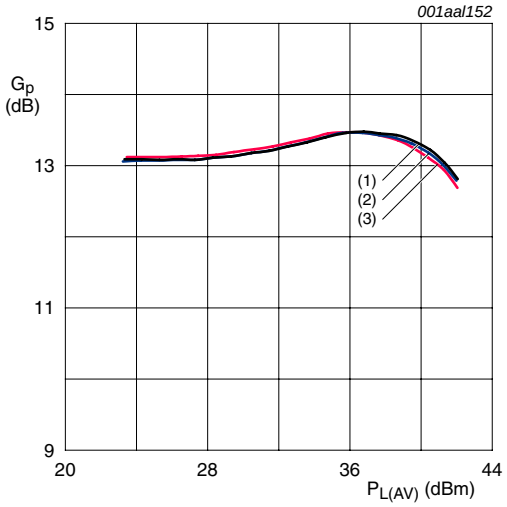
(1) $V_{GS(amp)peak}$ = 0 V
(2) $V_{GS(amp)peak}$ = 0.2 V
(3) $V_{GS(amp)peak}$ = 0.4 V
(4) $V_{GS(amp)peak}$ = 0.5 V
(5) $V_{GS(amp)peak}$ = 0.6 V
(6) $V_{GS(amp)peak}$ = 0.8 V

Fig 9. Drain efficiency as a function of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; f = 2140 MHz; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

Fig 10. Power gain and drain efficiency as function of load power; typical values



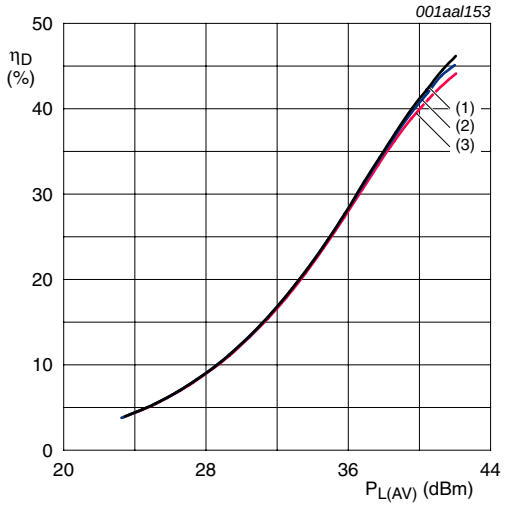
V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 11. Power gain as a function of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

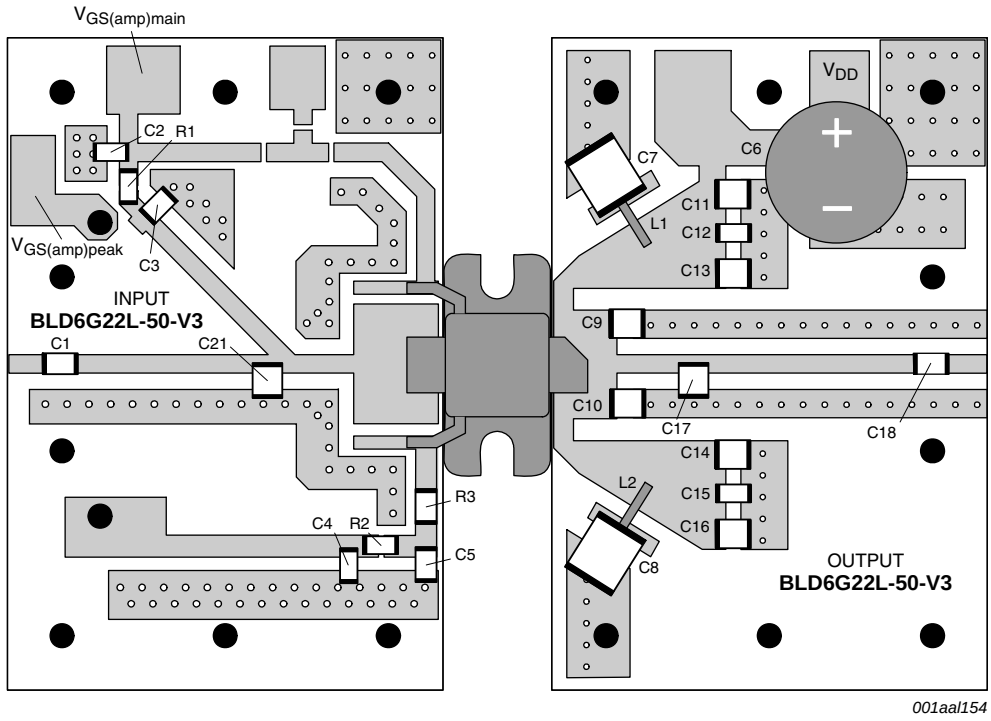
(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 12. Drain efficiency as a function of average load power; typical values

9. Test information



The striplines are on a double copper-clad gold plated Rogers 4350B Printed-Circuit Board (PCB) with ε_r = 3.5 and thickness = 0.76 mm.

See Table 9 for list of components.

Fig 13. Component layout

Table 9. List of components

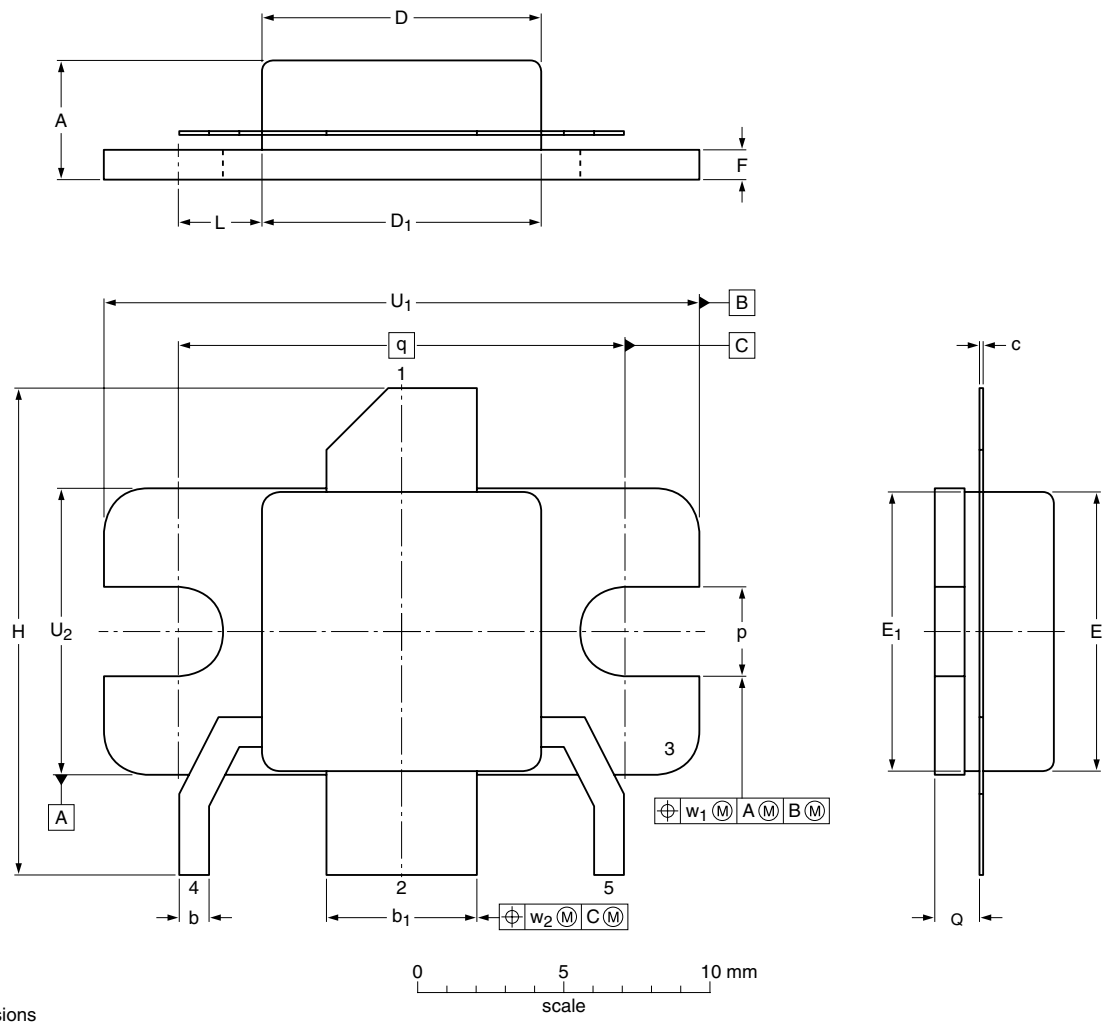
See Figure 13 for component layout.

Component	Description	Value		Dimensions
C1, C3, C5, C18	multilayer ceramic chip capacitor	9.1 pF	[1]	
C2, C4, C12, C15	multilayer ceramic chip capacitor	100 nF		
C6	electrolytic capacitor	470 μF; 63 V		
C7, C8	multilayer ceramic chip capacitor	10 μF		
C9, C10	multilayer ceramic chip capacitor	1.2 pF	[1]	
C11, C13, C14, C16	multilayer ceramic chip capacitor	8.2 pF	[1]	
C17	multilayer ceramic chip capacitor	0.8 pF	[1]	
C21	multilayer ceramic chip capacitor	1.0 pF	[1]	
L1, L2	copper wire	-		diameter = 0.8 mm; length = 8 mm
R1	SMD resistor	3.6 Ω		1206
R2	SMD resistor	33 Ω		1206
R3	SMD resistor	10 Ω		1206

[1] American Technical Ceramics type 100B or capacitor of same quality.

10. Package outline

Flanged ceramic package; 2 mounting holes; 4 leads **SOT1130A**



Dimensions

Unit[1]		A	b	b_1	c	D	D_1	E	E_1	F	H	L	p	Q[2]	q	U_1	U_2	w_1	w_2
mm	max	4.65	1.14	5.26	0.18	9.65	9.65	9.65	9.65	1.14	17.12	3.00	3.30	1.70		20.45	9.91		
	nom														15.24			0.25	0.51
	min	3.76	0.89	5.00	0.10	9.40	9.40	9.40	9.40	0.89	16.10	2.69	2.92	1.45		20.19	9.65		
inches	max	0.183	0.045	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.674	0.118	0.130	0.067		0.805	0.39		
	nom														0.6			0.01	0.02
	min	0.148	0.035	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.634	0.106	0.115	0.057		0.795	0.38		

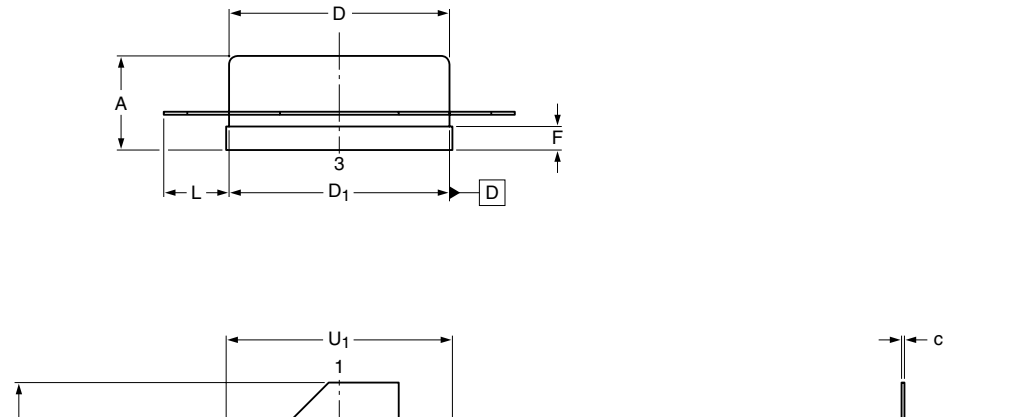
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1130a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1130A						~~09-10-12~~ 10-02-02

Fig 14. Package outline SOT1130A

Earless flanged ceramic package; 4 leads **SOT1130B**



Dimensions

Unit[1]		A	b	b_1	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2	Z	Z_1	α
mm	max	4.65	1.14	5.26	0.18	9.65	9.65	9.65	9.65	1.14	17.12	3.00	1.70	9.91	9.91		3.05	5.66	64°
	nom															0.51			
	min	3.76	0.89	5.00	0.10	9.40	9.40	9.40	9.40	0.89	16.10	2.69	1.45	9.65	9.65		2.79	5.41	62°
inches	max	0.183	0.045	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.674	0.118	0.069	0.39	0.39		0.120	0.223	64°
	nom															0.02			
	min	0.148	0.035	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.634	0.106	0.059	0.38	0.38		0.110	0.213	62°

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1130b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1130B						~~09-10-12~~ 09-12-14

Fig 15. Package outline SOT1130B

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLD6G22L-50_BLD6G22LS-50_2	20100318	Objective data sheet	-	BLD6G22L-50_ BLD6G22LS-50_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Figure 1 on page 3: some corrections were made • Table 5 on page 3: changed the typical value for $R_{th(j\text{-}case)}$ • Figure 13 on page 10: some corrections were made			
BLD6G22L-50_BLD6G22LS-50_1	20091215	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

13.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

14. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

15. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 18 March 2010
Document identifier: BLD6G22L-50_BLD6G22LS-50_2