Ultralow Distortion, Ultralow Noise Op Amp

AD797

FEATURES

Low noise
0.9 nV/√Hz typical (1.2 nV/√Hz maximum) input voltage noise at 1 kHz
50 nV p-p input voltage noise, 0.1 Hz to 10 Hz
Low distortion
−120 dB total harmonic distortion at 20 kHz
Excellent ac characteristics
800 ns settling time to 16 bits (10 V step)
110 MHz gain bandwidth (G = 1000)
8 MHz bandwidth (G = 10)
280 kHz full power bandwidth at 20 V p-p
20 V/µs slew rate
Excellent dc precision
80 µV maximum input offset voltage
1.0 µV/°C V_{OS} drift
Specified for ±5 V and ±15 V power supplies
High output drive current of 50 mA

APPLICATIONS

Professional audio preamplifiers
IR, CCD, and sonar imaging systems
Spectrum analyzers
Ultrasound preamplifiers
Seismic detectors
Σ-Δ ADC/DAC buffers

PIN CONFIGURATION

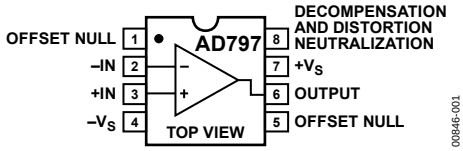


Figure 1. 8-Lead Plastic Dual In-Line Package [PDIP] and 8-Lead Standard Small Outline Package [SOIC]

GENERAL DESCRIPTION

The AD797 is a very low noise, low distortion operational amplifier ideal for use as a preamplifier. The low noise of 0.9 nV/√Hz and low total harmonic distortion of −120 dB at audio bandwidths give the AD797 the wide dynamic range necessary for preamps in microphones and mixing consoles.

Furthermore, the AD797's excellent slew rate of 20 V/µs and 110 MHz gain bandwidth make it highly suitable for low frequency ultrasound applications.

The AD797 is also useful in infrared (IR) and sonar imaging applications, where the widest dynamic range is necessary. The low distortion and 16-bit settling time of the AD797 make it ideal for buffering the inputs to Σ-Δ ADCs or the outputs of high resolution DACs, especially when the device is used in critical applications such as seismic detection or in spectrum analyzers. Key features such as a 50 mA output current drive and the specified power supply voltage range of ±5 V to ±15 V make the AD797 an excellent general-purpose amplifier.

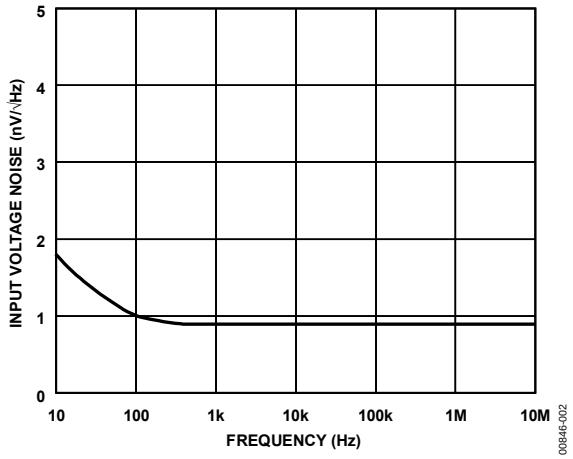


Figure 2. AD797 Voltage Noise Spectral Density

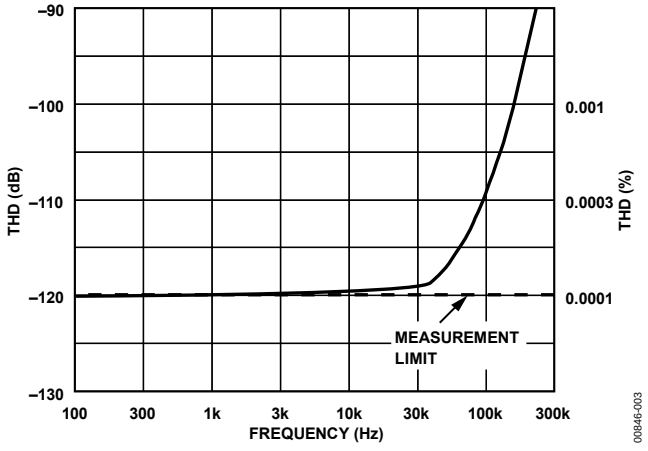


Figure 3. THD vs. Frequency

Rev. F

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

1/08—Rev. E to Rev. F

Changes to Absolute Maximum Ratings ... 5
Change to Equation 1 ... 12
Changes to the Noninverting Configuration Section ... 13
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 20

7/05—Rev. D to Rev. E

Updated Figure 1 Caption ... 1
Deleted Metallization Photo ... 6
Changes to Equation 1 ... 12
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 20

10/02—Rev. C to Rev. D

Deleted 8-Lead CERDIP Package (Q-8) ... Universal
Edits to Specifications ... 2
Edits to Absolute Maximum Ratings ... 3
Edits to Ordering Guide ... 3
Edits to Table I ... 9
Deleted Operational Amplifiers Graphic ... 15
Updated Outline Dimensions ... 15

SPECIFICATIONS

T_A = 25°C and V_S = ±15 V dc, unless otherwise noted.

Table 1.

Parameter	Conditions	Supply Voltage (V)	AD797A Min	AD797A Typ	AD797A Max	AD797B Min	AD797B Typ	AD797B Max	Unit
INPUT OFFSET VOLTAGE		±5 V, ±15 V		25	80		10	40	µV
	T_{MIN} to T_{MAX}			50	125/180		30	60	µV
Offset Voltage Drift		±5 V, ±15 V		0.2	1.0		0.2	0.6	µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		0.25	1.5		0.25	0.9	µA
	T_{MIN} to T_{MAX}			0.5	3.0		0.25	2.0	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		100	400		80	200	nA
	T_{MIN} to T_{MAX}			120	600/700		120	300	nA
OPEN-LOOP GAIN	V_{OUT} = ±10 V	±15 V	1	20		2	20		V/µV
	R_{LOAD} = 2 kΩ		1	6		2	10		V/µV
	T_{MIN} to T_{MAX}		1	15		2	15		V/µV
	R_{LOAD} = 600 Ω		1	5		2	7		V/µV
	T_{MIN} to T_{MAX} @ 20 kHz[1]		14,000	20,000		14,000	20,000		V/V
DYNAMIC PERFORMANCE									
Gain Bandwidth Product	G = 1000	±15 V		110		110			MHz
	G = 1000[2]	15 V		450		450			MHz
–3 dB Bandwidth	G = 10	±15 V		8		8			MHz
Full Power Bandwidth[1]	V_{OUT} = 20 V p-p, R_{LOAD} = 1 kΩ	±15 V		280			280		kHz
Slew Rate	R_{LOAD} = 1 kΩ	±15 V	12.5	20		12.5	20		V/µs
Settling Time to 0.0015%	10 V step	±15 V		800	1200		800	1200	ns
COMMON-MODE REJECTION	V_{CM} = CMVR	±5 V, ±15 V	114	130		120	130		dB
	T_{MIN} to T_{MAX}		110	120		114	120		dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±18 V		114	130		120	114		dB
	T_{MIN} to T_{MAX}		110	120		130	120		dB
INPUT VOLTAGE NOISE	f = 0.1 Hz to 10 Hz	±15 V		50			50		nV p-p
	f = 10 Hz	±15 V		1.7			1.7	2.5	nV/√Hz
	f = 1 kHz	±15 V		0.9	1.2		0.9	1.2	nV/√Hz
	f = 10 Hz to 1 MHz	±15 V		1.0	1.3		1.0	1.2	µV rms
INPUT CURRENT NOISE	f = 1 kHz	±15 V		2.0			2.0		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±15 V	±11	±12			±11	±12	V
		±5 V	±2.5	±3			±2.5	±3	V
OUTPUT VOLTAGE SWING	R_{LOAD} = 2 kΩ	±15 V	±12	±13		±12	±13		V
	R_{LOAD} = 600 Ω	±15 V	±11	±13		±11	±13		V
	R_{LOAD} = 600 Ω	±5 V	±2.5	±3		±2.5	±3		V
Short-Circuit Current		±5 V, ±15 V		80			80		mA
Output Current[3]		±5 V, ±15 V	30	50		30	50		mA
TOTAL HARMONIC DISTORTION	R_{LOAD} = 1 kΩ, C_N = 50 pF, f = 250 kHz, 3 V rms	±15 V		–98	–90		–98	–90	dB
	R_{LOAD} = 1 kΩ, f = 20 kHz, 3 V rms	±15 V		–120	–110		–120	–110	dB
INPUT CHARACTERISTICS									
Input Resistance									
Differential				7.5			7.5		kΩ
Common Mode				100			100		MΩ
Input Capacitance									
Differential[4]				20			20		pF
Common Mode				5			5		pF

Parameter	Conditions	Supply Voltage (V)	AD797A Min	AD797A Typ	AD797A Max	AD797B Min	AD797B Typ	AD797B Max	Unit
OUTPUT RESISTANCE	A_V = 1, f = 1 kHz			3				3	mΩ
POWER SUPPLY									
Operating Range			±5		±18	±5		±18	V
Quiescent Current		±5 V, ±15 V		8.2	10.5		8.2	10.5	mA

[1] Full power bandwidth = slew rate/2π V_{PEAK}.
[2] Specified using external decompensation capacitor.
[3] Output current for $|V_S - V_{OUT}| > 4$ V, $A_{OL} > 200$ kΩ.
[4] Differential input capacitance consists of 1.5 pF package capacitance and 18.5 pF from the input differential pair.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Ratings
Supply Voltage	±18 V
Internal Power Dissipation @ 25°C[1]	
PDIP	1.3 W – (T_A – 25°C)/θ_{JA}
SOIC	0.9 W (T_A – 25°C)/θ_{JA}
Input Voltage	±V_S
Differential Input Voltage[2]	±0.7 V
Output Short-Circuit Duration	Indefinite within maximum internal power dissipation
Storage Temperature Range (N, R Suffix)	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 60 sec)	300°C

[1] θ_{JA} = 95°C/W for the 8-lead PDIP; 155°C/W for the 8-lead SOIC.

[2] The AD797 inputs are protected by back-to-back diodes. To achieve low noise, internal current-limiting resistors are not incorporated into the design of this amplifier. If the differential input voltage exceeds ±0.7 V, the input current should be limited to less than 25 mA by series protection resistors. Note, however, that this degrades the low noise performance of the device.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

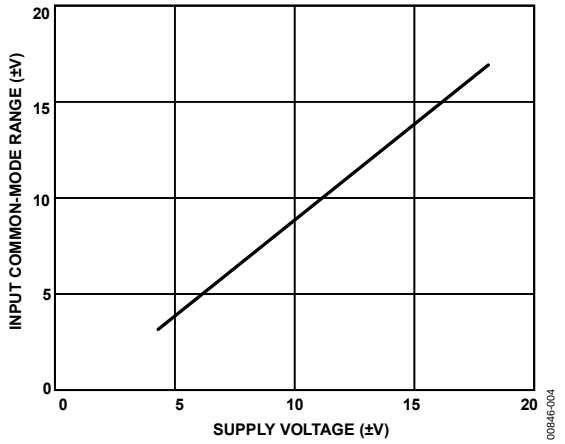


Figure 4. Input Common-Mode Voltage Range vs. Supply Voltage

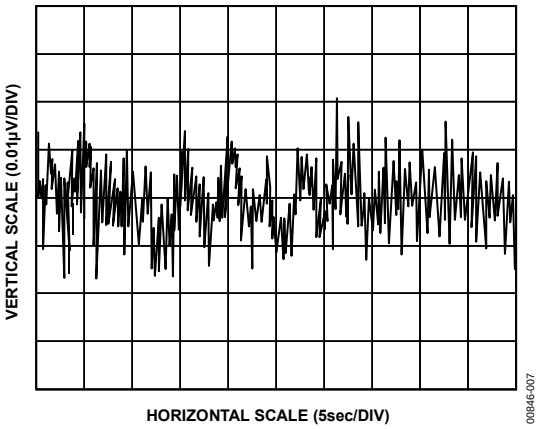


Figure 7. 0.1 Hz to 10 Hz Noise

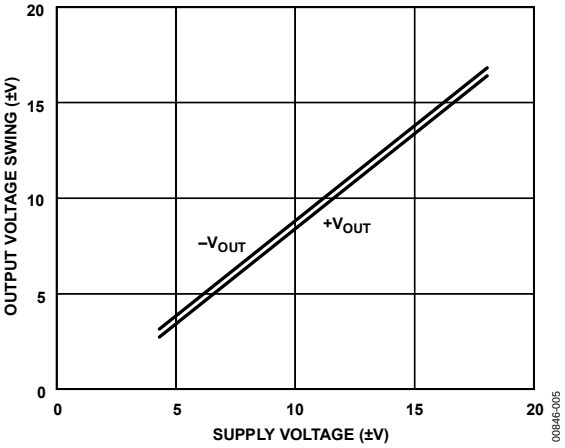


Figure 5. Output Voltage Swing vs. Supply Voltage

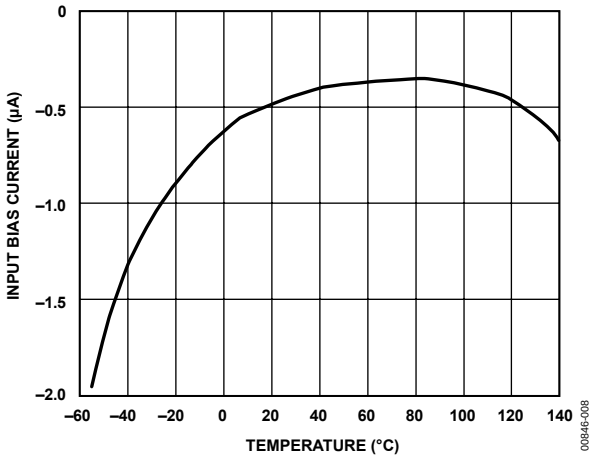


Figure 8. Input Bias Current vs. Temperature

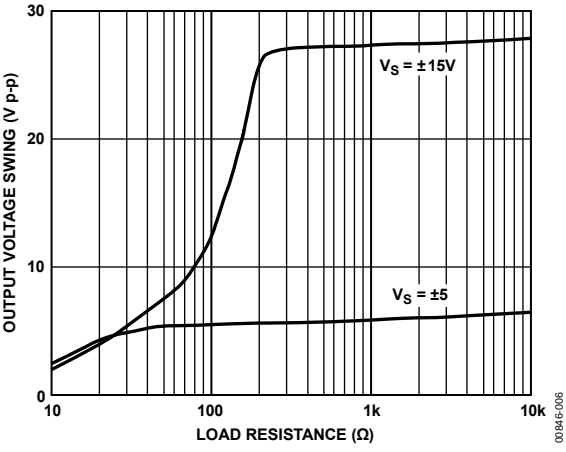


Figure 6. Output Voltage Swing vs. Load Resistance

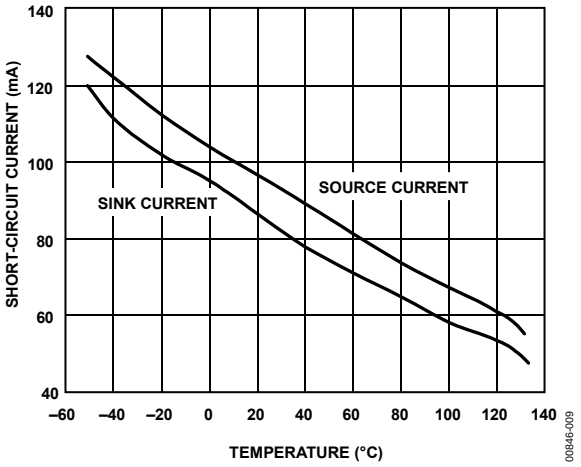


Figure 9. Short-Circuit Current vs. Temperature

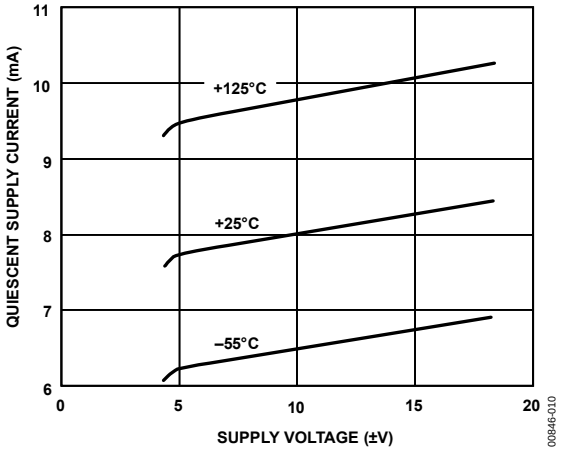


Figure 10. Quiescent Supply Current vs. Supply Voltage

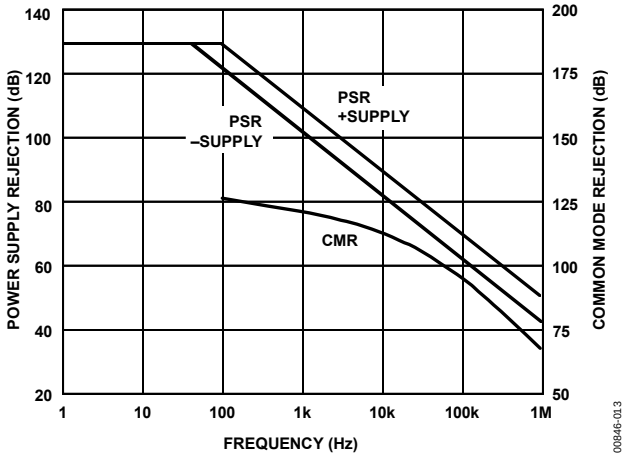


Figure 13. Power Supply and Common-Mode Rejection vs. Frequency

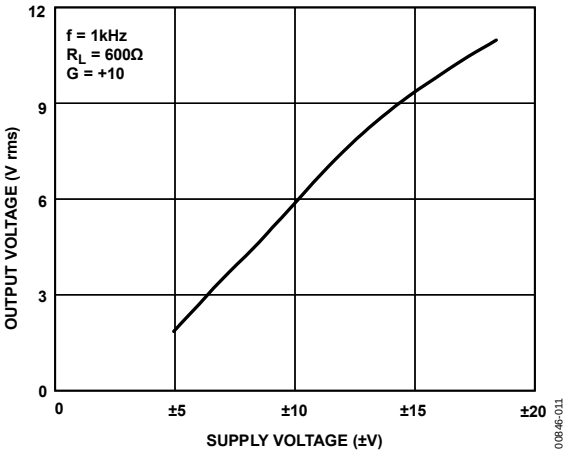


Figure 11. Output Voltage vs. Supply Voltage for 0.01% Distortion

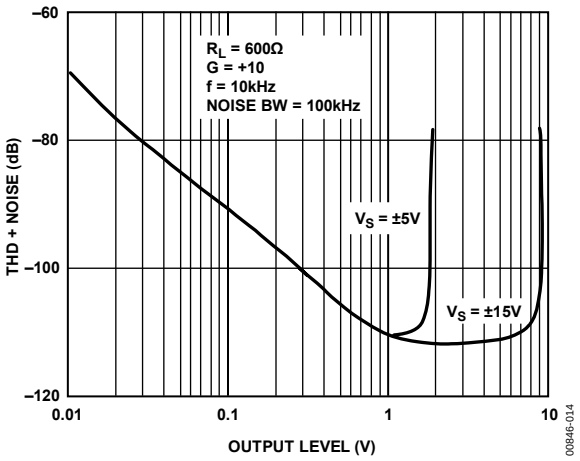


Figure 14. Total Harmonic Distortion (THD) + Noise vs. Output Level

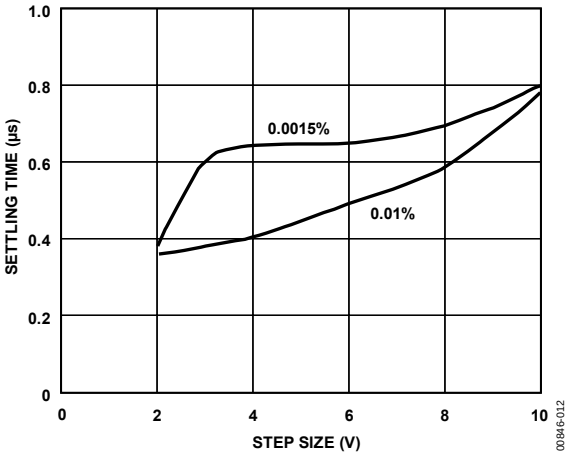


Figure 12. Settling Time vs. Step Size (±)

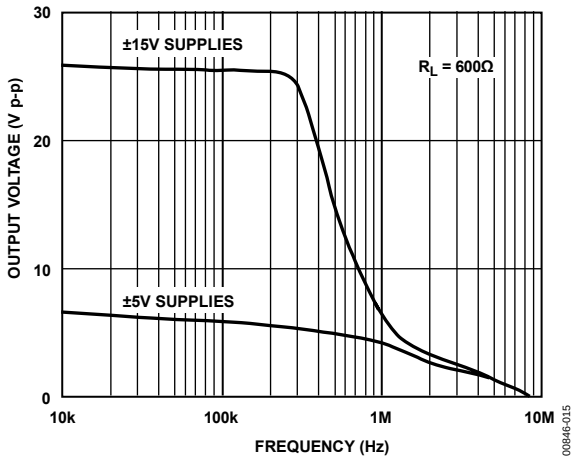


Figure 15. Large-Signal Frequency Response

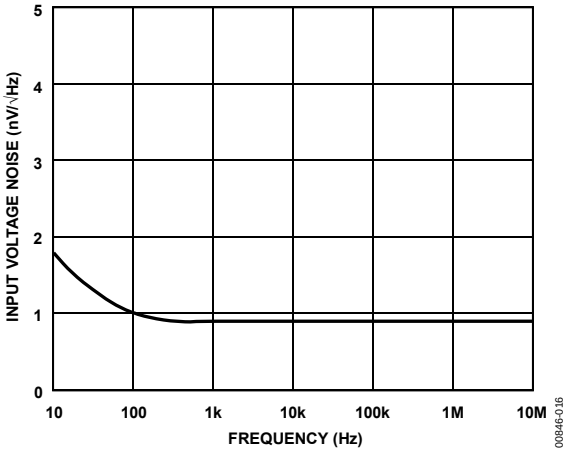


Figure 16. Input Voltage Noise Spectral Density

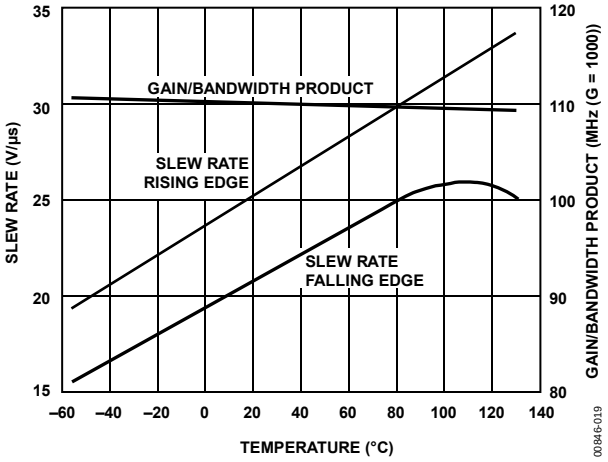


Figure 19. Slew Rate and Gain/Bandwidth Product vs. Temperature

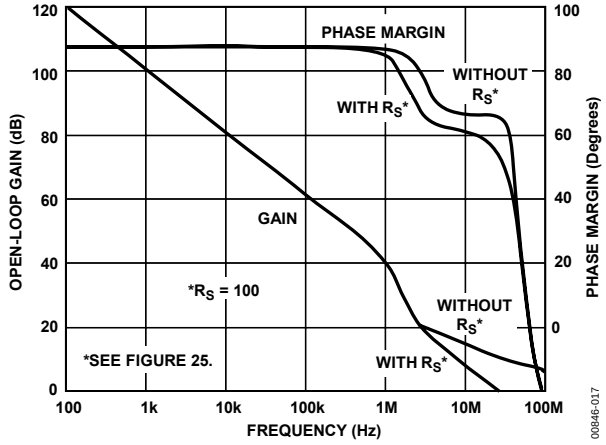


Figure 17. Open-Loop Gain and Phase Margin vs. Frequency

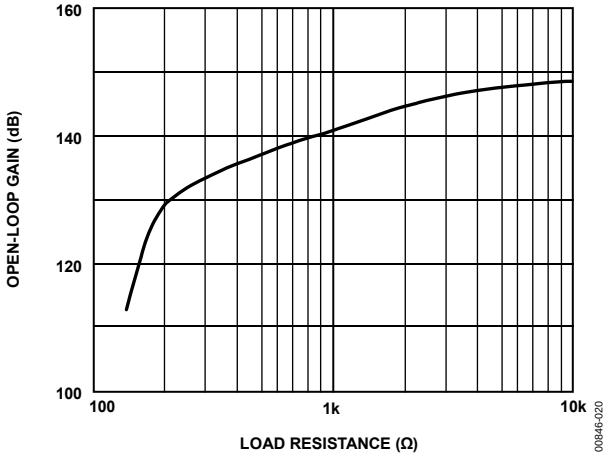


Figure 20. Open-Loop Gain vs. Load Resistance

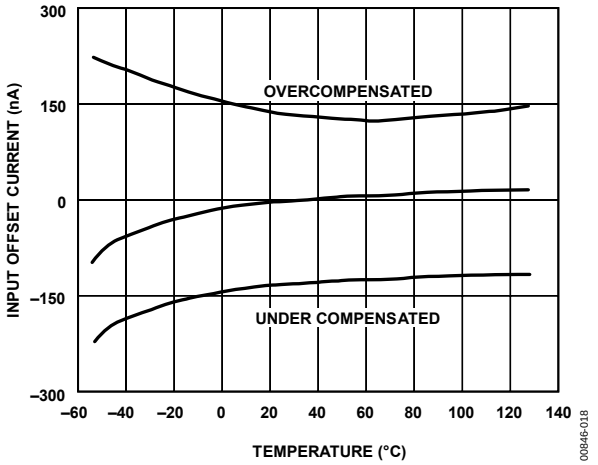


Figure 18. Input Offset Current vs. Temperature

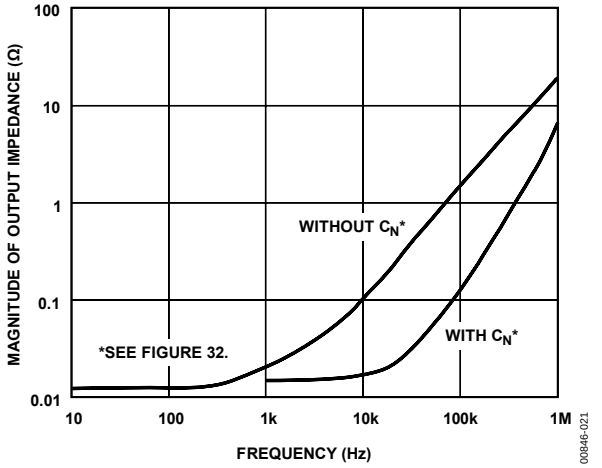


Figure 21. Magnitude of Output Impedance vs. Frequency

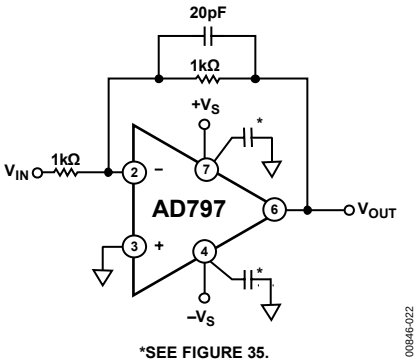


Figure 22. Inverter Connection

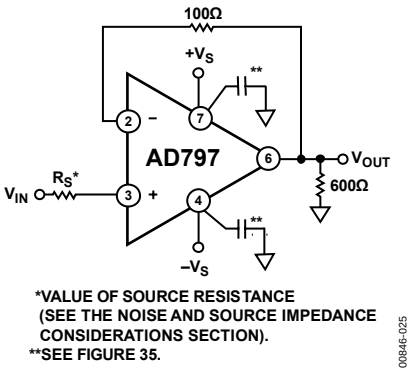


Figure 25. Follower Connection

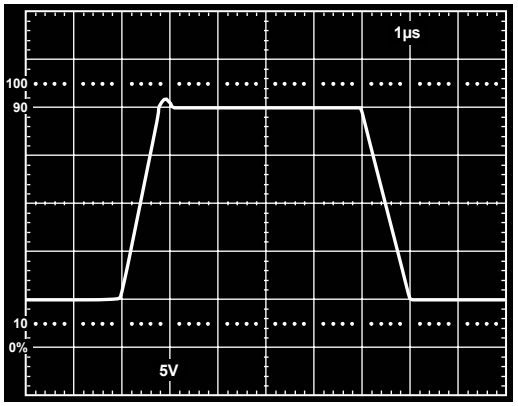


Figure 23. Inverter Large-Signal Pulse Response

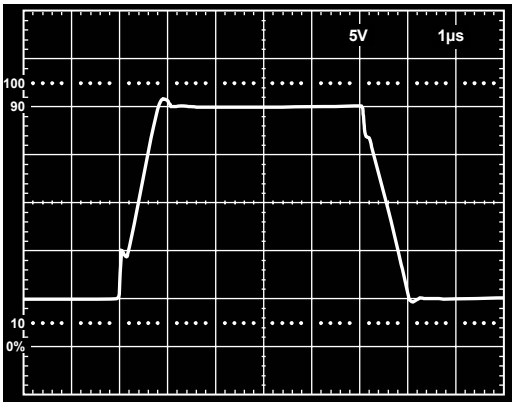


Figure 26. Follower Large-Signal Pulse Response

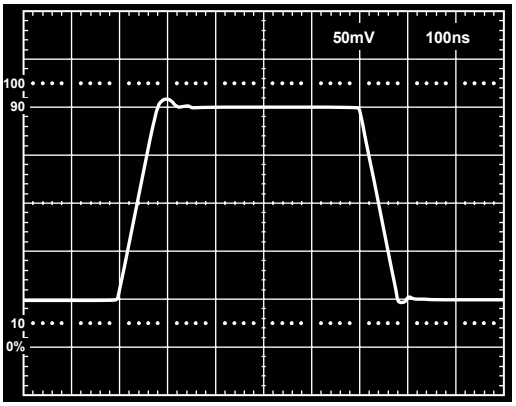


Figure 24. Inverter Small-Signal Pulse Response

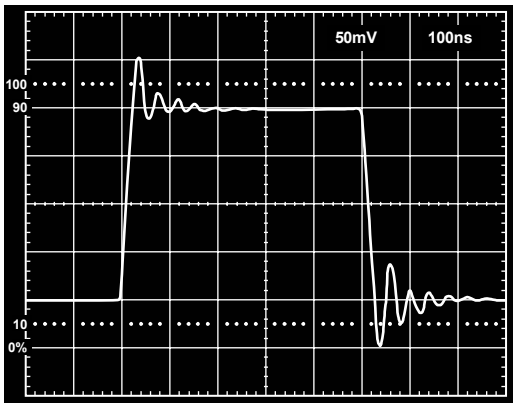


Figure 27. Follower Small-Signal Pulse Response

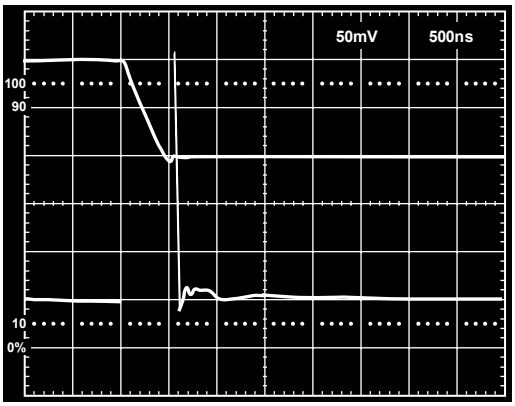


Figure 28. 16-Bit Settling Time Positive Input Pulse

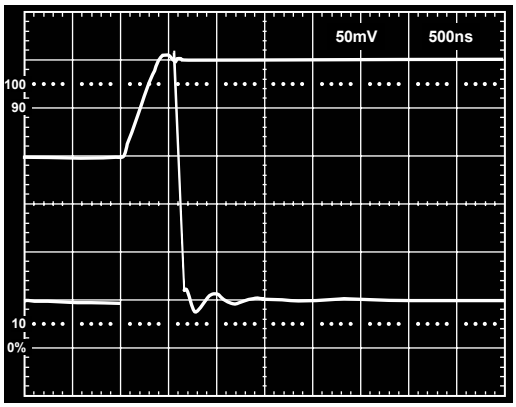


Figure 29. 16-Bit Settling Time Negative Input Pulse

THEORY OF OPERATION

The architecture of the AD797 was developed to overcome inherent limitations in previous amplifier designs. Previous precision amplifiers used three stages to ensure high open-loop gain (see Figure 30) at the expense of additional frequency compensation components. Slew rate and settling performance are usually compromised, and dynamic performance is not adequate beyond audio frequencies. As can be seen in Figure 30, the first stage gain is rolled off at high frequencies by the compensation network. Second stage noise and distortion then appears at the input and degrade performance. The AD797, on the other hand, uses a single ultrahigh gain stage to achieve dc as well as dynamic precision. As shown in the simplified schematic (Figure 31), Node A, Node B, and Node C track the input voltage, forcing the operating points of all pairs of devices in the signal path to match. By exploiting the inherent matching of devices fabricated on the same IC chip, high open-loop gain, CMRR, PSRR, and low V_{OS} are guaranteed by pairwise device matching (that is, NPN to NPN and PNP to PNP), not by an absolute parameter such as beta and the early voltage.

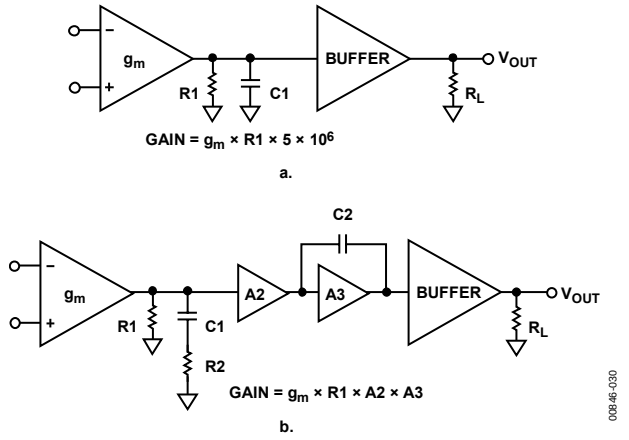


Figure 30. Model of AD797 vs. That of a Typical Three-Stage Amplifier

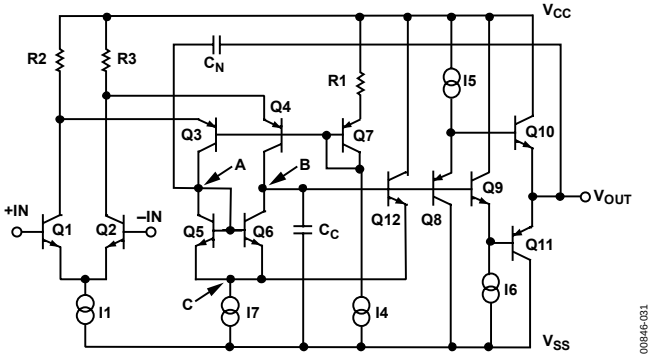


Figure 31. AD797 Simplified Schematic

This matching benefits not just dc precision, but, because it holds up dynamically, both distortion and settling time are also reduced. This single stage has a voltage gain of >5 × 10^6 and V_{OS} < 80 μV, while at the same time providing a THD + noise of less than −120 dB and true 16-bit settling in less than 800 ns. The elimination of second-stage noise effects has the additional benefit of making the low noise of the AD797 (<0.9 nV/√Hz) extend to beyond 1 MHz. This means new levels of performance for sampled data and imaging systems. All of this performance as well as load drive in excess of 30 mA are made possible by the Analog Devices, Inc., advanced complementary bipolar (CB) process.

Another unique feature of this circuit is that the addition of a single capacitor, C_N (see Figure 31), enables cancellation of distortion due to the output stage. This can best be explained by referring to a simplified representation of the AD797 using idealized blocks for the different circuit elements (Figure 32).

A single equation yields the open-loop transfer function of this amplifier; solving it at Node B yields

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_m}{\frac{C_N}{A}\,j\omega - C_N\,j\omega - \frac{C_C}{A}\,j\omega}$$

where:
g_m is the transconductance of Q1 and Q2.
A is the gain of the output stage (~1).
V_{OUT} is voltage at the output.
V_{IN} is differential input voltage.

When C_N is equal to C_C, the ideal single-pole op amp response is attained:

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_m}{j\omega C}$$

In Figure 32, the terms of Node A, which include the properties of the output stage, such as output impedance and distortion, cancel by simple subtraction. Therefore, the distortion cancellation does not affect the stability or frequency response of the amplifier. With only 500 μA of output stage bias, the AD797 delivers a 1 kHz sine wave into 60 Ω at 7 V rms with only 1 ppm of distortion.

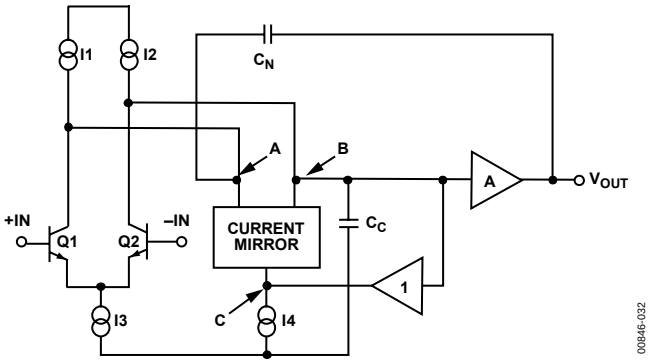


Figure 32. AD797 Block Diagram

NOISE AND SOURCE IMPEDANCE CONSIDERATIONS

The AD797 ultralow voltage noise of 0.9 nV/√Hz is achieved with special input transistors running at nearly 1 mA of collector current. Therefore, it is important to consider the total input-referred noise ($e_N$total), which includes contributions

from voltage noise (e_N), current noise (i_N), and resistor noise ($\sqrt{4}$ kTR$_S$).

$$e_N total = [e_N{}^2 + 4\,kTR_S + (i_N \times R_S)^2]^{1/2} \quad (1)$$

where R_S is the total input source resistance.

This equation is plotted for the AD797 in Figure 33. Because optimum dc performance is obtained with matched source resistances, this case is considered even though it is clear from Equation 1 that eliminating the balancing source resistance lowers the total noise by reducing the total R_S by a factor of 2.

At very low source resistance (R_S < 50 Ω), the voltage noise of the amplifier dominates. As source resistance increases, the Johnson noise of R_S dominates until a higher resistance of R_S > 2 kΩ is achieved; the current noise component is larger than the resistor noise.

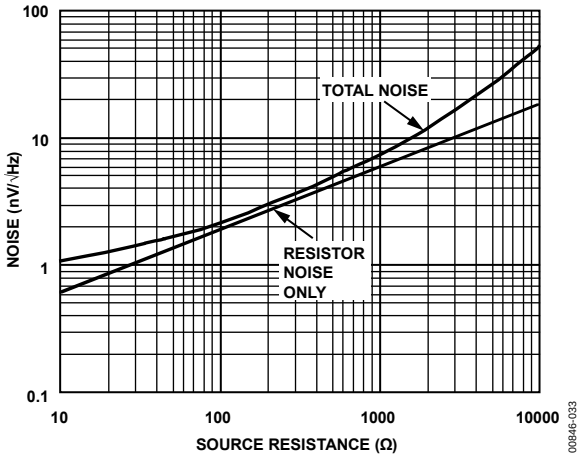


Figure 33. Noise vs. Source Resistance

The AD797 is the optimum choice for low noise performance if the source resistance is kept <1 kΩ. At higher values of source resistance, optimum performance with respect to only noise is obtained with other amplifiers from Analog Devices (Table 3).

Table 3. Recommended Amplifiers for Different Source Impedances

R_S (kΩ)	Recommended Amplifier
0 to <1	AD797
1 to <10	AD743/AD745, OP27/OP37, OP07
10 to <100	AD743/AD745, OP07
>100	AD548, AD549, AD711, AD743/AD745

LOW FREQUENCY NOISE

Analog Devices specifies low frequency noise as a peak-to-peak quantity in a 0.1 Hz to 10 Hz bandwidth. Several techniques can be used to make this measurement. The usual technique involves amplifying, filtering, and measuring the amplifier noise for a predetermined test time. The noise bandwidth of the filter is corrected for, and the test time is carefully controlled because the measurement time acts as an additional low frequency roll-off.

The plot in Figure 7 uses a slightly different technique: an FFT-based instrument (Figure 34) is used to generate a 10 Hz "brickwall" filter. A low frequency pole at 0.1 Hz is generated with an external ac coupling capacitor, which is also the instrument being dc coupled.

Several precautions are necessary to attain optimum low frequency noise performance:

- Care must be used to account for the effects of R_S. Even a 10 Ω resistor has 0.4 nV/√Hz of noise (an error of 9% when root sum squared with 0.9 nV/√Hz).
- The test setup must be fully warmed up to prevent e_{OS} drift from erroneously contributing to input noise.
- Circuitry must be shielded from air currents. Heat flow out of the package through its leads creates the opportunity for a thermoelectric potential at every junction of different metals. Selective heating and cooling of these by random air currents appears as 1/f noise and obscures the true device noise.
- The results must be interpreted using valid statistical techniques.

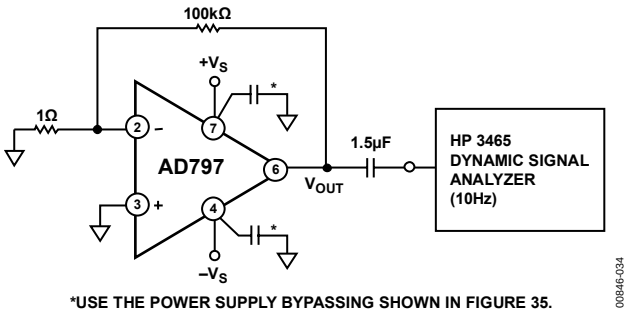


Figure 34. Test Setup for Measuring 0.1 Hz to 10 Hz Noise

WIDEBAND NOISE

Due to its single-stage design, the noise of the AD797 is flat over frequencies from less than 10 Hz to beyond 1 MHz. This is not true of most dc precision amplifiers, where second-stage noise contributes to input-referred noise beyond the audio frequency range. The AD797 offers new levels of performance in wideband imaging applications. In sampled data systems, where aliasing of out-of-band noise into the signal band is a problem, the AD797 outperforms all previously available IC op amps.

BYPASSING CONSIDERATIONS

Taking full advantage of the very wide bandwidth and dynamic range capabilities of the AD797 requires some precautions. First, multiple bypassing is recommended in any precision application. A 1.0 µF to 4.7 µF tantalum in parallel with 0.1 µF ceramic bypass capacitors are sufficient in most applications. When driving heavy loads, a larger demand is placed on the supply bypassing. In this case, selective use of larger values of tantalum capacitors and damping of their lead inductance with small-value (1.1 Ω to 4.7 Ω) carbon resistors can achieve an improvement. Figure 35 summarizes power supply bypassing recommendations.

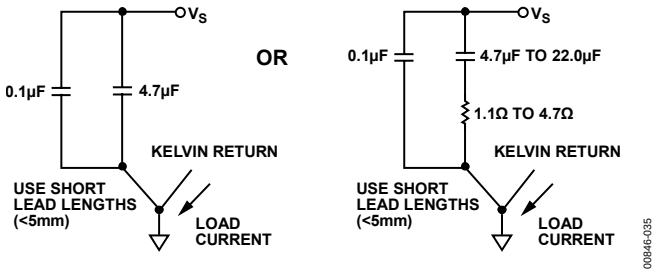


Figure 35. Recommended Power Supply Bypassing

THE NONINVERTING CONFIGURATION

Ultralow noise requires very low values of the internal parasitic resistance (r_{BB}) for the input transistors (≈6 Ω). This implies very little damping of input and output reactive interactions. With the AD797, additional input series damping is required for stability with direct output to input feedback. A 100 Ω resistor (R1) in the inverting input (Figure 36) is sufficient; the 100 Ω balancing resistor (R2) is recommended but is not required for stability. The noise penalty is minimal ($e_N$total ≈ 2.1 nV/√Hz), which is usually insignificant.

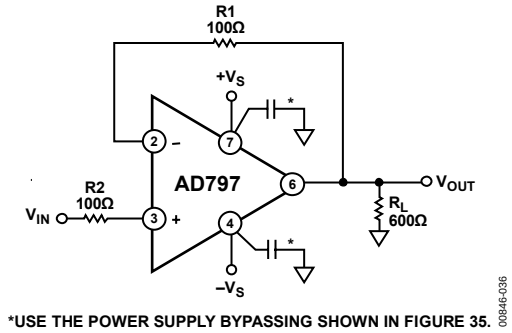


Figure 36. Voltage Follower Connection

Best response flatness is obtained with the addition of a small capacitor (C_L < 33 pF) in parallel with the 100 Ω resistor (Figure 37). The input source resistance and capacitance also affect the response slightly, and experimentation may be necessary for best results.

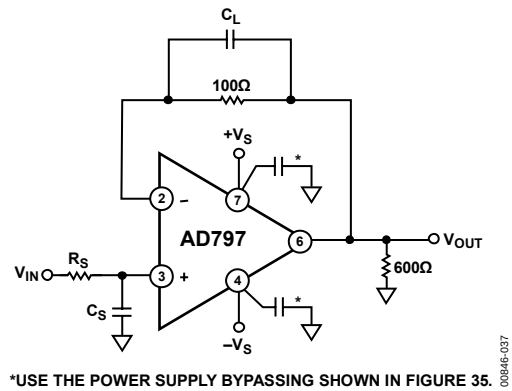


Figure 37. Alternative Voltage Follower Connection

Low noise preamplification is usually performed in the noninverting mode (Figure 38). For lowest noise, the equivalent resistance of the feedback network should be as low as possible. The 30 mA minimum drive current of the AD797 makes it easier to achieve this. The feedback resistors can be made as low as possible, with consideration to load drive and power consumption.

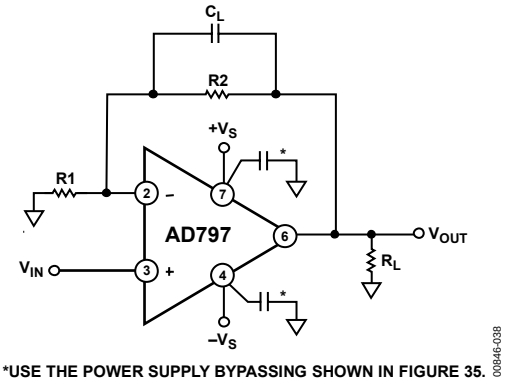


Figure 38. Low Noise Preamplifier

Table 4 provides some representative values for the AD797 when used as a low noise follower. Operation on 5 V supplies allows the use of a 100 Ω or less feedback network (R1 + R2). Because the AD797 shows no unusual behavior when operating near its maximum rated current, it is suitable for driving the AD600/AD602 (see Figure 50) while preserving low noise performance.

Optimum flatness and stability at noise gains >1 sometimes require a small capacitor (C_L) connected across the feedback resistor (R1 of Figure 38). Table 4 includes recommended values of C_L for several gains. In general, when R2 is greater than 100 Ω and C_L is greater than 33 pF, a 100 Ω resistor should be placed in series with C_L. Source resistance matching is assumed, and the AD797 should not be operated with unbalanced source resistance >200 kΩ/G.

Table 4. Values for Follower with Gain Circuit

Gain	R1	R2	C_L	Noise (Excluding R_S)
2	1 kΩ	1 kΩ	≈20 pF	3.0 nV/√Hz
2	300 Ω	300 Ω	≈10 pF	1.8 nV/√Hz
10	33.2 Ω	300 Ω	≈5 pF	1.2 nV/√Hz
20	16.5 Ω	316 Ω		1.0 nV/√Hz
>35	10 Ω	(G – 1) × 10 Ω		0.98 nV/√Hz

The I-to-V converter is a special case of the follower configuration. When the AD797 is used in an I-to-V converter, for example as a DAC buffer, the circuit shown in Figure 39 should be used. The value of C_L depends on the DAC, and if C_L is greater than 33 pF, a 100 Ω series resistor is required. A bypassed balancing resistor (R_S and C_S) can be included to minimize dc errors.

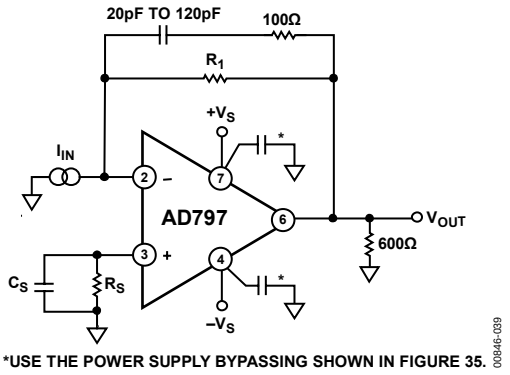


Figure 39. I-to-V Converter Connection

THE INVERTING CONFIGURATION

The inverting configuration (see Figure 40) presents a low input impedance, R1, to the source. For this reason, the goals of both low noise and input buffering are at odds with one another. Nonetheless, the excellent dynamics of the AD797 makes it the preferred choice in many inverting applications, and with careful selection of feedback resistors, the noise penalties are minimal. Some examples are presented in Table 5 and Figure 40.

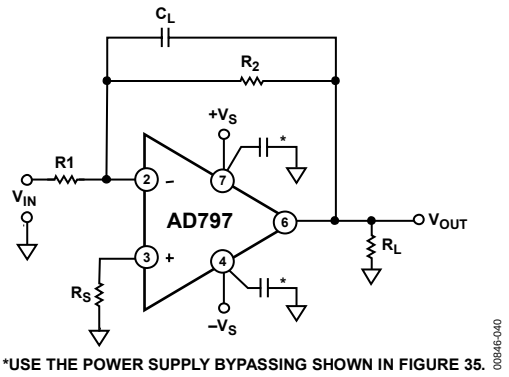


Figure 40. Inverting Amplifier Connection

Table 5. Values for Inverting Circuit

Gain	R1	R2	C_L	Noise (Excluding R_S)
−1	1 kΩ	1 kΩ	≈20 pF	3.0 nV/√Hz
−1	300 Ω	300 Ω	≈10 pF	1.8 nV/√Hz
−10	150 Ω	1500 Ω	≈5 pF	1.8 nV/√Hz

DRIVING CAPACITIVE LOADS

The capacitive load driving capabilities of the AD797 are displayed in Figure 41. At gains greater than 10, usually no special precautions are necessary. If more drive is desirable, however, the circuit shown in Figure 42 should be used. For example, this circuit allows a 5000 pF load to be driven cleanly at a noise gain ≥2.

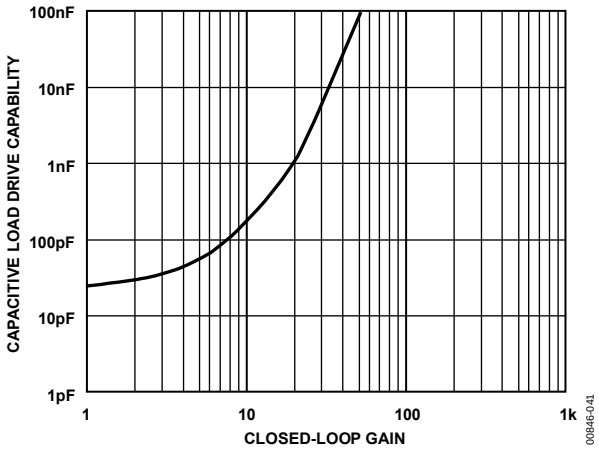


Figure 41. Capacitive Load Drive Capability vs. Closed-Loop Gain

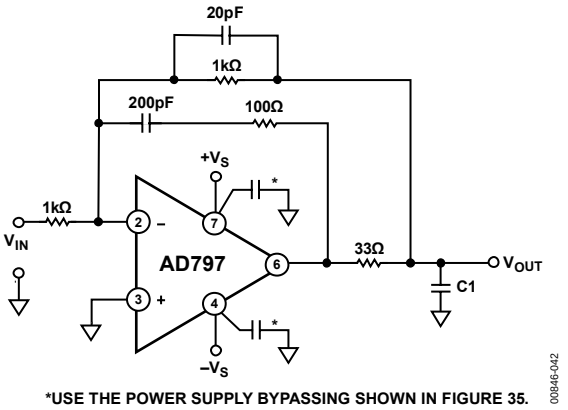


Figure 42. Recommended Circuit for Driving a High Capacitance Load

SETTLING TIME

The AD797 is unique among ultralow noise amplifiers in that it settles to 16 bits (<150 μV) in less than 800 ns. Measuring this performance presents a challenge. A special test circuit (see Figure 43) was developed for this purpose. The input signal was obtained from a resonant reed switch pulse generator, available from Tektronix as calibration Fixture No. 067-0608-00. When open, the switch is simply 50 Ω to ground and settling is purely a passive pulse decay and inherently flat. The low repetition rate signal was captured on a digital oscilloscope after being amplified and clamped twice. The selection of plug-in for the oscilloscope was made for minimum overload recovery.

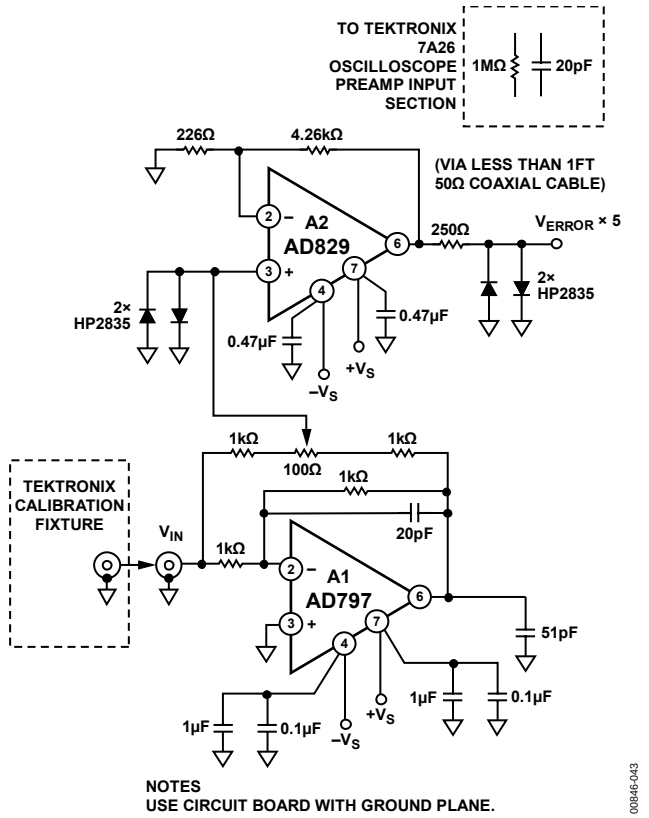


Figure 43. Settling Time Test Circuit

DISTORTION REDUCTION

The AD797 has distortion performance (THD < −120 dB, @ 20 kHz, 3 V rms, R_L = 600 Ω) unequaled by most voltage feedback amplifiers.

At higher gains and higher frequencies, THD increases due to a reduction in loop gain. However, in contrast to most conventional voltage feedback amplifiers, the AD797 provides two effective means of reducing distortion as gain and frequency are increased: cancellation of the output stage's distortion and gain bandwidth enhancement by decompensation. By applying these techniques, gain bandwidth can be increased to 450 MHz at G = 1000, and distortion can be held to −100 dB at 20 kHz for G = 100.

The unique design of the AD797 provides cancellation of the output stage's distortion. To achieve this, a capacitance equal to the effective compensation capacitance, usually 50 pF, is connected between Pin 8 and the output (see C2 in Figure 44). Use of this feature improves distortion performance when the closed-loop gain is more than 10 or when frequencies of interest are greater than 30 kHz.

Bandwidth enhancement via decompensation is achieved by connecting a capacitor from Pin 8 to ground (see C1 in Figure 44). Adding C1 results in subtracting from the value of the internal compensation capacitance (50 pF), yielding a smaller effective compensation capacitance and therefore a larger bandwidth.

The benefits of adding C1 are evident for closed-loop gains of ≥100. A maximum value of ≈33 pF at gains of ≥1000 is recommended. At a gain of 1000, the bandwidth is 450 kHz.

Table 6 and Figure 45 summarize the performance of the AD797 with distortion cancellation and decompensation.

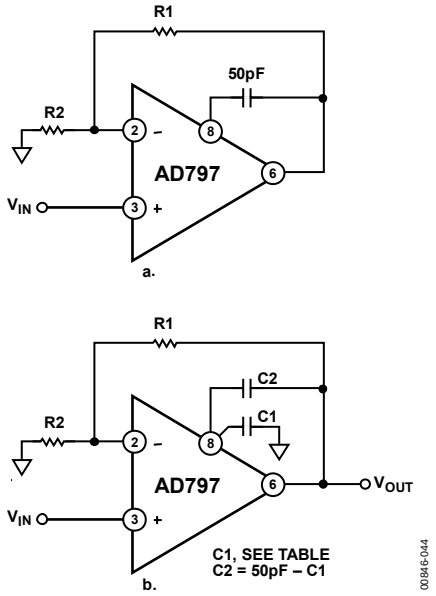


Figure 44. Recommended Connections for Distortion Cancellation and Bandwidth Enhancement

Table 6. Recommended External Compensation for Distortion Cancellation and Bandwidth Enhancement

	A/B		A			B		
Gain	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)	3 dB BW	C1 (pF)	C2 (pF)	3 dB BW
10	909	100	0	50	6 MHz	0	50	6 MHz
100	1 k	10	0	50	1 MHz	15	33	1.5 MHz
1000	10 k	10	0	50	110 kHz	33	15	450 kHz

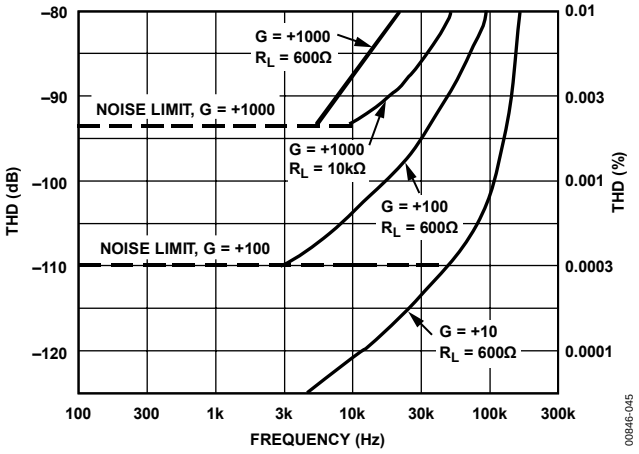


Figure 45. Total Harmonic Distortion (THD) vs. Frequency @ 3 V rms for Figure 44b

Differential Line Receiver

The differential receiver circuit of Figure 46 is useful for many applications, from audio to MRI imaging. The circuit allows

extraction of a low level signal in the presence of common-mode noise. As shown in Figure 47, the AD797 provides this function with only 9 nV/√Hz noise at the output. Figure 48 shows the AD797 20-bit THD performance over the audio band and the 16-bit accuracy to 250 kHz.

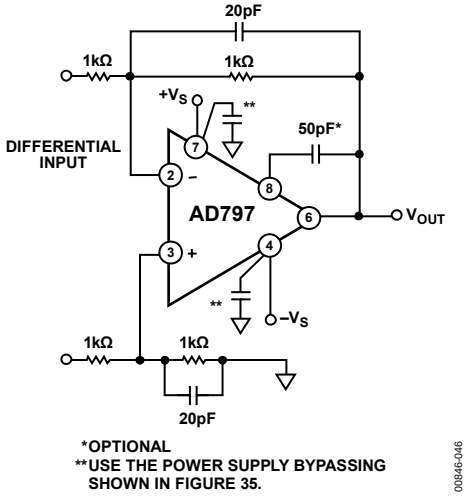


Figure 46. Differential Line Receiver

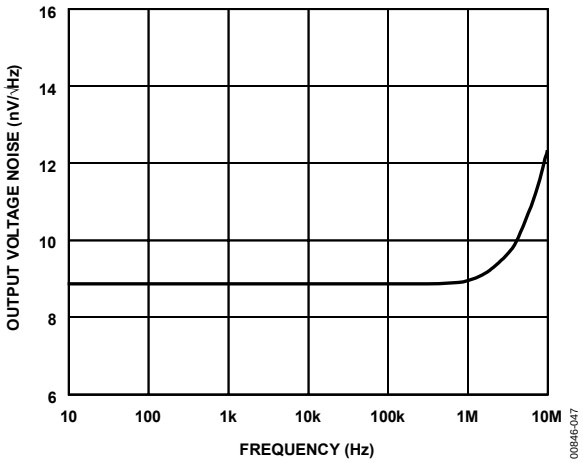


Figure 47. Output Voltage Noise Spectral Density for Differential Line Receiver

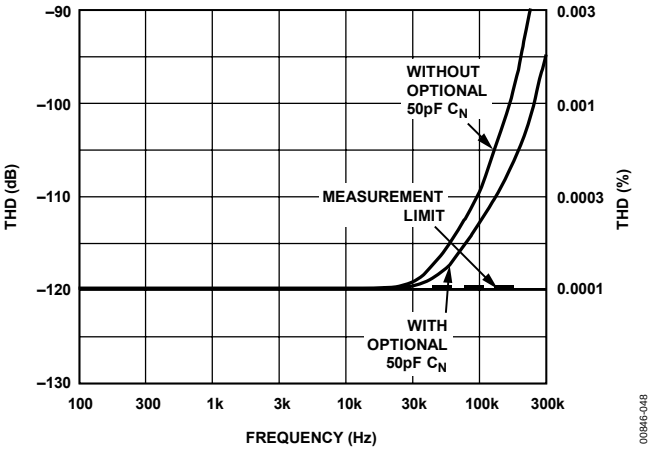


Figure 48. Total Harmonic Distortion (THD) vs. Frequency for Differential Line Receiver

A General-Purpose ATE/Instrumentation I/O Driver

The ultralow noise and distortion of the AD797 can be combined with the wide bandwidth, slew rate, and load drive of a current feedback amplifier to yield a very wide dynamic range general-purpose driver. The circuit shown in Figure 49 combines the AD797 with the AD811 in just such an application. Using the component values shown, this circuit is capable of better than −90 dB THD with a ±5 V, 500 kHz output signal. The circuit is, therefore, suitable for driving a high resolution ADC as an output driver in automatic test equipment (ATE) systems. Using a 100 kHz sine wave, the circuit drives a 600 Ω load to a level of 7 V rms with less than −109 dB THD and a 10 kΩ load at less than −117 dB THD.

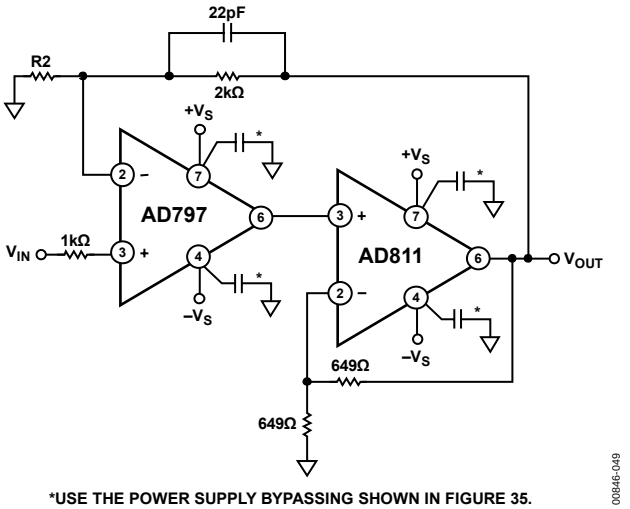


Figure 49. A General-Purpose ATE/Instrumentation I/O Driver

Ultrasound/Sonar Imaging Preamp

The AD600 variable gain amplifier provides the time-controlled gain (TCG) function necessary for very wide dynamic range sonar and low frequency ultrasound applications. Under some circumstances, it is necessary to buffer the input of the AD600 to preserve its low noise performance. To optimize dynamic range, this buffer should have a maximum of 6 dB of gain. The combination of low noise and low gain is difficult to achieve. The input buffer circuit shown in Figure 50 provides 1 nV/√Hz noise performance at a gain of 2 (dc to 1 MHz) by using 26.1 Ω resistors in its feedback path. Distortion is only −50 dBc at 1 MHz for a 2 V p-p output level and drops rapidly to better than −70 dBc at an output level of 200 mV p-p.

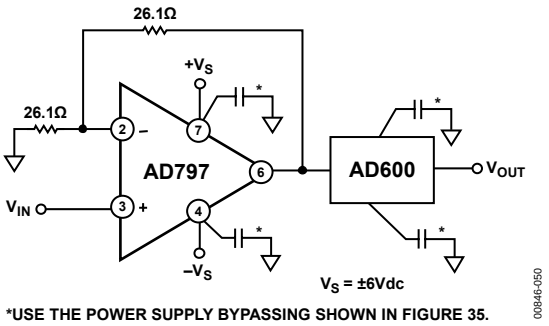


Figure 50. An Ultrasound Preamplifier Circuit

Amorphous (Photodiode) Detector

Large area photodiodes ($C_S \geq 500$ pF) and certain image detectors (amorphous Si) have optimum performance when used in conjunction with amplifiers with very low voltage (rather than very low current noise). Figure 51 shows the AD797 used with an amorphous Si (C_S = 1000 pF) detector. The response is adjusted for flatness using capacitor C_L, and the noise is dominated by voltage noise amplified by the ac noise gain. The AD797's excellent input noise performance gives 27 μV rms total noise in a 1 MHz bandwidth, as shown by Figure 52.

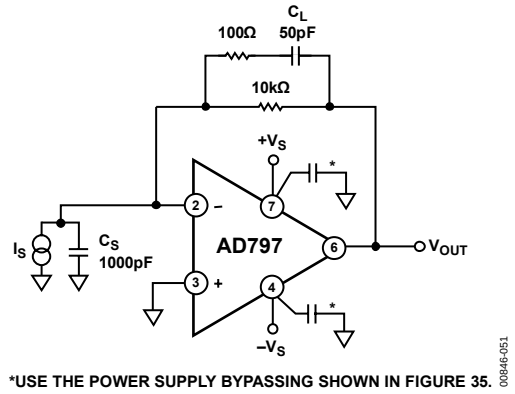


Figure 51. Amorphous Detector Preamp

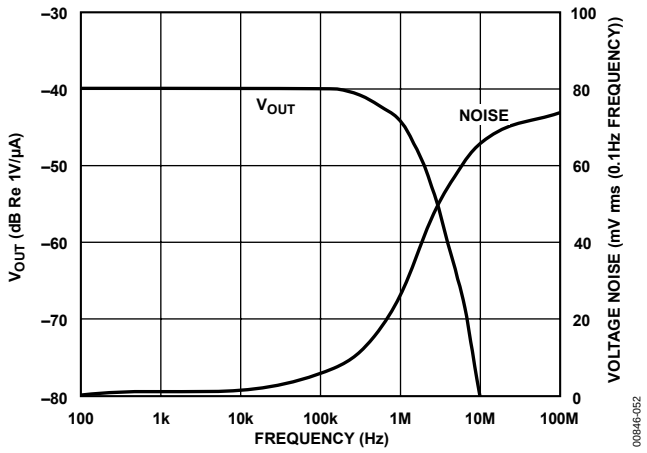


Figure 52. Total Integrated Voltage Noise and V_{OUT} of Amorphous Detector Preamp

Professional Audio Signal Processing—DAC Buffers

The low noise and low distortion of the AD797 make it an ideal choice for professional audio signal processing. An ideal I-to-V converter for a current output DAC would simply be a resistor to ground, were it not for the fact that most DACs do not operate linearly with voltage on their output. Standard practice is to operate an op amp as an I-to-V converter, creating a virtual ground at its inverting input. Normally, clock energy and current steps must be absorbed by the op amp output stage. However, in the configuration shown in Figure 53, Capacitor C_F shunts high frequency energy to ground while correctly reproducing the desired output with extremely low THD and IMD.

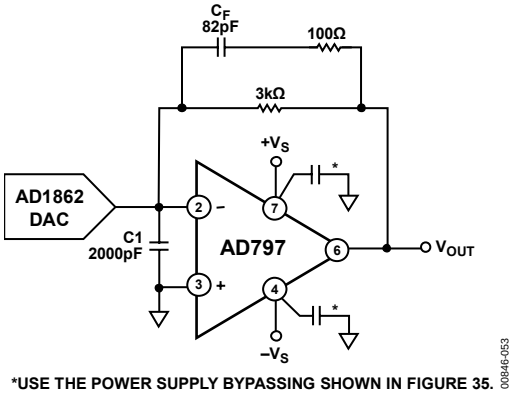


Figure 53. A Professional Audio DAC Buffer

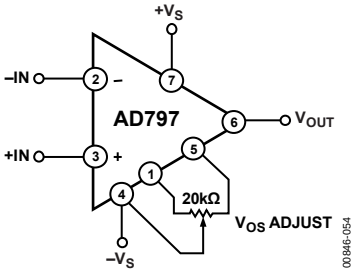
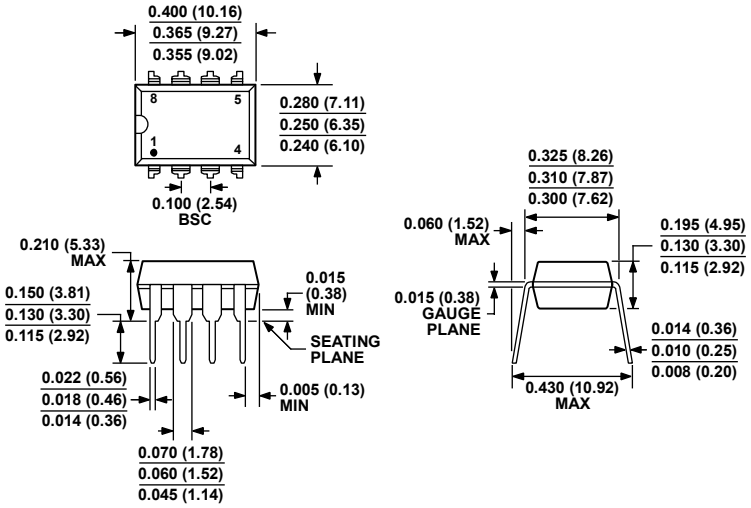


Figure 54. Offset Null Configuration

OUTLINE DIMENSIONS

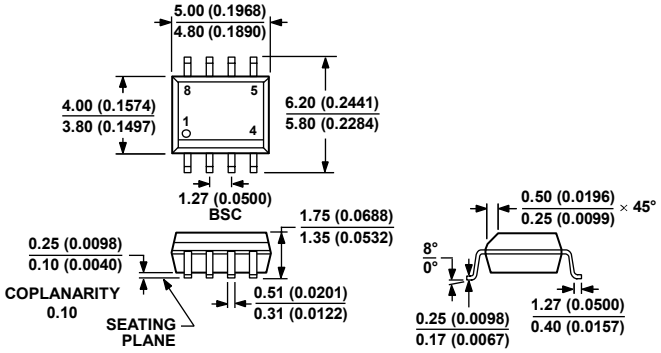


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 55. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 56. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD797AN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD797ANZ[1]	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD797AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797AR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797AR-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797ARZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797ARZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797ARZ-REEL7[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797BR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797BR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797BR-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797BRZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797BRZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD797BRZ-REEL7[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.

NOTES

D00846-0-1/08(F)