Control integrated Power System (CIPOS™)

IHCS22R60CE

Two Phase Switched Reluctance Drives

Power Management & Drives

Never stop thinking.

Control integrated Power System (CIPOS™)

Revision History:	**2009-05**	V 2.3
Previous Version:	2.2	
Page	Subjects (major changes since last revision)	
6	Corrected section “Pin assignment”	

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Table of contents:

Control integrated Power System

Two Phase switched Reluctance

600V / 15A @ 80°C

Features

- fully isolated package
- Infineon Trenchstop IGBTs with lowest $V_{CE(sat)}$
- optimal adapted Emcon diode for low EMI
- SOI gate driver with boot strap diode and capacitor (4.4 µF)
- rugged SOI gate driver technology with stability against transient and negative voltage
- temperature monitor and over temperature shutdown
- undervoltage lockout at all channels
- matched propagation delay for all channels
- shunt for current measurement integrated
- lead-free terminal plating; RoHS compliant
- qualified according to JEDEC[1] (high temperature stress tests for 1000h) for target applications

System configuration

- 2 Phases in asymmetric halfbridge topology IGBT + FW-diodes,
- SOI gate driver
- Shunt resistor for current measurement
- Bootstrap diodes for high side supply
- Integrated 4.4 µF bootstrap capacitance
- temp.sensor
- Isolated heatsink
- creepage distances typ. 3.2 mm

Typical Application

- Two Phase Switched Reluctance Drives

Description

CIPOS™ module family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs.

This module is designed to control two phase switched reluctance motors in variable speed drives for applications like vacuum cleaners. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also EMI-save control and overload protection. The features of Infineon TrenchStop® IGBTs and diodes are combined with a new optimized Infineon SOI gate driver for excellent electrical performance.

Certification

UL 1577 (UL file E314539)

[1] J-STD-020 and JESD-022

Internal Electrical Schematic

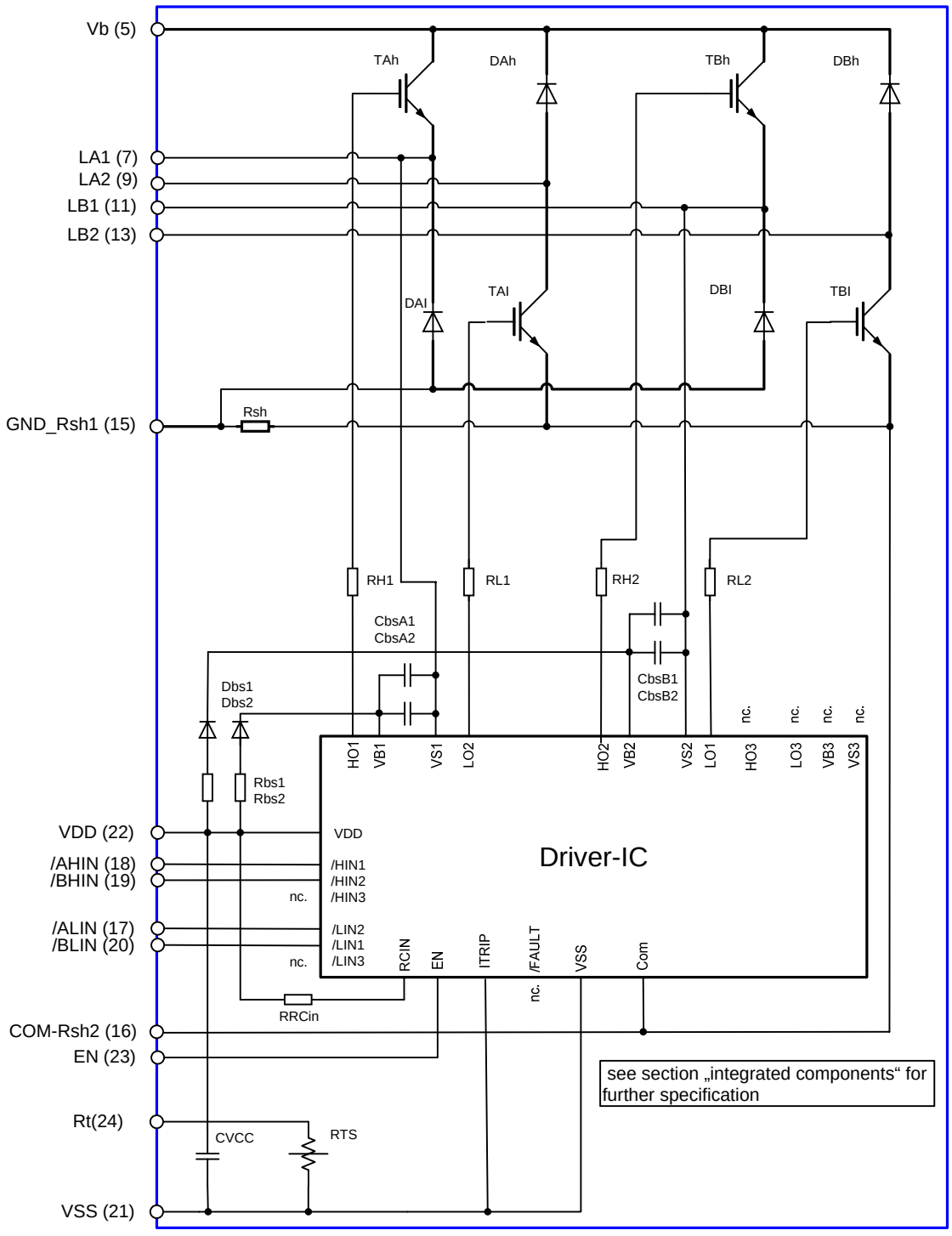


Figure 1: Internal Schematic

Pin Assignment

Pin	*Name*	*Description*
1		n.c.
2		n.c.
3		n.c.
4		n.c.
5	V+	Positive Bus Input Voltage
6		n.c.
7	LA1	Output Terminal 1 Phase A
8		n.c.
9	LA2	Output Terminal 2 Phase A
10		n.c.
11	LB1	Output Terminal 1 Phase B
12		n.c.
13	LB2	Output Terminal 2 Phase B
14		n.c.
15	GND-sh1	Negative Bus Input Voltage / Connection of internal Shunt
16	Rsh2-COM	Current measurement Signal, Reference of Low Side Gate Drive
17	/ALIN	Control Signal for Low Side Transistor of Phase A
18	/AHIN	Control Signal for High Side Transistor of Phase A
19	/BHIN	Control Signal for High Side Transistor of Phase B
20	/BLIN	Control Signal for Low Side Transistor of Phase B
21	VSS	Control Reference Signal
22	VDD	Control supply terminal
23	EN	Enable Control Terminal
24	Rt	Temperature read-out Terminal

Pin Description

/AHIN, /ALIN, /BHIN and /BLIN (low side and high side control pins, Pin 17 - 20)

These pins are active low and they are responsible for the control of the integrated IGBT. The Schmitt-trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-up resistor of about 75 kOhm is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time t_{FILIN}. The filter acts according to Figure E for other short signals ranges t_{FILIN1} and t_{FILIN2}.

It is recommended for proper work of CiPoS™ not

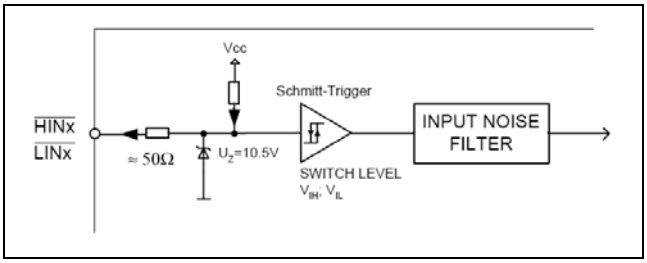


Figure 2: Input pin structure

to provide input pulse-width lower than 1us.

The integrated gate drive provides shoot through prevention capability which avoids the simultaneous on-state of a pair of gate outputs of the same number (i.e. HO1 and LO1, HO2 and LO2 of driver IC).

A minimum deadtime insertion of typ 380ns is also provided in these pairs, in order to reduce cross-conduction of the external power switches.

EN (enable, Pin 23)

The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. The internal structure of the pin is the same as Figure 2 made exception of the switching levels of the Schmitt-Trigger, which are here $V_{EN,TH+}$ = 2.1 V and $V_{EN,TH-}$ = 1.3 V. The typical propagation delay time is t_{EN} = 900 ns.

VDD, VSS (control side supply and reference, Pin 22, 23)

VDD is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 12.1 V is at least present.

The IC shuts down all the gate drivers power outputs, when the VDD supply voltage is below V_{DDUV-} = 10.4 V according to Figure 3. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage.

Due to the low power consumption, the floating driver stage is supplied by an integrated bootstrap circuit connected to VDD. This includes integrated bootstrap capacitors of 4.4µF at each floating supply, which are located very close to the gate drive circuit.

VS1,2,3 provide a high robustness against negative voltage in respect of VSS of -50 V. This ensures very stable designs even under rough conditions.

GND_Rsh1 (low side anode - Shunt reference, Pin 15) and COM_Rsh2 (Shunt signal)

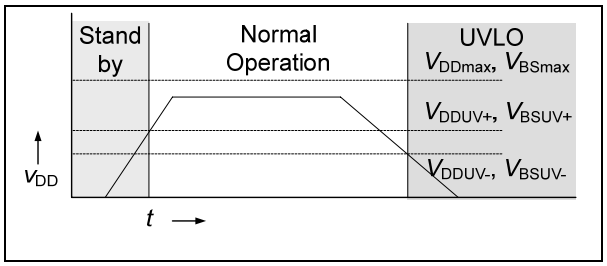


Figure 3: Operation modes

The emitters of the low side IGBT are connected to the shunt resistor. They are also connected to pin GND_Rsh2, which is the shunt signal. The low side anodes of the integrated diodes are connected directly to GND_Rsh1, so that only the transistor current of TAl and TBl contribute to the voltage drop over the shunt.

V+ (positive bus input voltage, Pin 10)

The high side IGBT are connected to the bus voltage. It is recommended, that the bus voltage does not exceed 500 V.

Rt (Temperature sense output)

A NTC-resistor is integrated with a resistance of 100kOhm at 25°C and a B-constant of B = 4250 K

Absolute Maximum Ratings

(T_J = 25°C, V_{DD} = 15V Unless Otherwise Specified):

Module section

Description	Condition	Symbol	Value	Unit
Storage temperature range		T_{stg}	-40 … 125	°C
Operating temperature Control PCB[1]		T_{PCB}	125°C	
Solder temperature	wavesoldering, 1.6 mm (0.063 in.) from case for 10s	T_{sol}	260	
Insulation test voltage	RMS, f = 50Hz, t = 1 min	V_{ISOL}	2500	V
Mounting torque	M3 screw	M_S	0.6	Nm

IGBT and Diode Section

Description	Condition	Symbol	Value	Unit
Max. Blocking Voltage		V_{CES}	600	V
DC Output current IGBT	T_c = 25 °C, T_{vJ}<150°C T_c = 80 °C, T_{vJ}<150°C	I_C	21.6 15	A
DC Output current Diode	T_c = 25 °C, T_{vJ}<150°C T_c = 80 °C, T_{vJ}<150°C	I_F	17 10	A
Repetitive IGBT peak collector current	T_p limited by T_{vJ}max.	I_{CRM}	45	A
Repetitive Diode peak collector current	T_p limited by T_{vJ}max.	I_{FRM}	30	A
Short circuit withstand time	VDC = 400V, T_{vJ} =150°C	t_{sc}	5	µs
Power dissipation per IGBT	T_c = 25°C	P_{tot}	65	W
Operating junction temperature range		T_{vjI} ,T_{vjD}	-40 … 150	°C
Single thermal resistance, junction-case	IGBT Diode	R_{thJC} R_{thJCD}	2.1 3.6	K/W

Control section

Description	Condition	Symbol	Value		Unit
			Min	max	
Module supply voltage		V_{DD}	-1	20	V
high side floating IC supply offset voltage	t_p < 500 ns	$V_{S1,2,3}$	VDD-VBS-6 VDD-VBS-50	600	V
Input Voltage	/ALIN, /AHIN, /BLIN, /BHIN, EN	V_{in}	-1	10	V
Operating junction temperature[2]		$T_{J,IC}$	-	125	
Max. switching frequency		f_{PWM}		10	kHz

[1] Monitored by pin 24
[2] Monitored by pin 24

Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -Potential unless otherwise specified.

Parameter	Symbol	min.	max.	Unit
High side floating supply offset voltage	V_S	-3	500	V
High side floating supply voltage (V_B vs. V_S)	V_{BS}	12.5	17.5	
High side output voltage (V_{HO} vs. V_S)	V_{HO}	0	V_{BS}	
Low side power supply	V_{DD}	12.5	17.5	
Logic input voltages LIN,HIN,EN,ITRIP	V_{IN}	0	5	

Static Characteristics

(T_c = 25°C, V_{DD} = 15V, if not stated otherwise)

Description	Condition	Symbol	min	Typ	max	Unit
Collector-Emitter breakdown voltage	V_{GE} = 0V, I_C=0.25mA	$V_{(BR)CES}$	600	-	-	V
Collector-emitter saturation voltage	I_{out} = +/-15A T_{vJ} = 25°C T_{vJ} = 150°C	$V_{CE(sat)}$	- -	1.65 1.9	2.15 -	V
Diode forward voltage	V_{IN} = 5V, I_{out} = +/-10A T_{vJ} = 25°C T_{vJ} = 150°C	V_F	- -	1.65 1.6	2.05	V
Logic "0" input voltage	/ALIN, /AHIN, /BLIN, /BHIN	V_{IH}	1.7	2.1	2.4	V
Logic "1" input voltage	/ALIN, /AHIN, /BLIN, /BHIN	V_{IL}	0.7	0.9	1.1	V
EN positive going threshold		$V_{EN,TH+}$	1.9	2.1	2.3	V
EN negative going threshold		$V_{EN,TH-}$	1.1	1.3	1.5	V
V_{DD} and V_{BS} supply undervoltage positive going threshold		V_{DDUV+} V_{BSUV+}	11.0	12.1	12.8	V
V_{DD} and V_{BS} supply undervoltage negative going threshold		V_{DDUV-} V_{BSUV-}	9.5	10.4	11.0	V
V_{CC} and V_{BS} supply undervoltage lockout hysteresis		V_{DDUVH} V_{BSUVH}	1.2	1.7	-	V
Input clamp voltage	I_{IN} = 4mA; /ALIN, /AHIN, /BLIN, /BHIN, EN	$V_{INCLAMP}$	9.0	10.1	13	V
Input bias current	V_{IN} = 5V	I_{LIN+} I_{HIN+}	-	55	100	µA
Input bias current	V_{IN} = 0V	I_{LIN-} I_{HIN-}	-	110	200	µA
EN Input bias current	V_{EN} = 5V	I_{EN+}	-	62	120	µA

Dynamic Characteristics

(T_c = 25°C, V_{DD} = 15V, if not stated otherwise)

Description	Condition	Symbol	min	typ	max	Unit
Turn-on propagation delay High side or low side	$V_{LIN,HIN}$ = 0V; I_{out} = 15A, V_{DC} = 300V	$t_{d(on)}$	-	656	-	ns
Turn-on rise time High side or low side	I_{out} = 15A, V_{DC} = 300V $V_{LIN,HIN}$ = 5V	t_r	-	40	-	ns
Turn-off propagation delay High side or low side	$V_{LIN,HIN}$ = 5V; I_{out} = 15A, V_{DC} = 300V	$t_{d(off)}$	-	1051	-	ns
Turn-off fall time High side or low side	I_{out} = 15A, V_{DC} = 300V $V_{LIN,HIN}$ = 0V	t_f	-	32.4	-	ns
Shutdown propagation delay ENABLE	V_{EN} = 0V	t_{EN}	-	900	-	ns
Input filter time at LIN for turn on and off and input filter time at HIN for turn on only	$V_{LIN,HIN}$= 0 V & 5V	t_{FILIN}	120	270	-	ns
Input filter time 1 at /AHIN, /BHIN for turn off	V_{HIN} = 5V	t_{FILIN1}	-	220	-	ns
Input filter time 2 at /AHIN, /BHIN for turn off	V_{HIN} = 5 V	t_{FILIN2}	-	400	-	ns
Input filter time EN		t_{FILEN}	300	430	-	ns
IGBT Turn-on Energy	I_{out} = 15A, V_{DC}=300V T_{vj} = 25°C T_{vj} = 150°C	E_{on}	 - -	 0.70 0.85	 - -	mJ
IGBT Turn-off Energy	I_{out} = 15A, V_{DC}=300V T_{vj} = 25°C T_{vj} = 150°C	E_{off}	 - -	 0.36 0.43	 - -	mJ
Diode recovery Energy	I_{out} = 10A, V_{DC}=300V T_{vj} = 25°C T_{vj} = 150°C	E_{rec}	 - -	 0.05 0.12	 - -	mJ

Integrated Components

Description	Condition	Symbol	min	typ	max	Unit
Integrated Resistor		Rbs1, Rbs2	-	10	-	Ω
Shunt Resistor		Rsh	-	5		mΩ
Integrated Capacitor		CVCC	-	0.1	-	µF
Integrated Bootstrap Capacitor		CbsA1, CbsA2, CbsB1, CbsB2	-	2.2	-	
Resistance of NTC	T_{NTC} = 25°C	RTS	-	100	-	kΩ
B-constant of NTC		B	-	4250	-	K
Forward Voltage of Bootstrap Diode	T_j = 25°C, I_F = 1 A	V_{Fbs}	-	1.3	-	V
Reverse Recovery of Bootsstrap Diode	T_j = 25°C, I_F = 1 A	t_{rrbs}		50		ns

Characteristics

(T_c = 25°C, V_{DD} = 15V, if not stated otherwise)

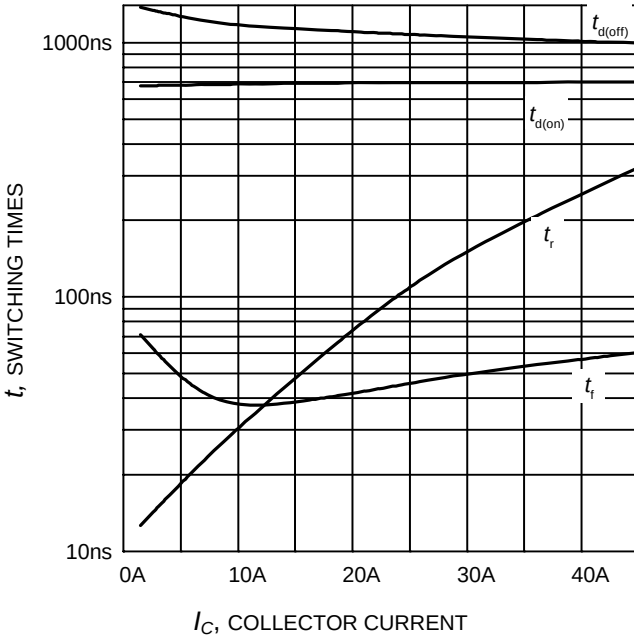


Figure 4. Typical switching times as a function of collector current
(inductive load, T_{vJ}=150°C,
V_{CE} = 300V
Dynamic test circuit in Figure E)

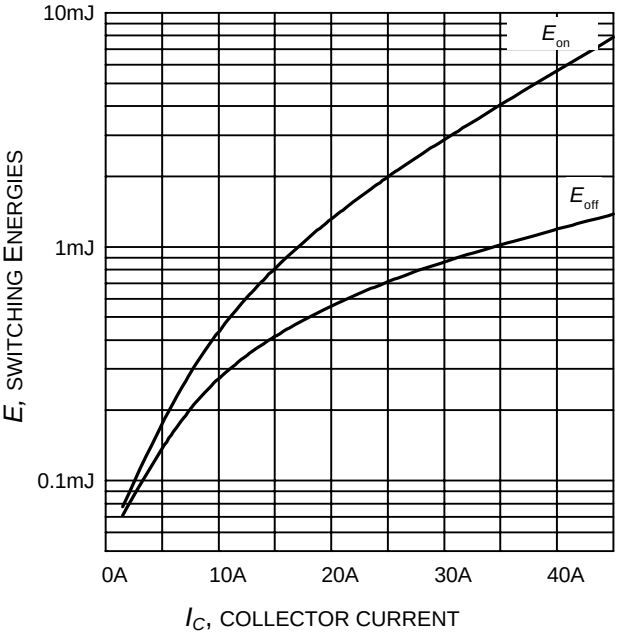


Figure 5. Typical switching energies as a function of collector current
(inductive load, T_{vJ} = 150°C,
V_{CE}= 300V
Dynamic test circuit in Figure E)

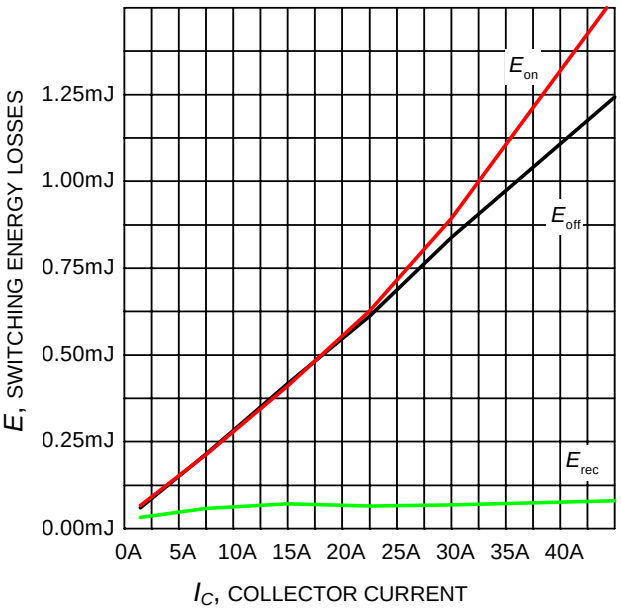


Figure 6. Typical switching energy losses as a function of collector current
(inductive load, Tv_J = 150°C,
V_{CE} = 300V
Dynamic test circuit in Figure A)

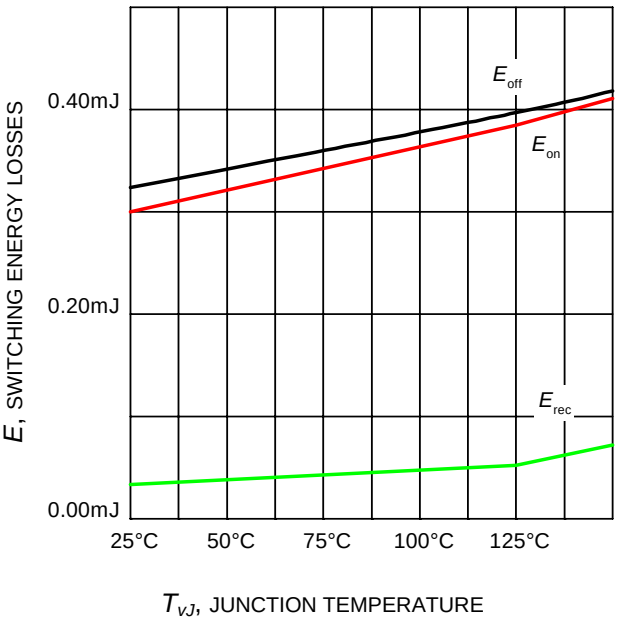


Figure 7. Typical switching energy losses as a function of junction temperature
(inductive load, V_{CE} = 300V, I_C = 15A
Dynamic test circuit in Figure A)

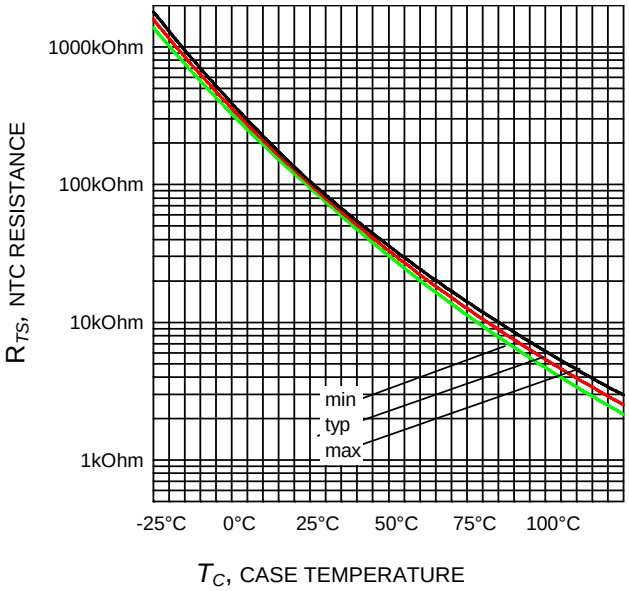


Figure 8. Typical NTC characteristic as a function of NTC temperature

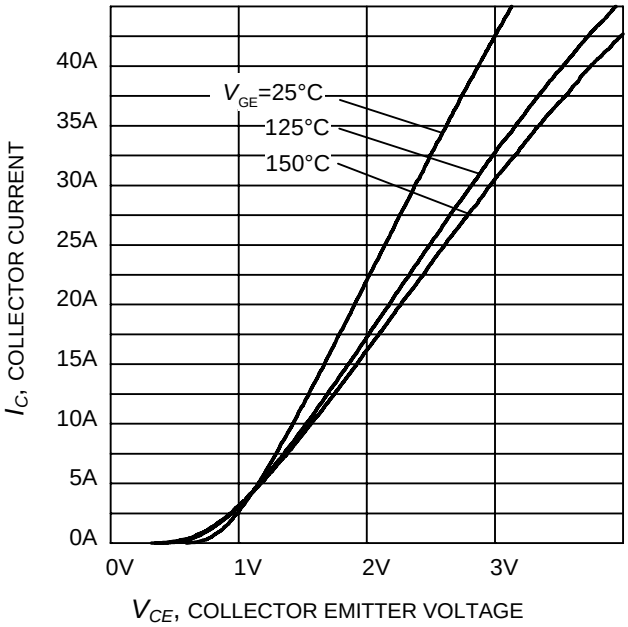


Figure 9. Typical IGBT output characteristic (V_{DD} = 15V)

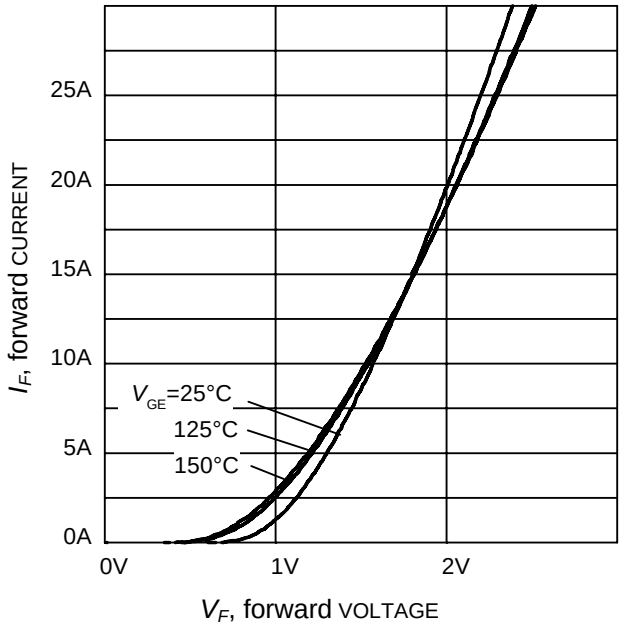


Figure 10. Typical diode forward current as a function of forward voltage

Test Circuits

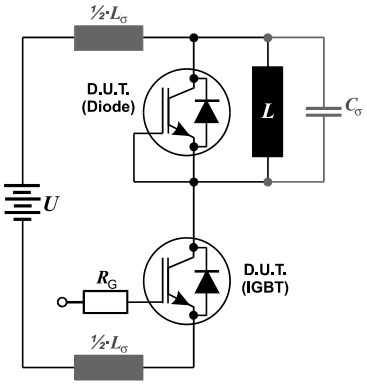


Figure A: Dynamic test circuit
Leakage inductance L_σ =180nH
Stray capacitance C_σ =39pF

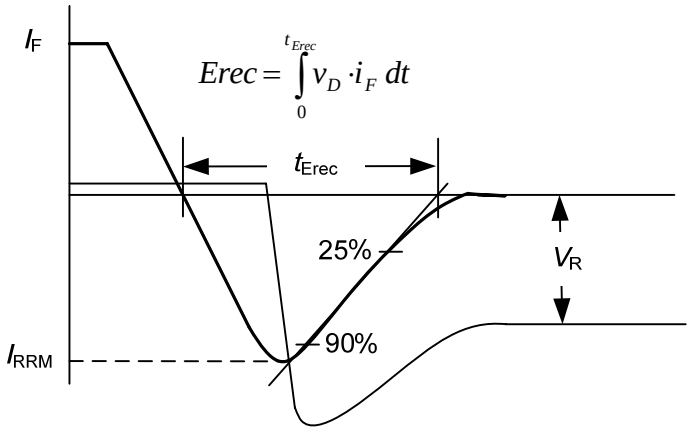


Figure B: Definition of diodes switching characteristics

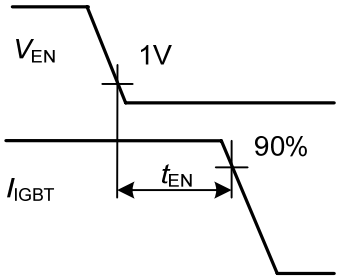


Figure C: Definition of Enable propagation delay

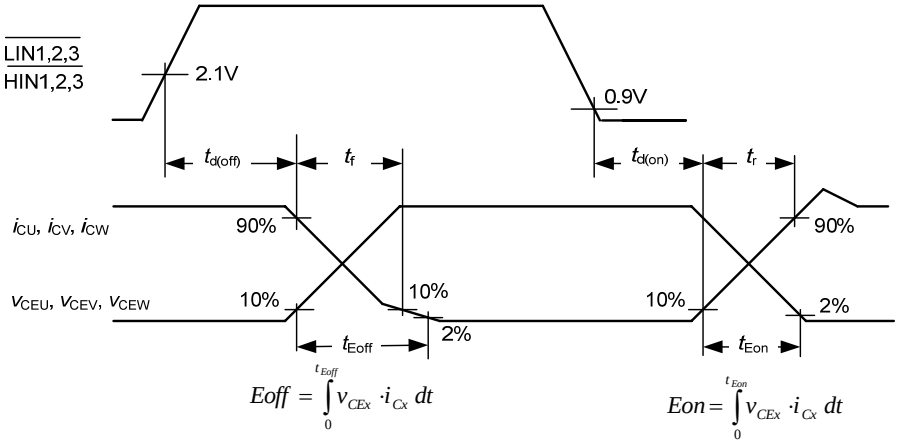


Figure D: Switching times definition and switching energy definition

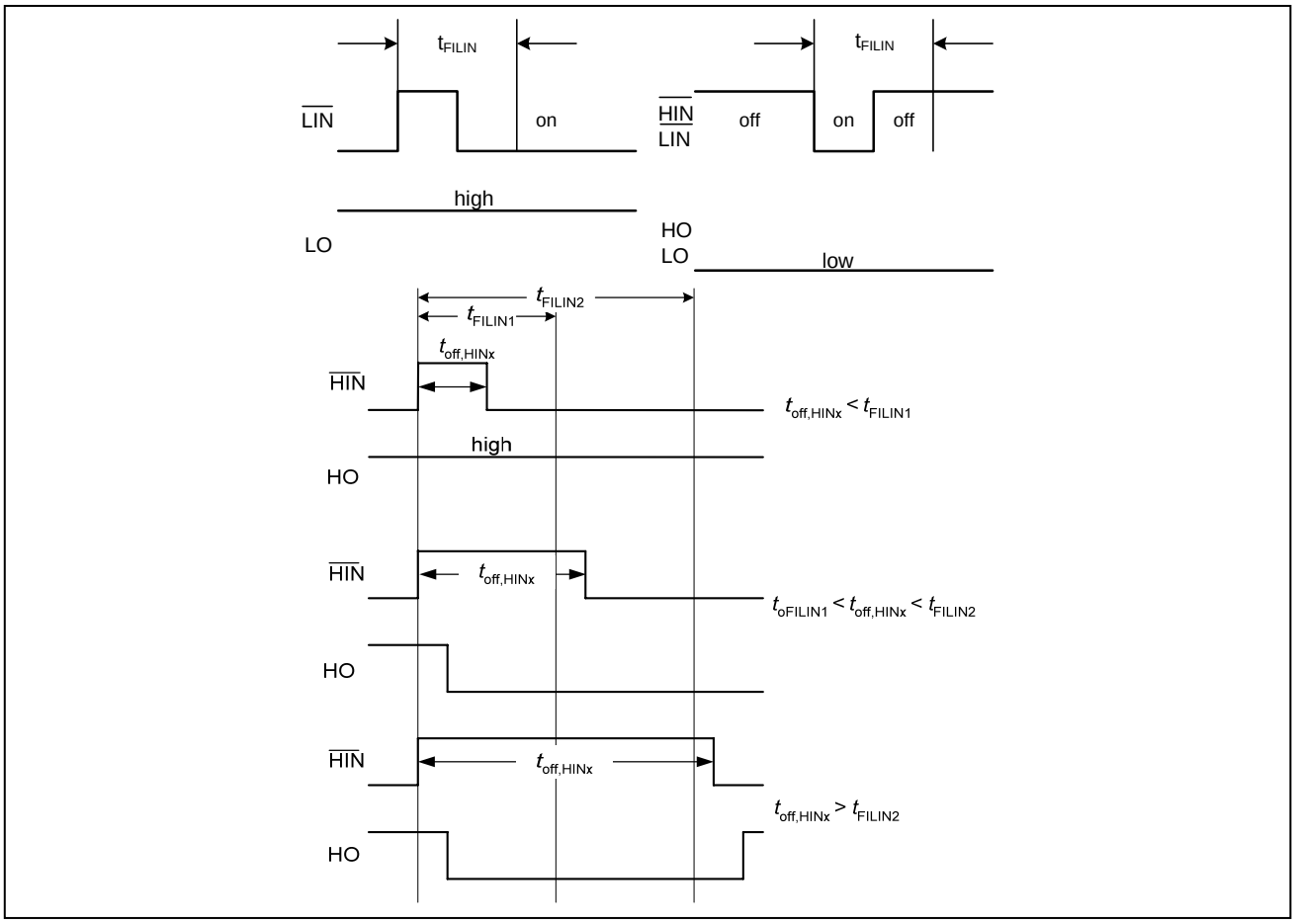
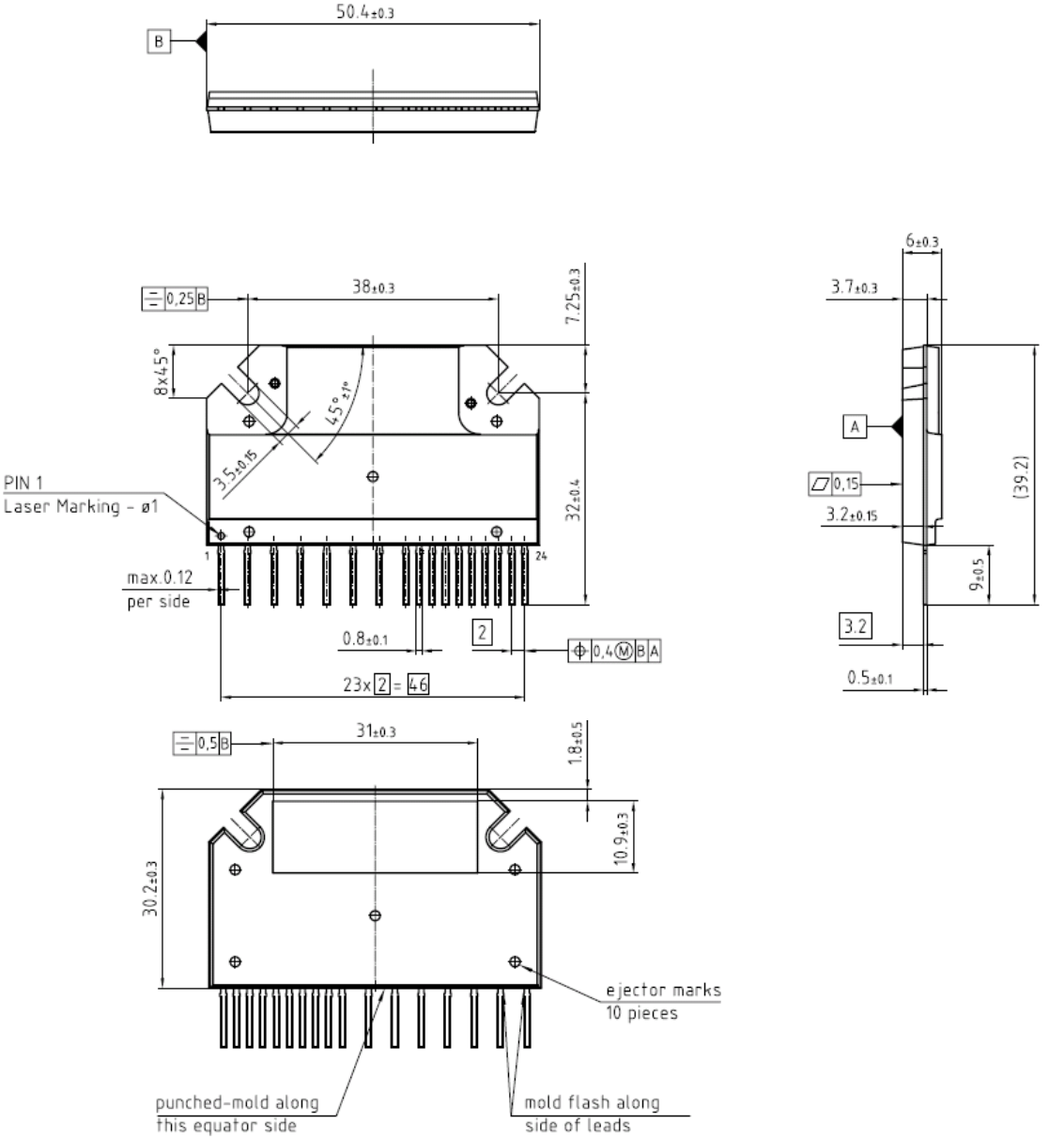
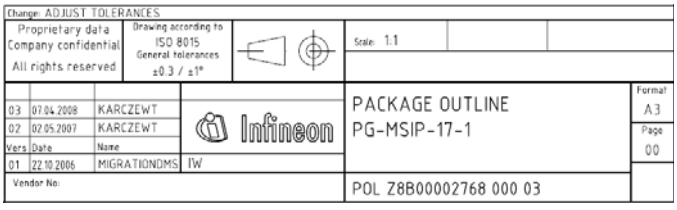


Figure E: Short Pulse suppression

Package Outline:





Package data

Description	Condition	Symbol	min	typ	max	Unit
Mounting Torque	M3 screw	M_S		0.5	0.6	Nm
Mounting pressure on surface	Package flat on mounting surface	N_{MC}			150	N/mm²