

# F-Type

## **Voltage Controlled Crystal Oscillator (VCXO)**



The FTV Voltage Controlled Crystal Oscillator

#### **Features**

- Industry Common Pinout
- Commercial or Industrial Temperature Range
- TTL or CMOS Drive Capability
- Hermetic Package
- 5.0 V or 3.3 V Supply

## **Description**

The F-Type Voltage Controlled Crystal Oscillator (VCXO) is used in a phase lock loop applications including clock recovery and frequency translation applications. The metal package is grounded for improved EMI performance.

## **Pin Information**

Table '	1. Pin Functio			
Pin	Symbol	Function	14	Q
1	V <sub>C</sub>	VCXO Control Voltage		
7	GND	Case Ground		
8	Output	VCXO Output	4	
14	$V_{DD}$	Power Supply Voltage (3.3 or 5.0 V ±10%)	<u>'</u>	<u> </u>

## **Performance Characteristics**

Table 2. Electrical Performance							
Parameter	Symbol	Minimum	Typical	Maximum	Units		
Operating Temperature Range	Temperature Range To 0 to 70, -20 To 70, or -40 to 85				°C		
Center Frequency <sup>1</sup>	f <sub>0</sub>	1	-	52	MHz		
Absolute Pull Range			ppm				
Supply Voltage <sup>2</sup>	$V_{DD}$	;	+/- 20 to +/-100 3.3 or 5.0 (+/-10%)				
Supply Current	I <sub>DD</sub>	-	0.45 mA/MHz	35	mA		
Output Voltage Levels <sup>3</sup>							
Output High	V <sub>OH</sub>	$0.9 V_{DD}$	-		V		
Output Low	V <sub>OL</sub>			$0.1 V_{DD}$	V		
Transition times <sup>3</sup>							
Rise Time	T <sub>R</sub>	-	-	5.0	ns		
Fall Time	T <sub>F</sub>	-	-	5.0	ns		
Fanout		-	-	10	TTL		
Start-Up Time	t <sub>su</sub>	-	2	-	ms		
Control Voltage	V <sub>C</sub>	0.1 V <sub>DD</sub>	-	0.9 V <sub>DD</sub>	V		
Fanout	Fo	-	-	10 TTL	Loads		

<sup>1.</sup> Other frequencies may be available, please contact factory with your special requirements.
2. A 0.1 μF low frequency tantalum bypass capacitor in parallel with a 0.01 μF high frequency ceramic capacitor is recommended. Both should be located as close to the FTU-Type bias pin as is practical 3. Figure 1 defines these parameters. Figure 2 illustrates the equivalent TTL load and operating conditions under which these parameters are specified and tested.

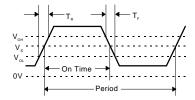


Figure 1. Output Waveform

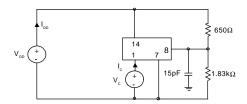


Figure 2. Output Test Conditions (25±5°C)

## F-Type VCXO

## **Handling Precautions**

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. VTI employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation.

ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance =  $1500\Omega$ , capacitance = 100pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 3. ESD Threshold Voltage							
Model	Threshold	Unit					
Human-Body (HBM)	1000*	Volts Min.					
Charged-Device (CDM)	500	Volts Min.					
*Mil-STD-883D, Method 3015, Class 1							

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Table 4. Mechanical and Environmental Compliance						
Parameter	Conditions					
Mechanical Shock	MIL-STD-883C, 2002.3, A					
Mechanical Vibration	MIL-STD-883C, 2007.1, A					
Temperature Cycle	MIL-STD-883C, 1010, A					
Gross Leak	100% Deionized Water					
Fine Leak	MIL-STD-883C, 1014.7					
Seal Strength	2 lbs Perpendicular to Top and Bottom					
Bend Test	MIL-STD-202E, 211A, C					
Marking	MIL-STD-202E, 215					
Storage Temperature	-55°C to 125°C					

### **Outline Diagram**

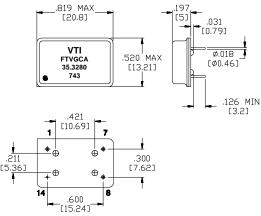


Figure 3 Outline Diagram

## **Ordering Information**

Example Part # ---

Ta	Table 5. Part Numbering										
<u>F</u>			Ţ	<u>V</u> <u>G</u>		<u>C</u>		<u>A</u>			
Package		V	Supply oltage (V)					Operating Temp. (°C)		Output Load	
F	4 pin DIP	Т	5.0±10%	٧	VCXO	F	±32	С	0 to 70	Α	TTL 50 ±5%
		D	3.3±10%			G	±50	L	-40 to 85	В	TTL 50 ±10%
						Н	±100	I	-20 to 70	J	CMOS 50 ±5%
					_	Α	±100 TPR			K	CMOS 50 ±10%

Other specifications may be available on request.

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