

STRUCTURE Silicon Monolithic Integrated Circuit

TYPE Voltage Tracker

PRODUCT SERIES **BD3925HFP-C**

FEATURES 1. Low dropout voltage/ Low quiescent current
 2. Built-in Overcurrent protection circuit/ Thermal shutdown circuit

○ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

| Parameter | Symbol | Limit | Unit |
|------------------------------|--------|----------|------|
| Supply Voltage | Vcc | 50 ※1 | V |
| Switch Supply Voltage | Vsw | 50 ※1 | V |
| ADJ Pin Voltage | VADJ | 28 | V |
| Vo Pin Voltage | Vo | 28 | V |
| Power Dissipation | Pd | 1.6 ※2 | W |
| Operating Temperature Range | Topr | -40~+125 | °C |
| Storage Temperature Range | Tstg | -55~+150 | °C |
| Maximum Junction Temperature | Tjmax | 150 | °C |

※1 Not to exceed Pd and AS0.

※2 Reduced by 12.8mW/°C over Ta=25°C , when mount on a glass epoxy board:70mm×70mm×1.6mm.

○OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|--------------------|--------|--------|------|------|
| Supply Voltage | Vcc | 4.5 ※3 | 36.0 | V |
| Output Current | Io | — | 500 | mA |
| ADJ Pin Voltage ※4 | VADJ | 2.5 | 14 | V |

※3 Please consider that the Output voltage would be dropped (Dropout voltage) according to the Output current.

※4 Not to exceed Vcc-0.5V

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

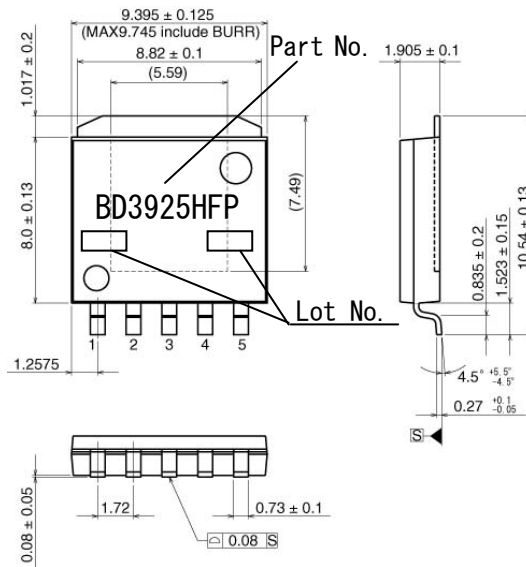
If there are any differences in translation version of this document, formal version takes priority.

○ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=-40~125°C, Vcc=13.2V, SW=3V, ADJ=5V)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|----------------------------|--------|--------|------|------|------|------------------------------|
| | | MIN | Typ | MAX | | |
| Shut Down Current | Ishut | — | — | 10 | μA | SW=GND |
| Bias Current | Ib | — | 45 | 90 | μA | Io=0mA |
| Offset Voltage | ΔVo | -15 | — | 15 | mV | 6V<Vcc<36V, 5mA<Io<200mA |
| Output Current | Io | 0.5 | — | — | A | |
| Dropout Voltage | ΔVd | — | 0.25 | 0.48 | V | Vcc=5V, ADJ=5V, Io=200mA |
| Ripple Rejection | R.R. | 45 | 55 | — | dB | f=120Hz, ein=1Vrms, Io=100mA |
| Switch Threshold Voltage H | SWH | 2.0 | — | — | V | ACTIVE MODE |
| Switch Threshold Voltage L | SWL | — | — | 0.5 | V | OFF MODE |
| Switch Bias Current | SWI | — | 22 | 60 | μA | SW=5V |
| ADJ Bias Current | ADJI | — | 5 | 12 | μA | ADJ=5V |

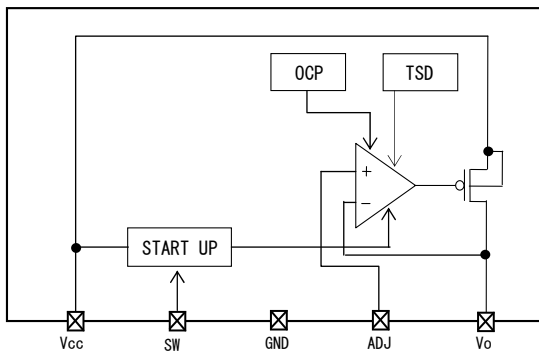
This product is not designed for protection against radio active rays.

○PHYSICAL DIMENSIONS · MARKING



HRP-5 (Unit : mm)

○BLOCK DIAGRAM



○PIN No. · PIN NAME · FUNCTION

| Pin No. | Pin Name | Function |
|---------|----------|-------------------------------|
| 1 | Vcc | Power Supply |
| 2 | SW | Output Voltage ON/OFF Control |
| 3 | N. C. | No Connection |
| 4 | ADJ | Output Voltage setting |
| 5 | Vo | Output Voltage |
| Fin | GND | Grand |

OPERATING NOTES

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Thermal design

The Power dissipation indicated on this specification is the value without heat sink. Use a thermal design that allows for a sufficient margin by attaching with heat sink in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake mounting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC. Ensure a minimum GND pin potential in all operating conditions.

5) Actions in strong magnetic field

Keep in mind that the IC may malfunction in strong magnetic fields.

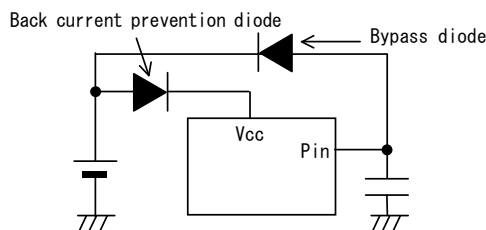
6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

7) Ground patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external parts, either.

8) Applications or inspection processes where the potentials of the Vcc pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 470 μF or lower in case Vcc is shorted with the GND pin while the external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with Vcc or bypass diodes between Vcc and each pin.



9) SW Pin, ADJ Pin

Do not apply the voltage to SW pin and ADJ pin when the Vcc is not applied. And when the Vcc is applied, the voltage of SW pin and ADJ pin must not exceed Vcc.

10) Thermal shutdown circuit (TSD)

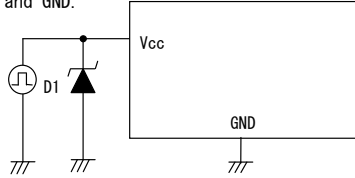
This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the junction temperature (Tj) will trigger the TSD circuit to turn off all output power elements (175°C:Typ). The circuit automatically resets once the junction temperature (Tj) drops (150°C:Typ). Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Overcurrent protection circuit (OCP)

The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

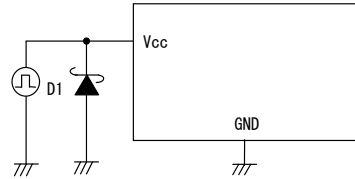
12) About positive surge voltage

To protect against a surge voltage that exceeds 50V between Vcc and GND please insert a power zener diode between Vcc terminal and GND.



13) About negative surge voltage

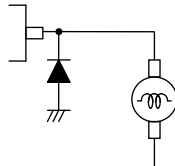
To protect against a negative surge voltage, please insert a Schottky diode between the Vcc terminal and GND.



14) We recommend using Diode for protection purpose when the temperature so output voltage is off.

This is to prevent against large loads of impedance or reverse current during initial stages or output off stage.

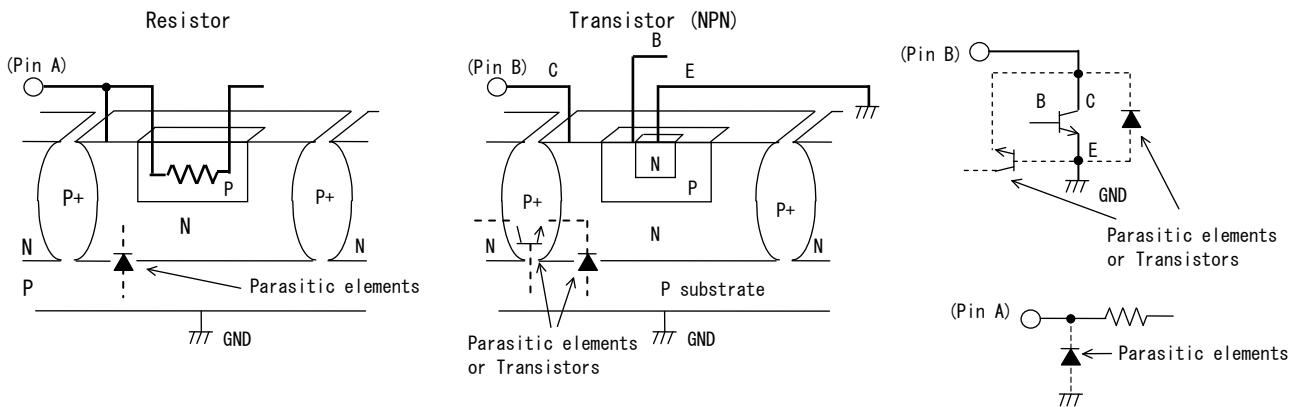
(Example)



15) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in the following figure,

- The P/N junction functions as a parasitic diode when $GND > Pin A$ for the resistor or $GND > Pin B$ for the transistor (NPN).
- Similarly, when $GND > Pin B$ for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins. Keep in mind that the IC may malfunction in strong magnetic fields.



16) For a steep change of the Vcc voltage

Because MOS for output Transistor is used when an input voltage change is very steep, it may evoke large current. When selecting the value of external circuit constants, please make sure that the operation on the actual application takes these conditions into account.

17) For an infinitesimal fluctuations of output voltage.

At the use of the application that infinitesimal fluctuations of output voltage caused by some factors (e.g. disturbance noise, input voltage fluctuations, load fluctuations, etc.), please take enough measures to avoid some influence (e.g. insert the filter, etc.).

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