Specification of

256Mb (8Mx32bit) Mobile DDR SDRAM

Memory Cell Array

- Organized as 4banks of 2,097,152 x32

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Document Title

256MBit (4Bank x 2M x 32bits) MOBILE DDR SDRAM

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	May 2008	Preliminary
0.2	IDD Specification updated	May 2008	Preliminary
1.0	The final version	Nov. 2008	
1.1	Correct Part No. (page 3)	Mar. 2009	
1.2	Insert DDR370 DC/AC Characteristics	Apr. 2009	

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FEATURES SUMMARY

● **Mobile DDR SDRAM**

- Double data rate architecture: two data transfer per clock cycle

● **Mobile DDR SDRAM INTERFACE**

- x32 bus width
- Multiplexed Address (Row address and Column address)

● **SUPPLY VOLTAGE**

- 1.8V device: VDD and VDDQ = 1.7V to 1.95V

● **MEMORY CELL ARRAY**

- 256Mbit (x32 device) = 2M x 4Bank x 32 I/O

● **DATA STROBE**

- x32 device: DQS0 ~ DQS3
- Bidirectional, data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
- Data and data mask referenced to both edges of DQS

● **LOW POWER FEATURES**

- PASR (Partial Array Self Refresh)
- AUTO TCSR (Temperature Compensated Self Refresh)
- DS (Drive Strength)
- DPD (Deep Power Down): DPD is an optional feature, so please contact Hynix office for the DPD feature

● **INPUT CLOCK**

- Differential clock inputs (CK, $\overline{CK}$)

● **Data MASK**

- DM0 ~ DM3: Input mask signals for write data
- DM masks write data-in at the both rising and falling edges of the data strobe

● **MODE RERISTER SET, EXTENDED MODE REGISTER SET and STATUS REGISTER READ**

- Keep to the JEDEC Standard regulation (Low Power DDR SDRAM)

● **CAS LATENCY**

- Programmable CAS latency 2 or 3 supported

● **BURST LENGTH**

- Programmable burst length 2 / 4 / 8 with both sequential and interleave mode

● **AUTO PRECHARGE**

- Option for each burst access

● **AUTO REFRESH AND SELF REFRESH MODE**

● **CLOCK STOP MODE**

- Clock stop mode is a feature supported by Mobile DDR SDRAM.
- Keep to the JEDEC Standard regulation

● **INITIALIZING THE MOBILE DDR SDRAM**

- Occurring at device power up or interruption of device power

● **PACKAGE**

- H5MS262(53)2JFR: 90 Ball FBGA, Lead & Halogen free

● **ADDRESS TABLE**

Part Number	Page Size	Row Address	Column Address
H5MS2622JFR	2KByte	A0 ~ A11	A0 ~ A8
H5MS2532JFR	1KByte	A0 ~ A12	A0 ~ A7

DESCRIPTION

The Hynix H5MS262(53)2JFR Series is 268,435,456-bit CMOS Low Power Double Data Rate Synchronous DRAM (Mobile DDR SDRAM), ideally suited for mobile applications which use the battery such as PDAs, 2.5G and 3G cellular phones with internet access and multimedia capabilities, mini-notebook, hand-held PCs. It is organized as 4banks of 2,097,152 x32.

The HYNIX H5MS262(53)2JFR series uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n* prefetch architecture with an interface designed to transfer two data per clock cycle at the I/O pins.

The Hynix H5MS262(53)2JFR Series offers fully synchronous operations referenced to both rising and falling edges of the clock. While all address and control inputs are latched on the rising edges of the CK (Mobile DDR SDRAM operates from a differential clock*: the crossing of CK going HIGH and $\overline{CK}$ going LOW is referred to as the positive edge of CK*), data, data strobe and data mask inputs are sampled on both rising and falling edges of it (*Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK*). The data paths are internally pipelined and 2-bit prefetched to achieve high bandwidth. All input voltage levels are compatible with LVCMOS.

Read and write accesses to the Low Power DDR SDRAM (Mobile DDR SDRAM) are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Low Power DDR SDRAM (Mobile DDR SDRAM) provides for programmable read or write bursts of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAM, the pipelined and multibank architecture of Low Power DDR SDRAM (Mobile DDR SDRAM) allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation times.

The Low Power DDR SDRAM (Mobile DDR SDRAM) also provides for special programmable Self Refresh options which are Partial Array Self Refresh (full, half, quarter and 1/8 and 1/16 array) and Temperature Compensated Self Refresh.

A burst of Read or Write cycles in progress can be interrupted and replaced by a new burst Read or Write command on any cycle (this pipelined design is not restricted by a 2N rule). Only Read bursts in progress with auto precharge disabled can be terminated by a burst terminate command. Burst Terminate command is undefined and should not be used for Read with Autoprecharge enabled and for Write bursts.

The Hynix H5MS262(53)2JFR series has the special Low Power function of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current consumption. Since an internal temperature sensor is implemented, it enables to automatically adjust refresh rate according to temperature without external EMRS command.

Deep Power Down Mode is an additional operating mode for Low Power DDR SDRAM (Mobile DDR SDRAM). This mode can achieve maximum power reduction by removing power to the memory array within Low Power DDR SDRAM (Mobile DDR SDRAM). By using this feature, the system can cut off almost all DRAM power without adding the cost of a power switch and giving up mother-board power-line layout flexibility.

All inputs are LVCMOS compatible. Devices will have a V_{DD} and V_{DDQ} supply of 1.8V (nominal).

The Hynix H5MS262(53)2JFR series is available in the following package:
- **90Ball FBGA [8mm x 13mm, t=1.0mm *max*]**

256Mb Mobile DDR SDRAM ORDERING INFORMATION

Part Number	Clock Frequency	Page Size	Org.	Interface	Operating temperature	Package
H5MS2622JFR-E3M	200MHz(CL3) / 83MHz(CL2)	2KByte	4banks x 2Mb x 32	LVCMOS	Mobile Temp (-30°C ~ 85°C)	Lead & Halogen Free
H5MS2622JFR-J3M	166MHz(CL3) / 83MHz(CL2)					
H5MS2622JFR-K3M	133MHz(CL3) / 83MHz(CL2)					
H5MS2622JFR-L3M	100MHz(CL3) / 66MHz(CL2)					
H5MS2532JFR-E3M	200MHz(CL3) / 83MHz(CL2)	1KByte				
H5MS2532JFR-J3M	166MHz(CL3) / 83MHz(CL2)					
H5MS2532JFR-K3M	133MHz(CL3) / 83MHz(CL2)					
H5MS2532JFR-L3M	100MHz(CL3) / 66MHz(CL2)					

INFORMATION for Hynix KNOWN GOOD DIE

With the advent of Multi-Chip package (MCP), Package on Package (PoP) and System in a Package (SiP) applications, customer demand for Known Good Die (KGD) has increased.

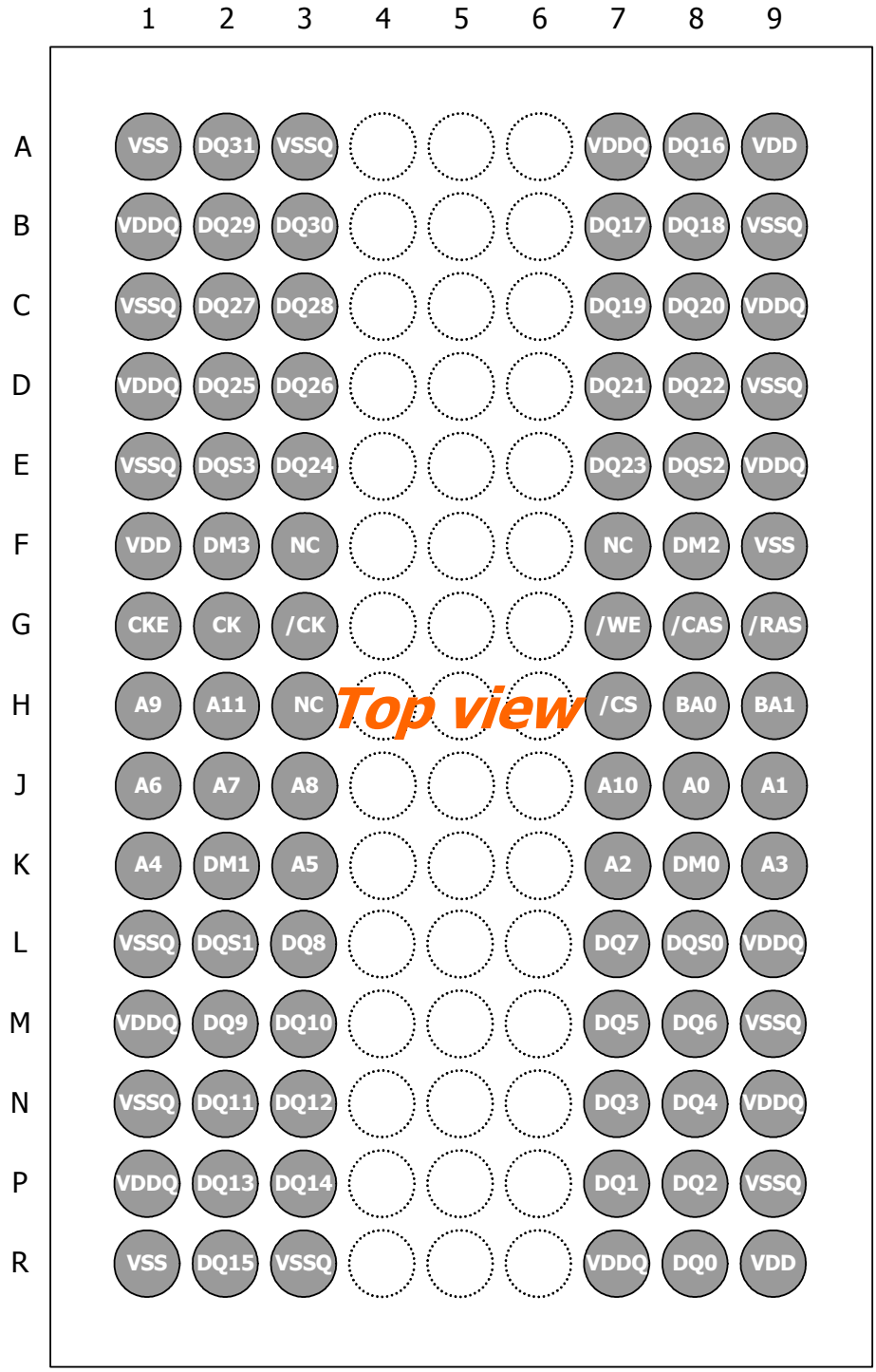
Requirements for smaller form factors and higher memory densities are fueling the need for Wafer-level memory solutions due to their superior flexibility. Hynix Known Good Die (KGD) products can be used in packaging technologies such as systems-in-a-package (SIP) and multi-chip package (MCP) to reduce the board area required, making them ideal for hand-held PCs, and many other portable digital applications.

Hynix Mobile SDRAM will be able to continue its constant effort of enabling the advanced package products of all application customers.

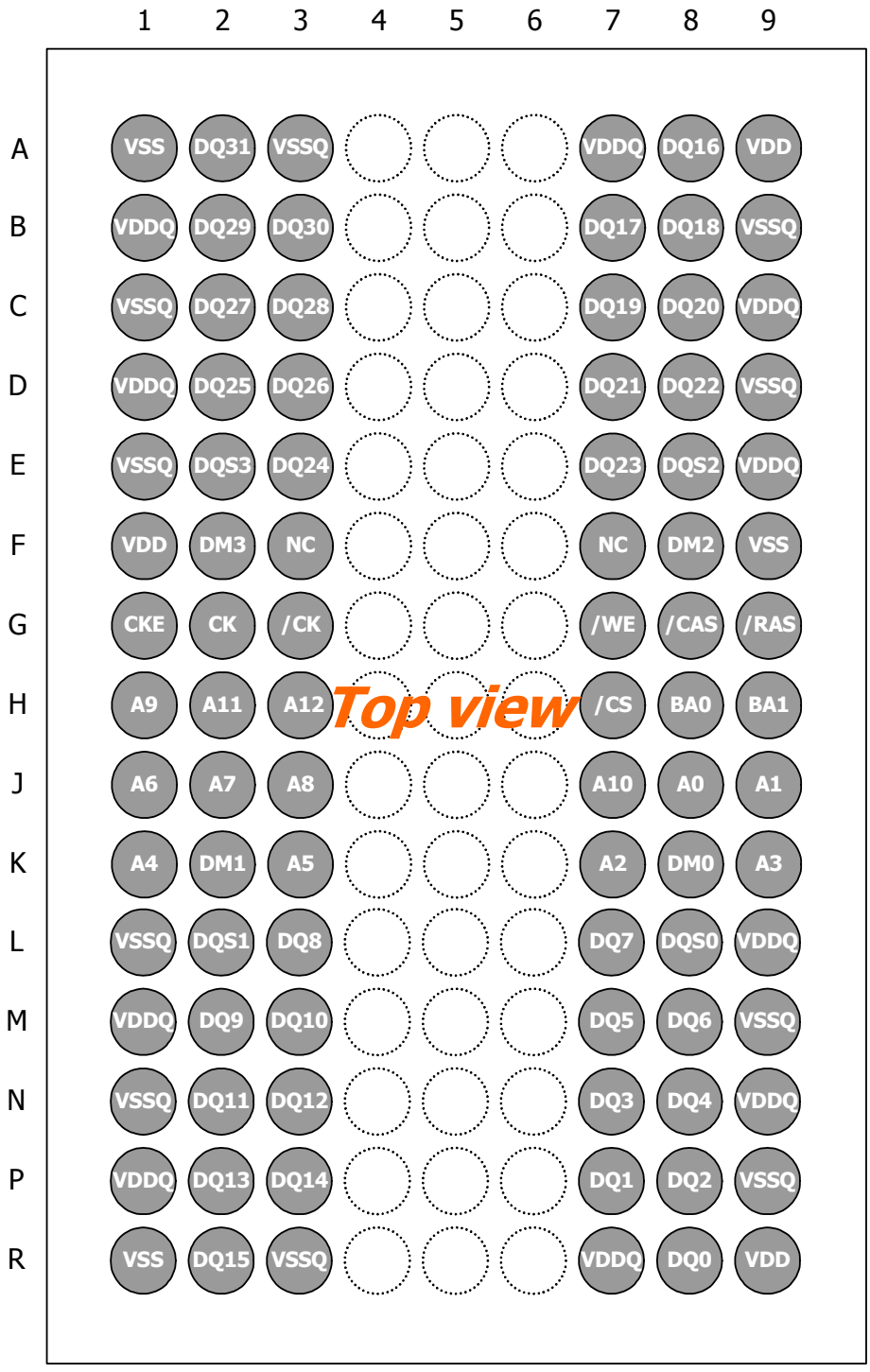
- Please Contact Hynix Office for Hynix KGD product availability and informations.

90Ball FBGA ASSIGNMENT

x32 (2Kbytes) Ballout



x32 (1Kbytes) Ballout

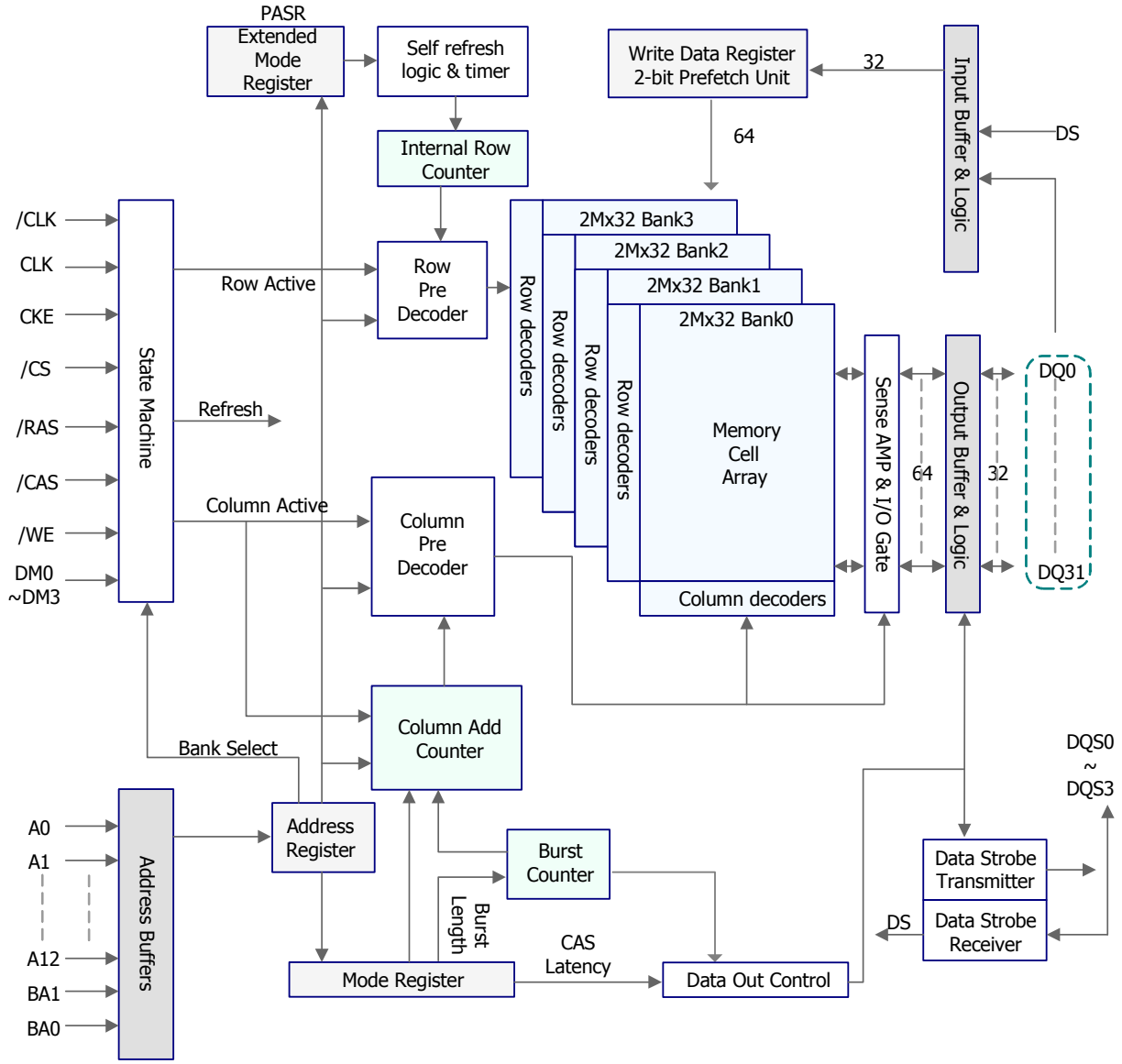


Mobile DDR SDRAM PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	INPUT	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	INPUT	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously.
$\overline{CS}$	INPUT	Chip Select: $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	INPUT	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered
BA0, BA1	INPUT	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS, EMRS or SRR).
A0 ~ A12	INPUT	Address inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a MODE REGISTER SET command. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. For 256Mb (x32, 2Kbytes), Row Address: A0 ~ A11, Column Address: A0 ~ A8 Auto-precharge flag: A10 For 256Mb (x32, 1Kbytes), Row Address: A0 ~ A12, Column Address: A0 ~ A7 Auto-precharge flag: A10
DQ0 ~ DQ31	I/O	Data Bus: data input / output pin
DM0 ~ DM3	INPUT	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled. HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Data Mask pins include dummy loading internally, to match the DQ and DQS loading. For x32 devices, DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
DQS0 ~ DQS3	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data. Used to capture write data. For x32 device, DQS0 corresponds to the data on DQ0-DQ7, DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, and DQS3 corresponds to the data on DQ24-DQ31.
V_{DD}	SUPPLY	Power supply
V_{SS}	SUPPLY	Ground
V_{DDQ}	SUPPLY	I/O Power supply
V_{SSQ}	SUPPLY	I/O Ground
NC	-	No Connect: No internal electrical connection is present.

FUNCTIONAL BLOCK DIAGRAM

2Mbit x 4banks x 32 I/O Mobile DDR SDRAM



REGISTER DEFINITION I

Mode Register Set (MRS) for Mobile DDR SDRAM

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	CAS Latency			BT	Burst Length		

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

REGISTER DEFINITION II

Extended Mode Register Set (EMRS) for Mobile DDR SDRAM

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	DS			0	0	PASR		

DS (Drive Strength)

A7	A6	A5	Drive Strength
0	0	0	Full
0	0	1	Half (Default)
0	1	0	Quarter
0	1	1	Octant
1	0	0	Three-Quarters

PASR (Partial Array Self Refresh)

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks (Default)
0	0	1	Half of Total Bank (BA1=0)
0	1	0	Quarter of Total Bank (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One Eighth of Total Bank (BA1 = BA0 = Row Address MSB=0)
1	1	0	One Sixteenth of Total Bank (BA1 = BA0 = Row Address 2 MSBs=0)
1	1	1	Reserved

REGISTER DEFINITION III

Status Register (SR) for Mobile DDR SDRAM

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Density			-	DW	Refresh Rate			Revision Identification				Manufacturers Identification			
0	0	1	0	1	X	X	X	X[1)]	X[1)]	X[1)]	X[1)]	0	1	1	0

Refresh Rate

DQ10	DQ9	DQ8	Refresh Rate
0	0	x	4[2)]
0	1	0	4
0	1	1	2
1	0	0	1
1	0	1	0.5
1	1	0	0.25
1	1	1	0.25[3)]

DW (Device Width)

DQ11	Device Width
0	16 bits
1	32 bits

Density

DQ15	DQ14	DQ13	Density
0	0	0	128
0	0	1	256
0	1	0	512
0	1	1	1024
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Manufacturers Identification

DQ3	DQ2	DQ1	DQ0	Manufacturer
0	1	1	0	Hynix
x	x	x	x	Reserved or other companies

Note)
1. The revision number starts at '0000' and increments by '0001' each time a change in the manufacturer's specification, IBIS, or process occurs.
2. Low temperature out of range.
3. High temperature out of range - no refresh rate can guarantee functionality.
4. The refresh rate multiplier is based on the memory's temperature sensor.
5. Required average periodic refresh interval = tREFI * multiplier.
6. Status Register is only for Read.
7. To read out Status Register values, BA[1:0] set to 01b and A[11:0] set to all 0 with MRS command followed by Read command with that BA[1:0] and A[11:0] are Don't care.

COMMAND TRUTH TABLE

Function	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10/AP	ADDR	Note
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (Select Bank and activate Row)	L	L	H	H	V	Row	Row	
READ (Select bank and column and start read burst)	L	H	L	H	V	L	Col	
READ with AP (Read Burst with Autoprecharge)	L	H	L	H	V	H	Col	3
WRITE (Select bank and column and start write burst)	L	H	L	L	V	L	Col	
WRITE with AP (Write Burst with Autoprecharge)	L	H	L	L	V	H	Col	3
BURST TERMINATE or enter DEEP POWER DOWN	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate Row in selected bank)	L	L	H	L	V	L	X	6
PRECHARGE ALL (Deactivate rows in all Banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7,8,9
MODE REGISTER SET	L	L	L	L	V	Op code		10

DM TRUTH TABLE

Function	DM	DQ	Note
Write Enable	L	Valid	11
Write Inhibit	H	X	11

Note:
1. All states and sequences not shown are illegal or reserved.
2. DESLECT and NOP are functionally interchangeable.
3. Autoprecharge is non-persistent. A10 High enables Autoprecharge, while A10 Low disables Autoprecharge
4. Burst Terminate applies to only Read bursts with auto precharge disabled. This command is undefined and should not be used for Read with Autoprecharge enabled, and for Write bursts.
5. This command is BURST TERMINATE if CKE is High and DEEP POWER DOWN entry if CKE is Low.
6. If A10 is low, bank address determines which bank is to be precharged. If A10 is high, all banks are precharged and BA0-BA1 are don't care.
7. This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.
8. All address inputs and I/O are "don't care" except for CKE. Internal refresh counters control Bank and Row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select among MRS, EMRS and SRR.
11. Used to mask write data, provided coincident with the corresponding data.
12. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.

CKE TRUTH TABLE

CKEn-1	CKEn	Current State	COMMAND*n*	ACTION*n*	Note
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	L	Deep Power Down	X	Maintain Deep Power Down	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5,6,9
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5,7,10
L	H	Deep Power Down	NOP or DESELECT	Exit Deep Power Down	5,8
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh entry	
H	L	All Banks Idle	BURST TERMINATE	Enter Deep Power Down	
H	H	See the other Truth Tables			

Note:
1. CKEn is the logic state of CKE at clock edge *n*; CKE*n*-1 was the state of CKE at the previous clock edge.
2. Current state is the state of LP DDR immediately prior to clock edge *n*.
3. COMMAND*n* is the command registered at clock edge n, and ACTION*n* is the result of COMMAND*n*.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (t_{XSR}) should elapse before a command other than NOP or DESELECT is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least one time during the t_{XP} period.
10. The clock must toggle at least once during the t_{XSR} time.

CURRENT STATE BANK*n* TRUTH TABLE (COMMAND TO BANK *n*)

Current State	Command					Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	L	L	H	H	ACTIVE	Select and activate row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MODE REGISTER SET	Mode register set	10
	L	L	H	H	PRECHARGE	No action if bank is idle	
Row Active	L	H	L	H	READ	Select Column & start read burst	
	L	H	L	L	WRITE	Select Column & start write burst	
	L	L	H	L	PRECHARGE	Deactivate Row in bank (or banks)	4
Read (without Auto recharge)	L	H	L	H	READ	Truncate Read & start new Read burst	5,6
	L	H	L	L	WRITE	Truncate Read & start new Write burst	5,6,13
	L	L	H	L	PRECHARGE	Truncate Read, start Precharge	
	L	H	H	L	BURST TERMINATE	Burst terminate	11
Write (without Auto precharge)	L	H	L	H	READ	Truncate Write & start new Read burst	5,6,12
	L	H	L	L	WRITE	Truncate Write & start new Write burst	5,6
	L	L	H	L	PRECHARGE	Truncate Write, start Precharge	12

Note:
1. The table applies when both CKE*n*-1 and CKE*n* are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE Burst with auto precharge is enabled.
6. The new Read or Write command could be auto precharge enabled or auto precharge disabled.

7. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met.
   No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank.
   DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table3, and according to Truth Table 4.
   Precharging: Starts with the registration of a PRECHARGE command and ends when tRP is met.
   Once tRP is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met.
   Once tRCD is met, the bank will be in the "row active" state.
   Read with AP Enabled: Starts with the registration of the READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

9. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied to each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met.
   Once tRFC is met, the LP DDR will be in an "all banks idle" state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met.
   Once tMRD is met, the LP DDR will be in an "all banks idle" state.
   Precharging All: Starts with the registration of a PRECHARGE ALL command and ends when tRP is met.
   Once tRP is met, the bank will be in the idle state.
10. Not bank-specific; requires that all banks are idle and no bursts are in progress.
11. Not bank-specific. BURST TERMINATE affects the most recent READ burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst terminate must be used to end the READ prior to asserting a WRITE command.

CURRENT STATE BANK*n* TRUTH TABLE (COMMAND TO BANK *m*)

Current State	Command					Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Pre-charging	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8,9
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8
	L	L	H	L	PRECHARGE	Precharge	

Note:
1. The table applies when both CKE*n*-1 and CKE*n* are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
5. Read with AP enabled and Write with AP enabled: The read with Autoprecharge enabled or Write with Autoprecharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with Auto precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period, of the Read with Autoprecharge enabled or Write with Autoprecharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
6. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
8. READs or WRITEs listed in the Command column include READs and WRITEs with AUTO PRECHARGE enabled and READs and WRITEs with AUTO PRECHARGE disabled.
9. Requires appropriate DM masking.
10. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Operating Case Temperature	TC	-30 ~ 85	°C
Storage Temperature	TSTG	-55 ~ 150	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.3 ~ VDDQ+0.3	V
Voltage on VDD relative to VSS	VDD	-0.3 ~ 2.7	V
Voltage on VDDQ relative to VSS	VDDQ	-0.3 ~ 2.7	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	0.7	W

AC and DC OPERATING CONDITIONS

OPERATING CONDITION

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	1.7	1.8	1.95	V	1
I/O Supply Voltage	VDDQ	1.7	1.8	1.95	V	1
Operating Case Temperature	TC	-30		85	°C	

CLOCK INPUTS (CK, $\overline{CK}$)

Parameter	Symbol	Min	Max	Unit	Note
DC Input Voltage	VIN	-0.3	VDDQ+0.3	V	
DC Input Differential Voltage	VID(DC)	0.4*VDDQ	VDDQ+0.6	V	2
AC Input Differential Voltage	VID(AC)	0.6*VDDQ	VDDQ+0.6	V	2
AC Differential Crosspoint Voltage	VIX	0.4*VDDQ	0.6*VDDQ	V	3

Address And Command Inputs (A0~An, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)

Parameter	Symbol	Min	Max	Unit	Note
Input High Voltage	VIH	0.8*VDDQ	VDDQ+0.3	V	
Input Low Voltage	VIL	-0.3	0.2*VDDQ	V	

Data Inputs (DQ, DM, DQS)

Parameter	Symbol	Min	Max	Unit	Note
DC Input High Voltage	VIHD(DC)	0.7*VDDQ	VDDQ+0.3	V	
DC Input Low Voltage	VILD(DC)	-0.3	0.3*VDDQ	V	
AC Input High Voltage	VIHD(AC)	0.8*VDDQ	VDDQ+0.3	V	
AC Input Low Voltage	VILD(AC)	-0.3	0.2*VDDQ	V	

Data Outputs (DQ, DQS)

Parameter	Symbol	Min	Max	Unit	Note
DC Output High Voltage (IOH = -0.1mA)	VOH	0.9*VDDQ	-	V	
DC Output Low Voltage (IOL = 0.1mA)	VOL	-	0.1*VDDQ	V	

Leakage Current

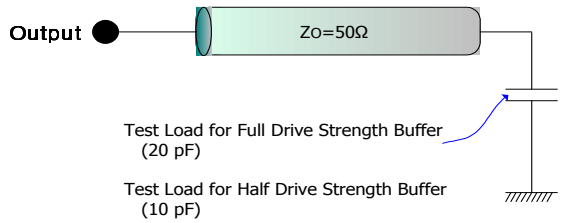
Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	4
Output Leakage Current	ILO	-1.5	1.5	uA	5

Note:
1. All voltages are referenced to VSS = 0V and VSSQ must be same potential and VDDQ must not exceed the level of VDD.
2. VID(DC) and VID(AC) are the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
3. The value of VIX is expected to be 0.5*VDDQ and must track variations in the DC level of the same.
4. VIN = 0 to 1.8V. All other pins are not tested under VIN=0V.
5. DOUT is disabled. VOUT= 0 to 1.95V.

AC OPERATING TEST CONDITION

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	0.8*VDDQ/0.2*VDDQ	V	
Input Timing Measurement Reference Level Voltage	Vtrip	0.5*VDDQ	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	0.5*VDDQ	V	
Output Load Capacitance for Access Time Measurement	CL		pF	1

Note: 1. The circuit shown on the right represents the timing load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design and characterization. Use of IBIS or other simulation tools for system design validation is suggested.



Input / Output Capacitance

Parameter	Symbol	Speed		Unit	Note
		Min	Max		
Input capacitance, CK, $\overline{CK}$	CCK	1.5	3.5	pF	
Input capacitance delta, CK, $\overline{CK}$	CDCK	-	0.25	pF	
Input capacitance, all other input-only pins	CI	1.5	3.0	pF	
Input capacitance delta, all other input-only pins	CDI	-	0.5	pF	
Input/output capacitance, DQ, DM, DQS	CIO	2.0	4.5	pF	4
Input/output capacitance delta, DQ, DM, DQS	CDIO	-	0.5	pF	4

Note:
1. These values are guaranteed by design and are tested on a sample base only.
2. These capacitance values are for single monolithic devices only. Multiple die packages will have parallel capacitive loads.
3. Input capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. VDD, VDDQ are applied and all other pins (except the pin under test) floating. DQ's should be in high impedance state. This may be achieved by pulling CKE to low level.
4. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS and DM in the system.

Mobile DDR OUTPUT SLEW RATE CHARACTERRISTICS

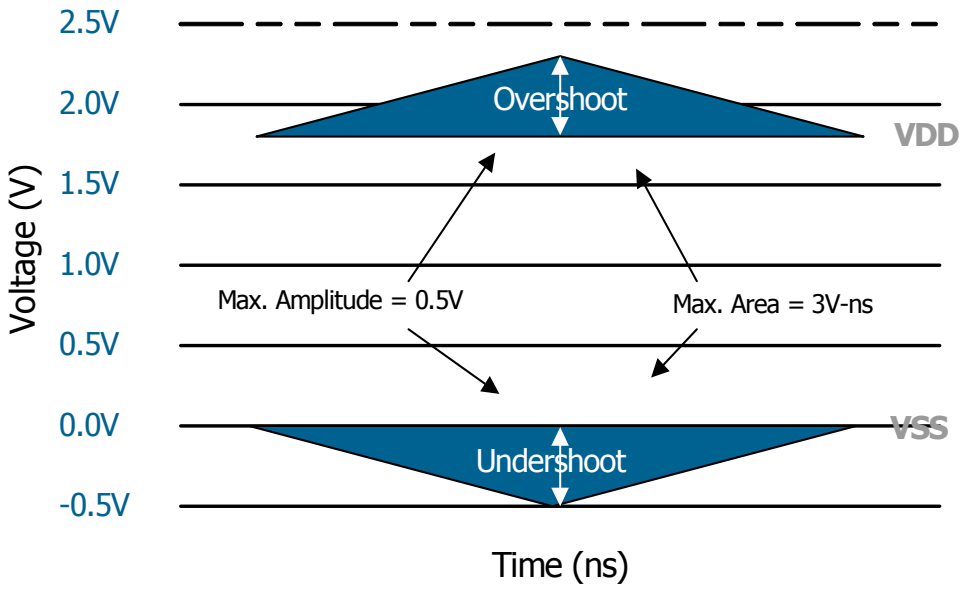
Parameter	Min	Max	Unit	Note
Pull-up and Pull-Down Slew Rate for Full Strength Driver	0.7	2.5	V/ns	1, 2
Pull-up and Pull-Down Slew Rate for Half Strength Driver	0.3	1.0	V/ns	1, 2
Output Slew Rate Matching ratio (Pull-up to Pull-down)	0.7	1.4	-	3

Note:
1. Measured with a test load of 20pF connected to VSSQ
2. Output slew rate for rising edge is measured between VILD(DC) to VIHD(AC) and for falling edge between VIHD(DC) to VILD(AC)
3. The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

Mobile DDR AC OVERSHOOT / UNDERSHOOT SPECIFICATION

Parameter	Specification
Maximum peak amplitude allowed for overshoot	0.5V
Maximum peak amplitude allowed for undershoot	0.5V
The area between overshoot signal and VDD must be less than or equal to	3V-ns
The area between undershoot signal and GND must be less than or equal to	3V-ns

Note:
1. This specification is intended for devices with no clamp protection and is guaranteed by design.



DC CHARACTERISTICS

Parameter	Symbol	Test Condition	Max					Unit	Note
			DDR 400	DDR 370	DDR 333	DDR 266	DDR 200		
Operating one bank active-precharge current	IDD0	tRC = tRC(min); tCK = tCK(min); CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	60	55	50	45	45	mA	1
Precharge power-down standby current	IDD2P	all banks idle; CKE is LOW; $\overline{CS}$ is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	0.3					mA	
Precharge power-down standby current with clock stop	IDD2PS	all banks idle; CKE is LOW; $\overline{CS}$ is HIGH; CK = LOW; $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	0.3					mA	
Precharge non power-down standby current	IDD2N	all banks idle; CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	12					mA	
Precharge non power-down standby current with clock stop	IDD2NS	all banks idle; CKE is HIGH; $\overline{CS}$ is HIGH; CK = LOW; $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	8						
Active power-down standby current	IDD3P	one bank active; CKE is LOW; $\overline{CS}$ is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	5					mA	
Active power-down standby current with clock stop	IDD3PS	one bank active; CKE is LOW; $\overline{CS}$ is HIGH; CK = LOW; $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	3						
Active non power-down standby current	IDD3N	one bank active; CKE is HIGH; $\overline{CS}$ is HIGH; tCK = tCK*(min);* address and control inputs are SWITCHING; data bus inputs are STABLE	15					mA	
Active non power-down standby current with clock stop	IDD3NS	one bank active; CKE is HIGH; $\overline{CS}$ is HIGH; CK = LOW; $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	10					mA	
Operating burst r ead current	IDD4R	one bank active; BL=4; CL=3; tCK = tCK*(min)*; continuous read bursts; IOUT=0mA; address inputs are SWITCHING, 50% data change each burst transfer	120	110	105	95	95	mA	1
Operating burst write current	IDD4W	one bank active; BL=4; tCK=tCK*(min)*; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	120	110	105	95	95	mA	
Auto Refresh Current	IDD5	tRC=tRFC*(min)*; tCK=tCK*(min);* burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	100					mA	
Self Refresh Current	IDD6	CKE is LOW; CK=LOW; $\overline{CK}$=HIGH; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	See Next Page					uA	2
Deep Power Down Current	IDD8	Address, control and data bus inputs are STABLE	10					uA	4

Note:
1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is 1V/ns.
3. Definitions for IDD:
   LOW is defined as $V_{IN} \leq 0.1 * V_{DDQ}$
   HIGH is defined as $V_{IN} \geq 0.9 * V_{DDQ}$
   STABLE is defined as inputs stable at a HIGH or LOW level
   SWITCHING is defined as
   - address and command: inputs changing between HIGH and LOW once per two clock cycles
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle
     DM and DQS are STABLE
4. Please contact Hynix office for more information and ability for DPD operation. Deep Power Down operation is a hynix optional function.
5. All IDD values are guaranteed by full range of operating voltage and temperature.
   VDD, VDDQ = 1.7V ~ 1.95V. Temperature = -30°C ~ +85°C

DC CHARACTERISTICS - IDD6

Temp. (°C)	Memory Array			Unit
	4 Banks	2 Banks	1 Bank	
45	200	150	130	uA
85	320	280	250	uA

Note:
1. Related numerical values in this 45°C are examples for reference sample value only.
2. With a on-chip temperature sensor, auto temperature compensated self refresh will automatically adjust the interval of self-refresh operation according to case temperature variations.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted) (Sheet 1 of 2)

Parameter		Symbol	DDR400		DDR370		DDR333		DDR266		DDR200		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ Output Access Time (from CK, $\overline{CK}$)		tAC	2.0	5.0	2.0	5.0	2.0	5.0	2.5	6.0	2.5	7.0	ns	
DQS Output Access Time (from CK, $\overline{CK}$)		tDQSCK	2.0	5.0	2.0	5.0	2.0	5.0	2.5	6.0	2.5	7.0	ns	
Clock High-level Width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock Low-level Width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock Half Period		tHP	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	ns	1,2
System Clock Cycle Time	CL = 3	tCK3	5.0	-	5.4	-	6.0	-	7.5	-	10	-	ns	3
	CL = 2	tCK2	12	-	12		12		12	-	15	-	ns	
DQ and DM Input Setup Time		tDS	0.48	-	0.54		0.6		0.8		1.1		ns	4,5,6
DQ and DM Input Hold Time		tDH	0.48	-	0.54		0.6		0.8		1.1		ns	4,5,6
DQ and DM Input Pulse Width		tDIPW	1.4	-	1.6	-	1.6	-	1.6	-	2.2	-	ns	7
Address and Control Input Setup Time		tIS	0.9	-	1.0		1.1		1.3		1.5		ns	6,8,9
Address and Control Input Hold Time		tIH	0.9	-	1.0		1.1		1.3		1.5		ns	6,8,9
Address and Control Input Pulse Width		tIPW	2.2	-	2.2	-	2.2	-	2.6	-	3.0	-	ns	7
DQ & DQS Low-impedance time from CK, $\overline{CK}$		tLZ	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	ns	10
DQ & DQS High-impedance time from CK, $\overline{CK}$		tHZ	-	5.0		5.0		5.0		6.0		7.0	ns	10
DQS - DQ Skew		tDQSQ	-	0.4		0.45		0.5		0.6		0.7	ns	11
DQ / DQS output hold time from DQS		tQH	tHP - tQHS	-	tHP - tQHS		tHP - tQHS		tHP - tQHS		tHP - tQHS		ns	2
Data Hold Skew Factor		tQHS	-	0.5		0.5		0.65		0.75		1.0	ns	2
Write Command to 1st DQS Latching Transition		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS Input High-Level Width		tDQSH	0.4	-	0.4		0.4		0.4		0.4		tCK	
DQS Input Low-Level Width		tDQSL	0.4	-	0.4		0.4		0.4		0.4		tCK	
DQS Falling Edge of CK Setup Time		tDSS	0.2	-	0.2		0.2		0.2		0.2		tCK	
DQS Falling Edge Hold Time from CK		tDSH	0.2	-	0.2		0.2		0.2		0.2		tCK	

AC CHARACTERISTICS (AC operating conditions unless otherwise noted) (Sheet 2 of 2)

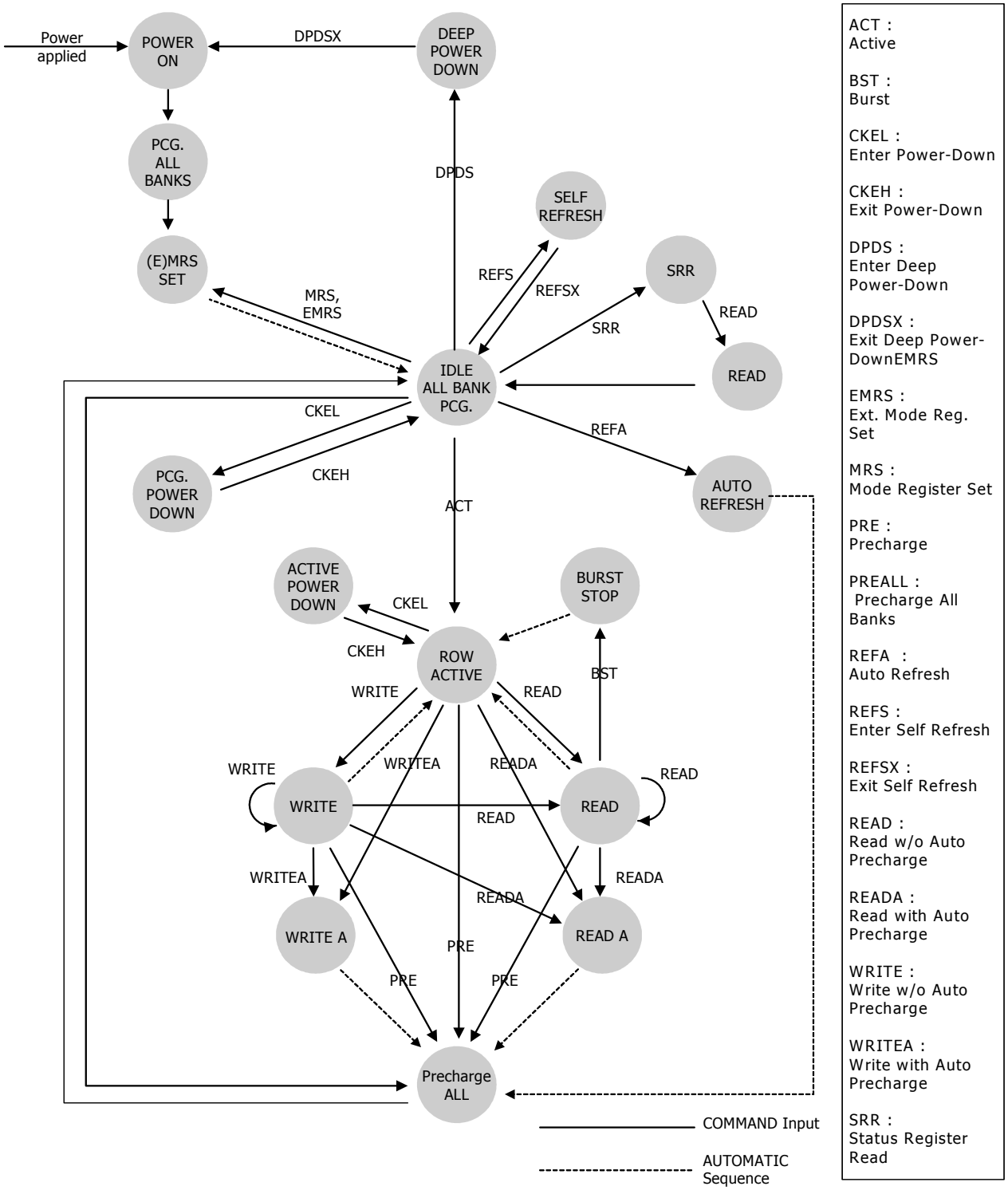
Parameter		Symbol	DDR400		DDR370		DDR333		DDR266		DDR200		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
MODE REGISTER SET Command Period		tMRD	2	-	2	-	2	-	2	-	2	-	tCK	
MRS(SRR) to Read Command Period		tSRR	2	-	2	-	2	-	2	-	2	-	tCK	
Minimum Time between Status Register Read to Next Valid Command		tSRC	CL+1	-	CL+1	-	CL+1	-	CL+1	-	CL+1	-	tCK	
Write Preamble Setup Time		tWPRES	0	-	0	-	0	-	0	-	0	-	ns	12
Write Postamble		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	13
Write Preamble		tWPRE	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	tCK	
Read Preamble	CL = 3	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	14
	CL = 2	tRPRE	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	tCK	14
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
ACTIVE to PRECHARGE Command Period		tRAS	40	70,000	42	70,000	42	70,000	45	70,000	50	70,000	ns	
ACTIVE to ACTIVE Command Period		tRC	55	-	58.2	-	60	-	75	-	80	-	ns	
AUTO REFRESH to ACTIVE/AUTO REFRESH Command Period		tRFC	72	-	72	-	72	-	72	-	72	-	ns	
ACTIVE to READ or WRITE Delay		tRCD	15	-	16.2	-	18	-	22.5	-	30	-	ns	15
PRECHARGE Command Period		tRP	15	-	16.2	-	18	-	22.5	-	30	-	ns	15
ACTIVE Bank *A* to ACTIVE Bank *B* Delay		tRRD	10	-	10.8	-	12	-	15	-	15	-	ns	
WRITE Recovery Time		tWR	15	-	15	-	15	-	15	-	15	-	ns	
Auto Precharge Write Recovery + Precharge Time		tDAL	(tWR/tCK) + (tRP/tCK)										tCK	16
Internal Write to Read Command Delay		tWTR	1	-	1	-	1	-	1	-	1	-	tCK	
Self Refresh Exit to next valid Command Delay		tXSR	120	-	120	-	120	-	120	-	120	-	ns	
Exit Power Down to next valid Command Delay		tXP	tIS + 2CLK	-	tIS + 1CLK	-	tIS + 1CLK	-	tIS + 1CLK	-	tIS + 1CLK	-	ns	
CKE *min.* Pulse Width (High and Low)		tCKE	1	-	1	-	1	-	1	-	1	-	tCK	
Average Periodic Refresh Interval (2Kbytes)		tREFI	-	15.6	-	15.6	-	15.6	-	15.6	-	15.6	us	17
Average Periodic Refresh Interval (1Kbytes)		tREFI	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	us	17
Refresh Period		tREF	-	64	-	64	-	64	-	64	-	64	ms	

Note:

1. Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH})
2. t_{QH} = t_{HP} - t_{QHS}, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
3. The only time that the clock frequency is allowed to change is during clock stop, power-down or self-refresh modes.
4. The transition time for DQ, DM and DQS inputs is measured between V_{IL}(DC) to V_{IH}(AC) for rising input signals, and V_{IH}(DC) to V_{IL}(AC) for falling input signals.
5. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
6. Input slew rate ≥ 1.0 V/ns.
7. These parameters guarantee device timing but they are not necessarily tested on each device.
8. The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
9. A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for this parameter.
10. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
11. t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
12. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
13. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
14. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
15. Speed bin (CL-t_{RCD}-t_{RP}) = 3-3-3
16. t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK}): for each of the terms above, if not already an integer, round to the next higher integer.
17. A maximum of eight Refresh commands can be posted to any given Low Power DDR SDRAM (Mobile DDR SDRAM), meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8*t_{REFI}.
18. All AC parameters are guaranteed by full range of operating voltage and temperature.
    VDD, VDDQ = 1.7V ~ 1.95V. Temperature = -30°C ~ +85°C.

Mobile DDR SDRAM OPERATION

State Diagram



ACT :
Active

BST :
Burst

CKEL :
Enter Power-Down

CKEH :
Exit Power-Down

DPDS :
Enter Deep Power-Down

DPDSX :
Exit Deep Power-DownEMRS

EMRS :
Ext. Mode Reg. Set

MRS :
Mode Register Set

PRE :
Precharge

PREALL :
Precharge All Banks

REFA :
Auto Refresh

REFS :
Enter Self Refresh

REFSX :
Exit Self Refresh

READ :
Read w/o Auto Precharge

READA :
Read with Auto Precharge

WRITE :
Write w/o Auto Precharge

WRITEA :
Write with Auto Precharge

SRR :
Status Register Read

DESELECT

The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the Mobile DDR SDRAM. The Mobile DDR SDRAM is effectively deselected. Operations already in progress are not affected.

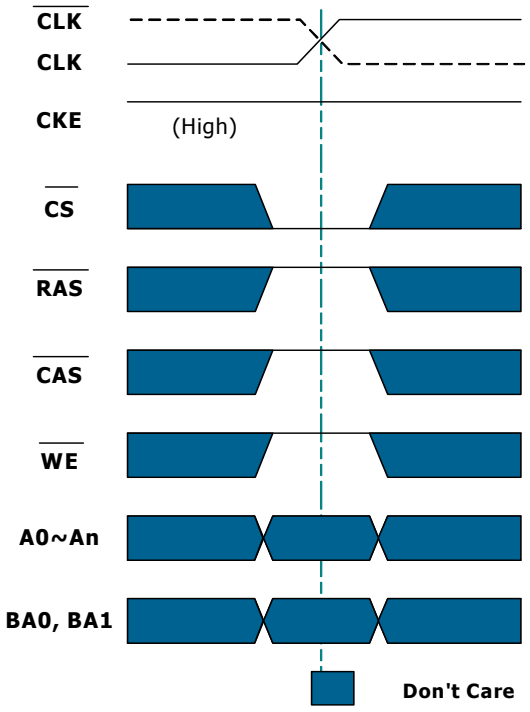
NO OPERATION

The NO OPERATION (NOP) command is used to perform a NOP to a Mobile DDR SDRAM that is selected ($\overline{CS}$ = Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. (see to next figure)

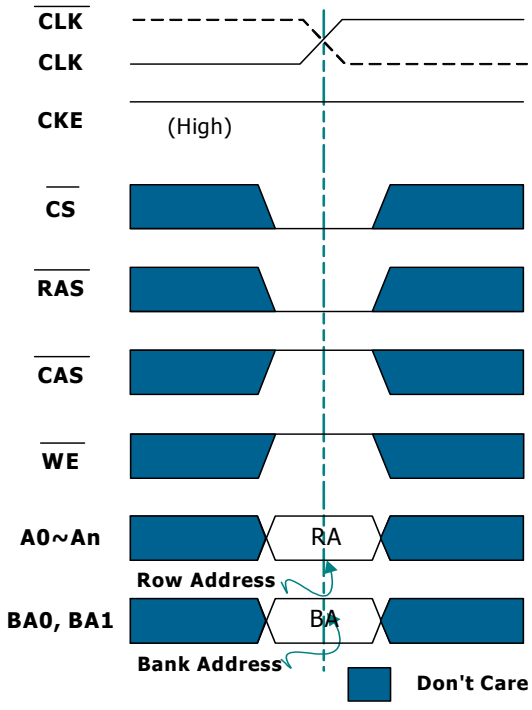
ACTIVE

The Active command is used to activate a row in a particular bank for a subsequent Read or Write access. The value of the BA0,BA1 inputs selects the bank, and the address provided on A0-An (the highest address bit) selects the row. (see to next figure)

Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be opened. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.
The row remains active until a PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command is issued to the bank.
A PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command must be issued before opening a different row in the same bank.



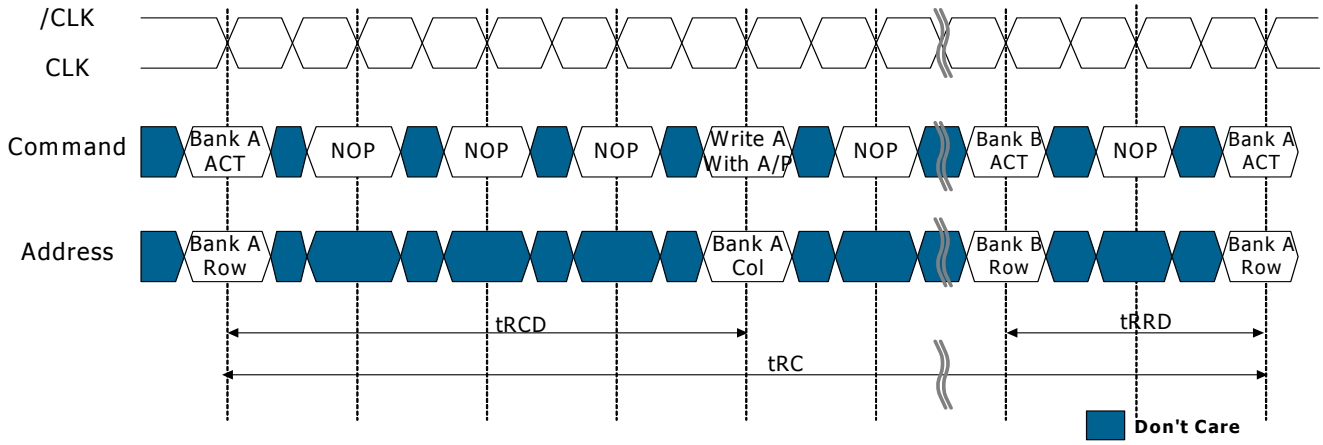
NOP Command



ACTIVE Command

Once a row is Open (with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (*MIN*) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharge). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

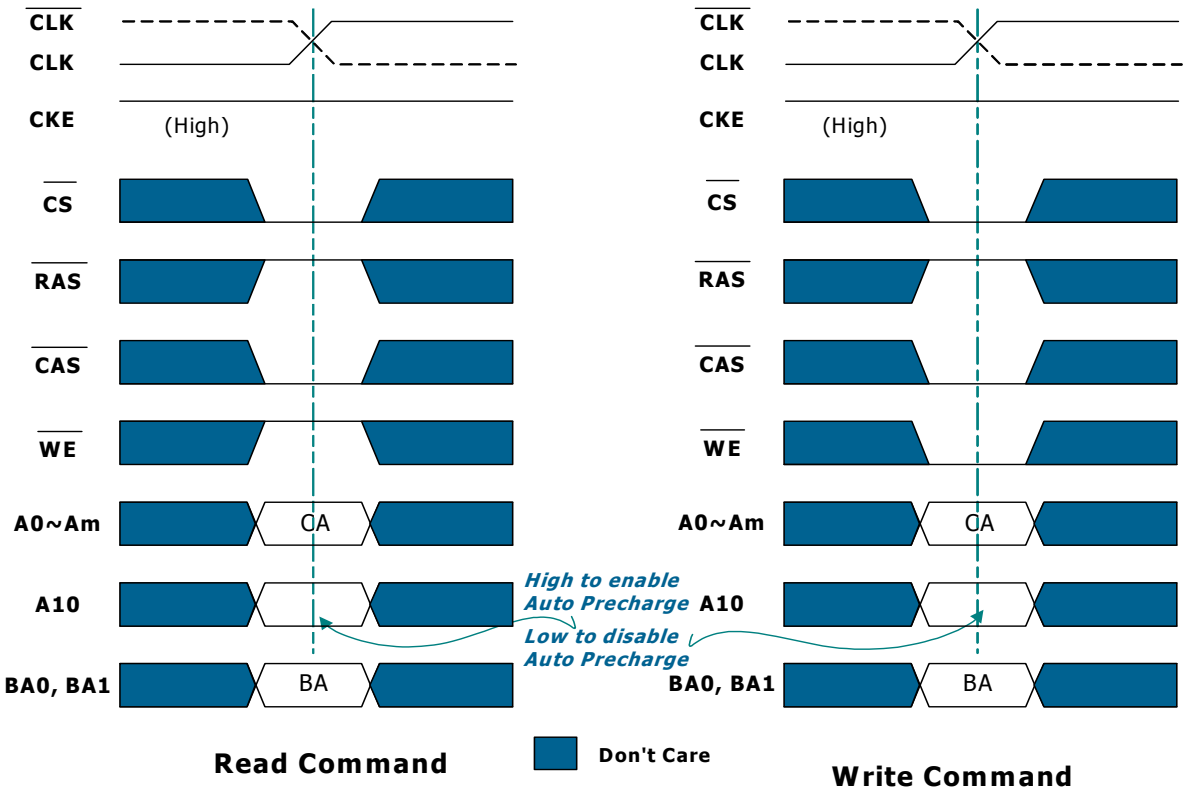


Once a row is Open(with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

READ / WRITE COMMAND

The READ command is used to initiate a Burst Read to an active row. The value of BA0 and BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent access. The valid data-out elements will be available CAS latency after the READ command is issued. The Mobile DDR drives the DQS during read operations. The initial low state of the DQS is known as the read preamble and the last data-out element is coincident with the read postamble. DQS is edge-aligned with read data. Upon completion of a burst, assuming no new READ commands have been initiated, the I/O's will go high-Z.

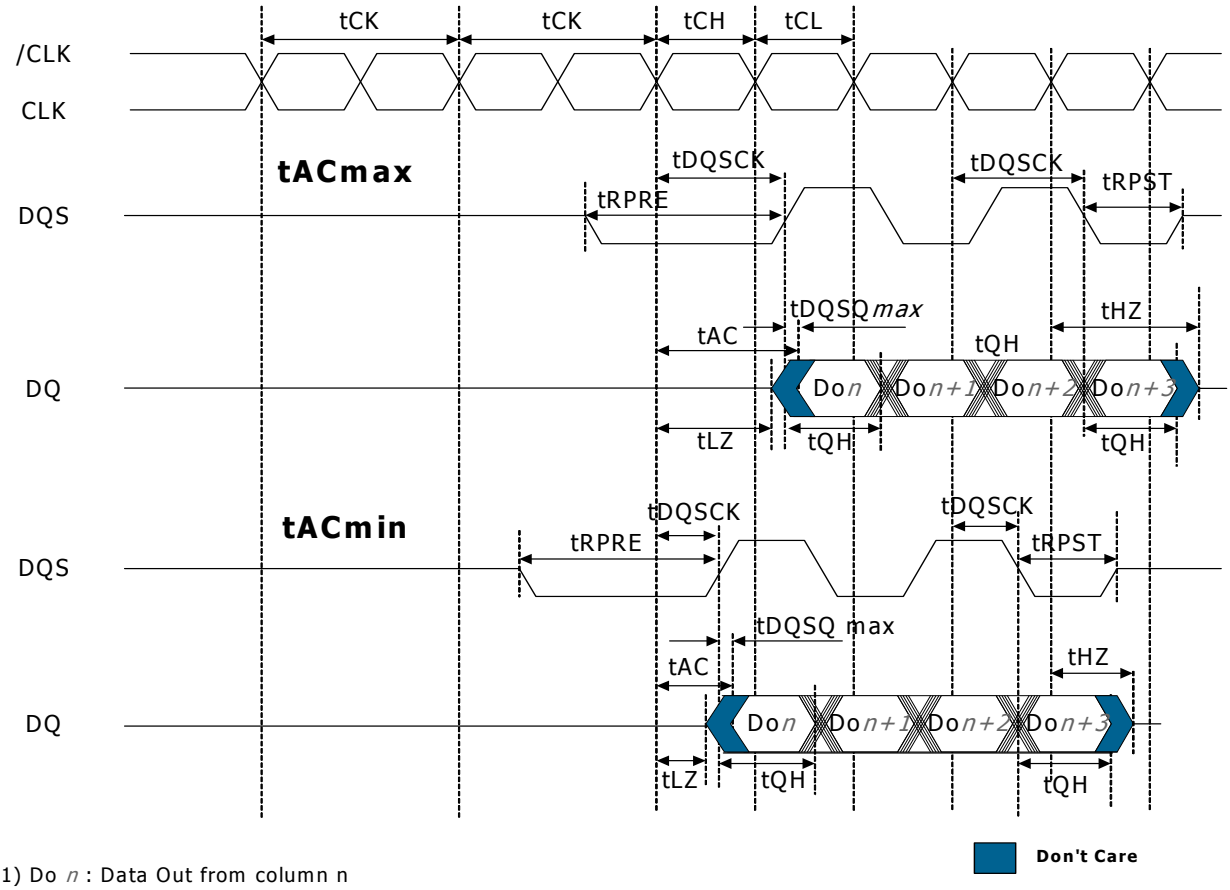
The WRITE command is used to initiate a Burst Write access to an active row. The value of BA0, BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used.If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent access. Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to the memory; if the DM signal is registered high, the corresponding data-inputs will be ignored, and a write will not be executed to that byte/column location. The memory controller drives the DQS during write operations. The initial low state of the DQS is known as the write preamble and the low state following the last data-in element is write postamble. Upon completion of a burst, assuming no new commands have been initiated, the I/O's will stay high-Z and any additional input data will be ignored.



READ / WRITE COMMAND

READ

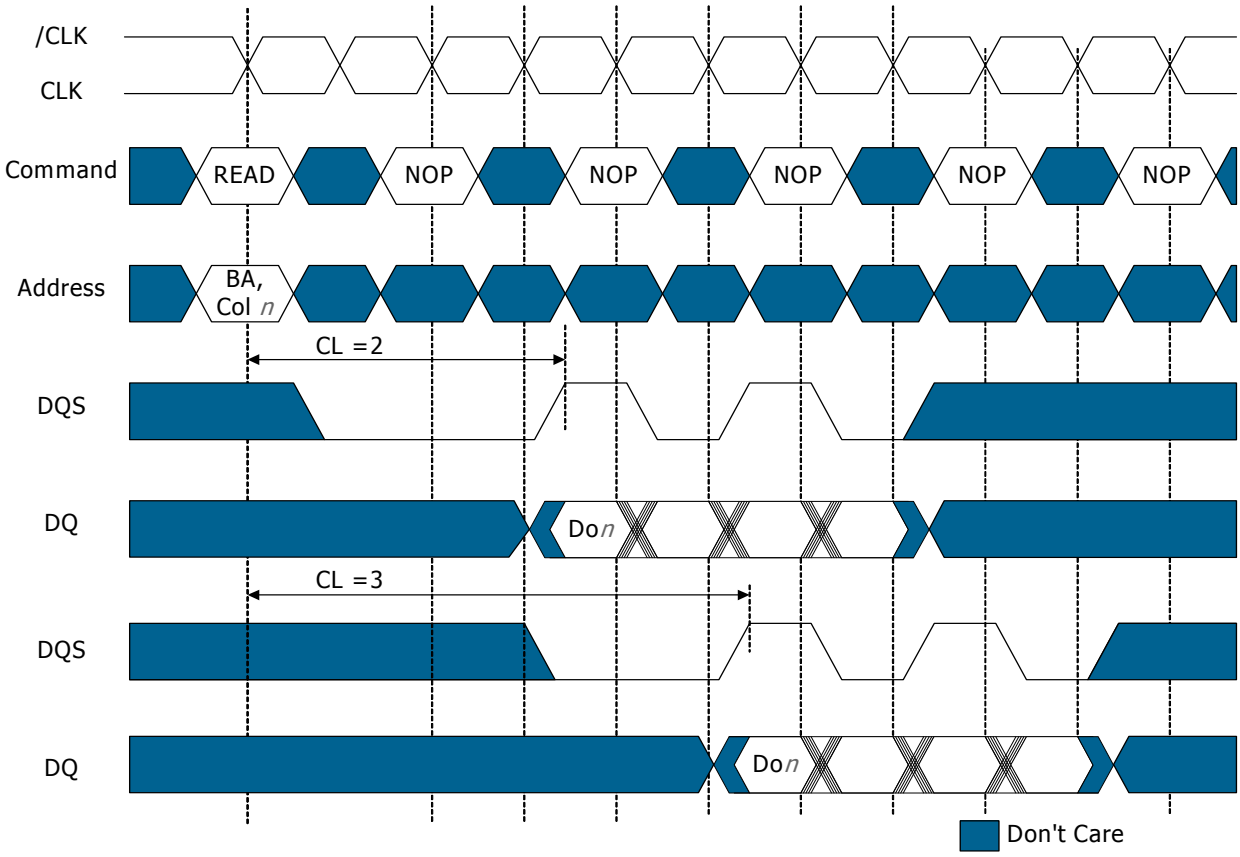
The basic Read timing parameters for DQ are shown next figure (Basic Read Timing Parameters). They apply to all Read operations. During Read bursts, DQS is driven by the Mobile DDR SDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble.



1) Do *n* : Data Out from column n
2) All DQ are vaild tAC after the CK edge
   All DQ are vaild tDQSQ after the DQS edge, regardless of tAC

Basic Read Timing Parameters

The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. This is shown in next figure with a CAS latency of 2 and 3.
Upon completion of a read burst, assuming no other READ command has been initiated, the DQ will go to High-Z.

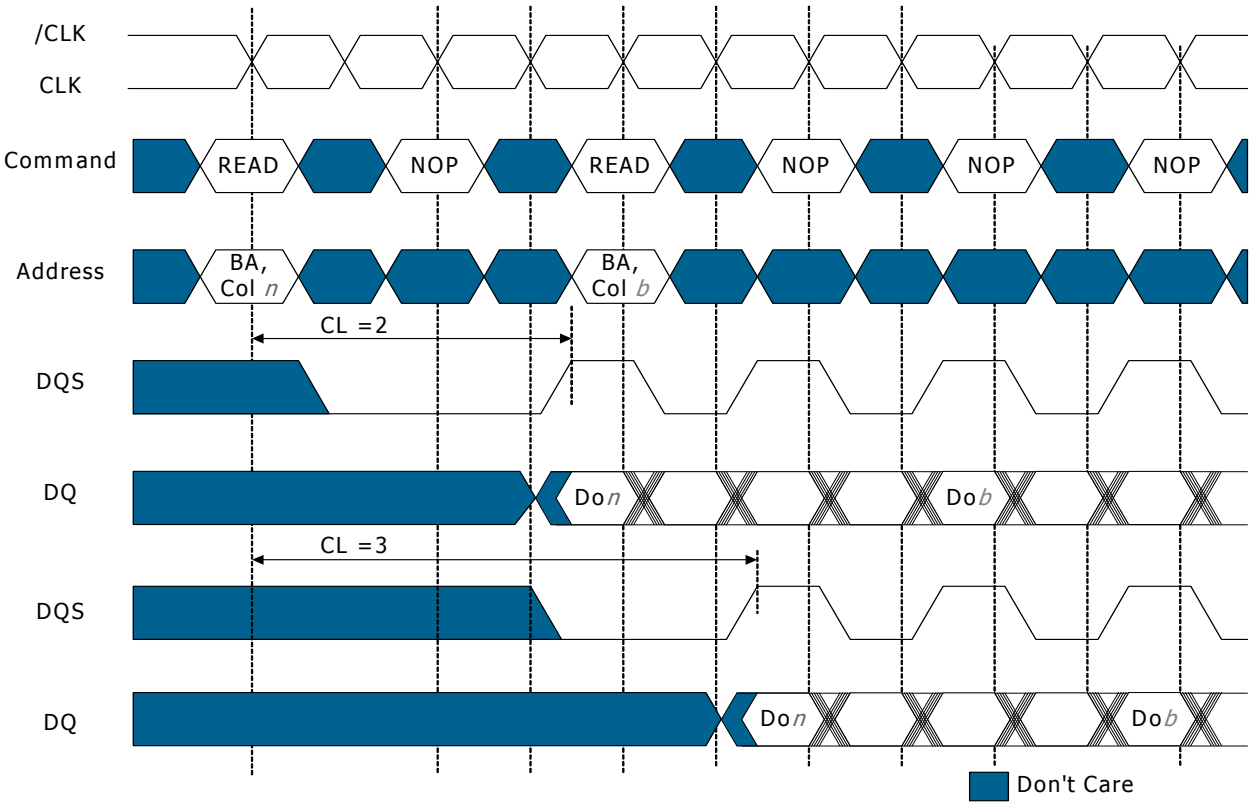


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 4; 3 subseqnent elements of Data Out appear in the programmed order following Do *n*
4) Shown with nominal tAC, tDQSCK and tDQSQ

Read Burst Showing CAS Latency

READ to READ

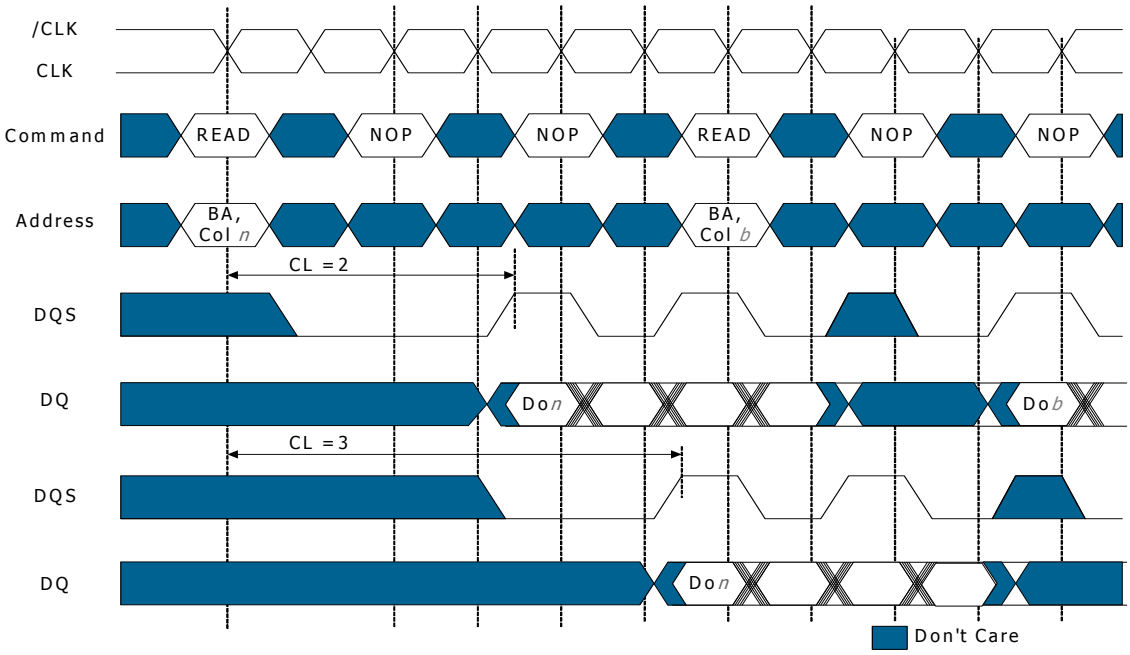
Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n prefetch architecture).



1) Do*n* (or *b*): Data out from column n (or column b)
2) BA, Col *n (b)* = Bank A, Column n (b)
3) Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
4) Read bursts are to an active row in any bank
5) Shown with nominal tAC, tDQSCK and tDQSQ

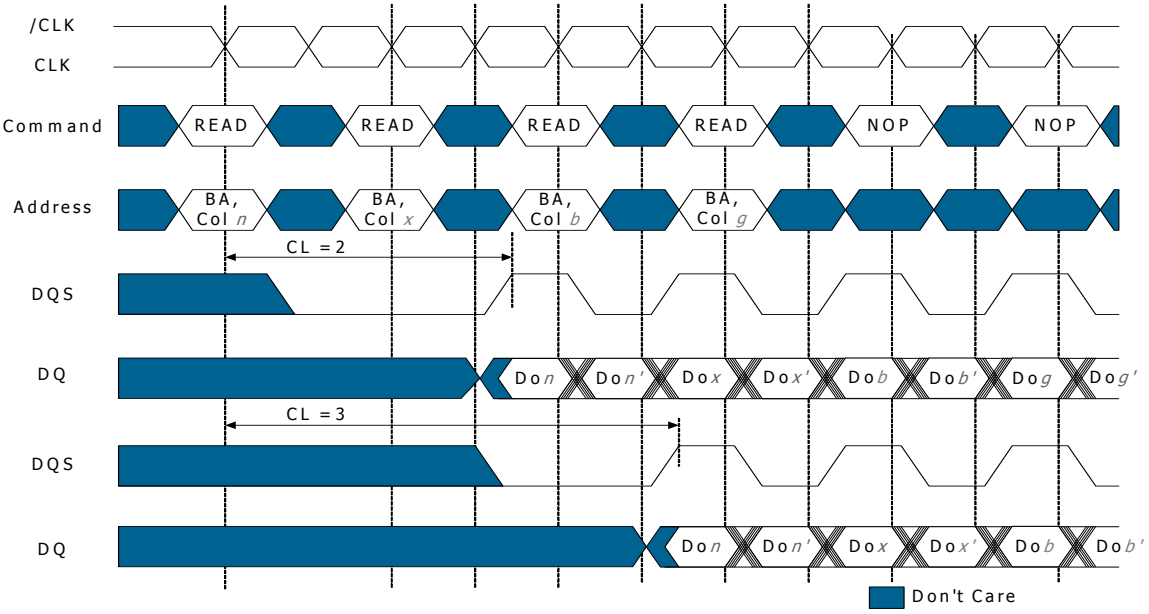
Consecutive Read Bursts

A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive Reads are shown in the first figure of next page. Random read accesses within a page or pages can be performed as shown in second figure of next page.



1) Do *n* (or *b*): Data out from column n (or column b)
2) BA, Col *n* (*b*) = Bank A, Column n (b)
3) Burst Length = 4; 3 subsequent elements of Data Out appear in the programmed order following Do *n* (*b*)
4) Shown with nominal tAC, tDQSCK and tDQSQ

Non-Consecutive Read Bursts

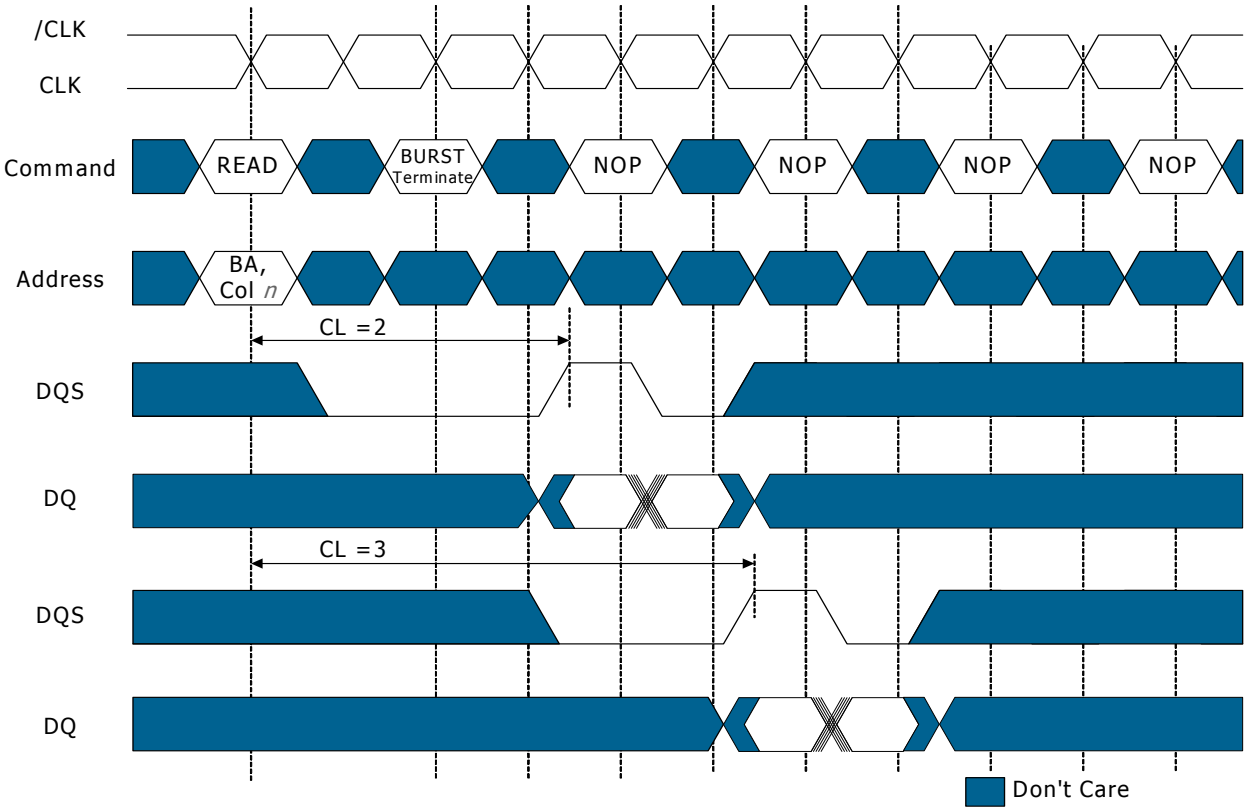


1) Do *n*, etc: Data out from column n, etc
n', x', etc : Data Out elements, accoding to the programmd burst order
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 2, 4 or 8 in cases shown (if burst of 4 or 8, the burst is interrupted)
4) Read are to active rows in any banks

Random Read Bursts

READ BURST TERMINATE

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs.

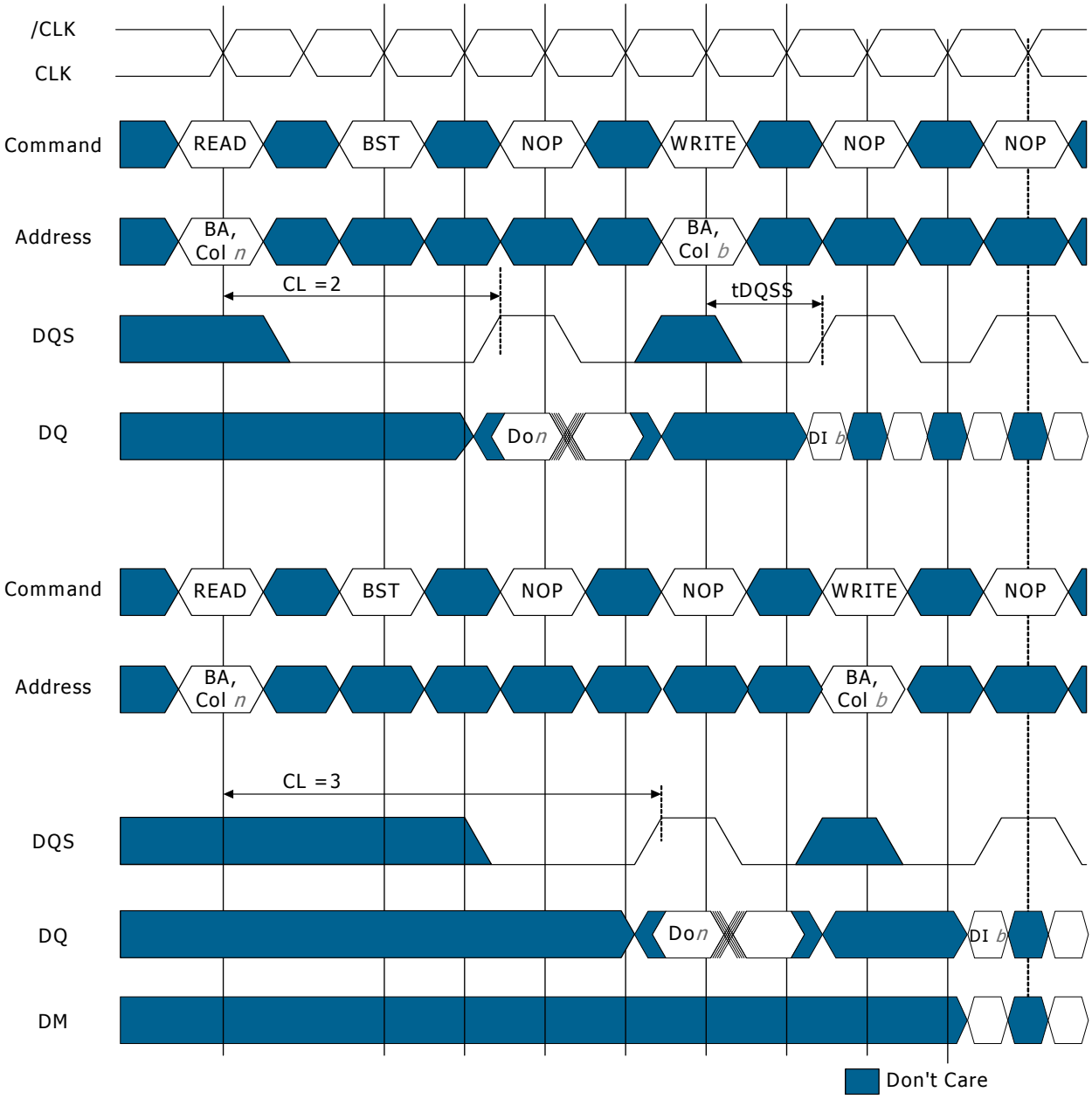


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Cases shown are bursts of 4 or 8 terminated after 2 data elements
4) Shown with nominal tAC, tDQSCK and tDQSQ

Terminating a Read Burst

READ to WRITE

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in next fig. for the case of nominal tDQSS.

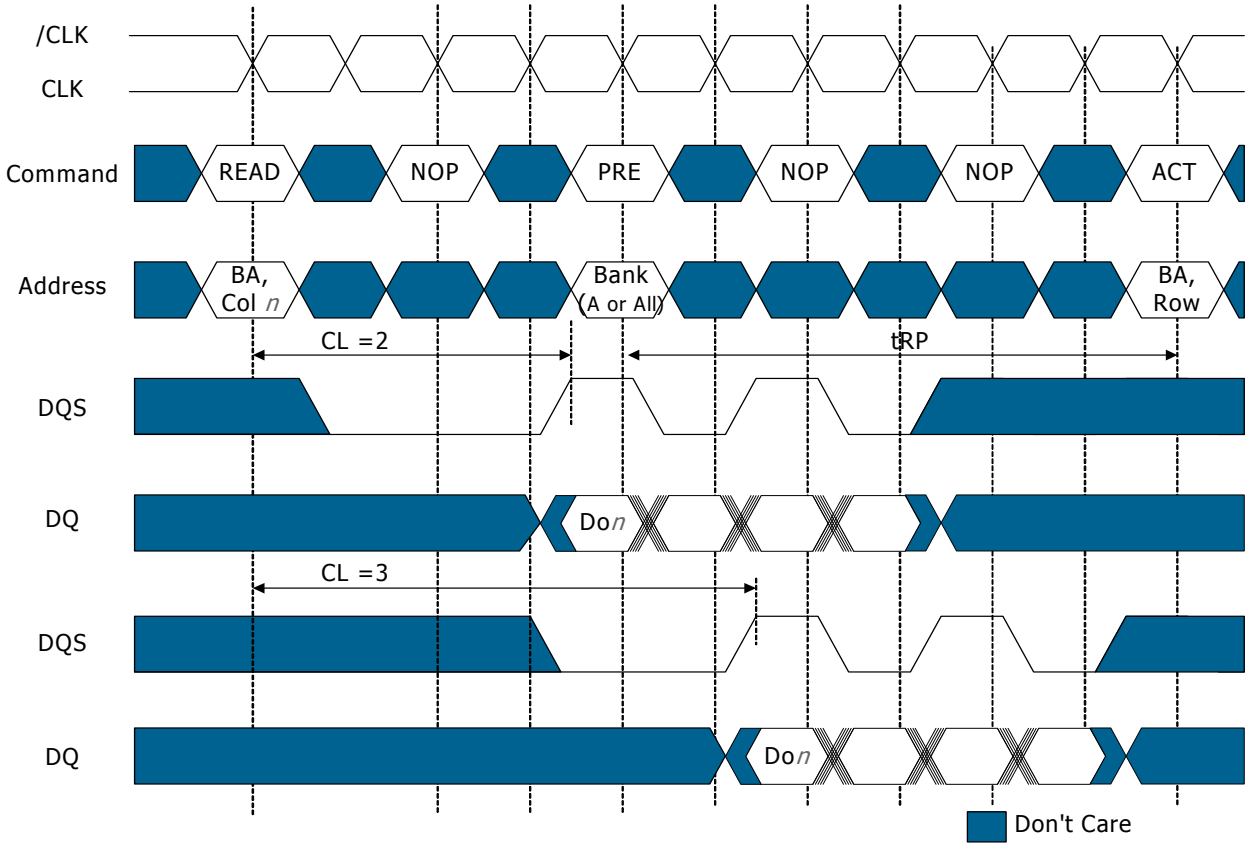


1) DO *n* = Data Out from column n; DI b = Data In to column b
2) Burst length = 4 or 8 in the cases shown; if the burst length is 2, the BST command can be ommitted
3) Shown with nominal tAC, tDQSCK and tDQSQ

Read to Write

READ to PRECHARGE

A Read burst may be followed by or truncated with a PRECHARGE command to the same bank (provided Auto Precharge was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equal the number of desired data-out element pairs.
Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data-out elements.In the case of a Read being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from Read burst with Auto Precharge enabled.
The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

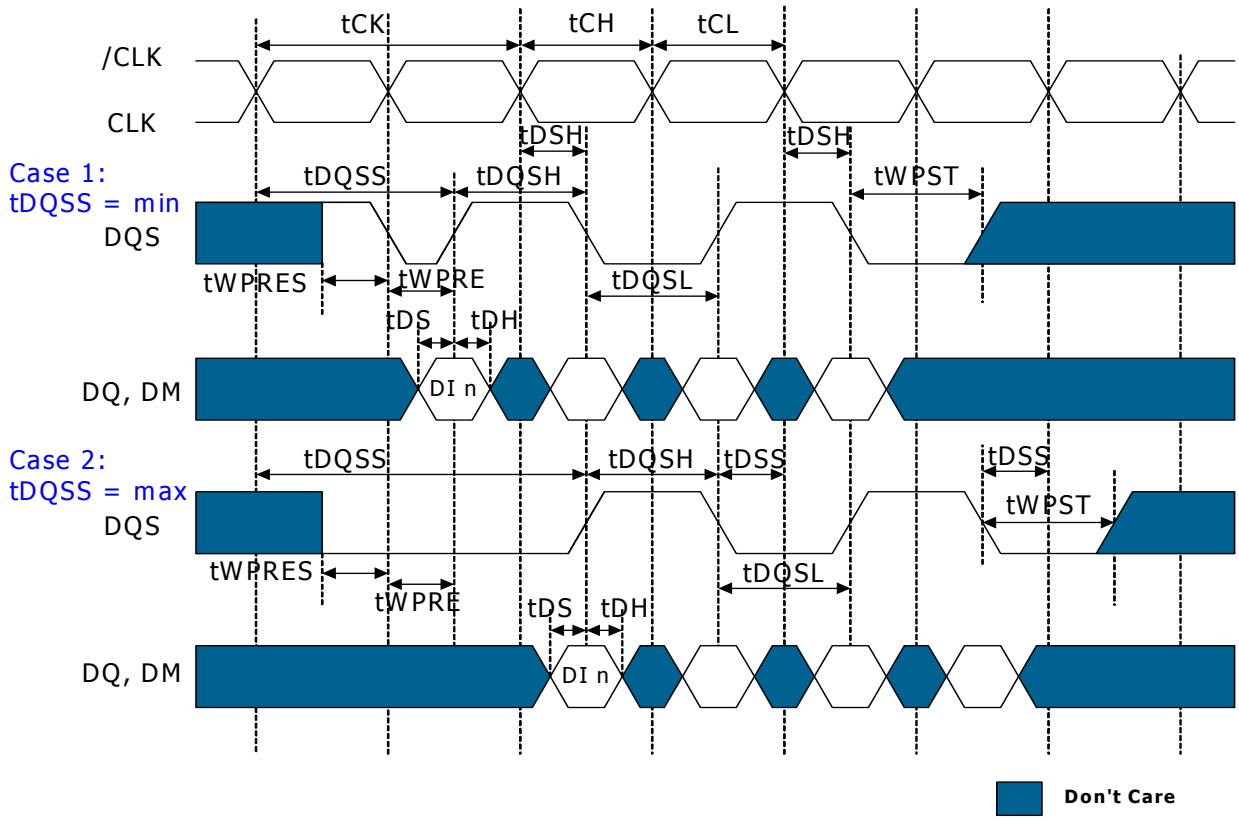


1) DO *n* = Data Out from column n
2) Cases shown are either uninterrupted burst of 4, or interrupted bursts of 8
3) Shown with nominal tAC, tDQSCK and tDQSQ
4) Precharge may be applied at (BL / 2) tCK after the READ command.
5) Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
6) The ACTIVE command may be applied if tRC has been met.

READ to PRECHARGE

Write

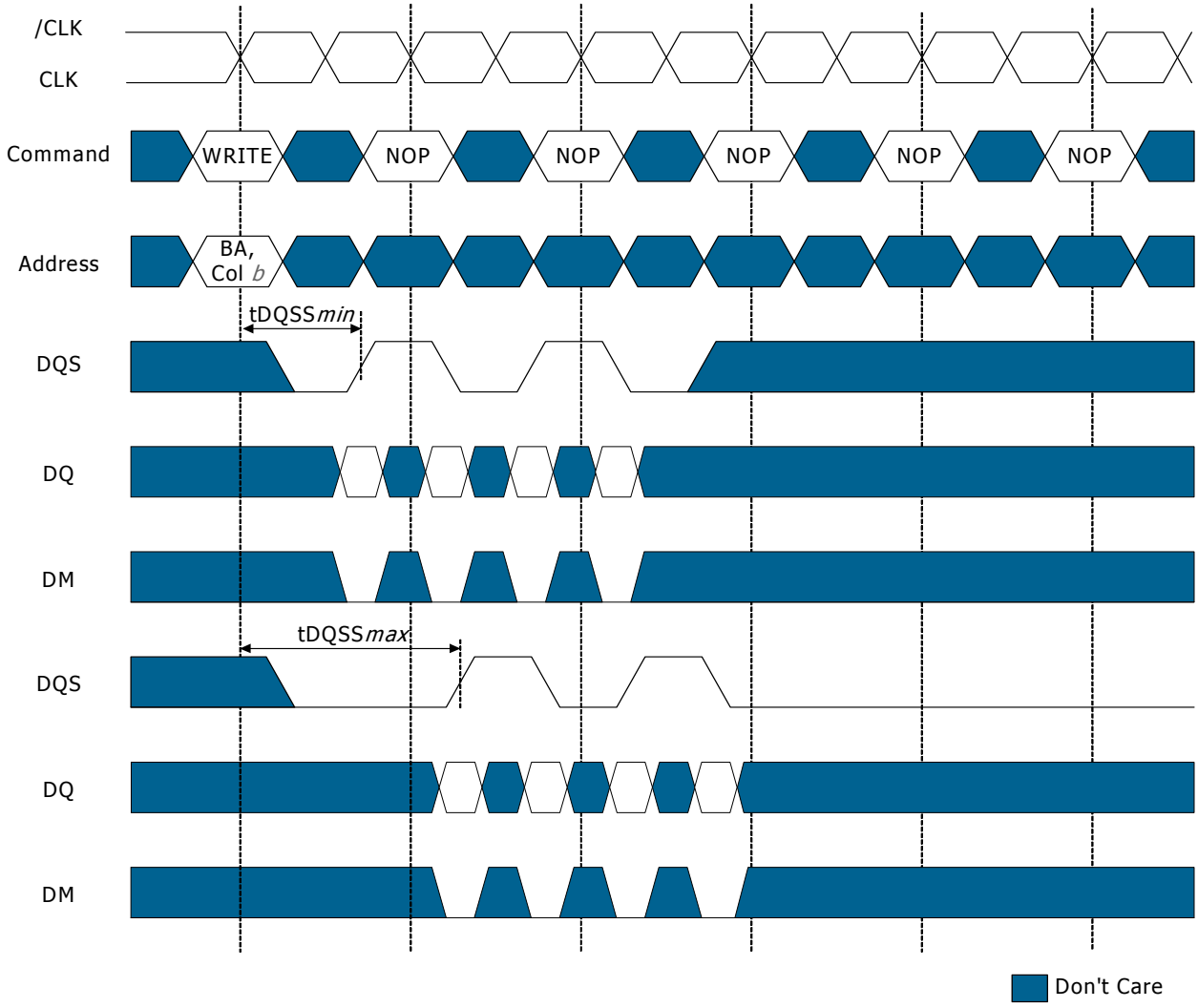
Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.
Basic Write timing parameters for DQ are shown in Figure; they apply to all Write operations.



1) DI n: Data in for column n
2) 3 subsequent elements of Data in are applied in the programmed order following DI n
3) tDQSS : each rising edge of DQS must fall within the +/-25 (percentage) window of the corresponding positive clock edge

Basic Write Timing Parameters

During Write bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and the subsequent data elements will be registered on successive edges of DQS. The Low state of DQS between the WRITE command and the first rising edge is called the write preamble, and the Low state on DQS following the last data-in element is called the write postamble.
The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range - from 75% to 125% of a clock cycle. Next fig. shows the two extremes of t_{DQSS} for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain high-Z and any additional input data will be ignored.

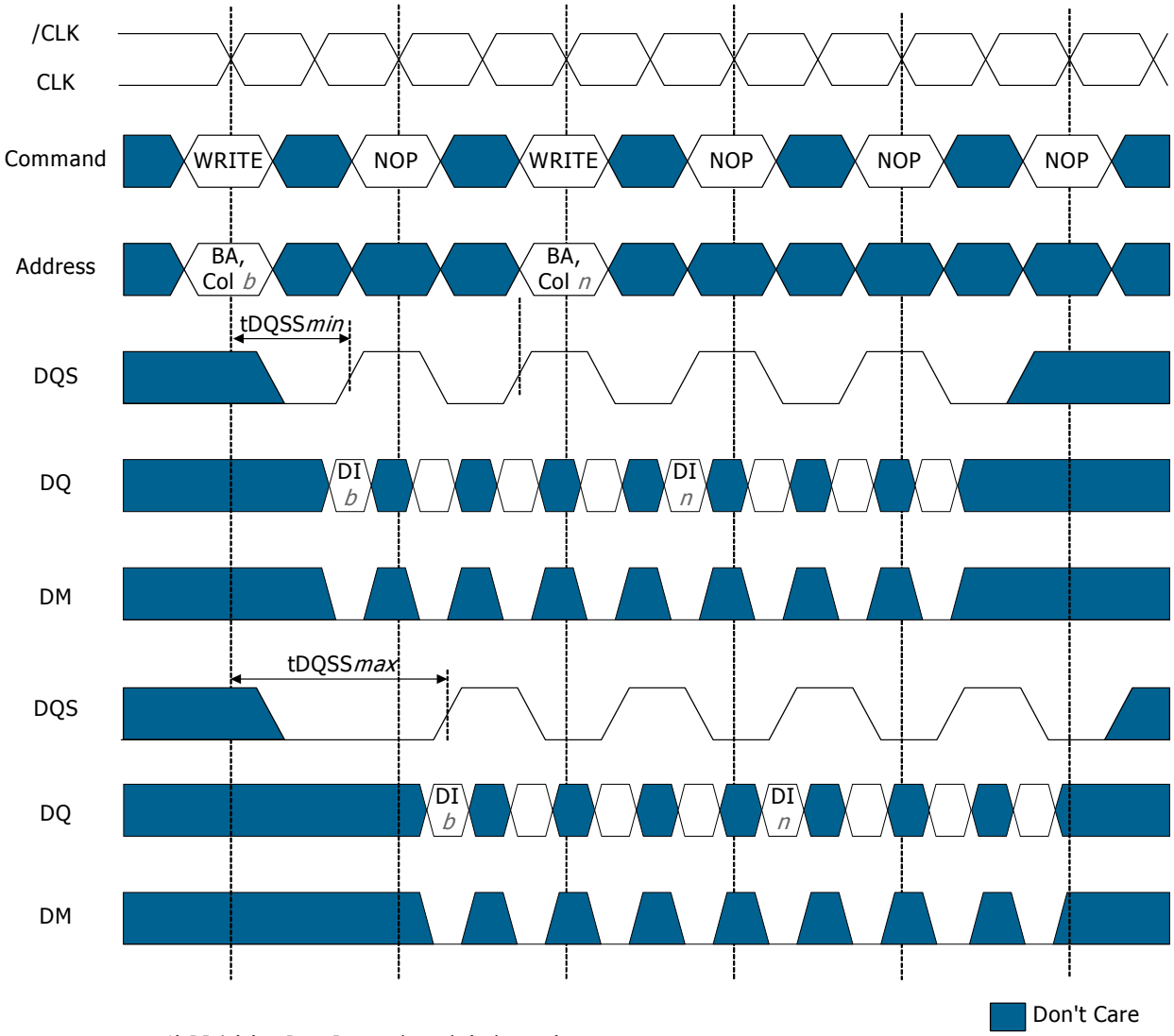


1) DI b = Data In to column b
2) 3 subsequent elements of Data In are applied in the programmed order following DI b
3) A non-interrupted burst of 4 is shown
4) A10 is low with the WRITE command (Auto Precharge is disabled)

Write Burst (min. and max. tDQSS)

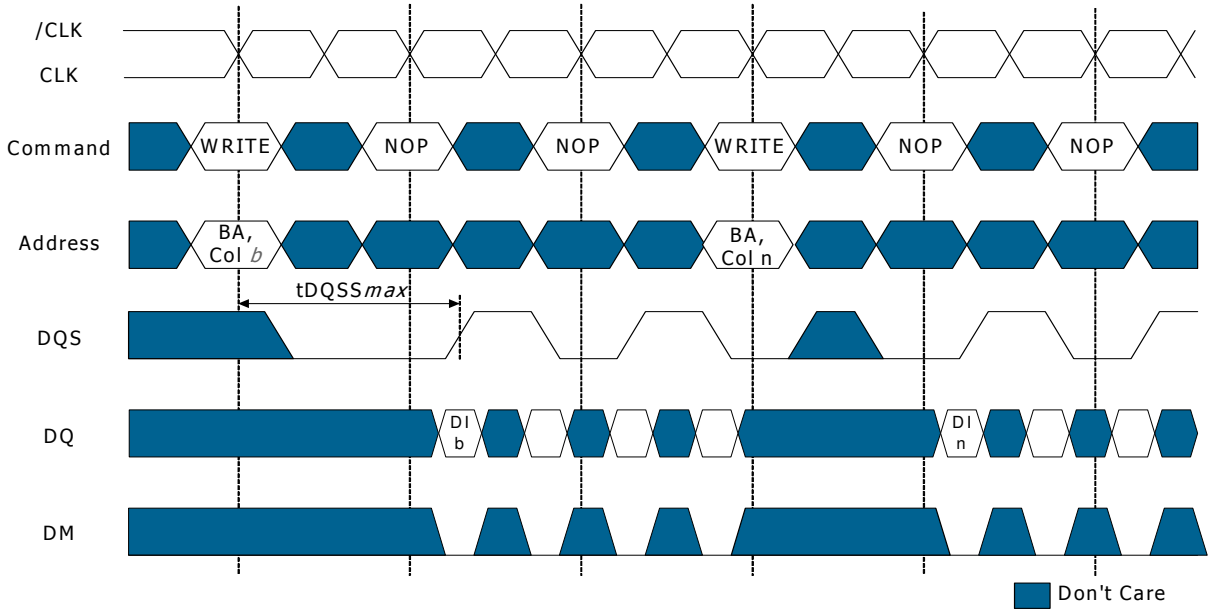
WRITE to WRITE

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command.The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element pairs.



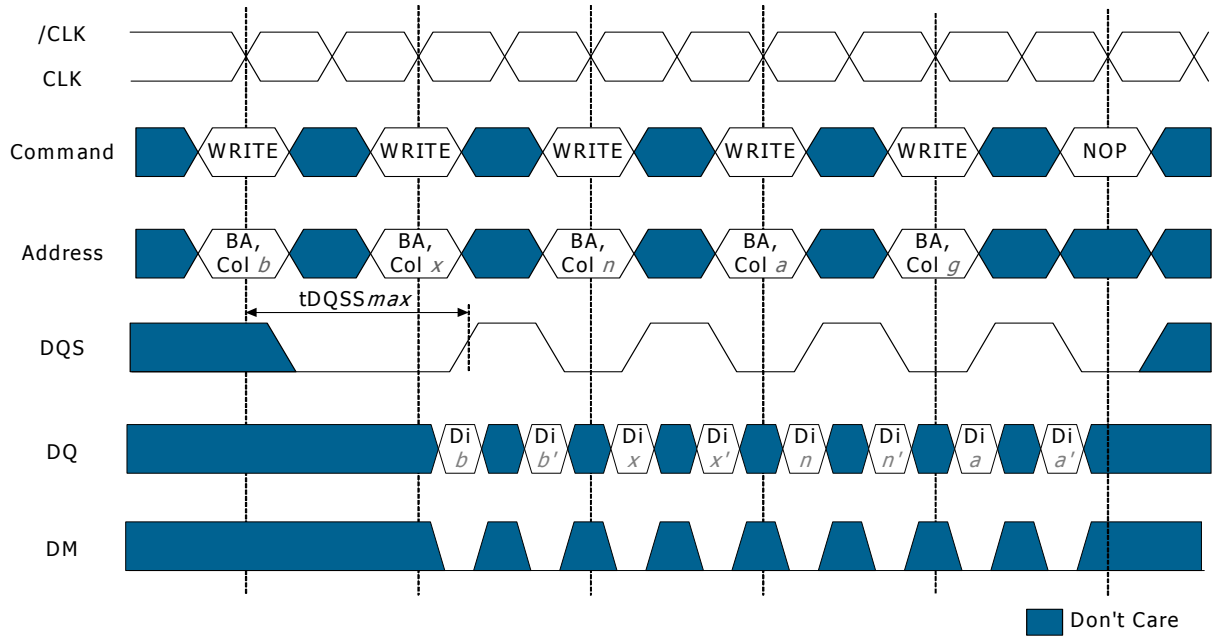
1) DI *b* (*n*) = Data In to column b (column n)
2) 3 subsequent elements of Data In are applied in the programmed order following DI b.
   3 subsequent elements of Data In are applied in the programmed order following DI n.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank

Concatenated Write Bursts



1) DI *b* (*n*) = Data In to column b (or column n).
2) 3 subsequent elements of Data In are applied in the programmed order following DI *b*.
   3 subsequent elements of Data In are applied in the programmed order following DI *n*.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank and may be to the same or different devices.

Non-Concatenated Write Bursts

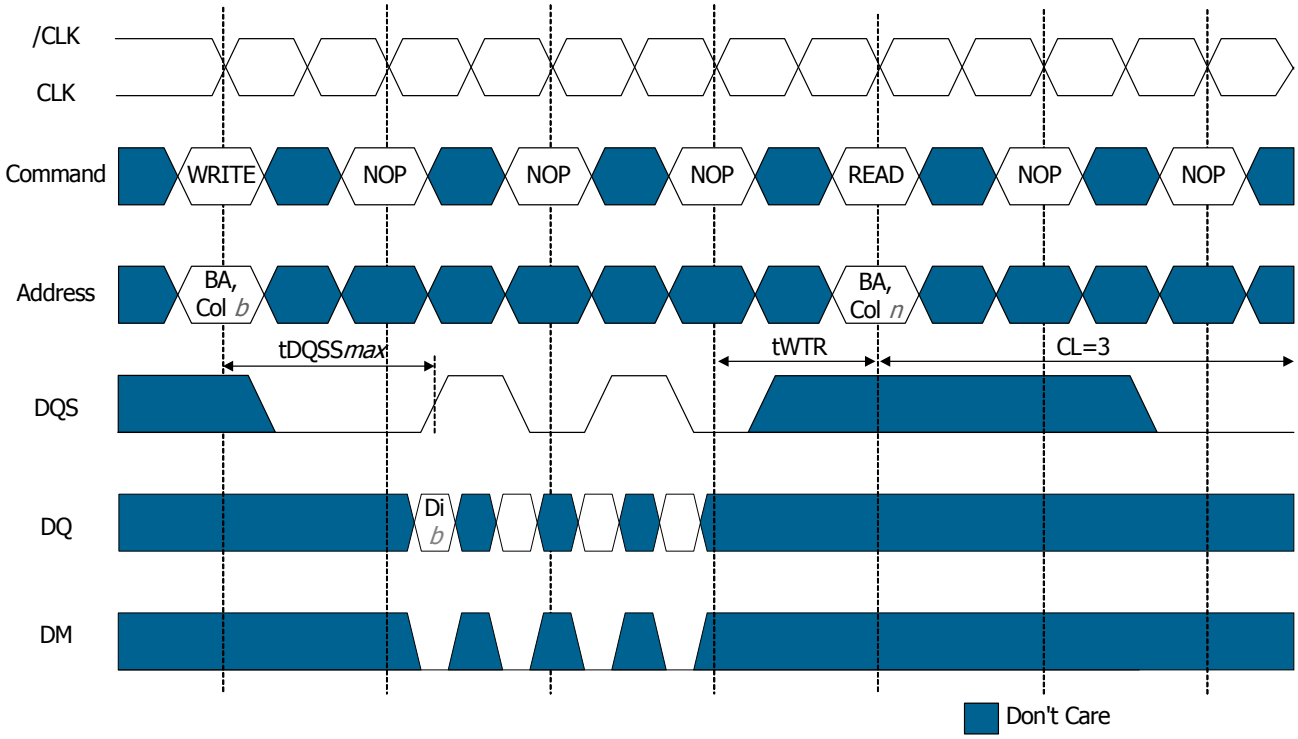


1) DI b etc. = Data In to column b, etc.
   ; b', etc. = the next Data In following DI b, etc. according to the programmed burst order
2) Programmed burst length = 2, 4 or 8 in cases shown. If burst of 4 or 8, burst would be truncated.
3) Each WRITE command may be to any active bank and may be to the same or different devices.

Random Write Cycles

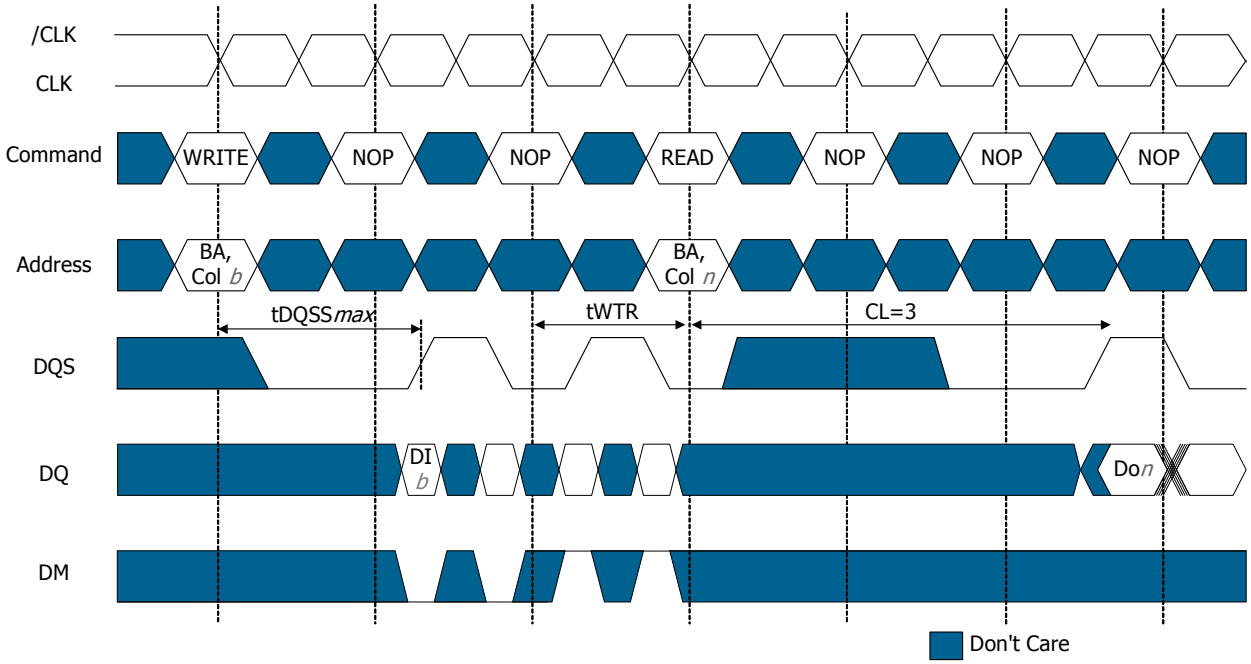
WRITE to READ

Data for any Write burst may be followed by a subsequent READ command. To follow a Write without truncating the write burst, tWTR should be met as shown in Figure.



1) DI *b* = Data In to column b . 3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted burst of 4 is shown.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Data for any Write burst may be truncated by a subsequent READ command as shown in Figure. Note that the only data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in must be masked with DM.

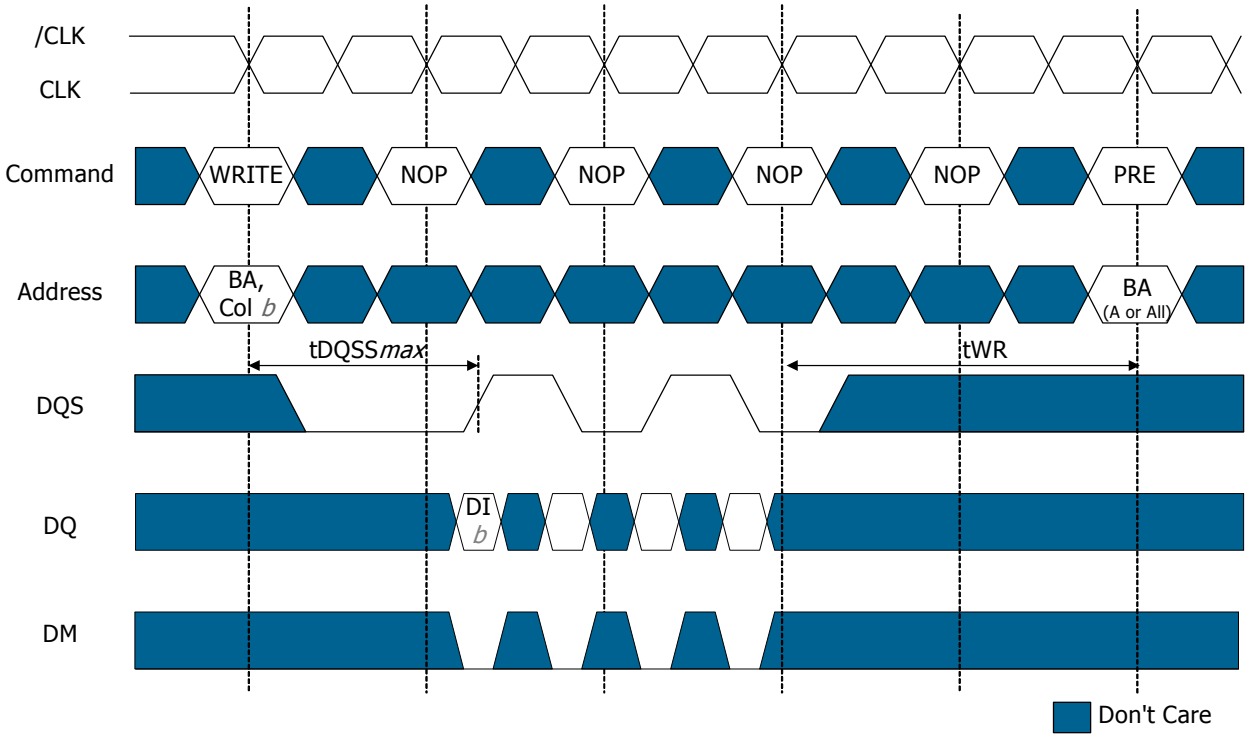


1) DI *b* = Data In to column b. DO *n* = Data Out from column n.
2) An interrupted burst of 4 is shown, 2 data elements are written.
   3 subsequent elements of Data In are applied in the programmed order following DI b.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Interrupting Write to Read

WRITE to PRECHARGE

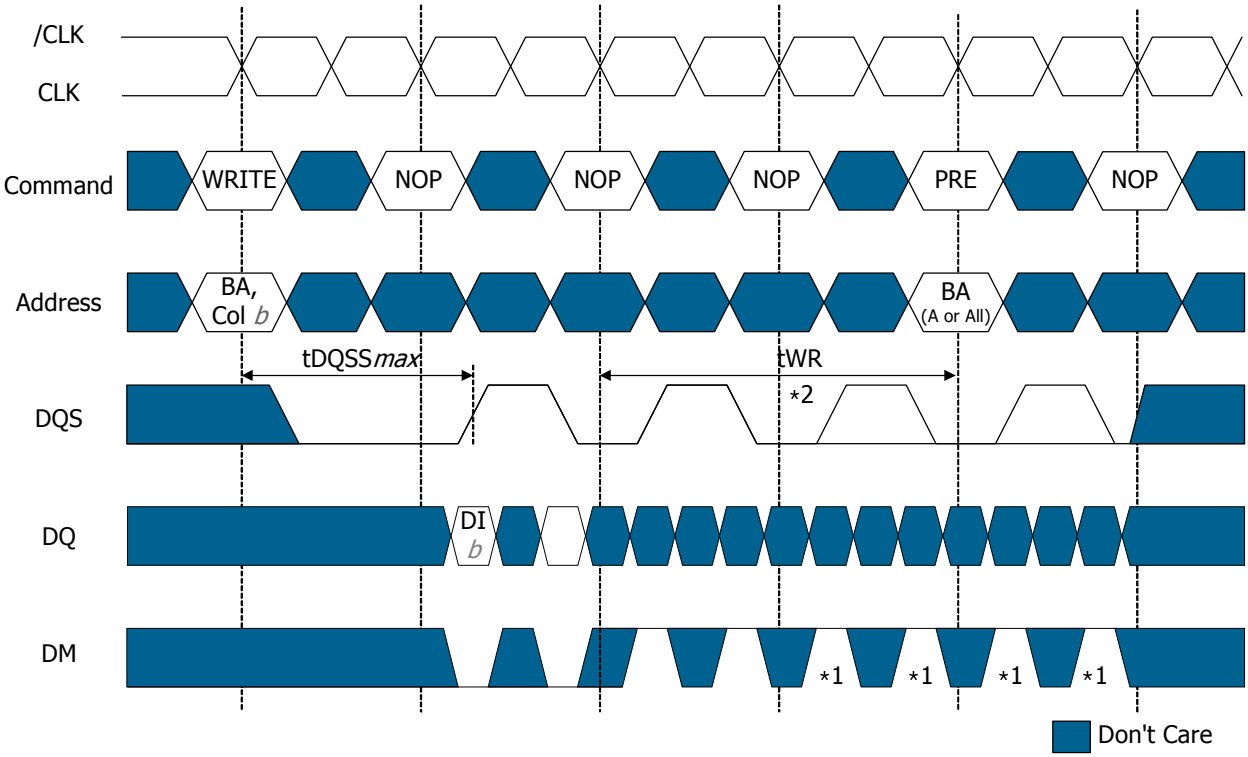
Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). To follow a WRITE without truncating the WRITE burst, tWR should be met as shown in Fig.



1) DI b (n) = Data In to column b (column n)
   3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted bursts of 4 are shown.
3) tWR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)

Non-Interrupting Write to Precharge

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command as shown in Figure.
Note that only data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in next Fig. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

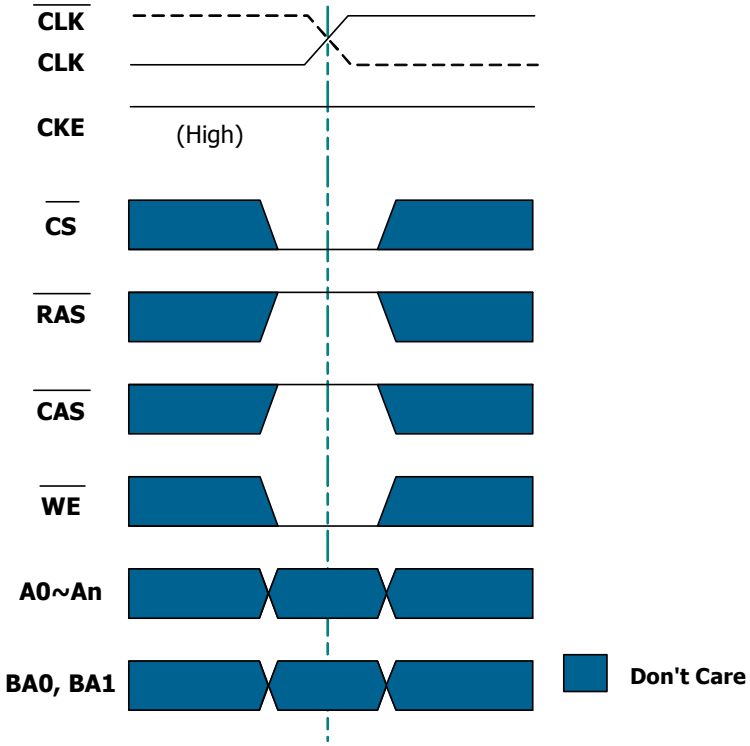


1) DI b = Data In to column b .
2) An interrupted burst of 4 or 8 is shown, 2 data elements are written.
3) tWR is referenced from the positive clock edge after the last desired Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) *1 = can be Don't Care for programmed burst length of 4
6) *2 = for programmed burst length of 4, DQS becomes Don't Care at this point

Interrupting Write to Precharge

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this datasheet. Note the BURST TERMINATE command is not bank specific. This command should not be used to terminate write bursts.

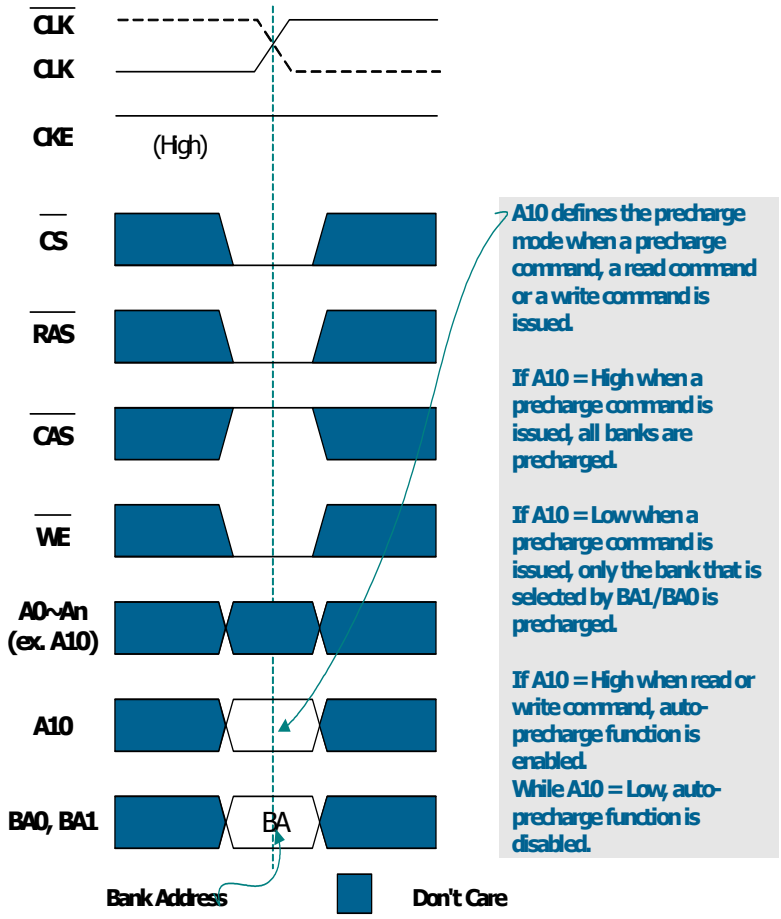


BURST TERMINATE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. Another command to the same bank (or banks) being precharged must not be issued until the precharge time (tRP) is completed.

If one bank is to be precharged, the particular bank address needs to be specified. If all banks are to be precharged, A10 should be set high along with the PRECHARGE command. If A10 is high, BA0 and BA1 are ignored. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.



PRECHARGE command

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command.

This is accomplished by using A10 (A10=high), to enable auto precharge in conjunction with a specific Read or Write command. This precharges the bank/row after the Read or Write burst is complete.

Auto precharge is non persistent, so it should be enabled with a Read or Write command each time auto precharge is desired. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst.

The user must not issue another command to the same bank until the precharge time (tRP) is completed.

AUTO REFRESH AND SELF REFRESH

Mobile DDR devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode:

– AUTO REFRESH.

This command is used during normal operation of the Mobile DDR. It is non persistent, so must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller.The Mobile DDR requires AUTO REFRESH commands at an average periodic interval of tREFI.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given Mobile DDR, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8*tREFI.

-SELF REFRESH.

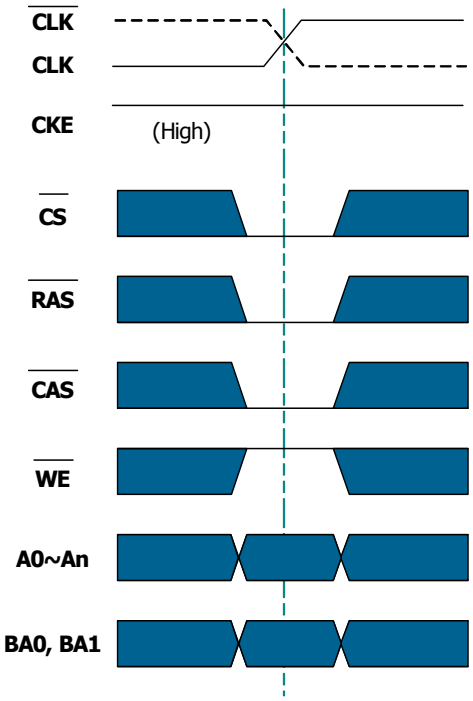
This state retains data in the Mobile DDR, even if the rest of the system is powered down (even without external clocking). Note refresh interval timing while in Self Refresh mode is scheduled internally in the Mobile DDR and may vary and may not meet tREFI time.

"Don't Care" except CKE, which must remain low. An internal refresh cycle is scheduled on Self Refresh entry. The procedure for exiting Self Refresh mode requires a series of commands. First clock must be stable before CKE going high. NOP commands should be issued for the duration of the refresh exit time (tXSR), because time is required for the completion of any internal refresh in progress.

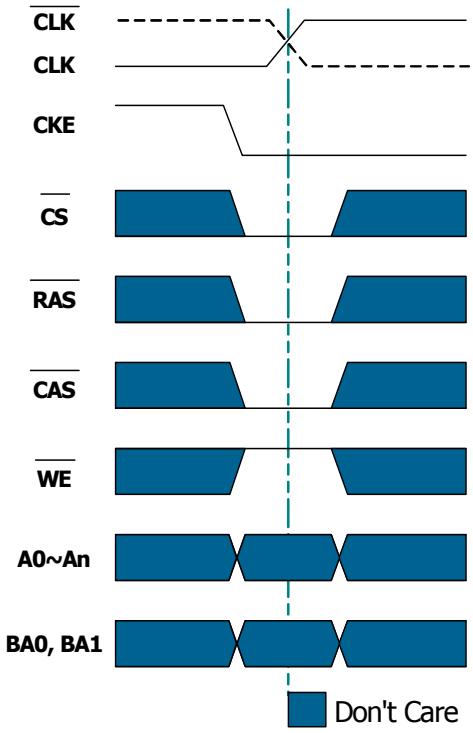
The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra AUTO REFRESH command is recommended. In the self refresh mode, two additional power-saving options exist. They are Temperature Compensated Self Refresh and Partial Array Self Refresh and are described in the Extended Mode Register section.

The Self Refresh command is used to retain cell data in the Mobile SDRAM. In the Self Refresh mode, the Mobile SDRAM operates refresh cycle asynchronously.

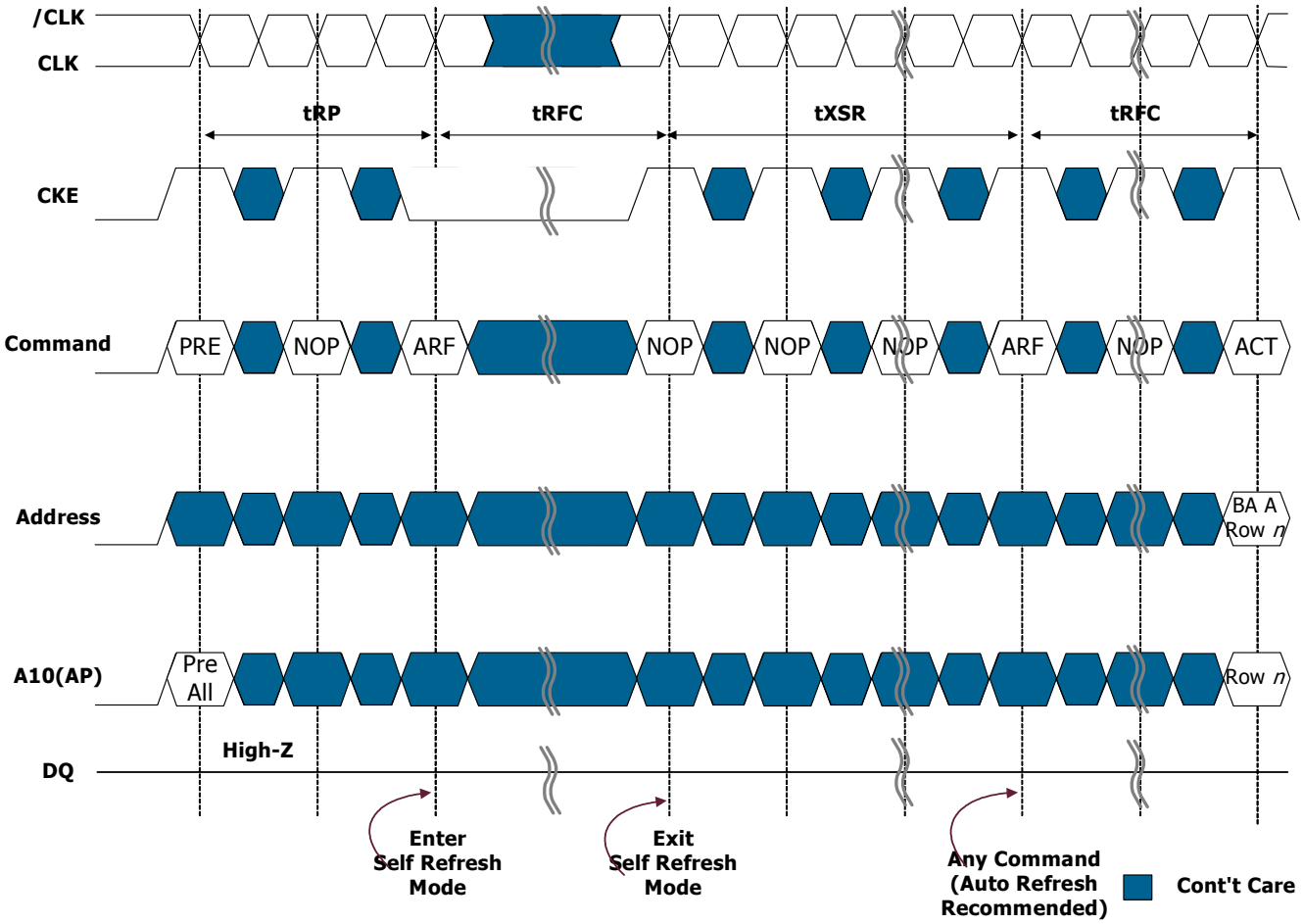
The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled (Low). The Mobile DDR can accomplish an special Self Refresh operation by the specific modes (PASR) programmed in extended mode registers. The Mobile DDR can control the refresh rate automatically by the temperature value of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current and select the memory array to be refreshed by the value of PASR (Partial Array Self Refresh). The Mobile DDR can reduce the self refresh current(IDD6) by using these two modes.



Auto Refresh Command



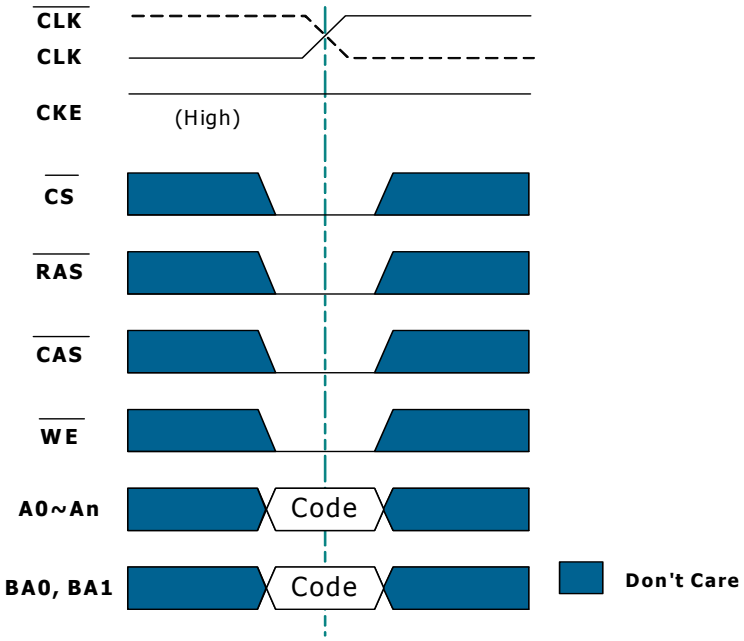
Self Refresh Command



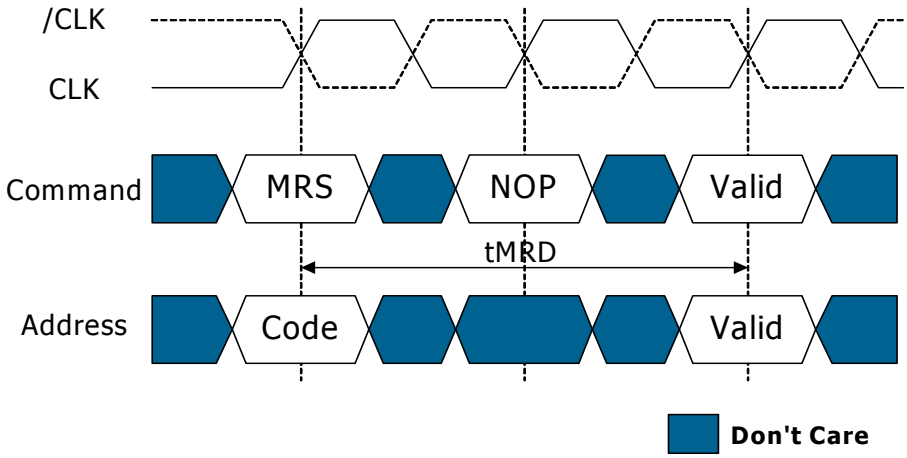
SELF REFRESH ENTRY AND EXIT

MODE REGISTER SET

The Mode Register and the Extended Mode Register are loaded via the address bits. BA0 and BA1 are used to select among the Mode Register, the Extended Mode Register and Status Register. See the Mode Register description in the register definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.



MODE REGISTER SET COMMAND

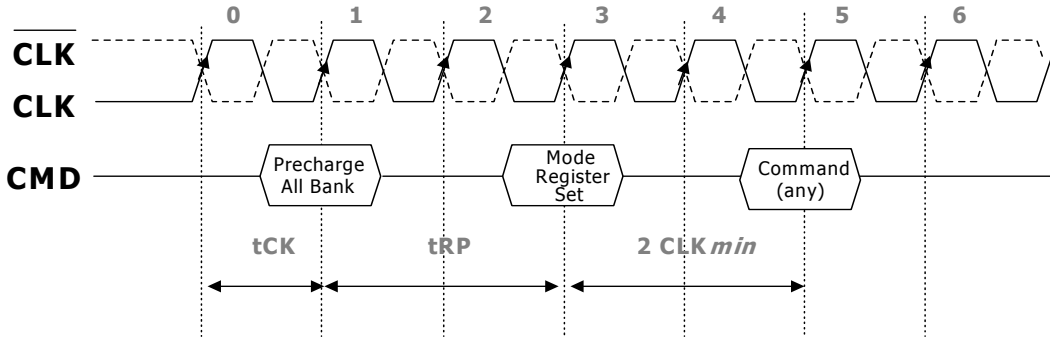


Code = Mode Register / Extended Mode Register selection
(BA0, BA1) and op-code (A0 - An)

tMRD DEFINITION

Mode Register

The mode register contains the specific mode of operation of the Mobile DDR SDRAM. This register includes the selection of a burst length(2, 4 or 8), a cas latency(2 or 3), a burst type. The mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.



Mode Register Set

BURST LENGTH

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Page10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved.

CAS LATENCY

The CAS latency is the delay between the registration of a READ command and the availability of the first piece of output data. If a READ command is registered at a clock edge *n* and the latency is 3 clocks, the first data element will be valid at *n* + 2tCK + tAC. If a READ command is registered at a clock edge *n* and the latency is 2 clocks, the first data element will be valid at *n* + tCK + tAC.

Extended Mode Register

The Extended Mode Register contains the specific features of self refresh operation of the Mobile DDR SDRAM.
The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed, the device is put in Deep Power-Down mode, or the device loses power. The Extended Mode Register should be loaded when all Banks are idle and no bursts are in progress, and subsequent operation should only be initiated after t_{MRD}. Violating these requirements will result in unspecified operation.
The Extended Mode Register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0. The state of address pins A0 ~ An and BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low are written in the extended mode register.
The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.
This register includes the selection of partial array to be refreshed (full array, half array, quarter array, etc.). The extended mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of extended mode register set command.

PARTIAL ARRAY SELF REFRESH (PASR)

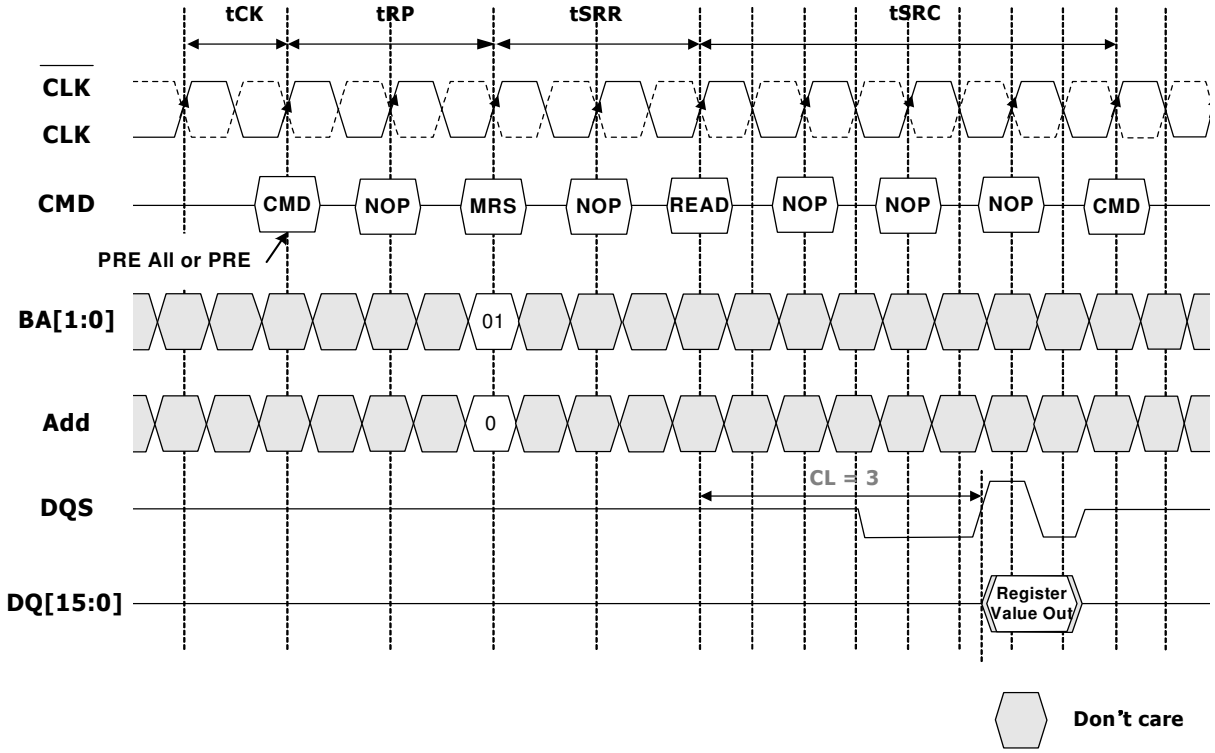
With PASR, the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array, 1/4 array, 1/8 array or 1/16 array could be selected.

DRIVE STRENGTH (DS)

The drive strength could be set to full or half via address bits A5 and A6. The half drive strength is intended for lighter loads or point-to-point environments.

Status Register Read

The Status Register contains the specific die information such as density, device type, data bus width, refresh rate, revision ID and manufacturers. The Status Register is only for READ. Below figure is Status Register Read Timing Diagram.
To read out the Status Register values, BA[1:0] set to 01b and A[11:0] set to all 0 with MRS command followed by Read command with that BA[1:0] and A[11:0] are Don't care.



Note)
1. SRR can only be issued after power-up sequence is complete.
2. SRR can only be issued with all banks precharged.
3. SRR CL is unchanged from value in the mode register.
4. SRR BL is fixed at 2.
5. tSRR = 2 CLK (min)
6. tSRC = CL + 1. (min time between READ to next valid command)
7. No commands other than NOP and DESELECT are allowed between the SRR and the READ.

POWER DOWN

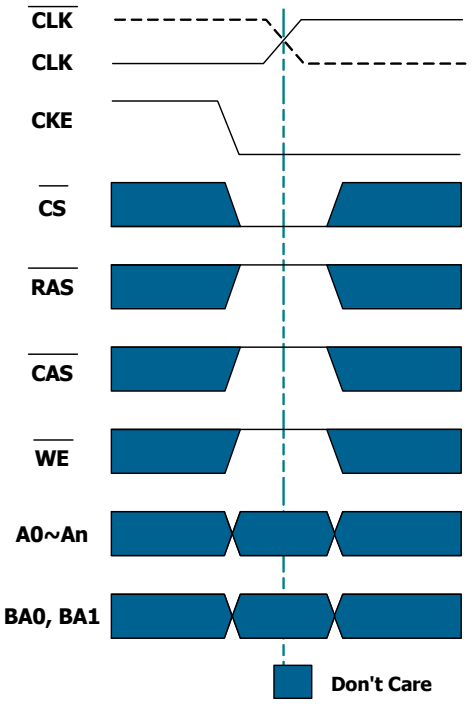
Power down occurs if CKE is set low coincident with Device Deselect or NOP command and when no accesses are in progress. If power down occurs when all banks are idle, it is Precharge Power Down.
If Power down occurs when one or more banks are Active, it is referred to as Active power down. The device cannot stay in this mode for longer than the refresh requirements of the device, without losing data. The power down state is exited by setting CKE high while issuing a Device Deselect or NOP command.
A valid command can be issued after t_{XP}. For Clock stop during power down mode, please refer to the Clock Stop sub-section in Operation section of this datasheet.

NOTE: This case shows CKE low coincident with NO OPERATION.

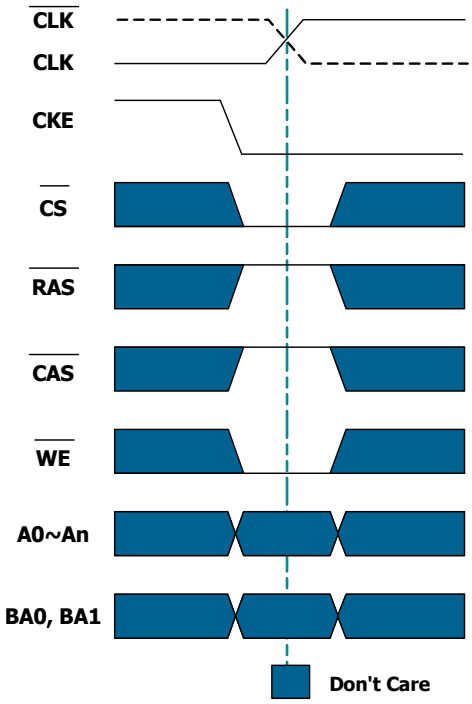
Alternately POWER DOWN entry can be achieved with CKE low coincident with Device DESELECT.

DEEP POWER DOWN

The Deep Power Down (DPD) mode enables very low standby currents. All internal voltage generators inside the Mobile DDR SDRAM are stopped and all memory data is lost in this mode.
All the information in the Mode Register and the Extended Mode Register is lost. Next Figure, *DEEP POWER DOWN COMMAND* shows the DEEP POWER DOWN command All banks must be in idle state with no activity on the data bus prior to entering the DPD mode. While in this state, CKE must be held in a constant low state.
To exit the DPD mode, CKE is taken high after the clock is stable and NOP command must be maintained for at least 200 us. After 200 us a complete re-initialization routing is required following steps 4 through 11 as defined in POWER-UP and INITIALIZATION SEQUENCES. DPD is an optional feature, so please contact Hynix office for DPD feature.



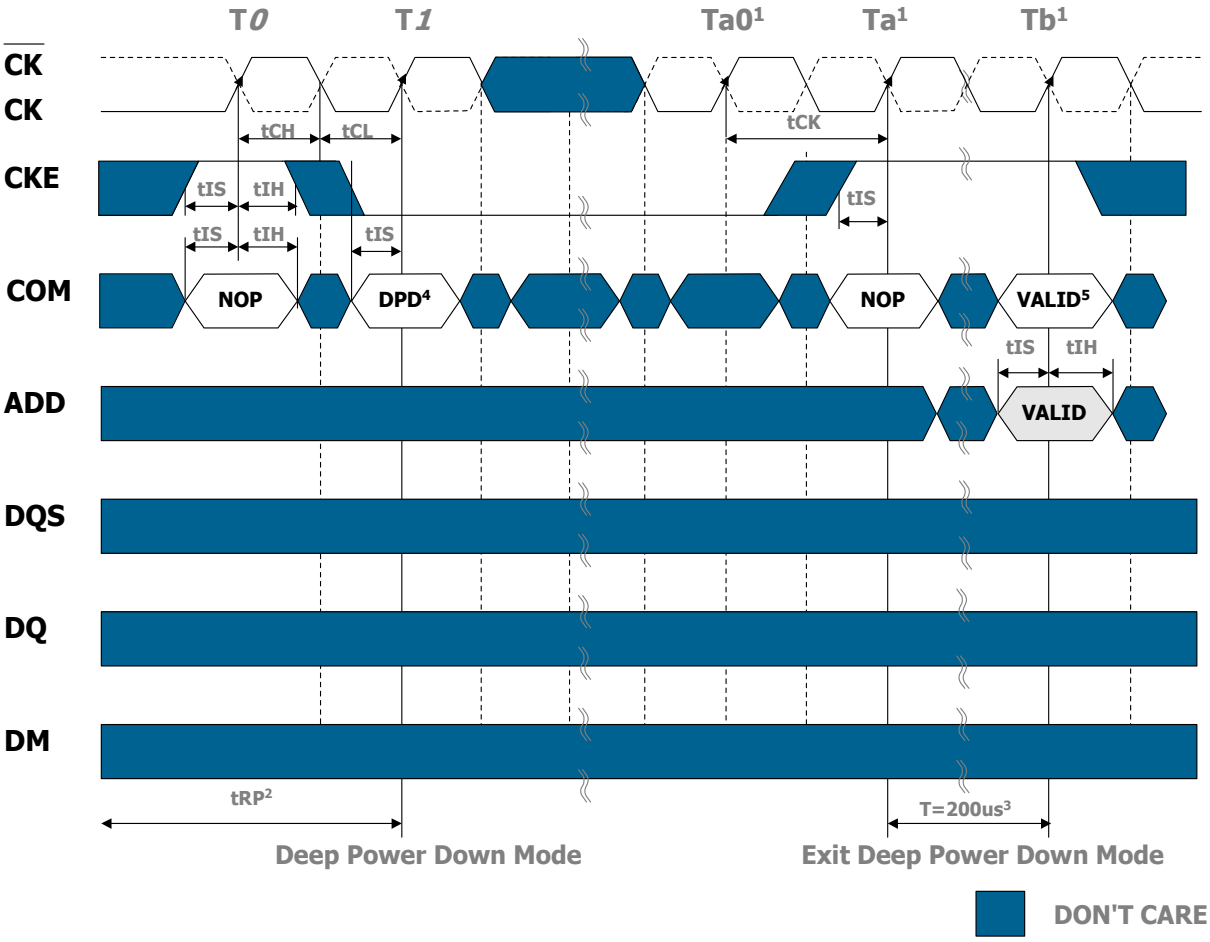
POWER-DOWN ENTRY COMMAND



DEEP POWER DOWN ENTRY COMMAND

Mobile DDR SDRAM Deep Power Down Entry and Exit

Before entering deep power down the DRAM must be in an all banks idle state with no activity on the data bus. Upon entering deep power down all data will be lost. While in deep power down CKE must be held in a constant low state. Upon exiting deep power down NOP command must be maintained for 200us. After 200us a complete initialization routine is required following steps 4 through 11 as defined in POWER-UP and INITIALIZATION SEQUENCES.



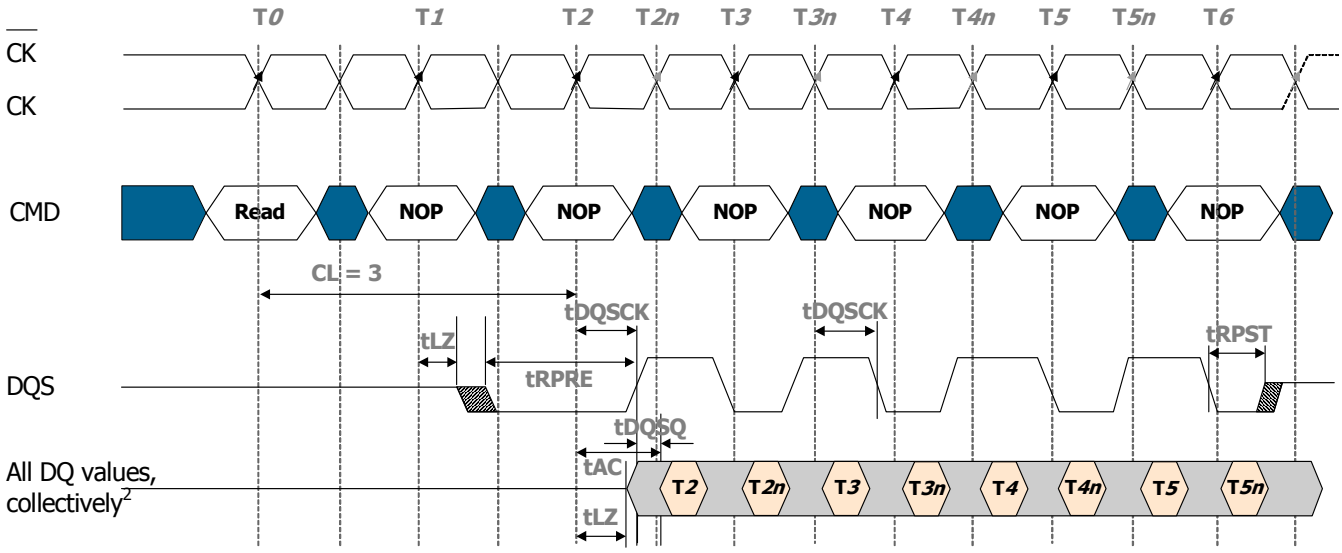
Mobile DDR SDRAM Deep Power-Down Entry and Exit

Note:
1. Clock must be stable before exiting deep power down mode. That is, the clock must be cycling within specifications by Ta0.
2. Device must be in the all banks idle state prior to entering Deep Power Down mode.
3. 200us is required before any command can be applied upon exiting DPD.
4. DPD = Deep Power Down command.
5. Upon exiting Deep Power Down a precharge all command must be issued followed by two auto refresh commands and a load mode register sequence.

CAS LATENCY DEFINITION

CAS latency definition of Mobile DDR SDRAM must be must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation.

CAS latency definition: with CL = 3 the first data element is valid at (2 * tCK + tAC) after the clock at which the READ command was registered (See Figure 2)



CAS LATENCY DEFINITION

NOTE

1. DQ transitioning after DQS transition define tDQSQ window.
2. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
3. tAC is the DQ output window relative to CK, and is the long term component of DQ skew.

Clock Stop Mode

Clock stop mode is a feature supported by Mobile DDR SDRAM devices. It reduces clock-related power consumption during idle periods of the device.

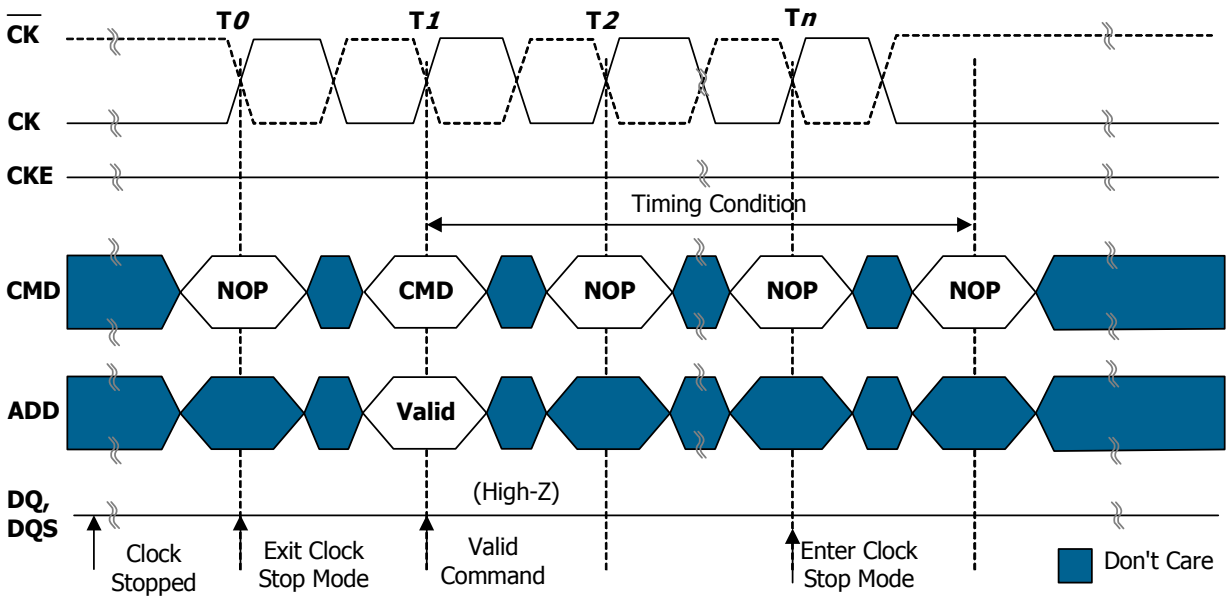
Conditions: the Mobile DDR SDRAM supports clock stop in case:

- The last access command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of required clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- The related timing condition (tRCD, tWR, tRP, tRFC, tMRD) has been met;
- CKE is held HIGH.

When all conditions have been met, the device is either in "idle" or "row active" state, and clock stop mode may be entered with CK held LOW and $\overline{CK}$ held HIGH. Clock stop mode is exited when the clock is restarted. NOPs command have to be issued for at least one clock cycle before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

Figure1 illustrates the clock stop mode:

- Initially the device is in clock stop mode;
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs;
- With T*1* a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command has completed;
- T*n* is the last clock pulse required by the access command latched with T*1.*
- The timing condition of this access command is met with the completion of T*n*; therefore Tn is the last clock pulse required by this command and the clock is then stopped.



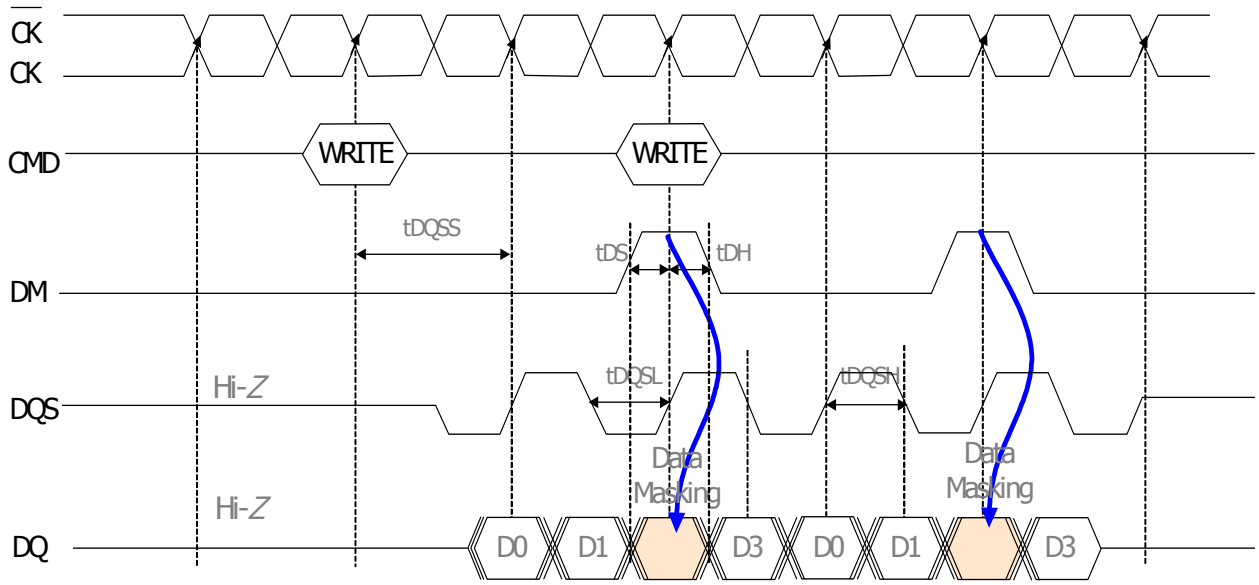
Clock Stop Mode

Data mask[1,2)]

Mobile DDR SDRAM uses a DQ write mask enable signal (DM) which masks write data.
Data masking is only available in the write cycle for Mobile DDR SDRAM. Data masking is available during write, but data masking during read is not available.
DM command masks burst write data with reference to data strobe signal and it is not related with read data. DM command can be initiated at both the rising edge and the falling edge of the DQS. DM latency for write operation is zero.
For x32 data I/O, Mobile DDR SDRAM is equipped with DM0, DM1, DM2 and DM3 which control DQ0~DQ7, DQ8~DQ15, DQ16~DQ23 and DQ24~DQ31 respectively.

Note:
1) Mobile SDR SDRAM can mask both read and write data, but the read mask is not supported by Mobile DDR SDRAM.
2) Differences in Functions and Specifications (next table)

Item	Mobile DDR SDRAM	Mobile SDR SDRAM
Data mask	Write mask only	Write mask/Read mask



Data Masking (Write cycle: BL=4)

POWER-UP AND INITIALIZATION SEQUENCES

Mobile DDR SDRAM must be powered up and initialized in a predefined manner. Operations procedures other thank those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below.

- Step1: Provide power, the device core power (V_{DD}) and the device I/O power (V_{DDQ}) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that V_{DD} and V_{DDQ} are from the same power source. Also assert and hold CLOCK ENABLE (CKE) to a LVCMOS logic high level.

- Step 2: Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.

- Step 3: There must be at least 200us of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.

- Step 4: Issue a PRECHARGE ALL command.

- Step 5: Provide NOPs or DESELECT commands for at least t_{RP} time.

- Step 6: Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time.
  Note as part of the initialization sequence there must be two auto refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.

- Step 7: Using the MRS command, load the base mode register. Set the desired operating modes.

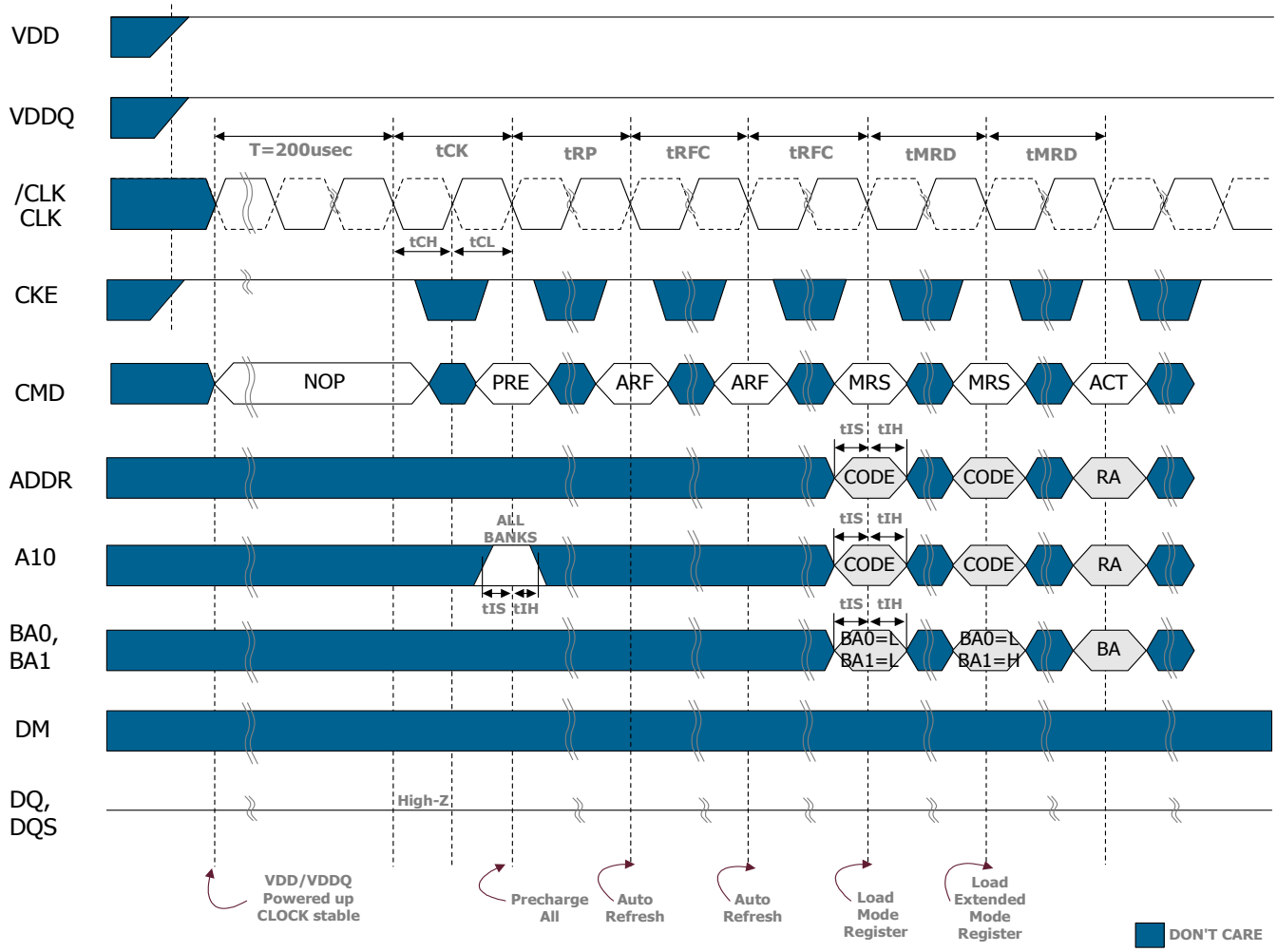
- Step 8: Provide NOPs or DESELECT commands for at least t_{MRD} time.

- Step 9: Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programming is not important.

- Step 10: Provide NOP or DESELCT commands for at least t_{MRD} time.

- Step 11: The DRAM has been properly initialized and is ready for any valid command.

The Initialization flow sequence is below.



Initialization Waveform Sequence

PACKAGE INFORMATION

90 Ball FBGA 0.8mm pitch [8.0 x 13.0 mm^2, t=1.0mm max]