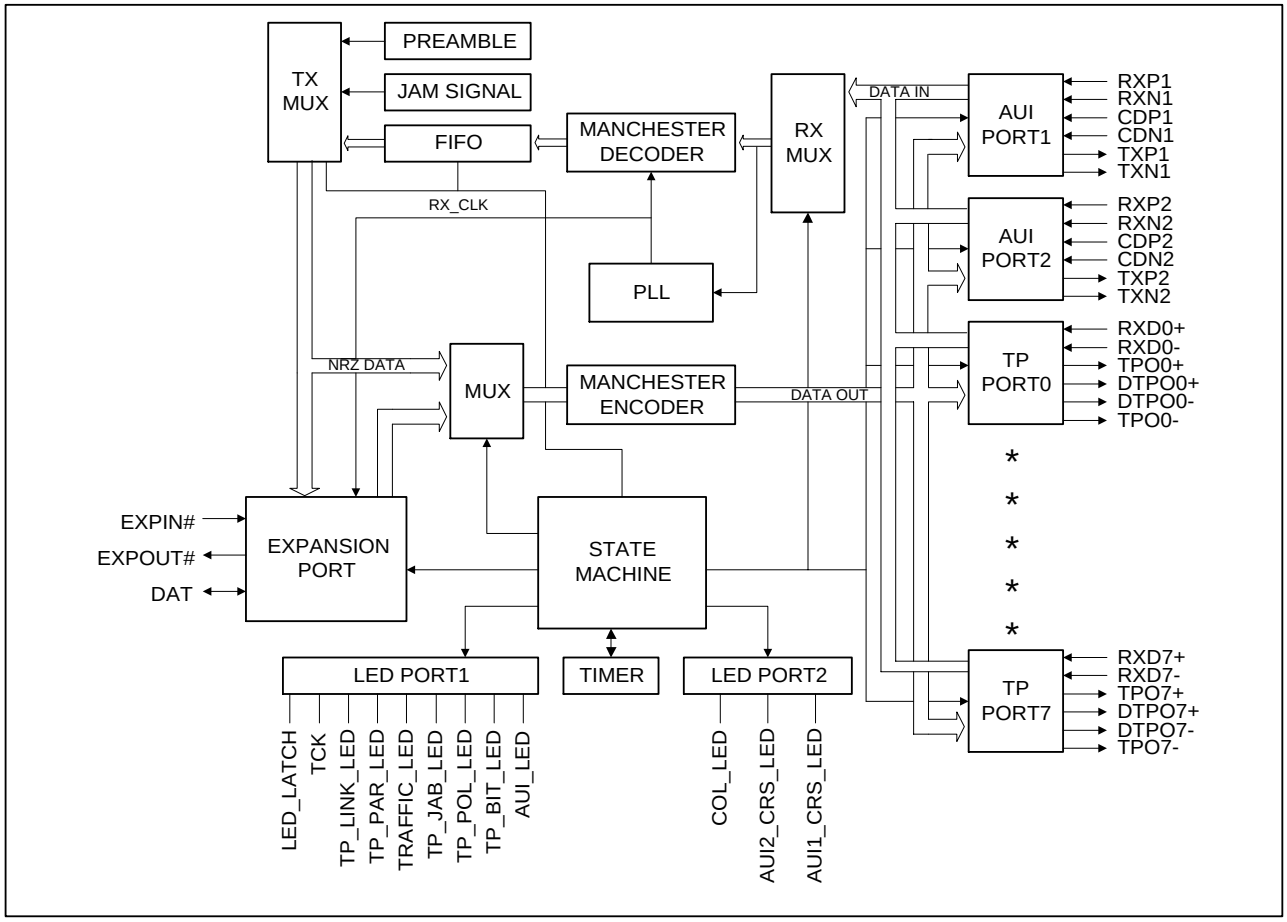
General Description

The 10BASE-T Hub Controller (DM9081) provides a system level solution for designing IEEE-compliant 802.3 repeaters that incorporate 10BASE-T transceivers. This device integrates the repeater functions specified by section 9 of the IEEE 802.3 standard. The Twisted Pair transceiver is compliant with 10BASE-T standards. The DM9081 provides eight integral Twisted Pair Media Attachment Units (MAUs) and two Attachment Unit Interface (AUI) ports in a 100-pin QFP package.

The total number of ports per repeater unit can be increased by connecting multiple DM9081 chips via their expansion ports. The DM9081 supports LED drivers to monitor port status. It displays Link, Carrier Sense, Collision, Partition, and Bit Rate Error Status. In minimum mode, Link, Carrier Sense, and Collision Status can be displayed without external TTL devices.

Block Diagram



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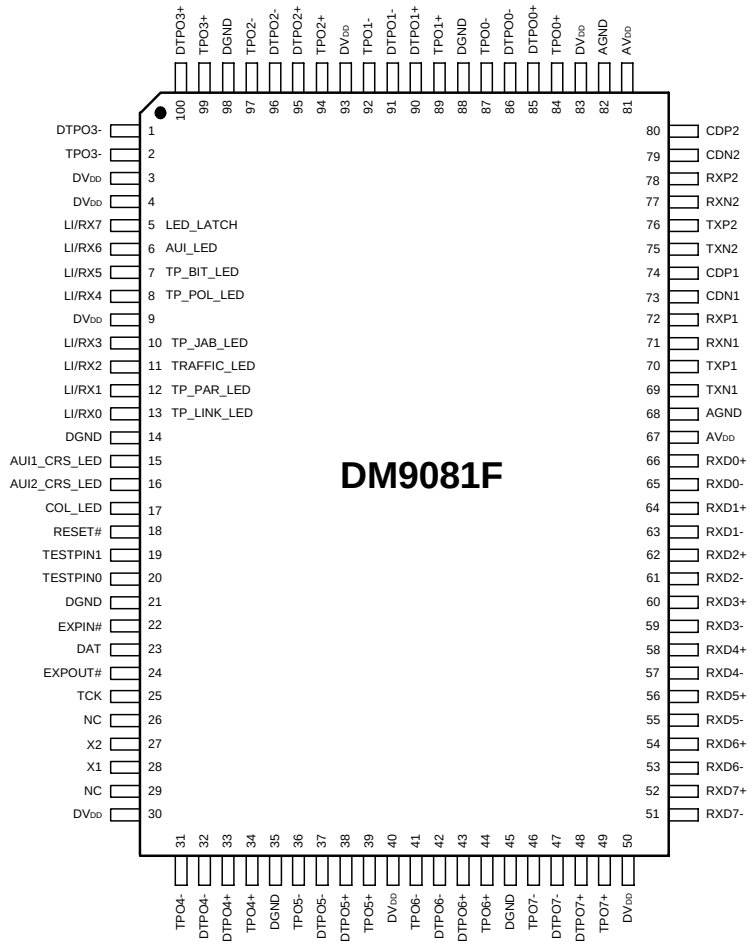
Features

- Repeater functions comply with IEEE 802.3 Repeater Unit specification
- Eight Integral 10BASE-T transceivers utilize the required pre-distortion transmission technique
- Two Attachment Unit Interface (AUI) ports allow connection with 10BASE5 (Ethernet) and 10BASE2 (Cheapernet) networks
- Design a Dumb Hub in minimum mode by using minimum external logic that can respond to Link, Carrier Sense and Collision Status from LED
- Supports one LED output per port for additional status indicators such as Link, Partition, Carrier Sense, etc.
- Built-in Jabber LED reports global Jabber information of the DM9081 Hub
- Built-in Traffic LED indicates Hub global 10MHz bandwidth utilization status
- Expandable to accommodate two DM9081 connections, with no external logic required
- On board PLL, Manchester encoder/decoder and FIFO
- Expandable to accommodate increased number of repeater ports. Recommended IC cascade number: under 3 and inclusive
- Preamble loss effects eliminated by deep FIFO
- Each port can be isolated (partitioned) and reconnected separately
- Twisted Pair Link Test capability
- Full amplitude and timing regeneration for retransmitted signals
- Low power CMOS process with single 5V supply
- 100-pin QFP package

Pin Configuration



Pin Description

Pin No.	Pin Name	I/O	Description
Transceiver			
100, 1 99, 2 34, 31 33, 32 39, 36 38, 37 44, 41 43, 42 49, 46 48, 47 84, 87 85, 86 89, 92 90, 91 94, 97 95, 96	DTPO3+/- TPO3+/- TPO4+/- DTPO4+/- TPO5+/- DTPO5+/- TPO6+/- DTPO6+/- TPO7+/- DTPO7+/- TPO0+/- DTPO0+/- TPO1+/- DTPO1+/- TPO2+/- DTPO2+/-	O	**TP Driver Outputs**. The TPO+/- output generate 10Mbits/s Manchester-encoded data. The DTPO+/- outputs are one-half bit time delayed and inverted with respect to TPO+/-. These four outputs provide the TP drivers with pre-distortion capability
52, 51 54, 53 56, 55 58, 57 60, 59 62, 61 64, 63 66, 65	RXD7+/- RXD6+/- RXD5+/- RXD4+/- RXD3+/- RXD2+/- RXD1+/- RXD0+/-	I	**10BASE-T Port Different Data Receivers**
70, 69 76, 75	TXP1, TXN1 TXP2, TXN2	O	**AUI Port Different Data Drivers**. The outputs are source followers that require a 270Ω pull-down resistor
72, 71 78, 77	RXP1, RXN1 RXP2, RXN2	I	**AUI Port Differential Receive Input Pair**
74, 73 80, 79	CDP1, CDN1 CDP2, CDN2	I	**AUI Port Different Collision Input Pair**
Expansion Port			
24	EXPOUT#	O	The assertion of this signal indicates that DM9081 is transmitting data on DAT pins. It is active low
22	EXPIN#	I	The assertion of this signal indicates that DM9081 is receiving data on DAT pins. The receiving data will be broadcast to the other ports. It is active low and is internally pulled high with a 100KΩ resistor
23	DAT	I/O,Z	The DAT pins of all DM9081 chips are inter-connected. The active DM9081 drives DAT with repeated data or jam signals in NRZ format. The inactive DM9081 receives the repeated data or jam signals from the DAT pin

Pin Description

Pin No.	Pin Name	I/O	Description
Miscellaneous			
3, 4, 9, 30, 40, 50, 83, 93	DVDD	P	**Digital Power**
14, 21, 35, 45, 88, 98	DGND	P	**Digital Ground**
18	RESET#	I	Active low to reset the internal logic of DM9081. It should be synchronized to X2 if multiple DM9081s are used
20, 19	TESTPIN0 TESTPIN1	I	These two pins are used to select LED display mode. Normal mode is selected if both pins are connected to VDD. Minimum mode is selected if both pins are connected to GND. Other settings are prohibited
26, 29	NC	-	These pins should be left open
27	X2	I	A 20MHz oscillator or crystal should be attached to this pin
28	X1	O	This pin is used in crystal connection only. It is left open when using an oscillator
67, 81	AVDD	P	**Analog Power**
68, 82	AGND	P	**Analog Ground**
LED Display Pins			
5	LED_LATCH (LI/RX7)	O	This pin is used to latch the serial LED information from pins 6 to 13 In minimum mode, this pin sends out TP7 Link and Carrier Sense status
6	AUI_LED (LI/RX6)	O	This pin transmits AUI port status synchronous to TCK In minimum mode, this pin sends out TP6 Link and Carrier Sense status
7	TP_BIT_LED (LI/RX5)	O	This pin sends out global bit rate error status of the DM9081 Hub In minimum mode, this pin sends out TP5 Link and Carrier Sense status
8	TP_POL_LED (LI/RX4)	O	In minimum mode, this pin sends out TP4 Link and Carrier Sense status
10	TP_JAB_LED (LI/RX3)	O	This pin transmits global jabber status of the DM9081 Hub In minimum mode, this pin sends out TP3 Link and Carrier Sense status
11	TRAFFIC_LED (LI/RX2)	O	This pin sends out utilization of 10MHz bandwidth synchronous to TCK In minimum mode, this pin sends out TP2 Link and Carrier Sense status
12	TP_PAR_LED (LI/RX1)	O	This pin sends out the partition status synchronous to TCK for the eight TP ports In minimum mode, this pin sends out TP1 Link and Carrier Sense status
13	TP_LINK_LED (LI/RX0)	O	This pin sends out the link and carrier sense status synchronous to TCK for the eight TP ports In minimum mode, this pin sends out TP0 Link and Carrier Sense status
15	AUI1_CRS_LED	O	Active low for 52ms when AUI Port 1 detects carrier
16	AUI2_CRS_LED	O	Active low for 52ms when AUI Port 2 detects carrier
17	COL_LED	O	Active low for 26ms when collision is detected
25	TCK	O	A 10MHz clock synchronous to X2

Functional Description

The DM9081 Integrated Multiport Controller is a single chip implementation of an IEEE 802.3 Ethernet repeater (Hub). The DM9081 chip provides eight integral 10BASE-T ports plus two AUI ports, comprising the basic repeater. The DM9081 is also expandable, enabling the implementation of high port count repeaters based on more than one DM9081 chip. The DM9081 chip complies with the full set of repeater basic functions, as defined in Section 9 of ISO 8802.3 (ANSI/IEEE 802.3C). These functions are summarized below.

Repeater Function

When any single network port senses the start of a packet on its receive lines, the DM9081 chip will broadcast the received data to all other network ports. The repeated data will also be presented on the expansion port to provide multiple DM9081 chip repeater applications.

Signal Regeneration

When re-transmitting a packet, the DM9081 chip makes sure that the outgoing packet complies with the 802.3 specification in terms of preamble instructions, voltage amplitude and timing characteristics. Data packets repeated by the DM9081 chip will contain a minimum of 62 preamble bits before the start of Frame Delimiter. Finally, signal symmetry is restored to data packets repeated by the DM9081 chip, removing jitter and distortion caused by network cabling.

Collision Function

The DM9081 will detect and respond to collision conditions as specified in IEEE 802.3. A multiple DM9081 repeater (Hub) implementation also complies with the 802.3 specification. Specifically, a repeater based on one or more DM9081 chips will handle the transmit collision and one-port-left collision conditions correctly.

Auto Partition/Reconnection

The DM9081 monitors any TP ports or AUI ports and partitions them once certain criteria are met. TP ports and AUI ports will be partitioned under extended duration or when frequent collisions occur. Each TP port and the AUI port are partitioned separately, and are independent of other network ports. The DM9081 chip will cause the port to partition under either of following conditions.

1. A collision condition exists continuously for 1024-bit times (for example, when the AUI port SQE signal is active and the TP port is transmitting simultaneously and receiving).

2. Whenever each of 32 consecutive attempts to transmit to that port results in a collision.

Any partitioned port can be reconnected if a packet longer than 512-bit times is transmitted or received from that port without collision.

Fragment Extension

If the total packet length received by the DM9081 is less than 96 bits, including preamble, the DM9081 chip will extend the repeated packet length to 96 bits by appending a Jam sequence to the original fragment.

Link Integrity Test

The integral TP ports implement the Link Test function, as specified in the 802.3 10BASE-T standard. The DM9081 will transmit Link Test pulses to any TP port after that port transmitter has been inactive for more than 8ms but less than 17 ms. Conversely, if a TP port does not receive any data packets or Link Test pulses for more than 65ms but less than 132ms, that port will enter link fail state. A port in link fail state will be disabled by the DM9081 chip (repeater transmit functions are disabled) until it receives either four consecutive Link Test pulses or a data packet. Note, however, that the DM9081 chip will always transmit Link Test pulses to all TP ports regardless of whether the port is enabled, partitioned, or in link fail state.

Jabber Lockup Protection

The DM9081 chip implements a built-in jabber protection scheme to ensure that the network is not disabled due to transmission of excessively long data packets. This protection scheme will automatically interrupt the transmitter circuits of the DM9081 for 96-bit times if the DM9081 chip has been transmitting continuously for more than 65,536-bit times. This is referred to as MAU Jabber Lockup Protection (MJLP).

Reset

An internal circuit ensures that a minimum reset pulse is generated for all internal circuits. For a RESET input with a slow rising edge, the input buffer threshold may be crossed several times due to ripples on the input waveform. During reset, the output signals are placed in their inactive states. This means that all analog signals are placed in their idle states, bidirectional signals are not driven, active LOW signals are driven HIGH, and all active HIGH signals and the LED_LATCH pin are driven LOW. In a multiple DM9081 chip repeater, the RESET signal should be applied simultaneously to all DM9081 chips, and should be synchrononized to the external X2 clock. Table 1 summarizes the state of the DM9081 chip following reset.

Function	State after Reset	Pull Up/Pull Down
DAT	Hi-Impedance	NO
Transmitters (TP and AUI)	Idle	NC
RECEIVERS (TP and AUI)	Enabled	Terminate
AUI Partition/Reconnection	Reconnect	N/A
TP Port Partition/Reconnection	Reconnect	N/A
LINK Test Function for TP Ports	Enabled	N/A
Active Low Output	High	NO
Active High Output	Low	NO

Table 1. Initial State of DM9081

Expansion Port

The DM9081 chip expansion port is comprised of three pins: a bi-directional signal (DAT), an input signal (EXPIN#), and an output signal (EXPOUT#). These signals are used for multiple-DM9081 chip repeater applications. In this configuration, all DM9081 chips must be synchronized with a common clock connected to the X2 inputs. An external synchronnous reset is required. The DM9081 expansion scheme allows the use of multiple DM9081 chips in either a single repeater or a modular multiple repeater with backplane architecture. The DAT pins of all DM9081 chips must be interconnected. The DAT pin is a bidirectional I/O pin that can be used to transfer data or a jam signal between the DM9081 chips. The data sent over the DAT line is in NRZ format, and is synchronized to the common clock.

In the multiple DM9081 configuration, the DM9081 chip asserts the EXPOUT# pin to indicate that it is active and is ready to drive the DAT pin. An external logic senses the EXPOUT# line from all the DM9081 chips and asserts the EXPIN# line to each DM9081. The active DM9081 asserts EXPOUT#, and sends data or jam on the DAT line. Other inactive DM9081 detect EXPIN# asserted, and receive data on the DAT line. If more than one DM9081 chip asserts EXPOUT# lines, then all DM9081s will broastcast jam signals.

External Logic

A simple logic scheme is required when more than two DM9081 chips are connected to increase the total number of repeater ports. The external logic should have one input (EXPOUT#) and one output (EXPIN#) for each DM9081 chip. This function is easily implemented in a PAL device, using the following logical equations:

EXPIN1# =	EXPOUT2# &	EXPOUT3# &	…..	EXPOUTn#
EXPIN2# =	EXPOUT1# &	EXPOUT3# &	…..	EXPOUTn#
EXPIN3# =	EXPOUT1# &	EXPOUT2# &	…..	EXPOUTn#
.	.	.		.
.	.	.		.
.	.	.		.
EXPINn# =	EXPOUT1# &	EXPOUT2# &	…..	EXPOUTN-1#

The above equations are in positive logic, i.e., a variable is true when asserted. An example of three banked DM9081 chips is shown in Figure 1. The cascade IC number recommended: under 3 and inclusive.

Note that if the design includes only two DM9081 chips, then EXPOUT1# is connected to EXPIN2#, EXPOUT2# is connected to EXPIN1#, and no external logic is required. A single PAL16L8 performs the arbitration function for a repeater based on several DM9081 chips.

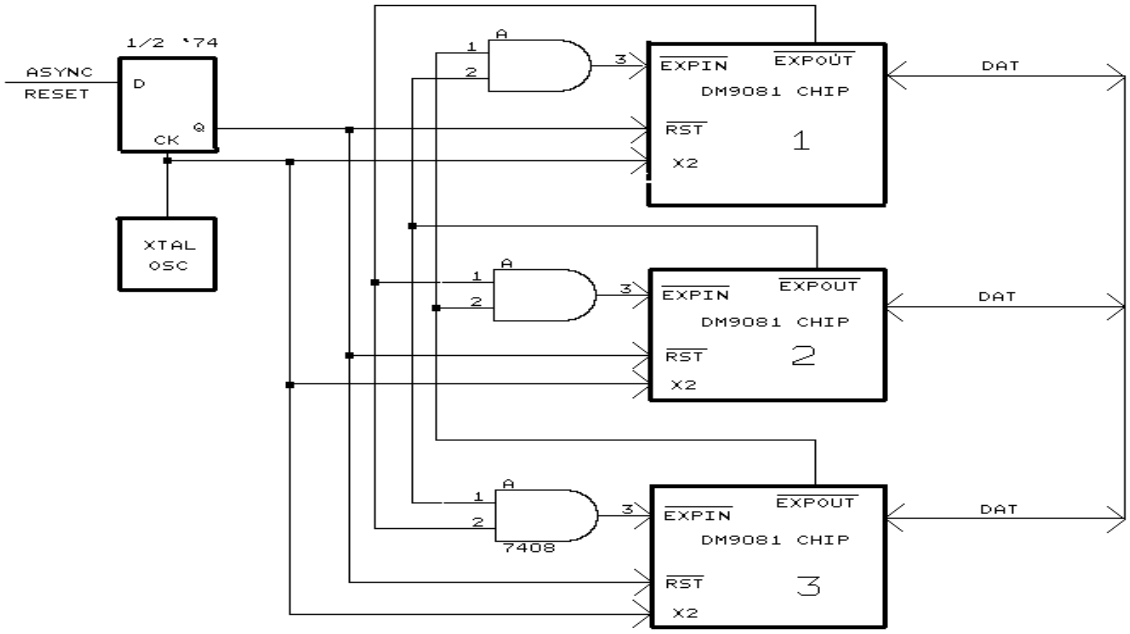


Figure 1. Multiple DM9081 Devices

LED Functions

The DM9081 provides LED functions to monitor the TP and AUI ports.

Collision Status

The COL_LED pin displays the collision status of the DM9081. When the DM9081 detects a collision, the COL_LED will drive low for more than 26ms and less than 52ms.

AUI1 Port Status

The AUI1_CRS_LED displays the AUI1 port status of the DM9081. When the DM9081 receives a data packet from AUI1 port, the AUI1_CRS_LED pin will drive low for 52ms, then drive high at least 78ms until it responds to the next packet.

AUI2 Port Status

The AUI2_CRS_LED displays the AUI2 port status of the DM9081. When the DM9081 receives a data packet from the AUI2 port, the AUI2_CRS_LED pin will drive low for 52ms, then drive high at least 78ms until it responds to the next packet.

Minimum Mode

In minimum mode, TESTPIN0 and TESTPIN2 should be pulled low and LI/RXn (n = 0~7) pins drive the LED without using external TTL logic. The description is given below in "TP Ports Status."

TP Ports Status

The LI/RXn (n=0~7) pin sends out the status for TP ports 0-7 of the DM9081. In link test fail state, the LI/RXn pin is driven high. In link test pass, the LI/RXn pin is driven low. When TP port receives a packet, the LI/RXn pin is driven high for 78ms, then driven low at least 52ms until it responds to the next packet. An example is shown in Figure 2.

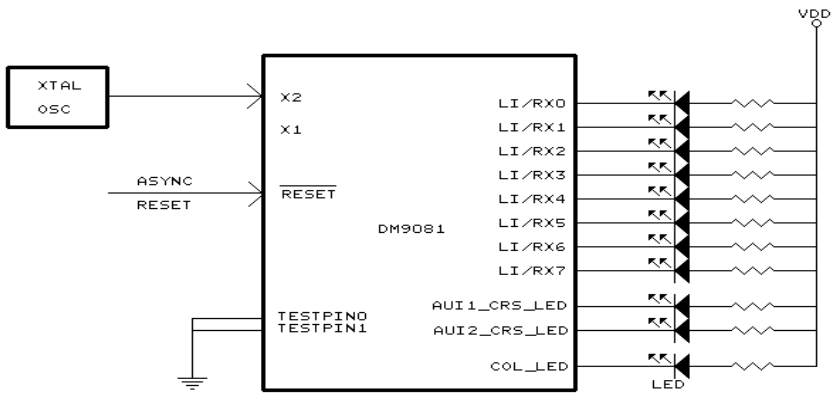


Figure 2. Minimum Mode Implementation

Normal Mode

In normal mode, TESTPIN0 and TESTPIN1 must be pulled high. The COL_LED, AUI1_CRS_LED and AUI2_CRS_LED pins are defined as minimum mode, whereas the other LED drive pins require external devices to display the status from the LED pins. These pins transmit information from the DM9081 by first sending Bit 7. A detailed timing diagram is given in Figure 3. The shift logic and latch device shown in Figure 4 is used to convert received serial data into byte- oriented data. The output data is used to drive the LED.

LED Latch

The LED_LATCH pin is used to latch the byte-oriented data. The rising edge of the TCK clock, occurring on the high state LED_LATCH, is used to strobe in the state of the following LED pins.

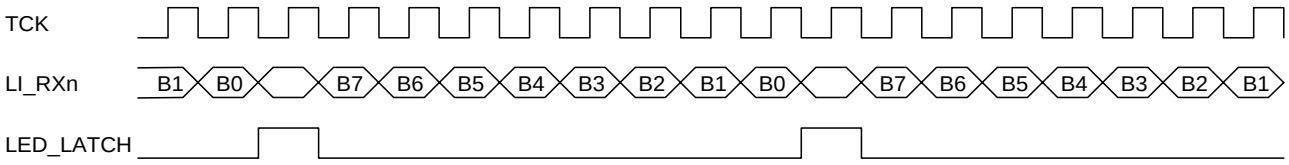


Figure 3. Serial LED Signal Timing

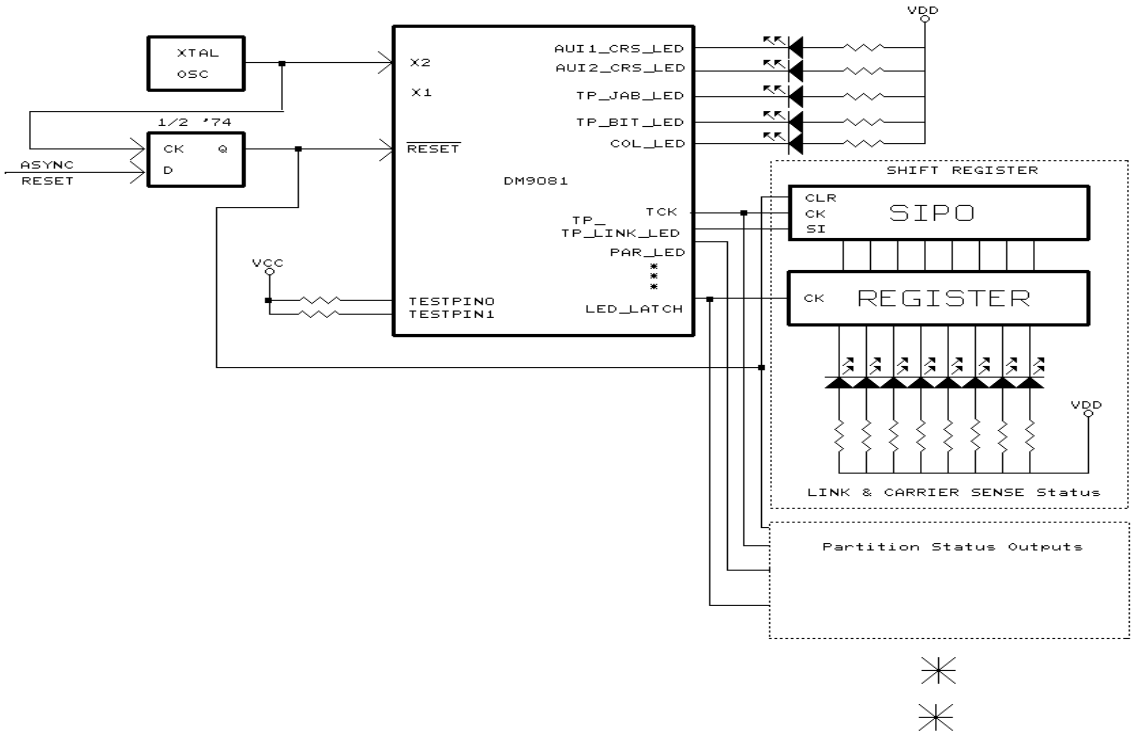


Figure 4. Normal Mode Implementation

AUI Ports Status

The AUI_LED pin transmits the status of DM9081's two AUI ports on the falling edge of TCK. Figure 5 shows a typical external hardware setup employed to convert a serial bit stream into parallel form. The accuracy of the AUI signals is within 8 Bit Times (BT). The contents of the output data for the AUI_LED are as followed:

Bit 0: AUI port 1 partition status (0: if partition)
Bit 1: AUI port 1 bit rate error status (0: if bit rate error)
Bit 2: AUI port 1 jabber status (0: if jabber)
Bit 3: AUI port 1 loopback status (0: if loopback error)
Bit 4: AUI port 2 partition status (0: if partition)
Bit 5: AUI port 2 bit rate error status (0: if bit rate error)
Bit 6: AUI port 2 jabber status (0: if jabber)
Bit 7: AUI port 2 loopback status (0: if loopback error)

TP Ports Bit Rate Error Status

The TP_BIT_LED pin sends out global bit rate error information of the DM9081's Hub.

TP Ports Jabber Status

The TP_JAB_LED pin sends out global jabber information of the DM9081's Hub.

TP Ports Partition Status

The TP_PAR_LED pin transmits partition information for the DM9081's eight TP ports on the falling edge of TCK. Figure 4 shows a typical external hardware configuration employed to convert the serial bit stream into parallel form. The accuracy of the partition signals is 8 bit. If a TP port is in partition status, its corresponding bit is set to low. The contents of the output data for the TP_PAR_LED are as followed:

Bit 0: TP port 0 partition status
Bit 1: TP port 1 partition status
Bit 2: TP port 2 partition status
Bit 3: TP port 3 partition status
Bit 4: TP port 4 partition status
Bit 5: TP port 5 partition status
Bit 6: TP port 6 partition status
Bit 7: TP port 7 partition status

Traffic Status

The TRAFFIC_LED pin transmits a utilization report for the 10MHz bandwidth on the falling edge of TCK. Figure 4 shows a typical external hardware configuration employed to convert the serial bit stream into parallel form. The accuracy of the traffic signals is 8 bit. The corresponding bit is set to low, if the following conditions are met. The contents of the output data for the TRAFFIC_LED are as followed:

Bit 0: Over 1% utilization of 10MHz bandwidth
Bit 1: Over 6.25% utilization of 10MHz bandwidth
Bit 2: Over 12.5% utilization of 10MHz bandwidth
Bit 3: Over 25% utilization of 10MHz bandwidth
Bit 4: Over 37.5% utilization of 10MHz bandwidth
Bit 5: Over 50% utilization of 10MHz bandwidth
Bit 6: Over 62.5% utilization of 10MHz bandwidth
Bit 7: Over 87.5% utilization of 10MHz bandwidth

As shown above, if all 8 bits are active low, the utilization is in excess of 87.5% for the 10MHz bandwidth.

TP Ports Link Status

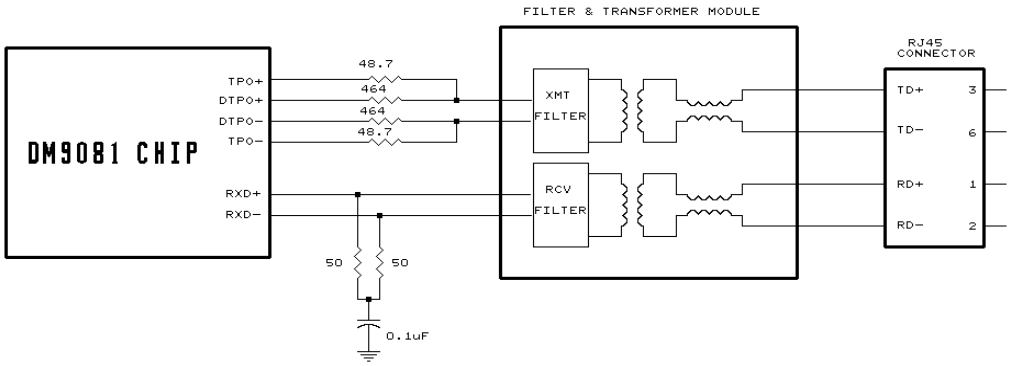
The TP_LINK_LED transmits link information for the DM9081's eight TP ports on the falling edge of TCK. Figure 5 shows a typical external hardware configuration employed to convert the serial bit stream into parallel form. The accuracy of the link signals is within 8 bit. If a TP port is line fail, its corresponding bit is set to high. If a TP port is line pass, its corresponding bit is set to low. When this port receives a packet, its corresponding bit is set high for 78ms, then driven low at least 52ms until it responds to the next packet. The contents of the output data for the TP_LINK_LED are as followed:

Bit 0: TP port 0 link/receive status
Bit 1: TP port 1 link/receive status
Bit 2: TP port 2 link/receive status
Bit 3: TP port 3 link/receive status
Bit 4: TP port 4 link/receive status
Bit 5: TP port 5 link/receive status
Bit 6: TP port 6 link/receive status
Bit 7: TP port 7 link/receive status

DM9081 Chip External Components

Figure 5 shows a typical twisted pair port external components schematic diagram. The resistor used should have a 1% tolerance to ensure compliance with 10BASE-T networks. The filters and pulse transformers are necessary devices that have a major impact on the performance and compliance of the 10BASE-T repeater ports. Specifically, the transmitted waveforms are heavily influenced by the filter characteristics, and the twisted pair receivers employ several criteria to continuously monitor the incoming signals' amplitude and timing characteristics to determine the necessity and the time to assert the internal carrier sense. For these reasons, it is crucial that the values of the resistors and the tolerances of the external components comply with given specifications. Several manufacturers produce modules that combine the functions of the transmit filters, receive filters, and pulse transformers into one package.

Figure 5. Typical Single TP Port Using External Components



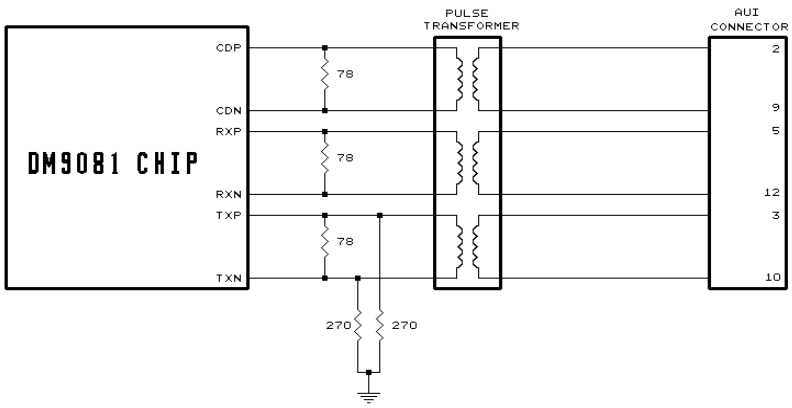


Figure 6. Typical Single AUI Port Using Components

Absolute Maximum Ratings

Absolute Maximum Ratings* (25°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC,AVCC	Supply Voltage	-0.5	7.0	V	
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	
VOUT	DC Output Voltage(VOUT)	-0.5	5.5	V	
Tc	Case Temperature Range	0	85	°C	
Tstg	Storage Temperature Rang (Tstg)	-65	150	°C	
LT	Lead Temp. (TL, Soldering, 10 sec.)	---	220	°C	
ESD	ESD Rating (Rzap=1.5K, Czap=100pF)	---	2000	V	

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VDD=5V ± 5%, Tc=0°C to 85°C, unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VIL	Input Low Voltage	-0.5		0.8	V	DGND=0.0V, Except DAT
VIH	Input High Voltage	3.0		DVDD+0.5	V	Except DAT
VOL	Output Low Voltage	-		0.4	V	IOL=4mA
VOH	Output High Voltage	3.5		-	V	IOH=-4mA
IIL	Input Leakage Current (also DAT as Input)	-		10	uA	DGND<VIN<DVDD
VILX	X2 Crystal Input Low Voltage	-0.5		1.0	V	DGND=0.0V
VIHX	X2 Crystal Input High Voltage	3.8		DVDD+0.5	V	DGND=0.0V
IILX	Crystal Input Low Current	-		10	uA	VIN=DGND
IIHX	Crystal Input High Current	-		10	uA	VIN=DVDD
AUI Port						
VOD	Differential Output Voltage (TXP, TXN)	550		1200	mV	78Ω termination, and 270Ω from each to GND
VOB	Differential Output Voltage Imbalance (TXP, TXN)	-		40	mV	78Ω termination, and 270Ω from each to GND
VU	Undershoot Voltage (TXP, TXN)	-		100	mV	78Ω termination, and 270Ω from each to GND
VDS	Differential Squelch Threshold (RXP/RXN and CDP/CDN)	175		300	mV	Negative pulse
VCM	Differential Input Common Mode Voltage (RXP/RXN and CDP/CDN)			VDD/2	V	
Twisted Pair Port						
VTIDF	TP Input Voltage	350		2000	mV	

VOL VOH	**TPO+/TPO-/DTPO+/DTPO-:** Low High	- 4.9		0.1 -	V V	
DC Output Series Impedance:						
RTP0	TP Drives	-		10	Ω	
RTPI	RXD+/RXD- Input Resistance	16		24	KΩ	
Power Supply Current						
IDD	Power Supply Current (idle)	-	130	-	mA	
	Power Supply Current (Transmitting with TP Port load)	-	240	-	mA	

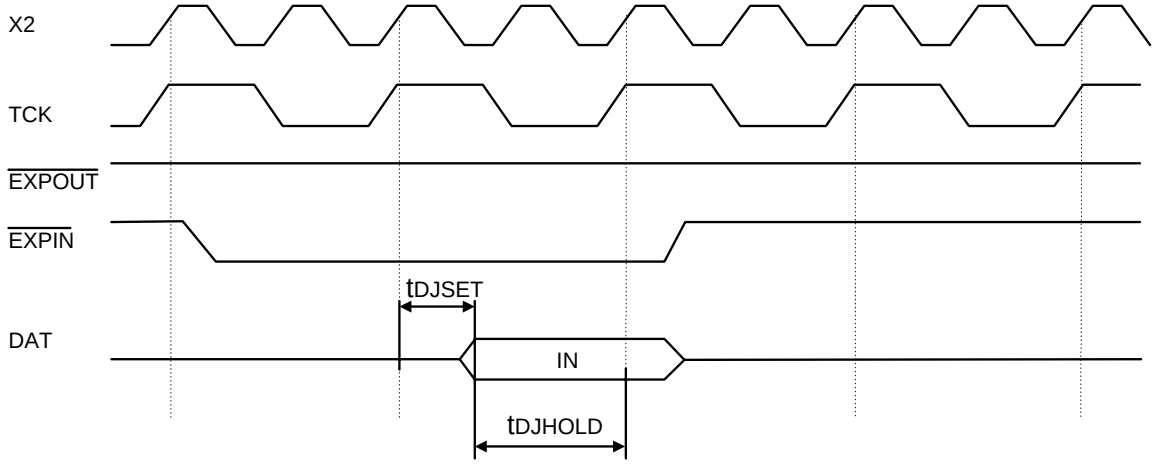
AC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
AUI Port						
TCB	Collision Turn-on Time	0		900	ns	
TCE	Collision Turn-off Time	0		900	ns	
tCIDL	CDP High To Idle Time	250		350	ns	
tCPH	Collision High-Pulse Width	40	50	60	ns	
tCP	Collision Period	80	100	120	ns	
tRIDL	RXP High To Idle Time	250		350	ns	
Twisted Pair Port						
tTPDY	DTPO- To TPO+ & DTPO+ To TPO- Delay	47		53	ns	
tRD	Receive Delay From RXD To RXP/RXN	0		500	ns	
tROFF	RXD+ High To Idle Time	200			ns	
tLP	Transmitted Link Integrity Pulse Period	8	16	24	ms	
tLPWT	Link Integrity Pulse Width For TPO+	80	100	120	ns	
tLPWD	Link Integrity Pulse Width For DTPO	40	50	60	ns	
Jabber Timing						
tJMT	Maximum Transmit Time for TPO	45	50	55	ms	
tJCB	Time from Jabber to Enable CI Output	0		900	ms	
tJU	Unjab Time	250	450	750	ms	

Timing Waveforms

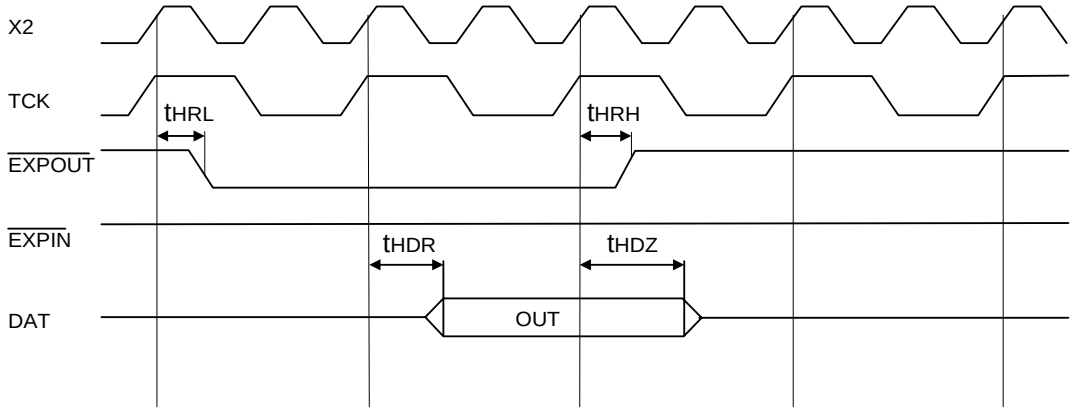
Expansion Port Input Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tDJSET	DAT Setup Time	-		20	ns	
tDJHOLD	DAT Hold Time	60		-	ns	



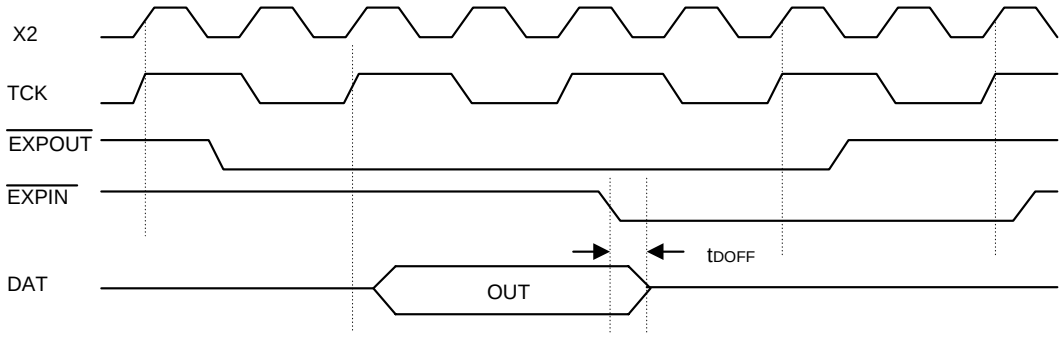
Expansion Port Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tHRL	TCK Rising Edge to EXPOUT# Driven Low	-		20	ns	CL=100pF
tHRH	TCK Rising Edge to EXPOUT# Driven High	-		20	ns	CL=100pF
tHDR	TCK Rising Edge to DAT Driven	-		20	ns	CL=100pF
tHDZ	TCK Rising Edge to DAT Not Driven	-		20	ns	CL=100pF



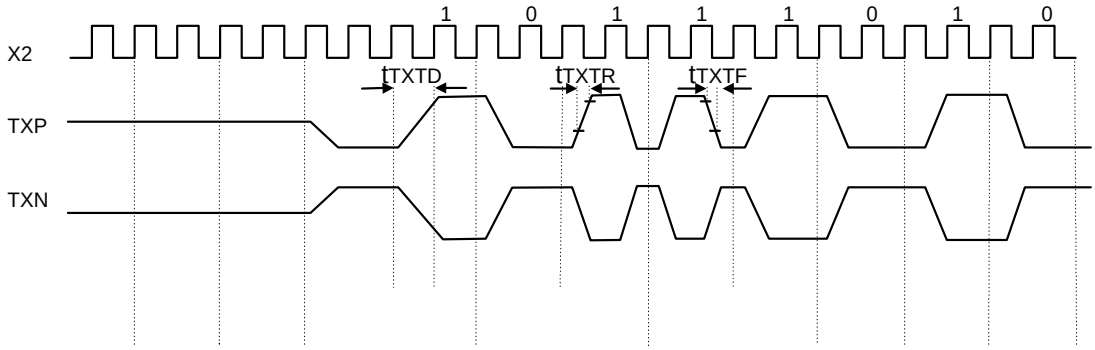
Expansion Port Collision Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{DOFF}	DAT Data Off	-		20	ns	CL=100pF



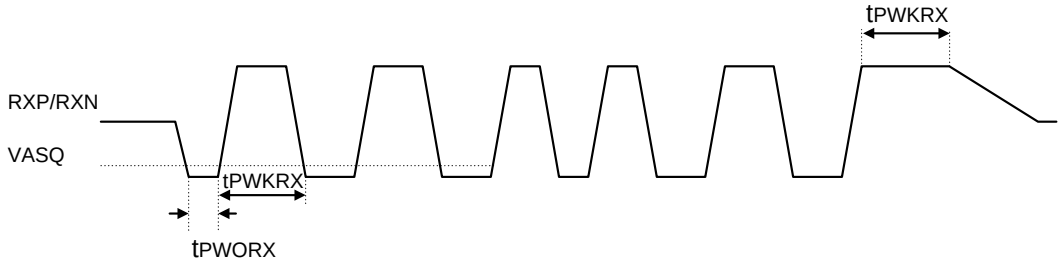
AUI Transmit Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{TXTD}	X2 Rising Edge To TXP/TXN Toggle	-		30	ns	
t_{TXTR}	TXP, TXN Rise Time (10% to 90%)	2.5		5.0	ns	
t_{TXTF}	TXP, TXN Fall Time (90% to 10%)	2.5		5.0	ns	
t_{TXRM}	TXP, TXN Rise & Fall Time Mismatch	-		1.0	ns	



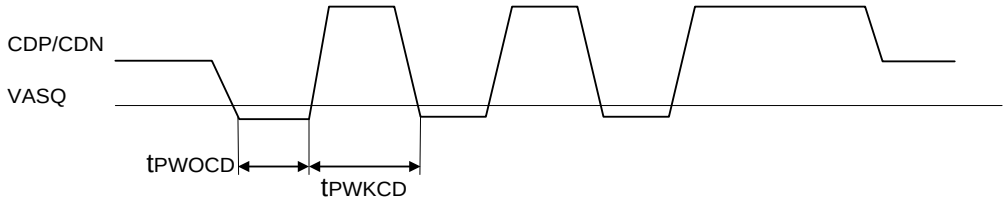
AUI Receive Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tPWORX	RXP/RXN Pulse Width Accept/Reject Threshold	15		45	ns	|VIN|>|VASQ|
tPWKRX	RXP/RXN Pulse Width Maintain/Turn-Off Threshold	136		200	ns	|VIN|>|VASQ|



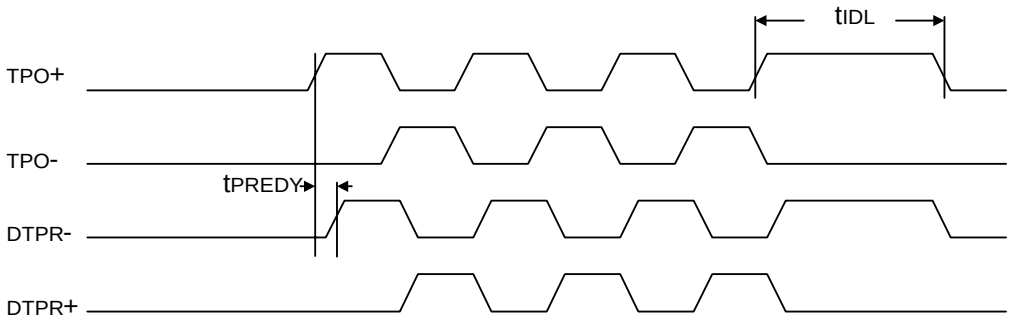
AUI Collision Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tPWOCD	CDP/CDN Pulse Width Accept/Reject Threshold	10		26	ns	|VIN|>|VASQ|
tPWKCD	CDP/CDN Pulse Width Maintain/Turn-off Threshold	90		160	ns	|VIN|>|VASQ|



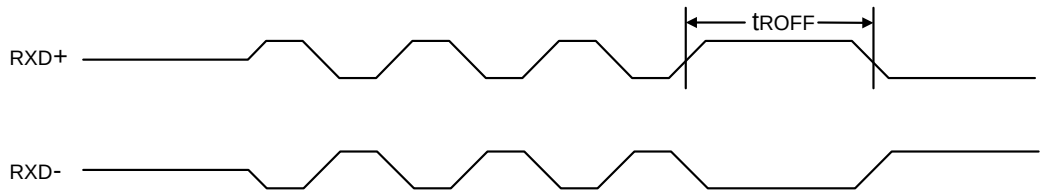
Transmit Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tPREDY	DTPO- to TPO+ and DTPO+ To TPO- Delay	47		53	ns	
tIDL	TPO+ High To Idle Time	250		350	ns	



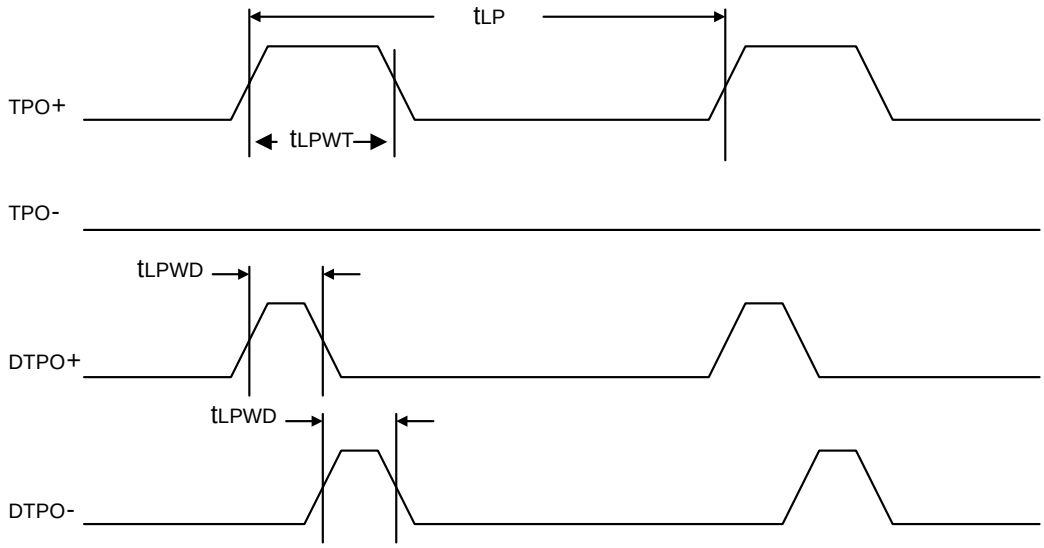
Receive Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tROFF	RXD+ High To Idle Time	200			ns	



Link Integrity Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tLP	Transmitted Link Integrity Pulse Period	8	16	24	ms	
tLPWT	Link Integrity Pulse Width For TPO+	80	100	120	ns	
tLPWD	Link Integrity Pulse Width For DTPO+/-	40	50	60	ns	



Layout Recommendation

Decoupling

The DM9081 contains both analog and digital elements. Separate power pins are provided for the analog sections, the digital portion of TP line drivers, the TP line drivers, and the digital core logic. Care should be taken in board design to minimize coupling of noise from the power supply and digital logic to the analog power pins. Decoupling capacitors should be placed as close to the appropriate VDD and GND pins as possible. Figure 7 shows the recommended decoupling values for the DM9081 chip.

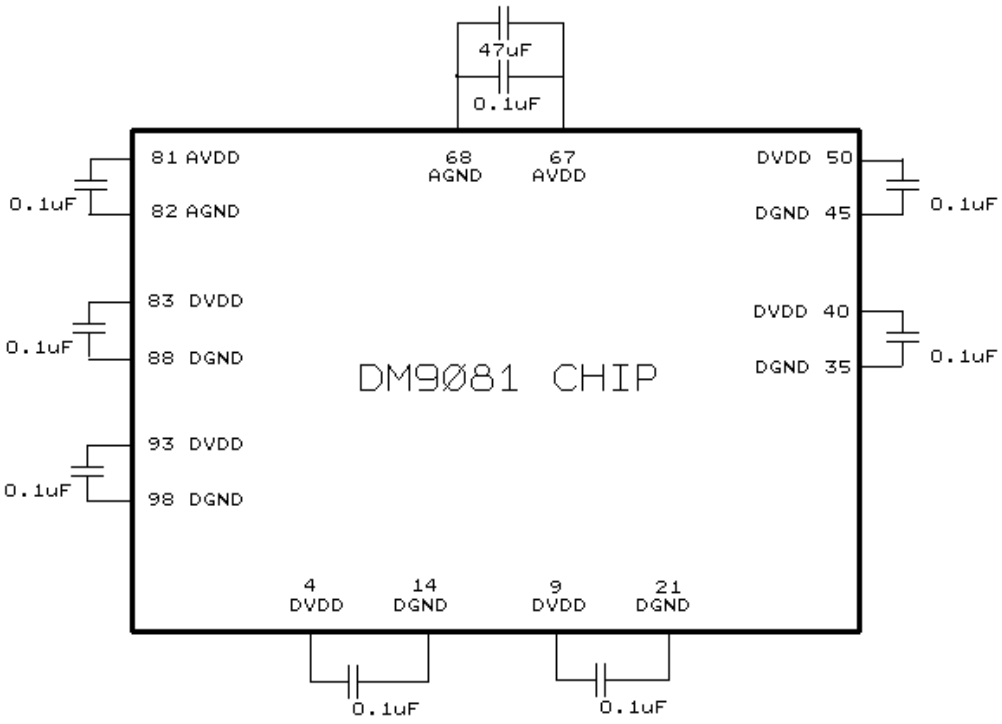


Figure 7. DM9081 Device Power Supply Decouping Recommendations

Power Plane

The board power planes must be separated into analog and digital portions. The +5V and ground planes can be laid out according to the configuration shown in Figure 8. The analog portion should be located under the analog power pins of the DM9081 chip and the AUI logic. The digital portion should be located close enough to the 10BASE-T filter to attach a 0.1mF capacitor to the filter ground pin. Extending the digital power plane under the 10BASE-T filter is not recommended. The analog and digital power planes should be connected at a single point with either a 1.8-2.2Ω or 120Z ferrite bead. In the diagram below, a 47mF capacitor is used in parallel with a 0.1mF capacitor to connect the analog and digital planes. Shielded RJ-45 connectors are recommended. The shielded pins should be tied to the frame ground. Depending on the characteristics of the 10BASE-T filter, either the frame ground or a void in the planes should be extended under the filters. Consult the filter manufacturer to determine if the frame ground is needed to minimize the effects of cross-talk within the filters.

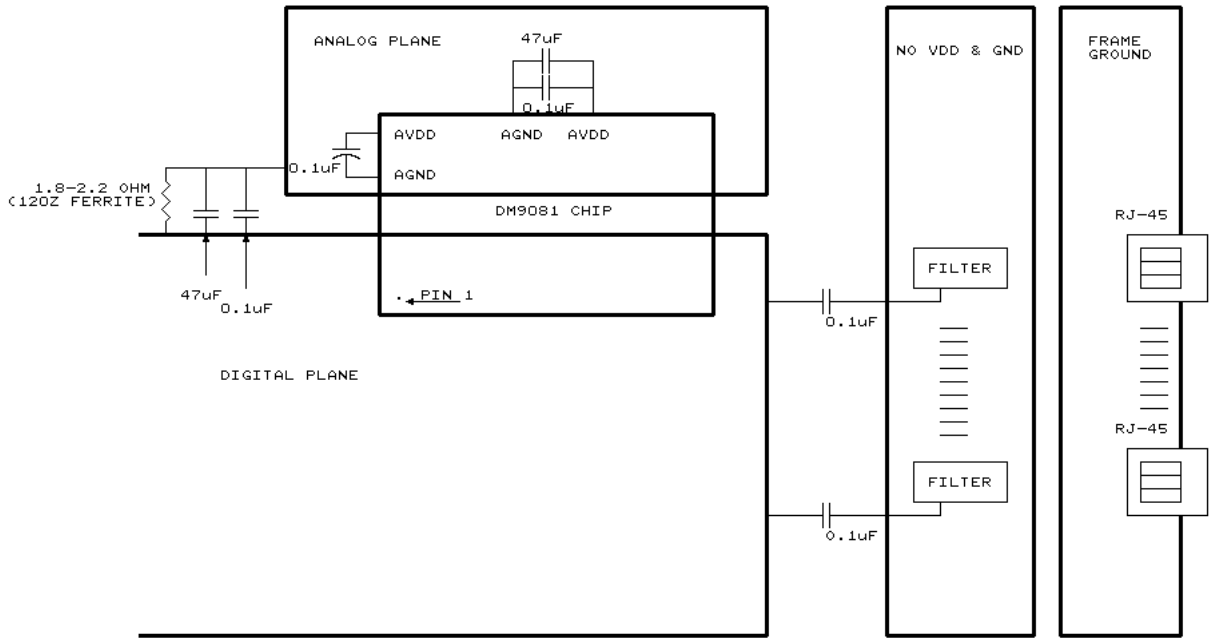
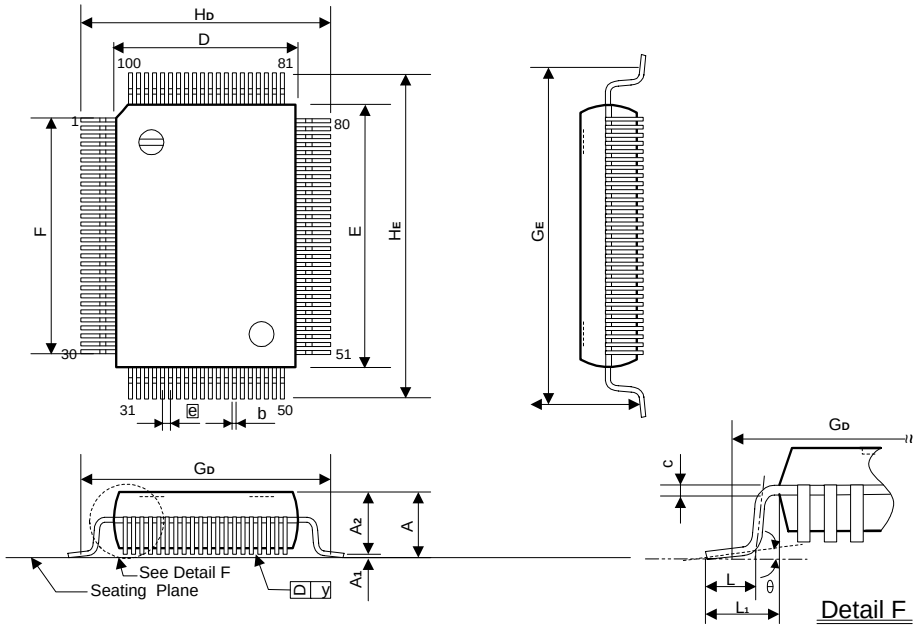


Figure 8. DM9081 Device Power Plane Recommendations

Package Information

QFP 100L Outline Dimensions Unit: Inches/mm



Symbol	Dimensions In Inches	Dimensions In mm
A	0.130 Max.	3.30 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.112±0.005	2.85±0.13
b	0.012 +0.004 -0.002	0.31 +0.10 -0.05
c	0.006 +0.004 -0.002	0.15 +0.10 -0.05
D	0.551±0.005	14.00±0.13
E	0.787±0.005	20.00±0.13
e	0.026 ±0.006	0.65±0.15
F	0.742 NOM.	18.85 NOM.
G_D	0.693 NOM.	17.60 NOM.
G_E	0.929 NOM.	23.60 NOM.
H_D	0.740±0.012	18.80±0.31
H_E	0.976±0.012	24.79±0.31
L	0.047±0.008	1.19±0.20
L_1	0.095±0.008	2.41±0.20
y	0.006 Max.	0.15 Max.
θ	0° ~ 12°	0° ~ 12°

Note:

1. Dimensions D&E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.
3. All dimensions are based on metric system.

Ordering Information

Part Number	Pin Count	Package
DM9081F	100	QFP
DM9081FP	100	QFP (Pb-Free)

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