

STRUCTURE	Silicon Monolithic Integrated Circuit
Type	6 Channel Switching Regulator control system
PRODUCT SERIES	<b>BD9839MWV</b>
PHYSICAL DIMENSIONS	Fig. 1 (Plastic Mold)
BLOCK DIAGRAM	Fig. 2
FEATURES	<ul style="list-style-type: none"> <li>● Step Down 5CH, Step Up 1CH total 6CH included.</li> <li>● FET 4ch (CH1~CH4) for Synchronous Switching Regulator</li> <li>● Short Circuit Protection (SCP)</li> <li>● Under Voltage Lockout Function (UVLO)</li> <li>● Thermal Shut Down Function (TSD)</li> <li>● Independent ON/OFF Function Each Channel(Stand_by Current Is Under 5uA)</li> <li>● UQFN056V7070 Package</li> </ul>

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Units
Power Supply Voltage	VCC,PVCC1~6	12	V
Input Voltage	BOOT1~4	17.5	V
	Lx1~4,OUT5,6	12	V
BOOT-Lx Voltage	$\Delta$ BOOT1~4	6.5	V
Power Dissipation	Pd	420(*1)	mW
		930(*2)	mW
Operating Temperature	Topr	-30~+85	°C
Storage Temperature	Tstg	-55~+125	°C
Junction Temperature	Tjmax	125	°C

(\*1) Without external heat sink, the power dissipation degrades by 4.2mW/°C above 25°C.

(\*2) Power dissipation degrades by 9.3mW/°C above 25°C, when mounted on a PCB (74.2mm × 74.2mm × 1.6mm).

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Spec.			Units
		Min	Typ	Max	
Power Supply Voltage	VCC,PVCC1~56	4	7	11	V
	BOOT1~4	3.5	-	16	V
BOOT-Lx Voltage	$\Delta$ BOOT1~4	3.5	-	5.0	V
CH1~4 H NMOS Drain Current	Idhnl	-	-	1.5(*3)	A
CH1~4 L NMOS Drain Current	Idlnl	-	-	1.5(*3)	A
Frequency Stability (*4)	fosc	300	500	2000	kHz
VREGA - GND Capacitor	CVREGA	0.47	1.0	2.2	uF
VCC - VREGD Capacitor	CVREGD	0.47	1.0	2.2	uF
BOOT - Lx Capacitor	CBOOT	0.047	0.1	0.22	uF

(\*3) FET Drain Current Max value. Set the current value within Power dissipation in the application.

(\*4) Max 1MHz for Ch1 ~ Ch4.

Status of this document

The Japanese language version of this document shall be the official specification.

Any translation of this document shall be for reference only.

● Electrical Characteristics (Ta=25°C, VCC=7V, fosc=500kHz with no designation)

Parameter	Symbol	Limits			Units	Condition
		Min	Typ	Max		
[Whole Device]						
Standby Current	Ist	-	0.1	5	μA	
Circuit Current	Icc	-	60	90	mA	FB=0V
[Reference Voltage]						
Output Voltage	VREGA	2475	2500	2525	V	VREGA=1mA
Line regulation	ΔVi	-	-	10	mV	VCC=4V~10V, VREGA=1mA
Load regulation	ΔVlo	-	-	10	mV	VREGA=1mA~5mA
Output current at VREGA pin shorted	Ios	-30	-	-5	mA	VREGA=0V
[Bias Voltage]						
Output Voltage	VREGD	490	500	510	V	VREGD=10mA
[Oscillator]						
Oscillator Frequency CH1~6	fosc	450	500	550	kHz	RT=10kΩ, CT=220pF, SEL="L"
Oscillator Frequency coefficient	Df	-	0	2	%	VCC=4V~10V
[Current Mode Circuit]						
Minimum OFF time of H Nch(CH1)	Toffmin1	-	-	100	nsec	
Minimum OFF time of H Nch(CH2)	Toffmin2	-	-	100	nsec	
Minimum OFF time of H Nch(CH3)	Toffmin3	-	-	100	nsec	
Minimum OFF time of H Nch(CH4)	Toffmin4	-	-	100	nsec	
SEL control voltage	VSELH	2	-	VCC	V	(fosc=fosc/2) (CH1~4)
	VSELL	-0.3	-	0.8	V	
[PWM Comparator]						
0% Duty threshold(CH5/6)	Vt0	100	110	-	V	
100% Duty threshold(CH5)	Vt100	-	160	170	V	
MAX Duty cycle CH6	Dmax6	81	90	99	%	
[ERRORAMP1](CH1)						
Threshold Voltage	VETH	0.700	0.800	0.810	V	
Output Voltage L	VOL	-	0.03	0.2	V	INV=0.9V
Output Voltage H	VOH	2.2	2.4	-	V	INV=0.7V
Output Sink Current	ISINK	1.8	3.6	-	mA	INV=0.9V, FB=1.25V
Output Source Current	ISOURCE	-	-100	-50	μA	INV=0.7V, FB=1.25V
Input Bias Current	IBIAS	-150	-50	-	nA	INV=0V
Voltage Gain	AV	60	80	-	dB	Open loop gain
Frequency Bandwidth	BW	1	4	-	MHz	
[ERRORAMP2](CH2~5)						
Threshold Voltage	VETH	0.990	1.000	1.010	V	
Output Voltage L	VOL	-	0.03	0.2	V	INV=1.1V
Output Voltage H	VOH	2.2	2.4	-	V	INV=0.9V
Output Sink Current	ISINK	1.8	3.6	-	mA	INV=1.1V, FB=1.25V
Output Source Current	ISOURCE	-	-100	-50	μA	INV=0.9V, FB=1.25V
Input Bias Current	IBIAS	-150	-50	-	nA	INV=0V
Voltage Gain	AV	60	80	-	dB	Open loop gain
Frequency Bandwidth	BW	1	4	-	MHz	
[ERRORAMP3](CH6)						
Threshold Voltage	VETH	0.285	0.300	0.315	V	
Output Voltage L	VOL	-	0.03	0.2	V	INV=0.4V
Output Voltage H	VOH	2.2	2.4	-	V	INV=0.2V
Output Sink Current	ISINK	1.8	3.6	-	mA	INV=0.4V, FB=1.25V
Output Source Current	ISOURCE	-	-100	-50	μA	INV=0.2V, FB=1.25V
Input Bias Current	IBIAS	-150	-50	-	nA	INV=0V
Voltage Gain	AV	60	80	-	dB	Open loop gain
Frequency Bandwidth	BW	1	4	-	MHz	
[Driver 部]						
Lx Pull-down resistor(CH1~CH4)	RLx	300	500	700	Ω	CTL=0V
Simultaneous off time setting(CH1~CH4)	TUPPER	-	25	50	nsec	
	TLOWER	-	25	50	nsec	
H Nch resistor(CH1)	RonH1	-	0.38	0.65	Ω	Lx1=50mA
L Nch resistor(CH1)	RonL1	-	0.18	0.31	Ω	Lx1=50mA
H Nch resistor(CH2)	RonH2	-	0.28	0.48	Ω	Lx2=50mA
L Nch resistor(CH2)	RonL2	-	0.28	0.48	Ω	Lx2=50mA
H Nch resistor(CH3)	RonH3	-	0.27	0.46	Ω	Lx3=50mA
L Nch resistor(CH3)	RonL3	-	0.22	0.37	Ω	Lx3=50mA
H Nch resistor(CH4)	RonH4	-	0.28	0.48	Ω	Lx4=50mA
L Nch resistor(CH4)	RonL4	-	0.28	0.48	Ω	Lx4=50mA
Output ON resistor(CH5)	RonH5	-	9	16	Ω	IOUT5=15mA
	RonL5	-	9	16	Ω	IOUT5=15mA
Output ON resistor(CH6)	RonH6	-	9	16	Ω	IOUT6=15mA
	RonL6	-	9	16	Ω	IOUT6=15mA
[Control Block]						
CTL vd	ON	VCTLH	2	-	VCC	V
	OFF	VCTL	-0.3	-	0.8	V
CTL1~6 Pull-down resistor	RCTL	250	400	700	kΩ	
[Soft Start Block]						
Standby Voltage	Vstsc	-	10	100	mV	
Input Charge Current	ISOFT	-14	-10	-0.6	μA	SOFT1~6=0.1V
[Short Circuit Protection (SCP) Timer]						
Timer Start Voltage	Vtime	2.1	2.2	2.3	V	FB1~6 voltage
Threshold Voltage	Vtsc	0.9	1.0	1.1	V	
Source Current	Iscp	-14	-10	-0.6	μA	SCP=0.1V
Standby Voltage	Vstsc	-	10	100	mV	
[Short Circuit Detective Comparator]						
Threshold Voltage	VTH	0.95	1.0	1.05	V	
Input Bias Current	IBIAS	-15	-10	-5	μA	SCP1=0V
[Under Voltage Lockout (UVLO)]						
Threshold Voltage1	Vstd1	3.3	3.4	3.5	V	VCC voltage
Hysteresis Voltage	ΔVst	25	100	200	mV	VCC voltage
Threshold Voltage2	Vstd2	1.8	2.0	2.2	V	VREGA voltage
Threshold Voltage3	Vstd3	2.8	3.0	3.2	V	VREGD voltage



## ● Operation Notes

### 1.) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

### 2.) GND potential

Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena.

### 3.) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

### 4.) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.

### 5.) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

### 6.) Common impedance

Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

### 7.) Voltage of CTL pin

The threshold voltages of CTL pin are 0.8V and 2.0V. STB state is set below 0.8V while action state is set beyond 2.0V.

The region between 0.8V and 2.0V is not recommended and may cause improper operation.

The rise and fall time must be under 10msec. In case to put capacitor to STB pin, it is recommended to use under 0.01  $\mu$ F.

### 8.) Thermal shutdown circuit (TSD circuit)

This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

### 9.) Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits.

For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.

### 10.) Relationship between PVCC - VCC

Because diode was connecting between PVCC (Anode) - VCC (Cathode) for prevent electrostatic breakdown, it must be set PVCC - VCC < 0.3V voltage relationship.

### 11.) Rush current at the time of power supply injection.

An IC which has plural power supplies, or CMOS IC could have momentary rush current at the time of power supply injection.

Because there exists inside logic uncertainty state. Please take care about power supply coupling capacity and width of power supply and GND pattern wiring.

### 12.) Please use it so that VCC and PVCC terminal should not exceed the absolute maximum ratings. Ringing might be caused by L element of the pattern

according to the position of the input capacitor, and ratings be exceeded. Please will assume the example of the reference, the distance of IC and capacitor, use it by 5.0mm or less when thickness of print pattern are 35 $\mu$ m, pattern width are 1.0mm.

### 13.) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

### 14.) IC pin input

This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated.

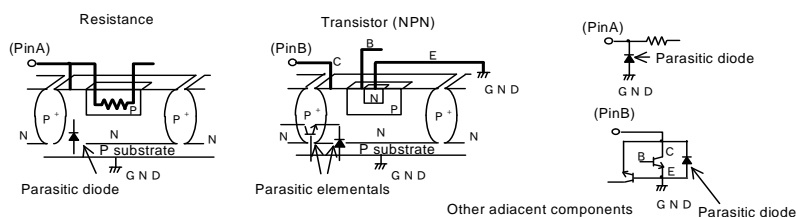
P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when a resistor and transistor are connected to pins as shown in following chart,

○ the P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).

○ Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.



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