

Structure	Silicon Monolithic IC
Products	High side switch IC
Type	BD82065FVJ
Features	Low on resistance 70mΩ MOSFET Switch 1A Continuous current load Active “High” control logic Soft start circuit Over current detection Thermal shutdown Under voltage lockout Open drain error flag output Reverse-current protection when power switch off TSSOP-B8J Package ESD protection

◇Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{IN}	-0.3 ~ 6.0	V
Enable voltage	V _{EN}	-0.3 ~ 6.0	V
/OC voltage	V _{/OC}	-0.3 ~ 6.0	V
/OC sink current	I _{S/OC}	~ 5	mA
OUT voltage	V _{OUT}	-0.3 ~ 6.0	V
Storage temperature	T _{STG}	-55 ~ 150	°C
Power dissipation	PD	587.5 *1	mW

*1 Mounted on 70mm*70mm*1.6mm glass-epoxy PCB. Derating : 4.7mW/°C above Ta=25°C.

* This product is not designed for protection against radioactive rays.

◇Operating conditions

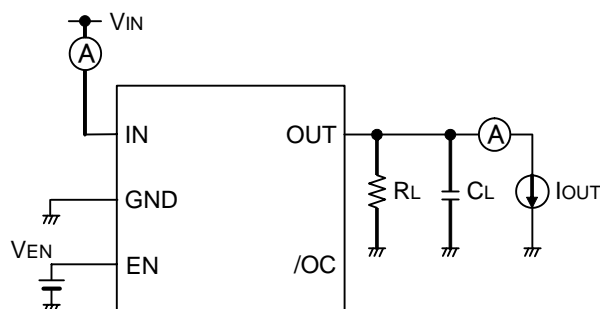
Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating voltage	V _{IN}	2.7	-	5.5	V
Operating temperature	T _{OPR}	-40	-	85	°C
Continuous output current	I _{OUT}	0.0	-	1.0	A

◇Electric characteristics

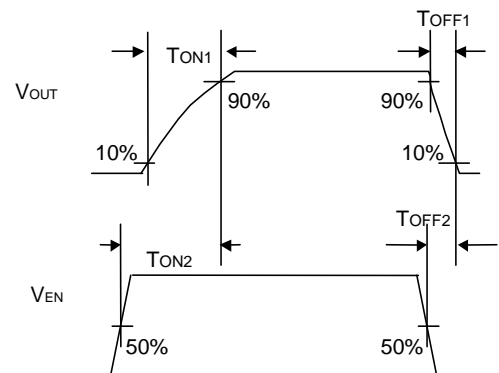
Unless otherwise specified $V_{IN} = 5.0V$, $T_a = 25^\circ C$

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current consumption						
Operating Current	I_{DD}	-	110	160	μA	$V_{EN} = 5V$, $V_{OUT} = \text{Open}$
Standby Current	I_{STB}	-	0.01	1	μA	$V_{EN} = 0V$, $V_{OUT} = \text{Open}$
I/O						
EN input voltage	V_{EN}	2.0	-	-	V	High input
	V_{EN}	-	-	0.8	V	Low input
EN input current	I_{EN}	-1.0	0.01	1.0	μA	$V_{EN} = 0V$ or $5V$
/OC output LOW voltage	$V_{/OC}$	-	-	0.5	V	$I_{/OC} = 0.5mA$
/OC output leak current	$I_{L/OC}$	-	0.01	1	μA	$V_{/OC} = 5V$
/OC delay time	$T_{/OC}$	10	15	20	ms	
Power switch						
ON resistance	R_{ON}	-	70	110	$m\Omega$	$I_{OUT} = 500mA$
Current Limit Threshold	I_{TH}	1.5	2.4	3.0	A	
Short-circuit current	I_{SC}	1.1	1.5	2.1	A	$V_{OUT} = 0V$, $C_L = 47\mu F$ RMS
Output rise time	T_{ON1}	-	0.8	10	ms	$R_L = 10\Omega$
Output rise delay time	T_{ON2}	-	1.1	20	ms	$R_L = 10\Omega$
Output fall time	T_{OFF1}	-	5	20	μs	$R_L = 10\Omega$
Output fall delay time	T_{OFF2}	-	10	40	μs	$R_L = 10\Omega$
Switch leak current	$I_{L_{SW}}$	-	-	1.0	μA	$V_{EN} = 0V$, $V_{OUT} = 0V$
Reverse leak current	$I_{L_{REV}}$	-	-	1.0	μA	$V_{OUT} = 5.5V$, $V_{IN} = 0V$
UVLO						
UVLO Threshold	V_{TUVH}	2.1	2.3	2.5	V	Increasing V_{IN}
	V_{TUVL}	2.0	2.2	2.4	V	Decreasing V_{IN}

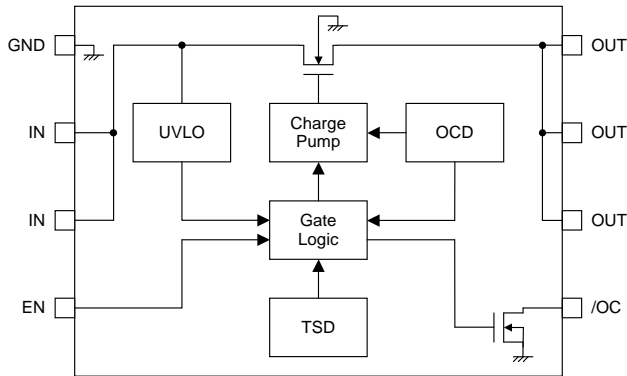
◇Measurement circuit



◇Timing chart at output rise / fall time



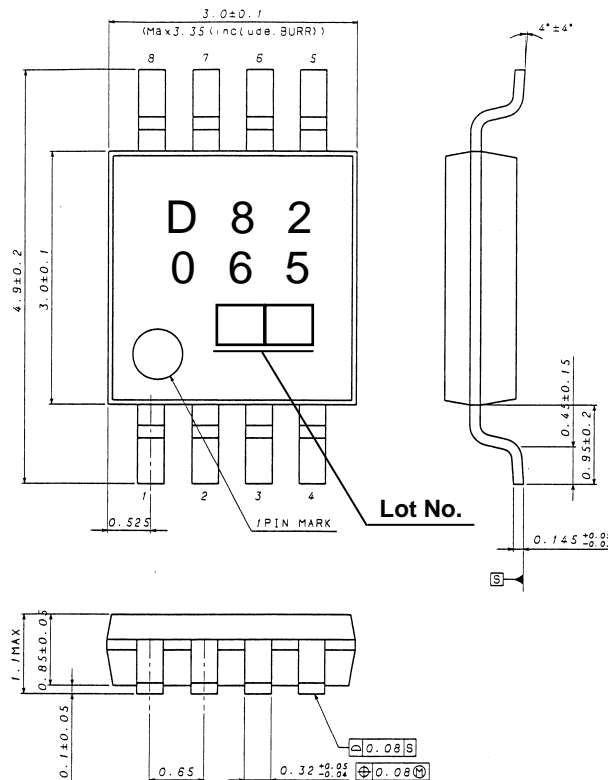
◇Block diagram



◇Pin description

Pin No.	Pin Name	Function
1	GND	Ground
2,3	IN	Power supply input. Input terminal to the power switch and power supply input terminal of the internal circuit.
4	EN	Enable input. Power switch on at High level.
5	/OC	Over current output. Low level at over current, over temperature detection. Open drain output.
6,7,8	OUT	Power switch output.

◇Package



TSSOP-B8J
(Unit : mm)

- Cautions on use

- (1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

- (2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

- (3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

- (4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

- (5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

- (6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

- (7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

- (8) Thermal shutdown circuit (TSD)

When junction temperatures become 170°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

- (9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

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