Data Sheet | May 28, 2009 | FN6826.1

Triple Analog Video Delay Lines

The ISL59920, ISL59921, ISL59922, and ISL59923 are triple analog delay lines that provide skew compensation between three high-speed signals. These parts are ideal for compensating for the skew introduced by a typical CAT-5, CAT-6 or CAT-7 cable (with differing electrical lengths on each twisted pair) when transmitting analog video.

Using a simple serial interface, the ISL59920, ISL59921, ISL59922, and ISL59923's delays are programmable in steps of 2, 1.5, 1, or 2ns (respectively) for up to a total delay of 62, 46.5, 31, or 30ns (respectively) on each channel. The gain of the video amplifiers can be set to x1 (0dB) or x2 (6dB) for back-termination. The delay lines require a ±5V supply.

Features

- 30, 31, 46.5, or 62ns Total Delay
- 1.0, 1.5, or 2.0ns Delay Step Increments
- Very Low Offset Voltage
- Drop-in Compatible with the EL9115
- Low Power Consumption
- 20 Ld QFN Package
- Pb-Free (RoHS Compliant)

Applications

- Skew Control for RGB Video Signals
- Generating Programmable High-speed Analog Delays

Ordering Information

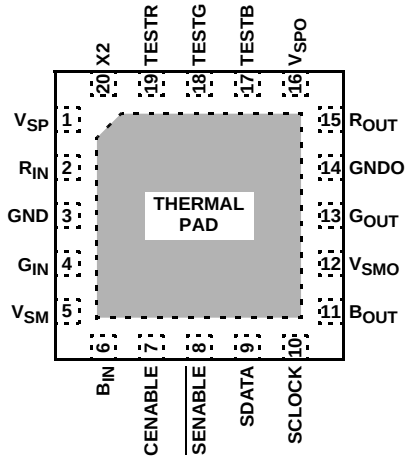
PART NUMBER (Note)	PART MARKING	MAX DELAY (ns)	DELAY STEP SIZE (ns)	TYPICAL POWER DISSIPATION (mW)	PACKAGE (Pb-free)	PKG. DWG. #
ISL59920IRZ*	59920 IRZ	62	2.0	645	20 Ld 5mmx5mm QFN	L20.5x5C
ISL59921IRZ*	59921 IRZ	46.5	1.5	645	20 Ld 5mmx5mm QFN	L20.5x5C
ISL59922IRZ*	59922 IRZ	31	1.0	645	20 Ld 5mmx5mm QFN	L20.5x5C
ISL59923IRZ*	59923 IRZ	30	2.0	540	20 Ld 5mmx5mm QFN	L20.5x5C

*Add "-T7" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL59920, ISL59921, ISL59922, ISL59923
(20 LD 5X5 QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_S+ to V_S-) 12V
Maximum Output Current. . . . . ±60mA
Storage Temperature Range . . . . . .-65°C to +150°C
ESD Classification
Human Body Model 3000V
Machine Model 300V
Charged Device Model 1200V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
20 Lead QFN 31
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Operating Junction Temperature . . . . . .+135°C
Ambient Operating Temperature . . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

$V_{SP} = V_{SPO}$ = +5V, $V_{SM} = V_{SMP}$ = -5V, GAIN = 2, T_A = +25°C, exposed die plate = -5V, x2 = 5V, R_{LOAD} = 150Ω on all video outputs, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
d_t	Nominal Delay Increment (Note 2)	ISL59920	1.8	2	2.2	ns
		ISL59921	1.4	1.5	1.7	ns
		ISL59922	0.9	1	1.2	ns
		ISL59923	1.8	2	2.3	ns
t_{MAX}	Maximum Delay	ISL59920	55	62	68	ns
		ISL59921	42.5	46.5	53.5	ns
		ISL59922	26.5	31	38.5	ns
		ISL59923	26.5	30	34.5	ns
D_{ELDT}	Delay Difference Between Channels for Same Delay Settings On All Channels			1		ns
t_{PD}	Propagation Delay	ISL59920, ISL59923, measured input to output, delay setting = 0ns		10		ns
		ISL59921, measured input to output, delay setting = 0ns		8		ns
		ISL59922, measured input to output, delay setting = 0ns		7		ns
BW -3dB	3dB Bandwidth, 0ns Delay Time	ISL59920, ISL59923		153		MHz
		ISL59921		200		MHz
		ISL59922		230		MHz
BW ±0.1dB	±0.1dB Bandwidth, 0ns Delay Time	ISL59920, ISL59923		50		MHz
		ISL59921		60		MHz
		ISL59922		50		MHz
SR	Slew Rate	ISL59920, 20-80, delay = 0ns		550		V/µs
		ISL59921, 20-80, delay = 0ns		640		V/µs
		ISL59922, 20-80, delay = 0ns		700		V/µs
		ISL59923; 20-80, delay = 0ns		550		V/µs

Electrical Specifications $V_{SP} = V_{SPO} = +5V$, $V_{SM} = V_{SMP} = -5V$, GAIN = 2, $T_A = +25°C$, exposed die plate = -5V, x2 = 5V, $R_{LOAD} = 150\Omega$ on all video outputs, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
t_R - t_F	Transient Response Time	ISL59920, 20% to 80%, for any delay, 1V step delay = 0ns		1.7		ns
		ISL59921, 20% to 80%, for any delay, 1V step delay = 0ns		1.6		ns
		ISL59922, 20% to 80%, for any delay, 1V step delay = 0ns		1.43		ns
		ISL59923, 20% to 80%, for any delay, 1V step delay = 0ns		1.7		ns
V_{OVER}	Voltage Overshoot	For any delay, response to 1V step input		4		%
Glitch	Switching Glitch	Output settling time from last SCLK edge		100		ns
THD	Total Harmonic Distortion	$1V_{P-P}$ 10MHz sinewave, offset by +0.2V at mid delay setting		-43	-38	dB
X	Crosstalk	Stimulate G, measure R/B at 1MHz, ISL59920, ISL59921, ISL59923		-80	-63	dB
		ISL59922		-78	-59	dB
V_N	Output Noise	Bandwidth = 150MHz		2		mV_{RMS}
G_0	Gain Zero Delay		1.74	1.8	1.92	V/V
G_m	Gain Mid Delay		1.67	1.8	1.97	V/V
G_f	Gain Full Delay		1.6	1.8	2	V/V
DG_m0	Difference in Gain, 0 to Mid		-8	0.6	7.5	%
DG_f0	Difference in Gain, 0 to Full		-12	-1.8	10	%
DG_fm	Difference in Gain, Mid to Full		-10	-1.7	7.5	%
V_{IN}	Input Voltage Range	ISL59920, Gain remains > 90% of nominal, Gain = 2	-0.7		1.1	V
		ISL59921, Gain remains > 90% of nominal, Gain = 2	-0.7		1.04	V
		ISL59922, Gain remains > 90% of nominal, Gain = 2	-0.7		1.04	V
		ISL59923, Gain remains > 90% of nominal, Gain = 2	-0.7		1.15	V
I_B	R_{IN}, G_{IN}, B_{IN} Input Bias Current	ISL59920, ISL59921	3	6	8	µA
		ISL59922, ISL59923	1.5		8	µA
V_{OS}	Output Offset Voltage	Post offset calibration (Note 4), Delay = 0ns and Delay = Full	-25	-4	+20	mV
Z_{OUT}	Output Impedance	ISL59920, ISL59921, Enabled, Chip enable = 5V	4.5	5.4	6.3	Ω
		ISL59922, ISL59923, Enabled, Chip enable = 5V	3.5		6.3	Ω
		Disabled, Chip enable = 0V		8		MΩ
+PSRR	Rejection of Positive Supply			-42	-29	dB
-PSRR	Rejection of Negative Supply			-58	-46	dB
I_{OUT}	Output Drive Current	10Ω load, 0.5V drive	43	53	70	mA
V_{IH}	Logic High	Switch high threshold			1.6	V
V_{IL}	Logic Low	Switch low threshold	0.8			V

Electrical Specifications $V_{SP} = V_{SPO} = +5V$, $V_{SM} = V_{SMP} = -5V$, GAIN = 2, $T_A = +25°C$, exposed die plate = -5V, x2 = 5V, $R_{LOAD} = 150\Omega$ on all video outputs, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS						
V+	V_{SP}, V_{SPO} Positive Supply Range		+4.5		+5.5	V
V-	V_{SM}, V_{SMO} Negative Supply Range		-4.5		-5.5	V
I_{SP}	Positive Supply Current (Note 3)	ISL59920	98	115	127	mA
		ISL59921, ISL59922	98	125	146	mA
		ISL59923	74	90	106	mA
I_{SPO}	Positive Output Supply Current (Note 3)	ISL59920	11.3	13	15.3	mA
		ISL59921, ISL59922	11.3	13	16.3	mA
		ISL59923	9.9	13	16	mA
I_{SM}	Negative Supply Current (Note 3)		-35.45	-31	-26	mA
I_{SMO}	Negative Output Supply Current (Note 3)	ISL59920, ISL59921, ISL59922	-15.5	-13	-11	mA
		ISL59923	-17.5	-13	-9.5	mA
ΔI_{SP}	Supply Current (Note 3)	Increase in I_{SP} per unit step in delay per channel		0.9		mA
$I_{STANDBY}$	Positive Supply Standby Current (Note 3)	Chip enable = 0V		2.6		mA
SERIAL INTERFACE CHARACTERISTICS						
t_{MAX}	Max SCLOCK Frequency	Maximum programming clock speed			10	MHz
$t_{\overline{SEN}\_SETUP}$	$\overline{SENABLE}$ to SCLOCK falling edge setup time. See Figure 34.	$\overline{SENABLE}$ falling edge should occur at least $t_{\overline{SEN}\_SETUP}$ ns after previous (ignored) clock and $t_{\overline{SEN}\_SETUP}$ before next (desired) clock. Clock edges occurring within t_en_ck of the $\overline{SENABLE}$ falling edge will have indeterminate effect.		10		ns
$t_{\overline{SEN}\_CYCLE}$	Minimum Separation Between $\overline{SENABLE}$ rising edge and next $\overline{SENABLE}$ falling edge. See Figure 34.	If $\overline{SENABLE}$ is taken low less than 3µs after it was taken high, there is a small possibility that an offset correction will not be initiated.	3			µs

NOTES:

2. The limits for the “Nominal Delay Increment” are derived by taking the limits for the “Maximum Delay” and dividing by the number of steps for the device. For the ISL59920, ISL59921, and ISL59922 the number of steps is 31; for the ISL59923 the number of steps is 15.
3. All supply currents measured with Delay R = 0ns, G = mid delay, B = full delay.
4. Offset measurements are referred to 75Ω load as shown in Figure 1.

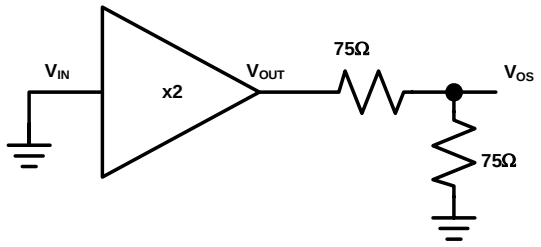


FIGURE 1. V_{OS} MEASUREMENT CONDITIONS

Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	V_{SP}	+5V for delay circuitry and input amp
2	R_{IN}	Red channel video input
3	GND	0V for delay circuitry supply
4	G_{IN}	Green channel video input
5	V_{SM}	-5V for input amp
6	B_{IN}	Blue channel video input
7	CENABLE	Chip Enable input, active high: logical high enables chip, low disables chip
8	$\overline{\text{SENABLE}}$	Serial Enable input, active low: logical low enables serial communication
9	SDATA	Serial Data input, logic threshold 1.2V: data to be programmed into chip
10	SCLOCK	Serial Clock input: Clock to enter data; logical; data written on negative edge
11	B_{OUT}	Blue channel video output
12	V_{SMO}	-5V for video output buffers
13	G_{OUT}	Green channel video output
14	GNDO	0V reference for input and output buffers
15	R_{OUT}	Red channel video output
16	V_{SPO}	+5V for video output buffers
17	TESTB	Blue channel phase detector output
18	TESTG	Green channel phase detector output
19	TESTR	Red channel phase detector output
20	X2	Gain Select Input: logical high = 2x (+6dB), logical low = 1x (0dB)
Thermal Pad		MUST be tied to -5V. For best thermal conductivity also tie to a larger -5V copper plane (inner or bottom). Use many vias to minimize thermal resistance between thermal pad and copper plane. Do not connect to GND - connection to GND is equivalent to shorting the -5V and GND planes together.

Typical Performance Curves

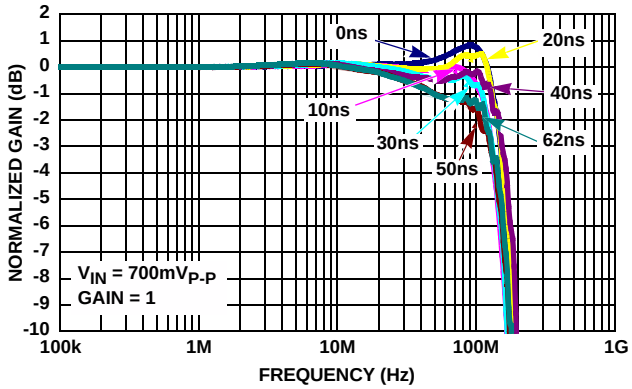


FIGURE 2. ISL59920 FREQUENCY RESPONSE (GAIN = 1)

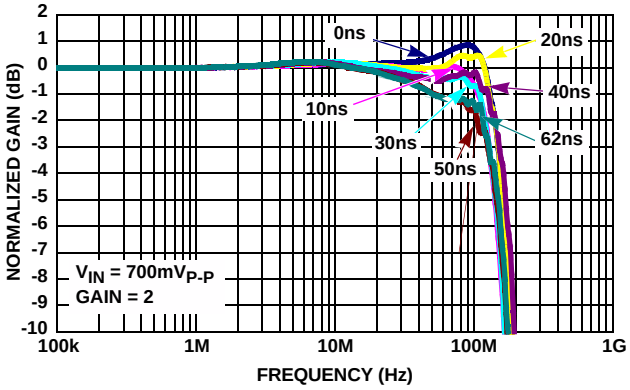


FIGURE 3. ISL59920 FREQUENCY RESPONSE (GAIN = 2)

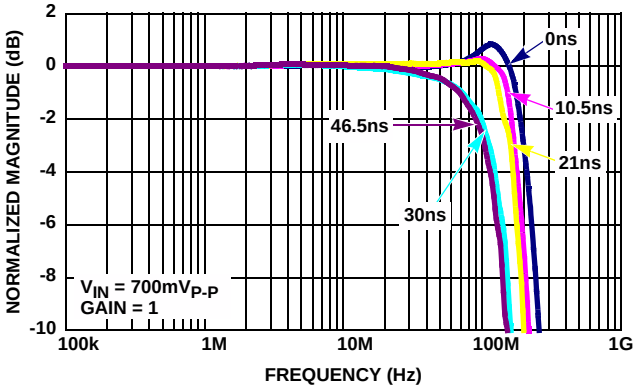


FIGURE 4. ISL59921 FREQUENCY RESPONSE (GAIN = 1)

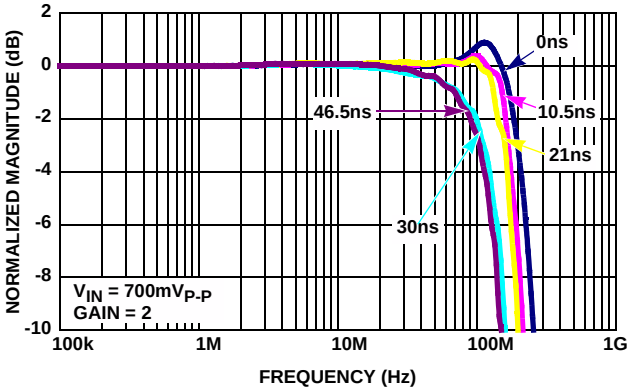


FIGURE 5. ISL59921 FREQUENCY RESPONSE (GAIN = 2)

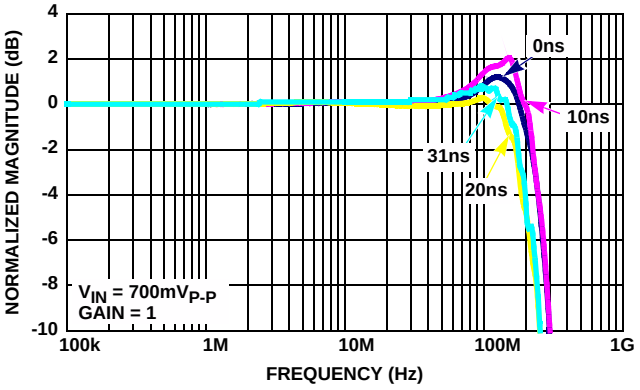


FIGURE 6. ISL59922 FREQUENCY RESPONSE (GAIN = 1)

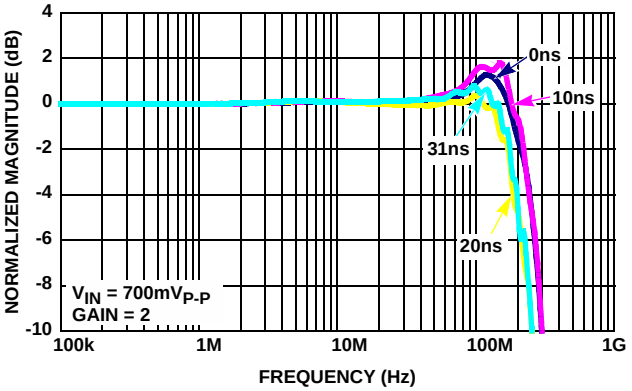


FIGURE 7. ISL59922 FREQUENCY RESPONSE (GAIN = 2)

Typical Performance Curves (Continued)

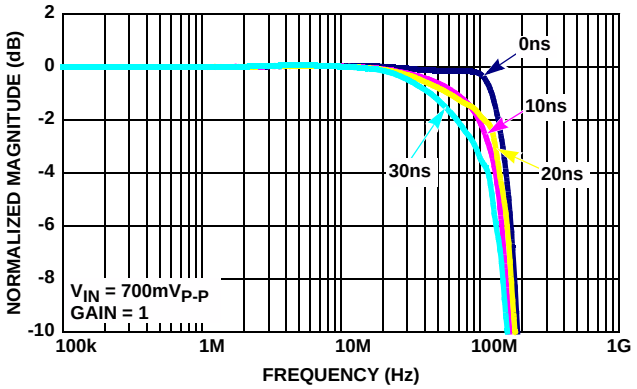


FIGURE 8. ISL59923 FREQUENCY RESPONSE (GAIN = 1)

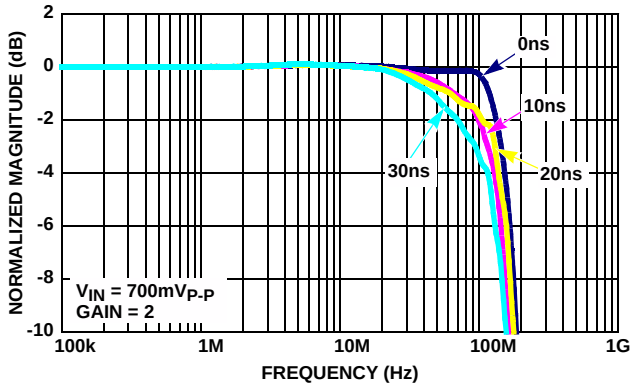


FIGURE 9. ISL59923 FREQUENCY RESPONSE (GAIN = 2)

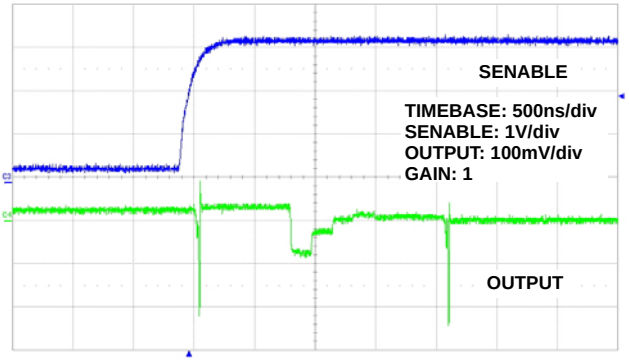


FIGURE 10. OFFSET CORRECTION DAC ADJUST

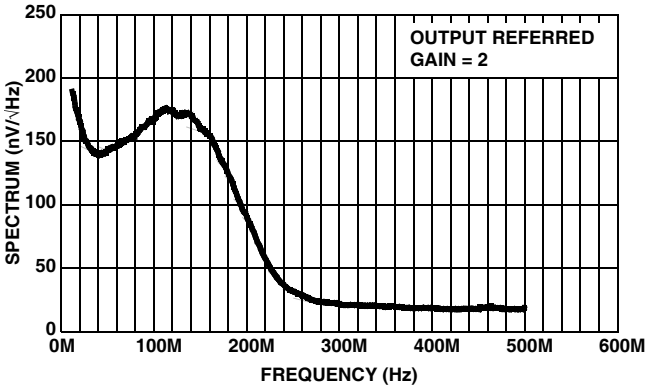


FIGURE 11. ISL59920 NOISE SPECTRUM (10k TO 500MHz)

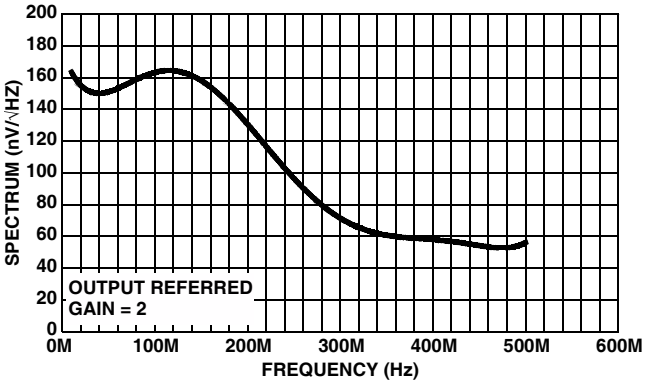


FIGURE 12. ISL59921 NOISE SPECTRUM (10k TO 500MHz)

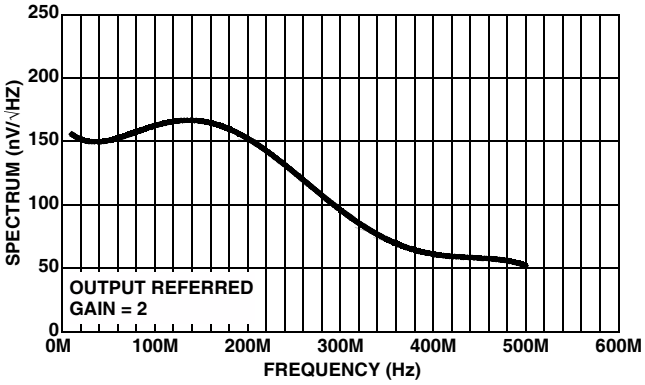


FIGURE 13. ISL59922 NOISE SPECTRUM (10k TO 500MHz)

Typical Performance Curves (Continued)

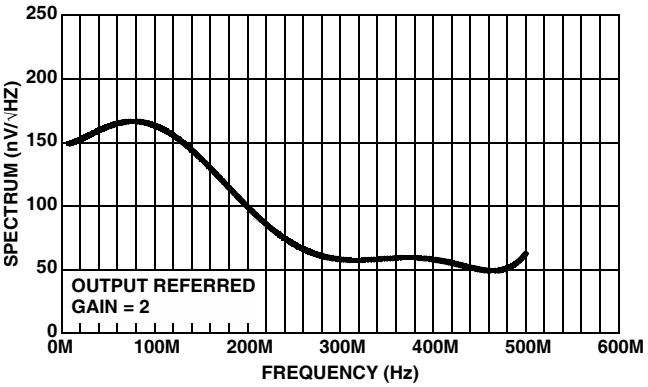


FIGURE 14. ISL59923 NOISE SPECTRUM (10k TO 500MHz)

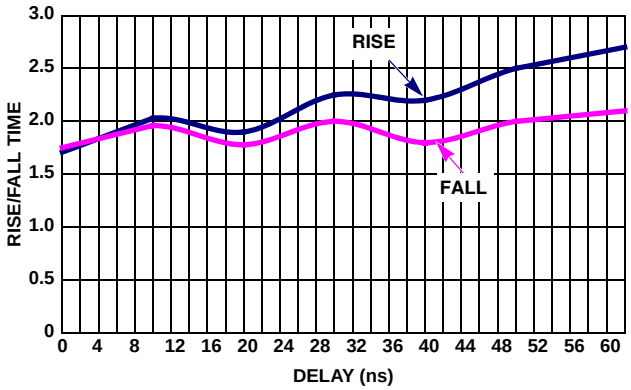


FIGURE 15. ISL59920 RISE/FALL TIME vs DELAY TIME (GAIN = 2)

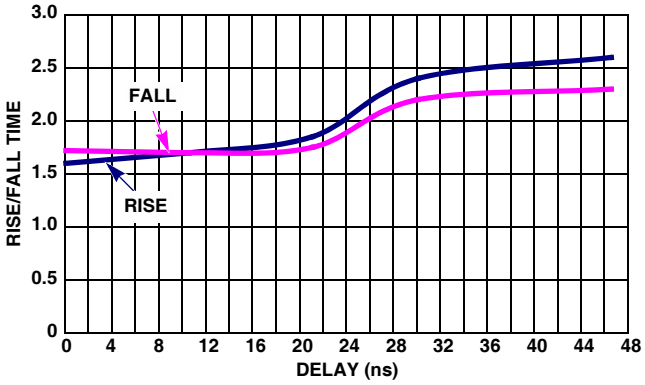


FIGURE 16. ISL59921 RISE/FALL TIME vs DELAY TIME (GAIN = 2)

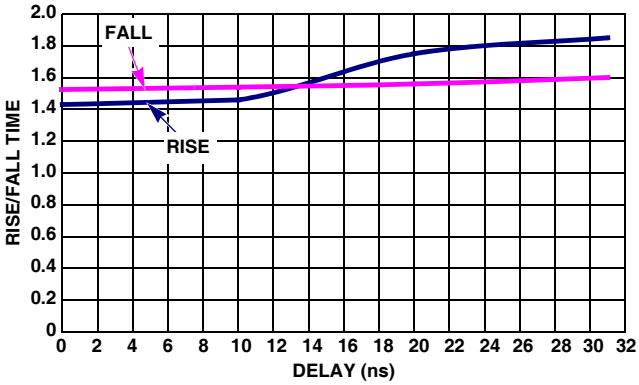


FIGURE 17. ISL59922 RISE/FALL TIME vs DELAY TIME (GAIN = 2)

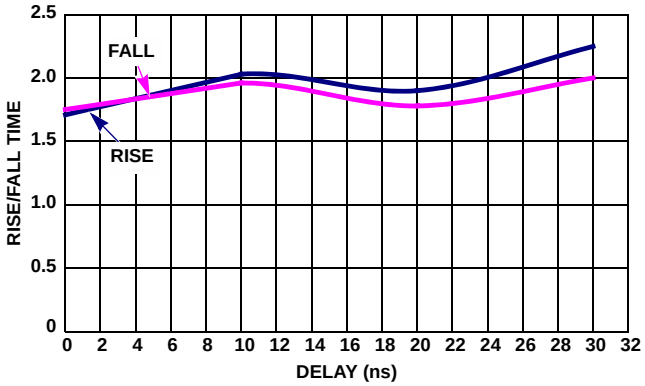


FIGURE 18. ISL59923 RISE/FALL TIME vs DELAY TIME (GAIN = 2)

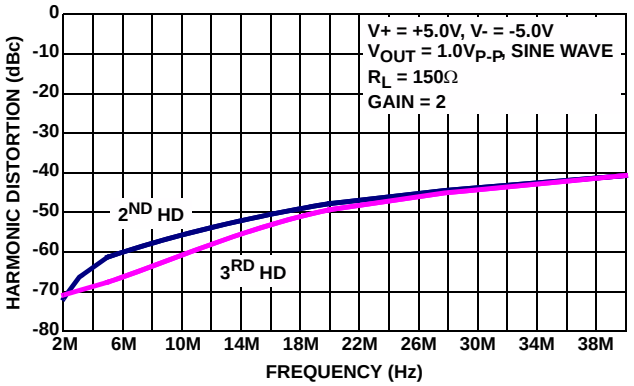


FIGURE 19. HARMONIC DISTORTION vs FREQUENCY

Typical Performance Curves (Continued)

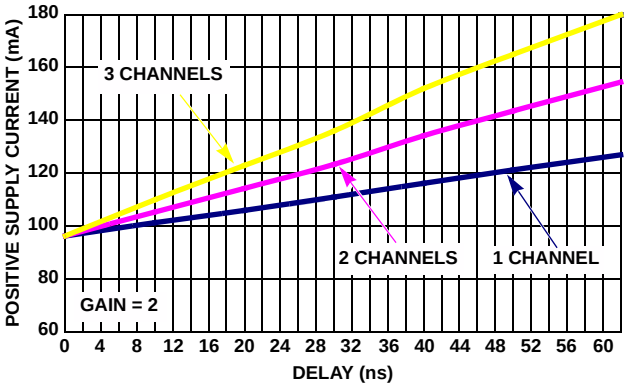


FIGURE 20. ISL59920 POSITIVE SUPPLY CURRENT (V_{SP}) vs DELAY TIME

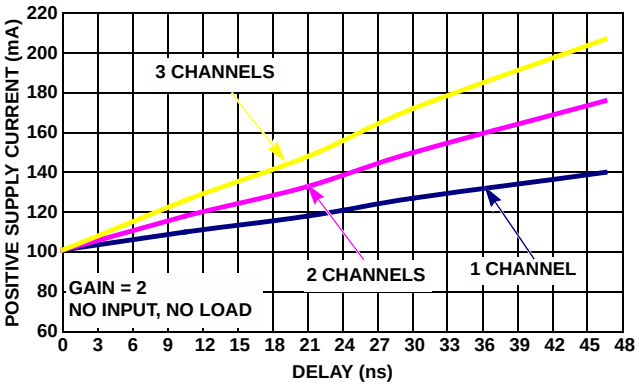


FIGURE 21. ISL59921 POSITIVE SUPPLY CURRENT (V_{SP}) vs DELAY TIME

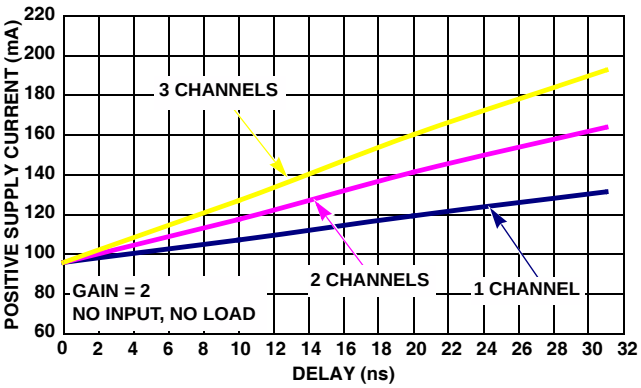


FIGURE 22. ISL59922 POSITIVE SUPPLY CURRENT (V_{SP}) vs DELAY TIME

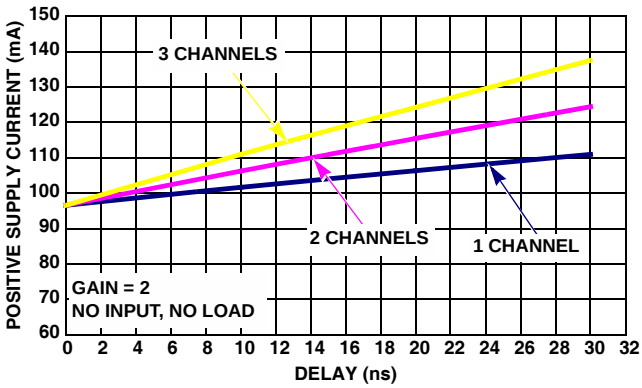


FIGURE 23. ISL59923 POSITIVE SUPPLY CURRENT (V_{SP}) vs DELAY TIME

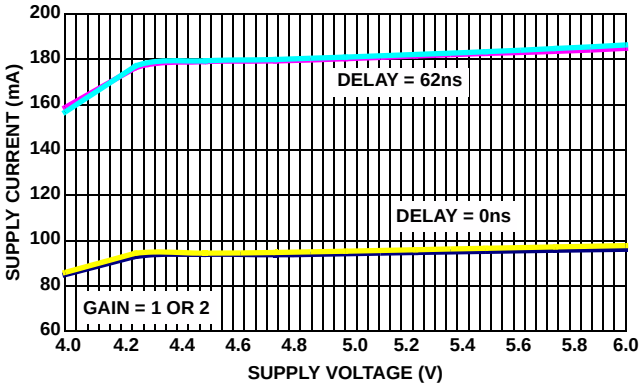


FIGURE 24. ISL59920 $I_{SUPPLY+}$ vs $V_{SUPPLY+}$

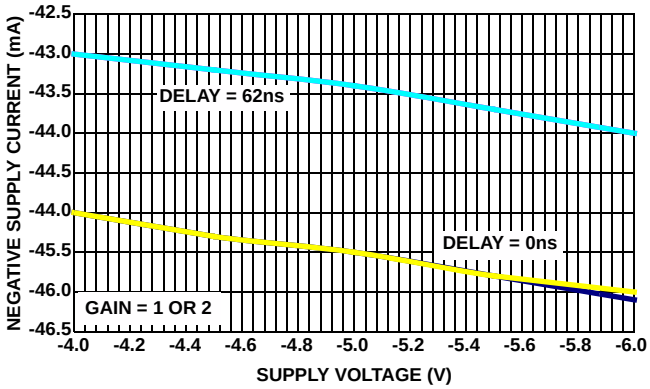


FIGURE 25. ISL59920 $I_{SUPPLY-}$ vs $V_{SUPPLY-}$

Typical Performance Curves (Continued)

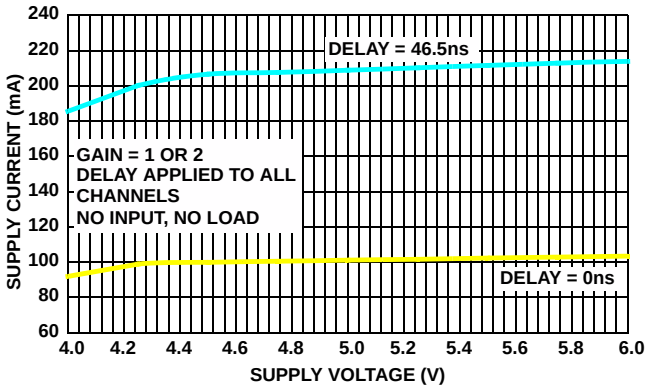


FIGURE 26. ISL59921 $I_{SUPPLY+}$ vs $V_{SUPPLY+}$

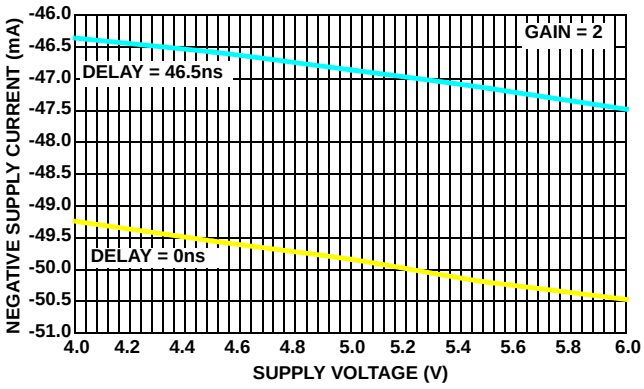


FIGURE 27. ISL59921 $I_{SUPPLY-}$ vs $V_{SUPPLY-}$

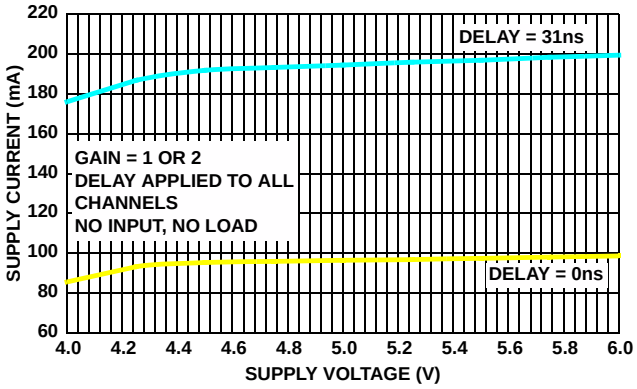


FIGURE 28. ISL59922 $I_{SUPPLY+}$ vs $V_{SUPPLY+}$

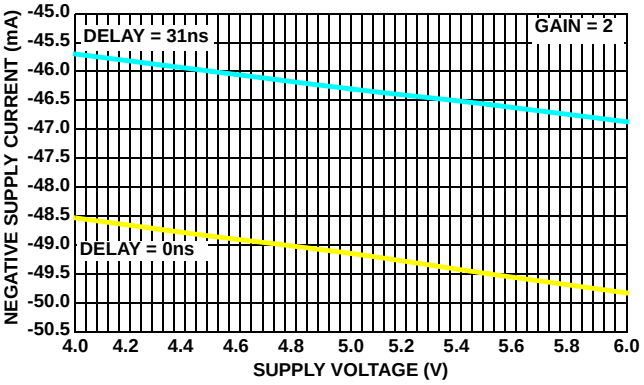


FIGURE 29. ISL59922 $I_{SUPPLY-}$ vs $V_{SUPPLY-}$

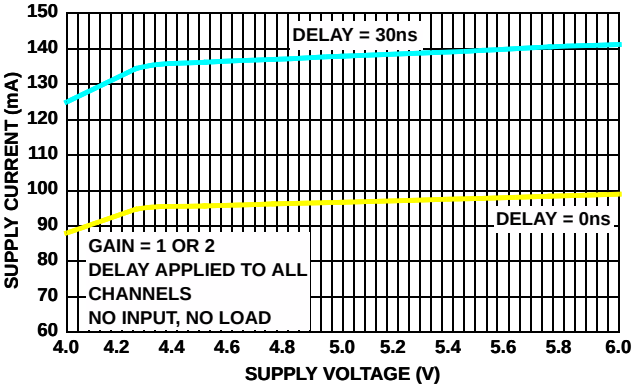


FIGURE 30. ISL59923 $I_{SUPPLY+}$ vs $V_{SUPPLY+}$

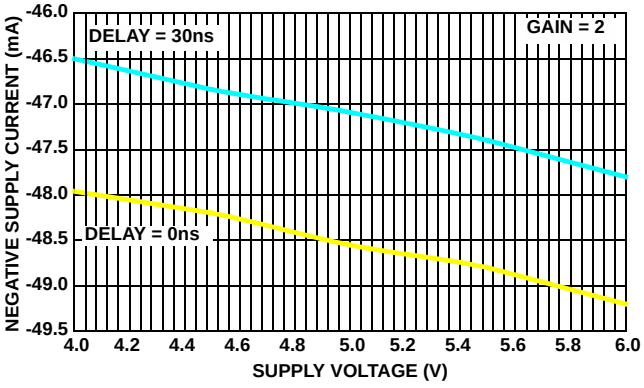


FIGURE 31. ISL59923 $I_{SUPPLY-}$ vs $V_{SUPPLY-}$

Typical Performance Curves (Continued)

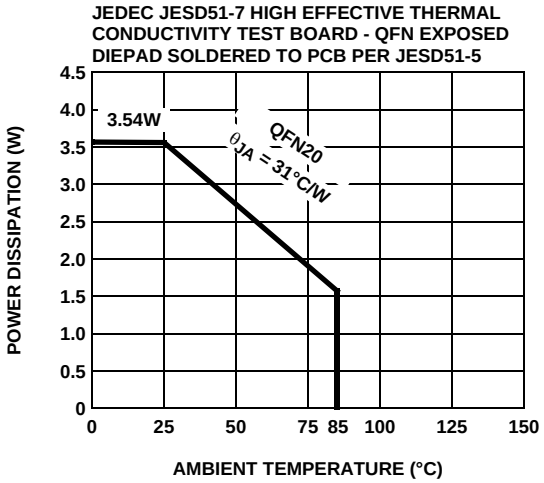


FIGURE 32. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

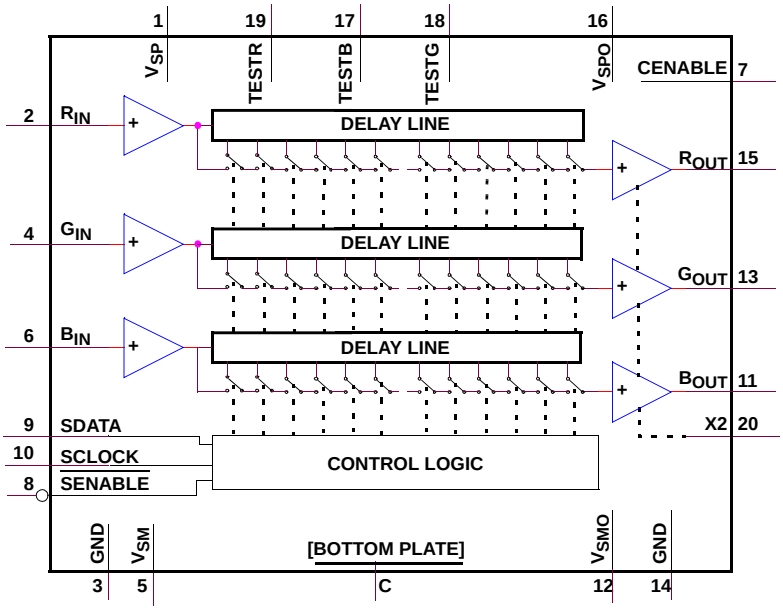


FIGURE 33. ISL59920, ISL59921, ISL59922, ISL59923 BLOCK DIAGRAM

Applications Information

The ISL59920, ISL59921, ISL59922, and ISL59923 are triple analog delay lines that provide skew compensation between three high-speed signals. These devices compensate for time skew introduced by a typical CAT-5, CAT-6 or CAT-7 cable with differing electrical lengths (due to different twist ratios) on each pair. Via their SPI interface, these devices can be programmed to independently compensate for the three different cable delays while maintaining 80MHz bandwidth at their maximum setting. There are four different variations of the ISL5992x (ISL5992x will be used when talking about characteristics that are common to all four devices).

TABLE 1.

PART NUMBER	MAX DELAY (ns)	NOMINAL DELAY INCREMENT (ns)
ISL59920	62	2.0
ISL59921	46.5	1.5
ISL59922	31	1.0
ISL59923	30	2.0

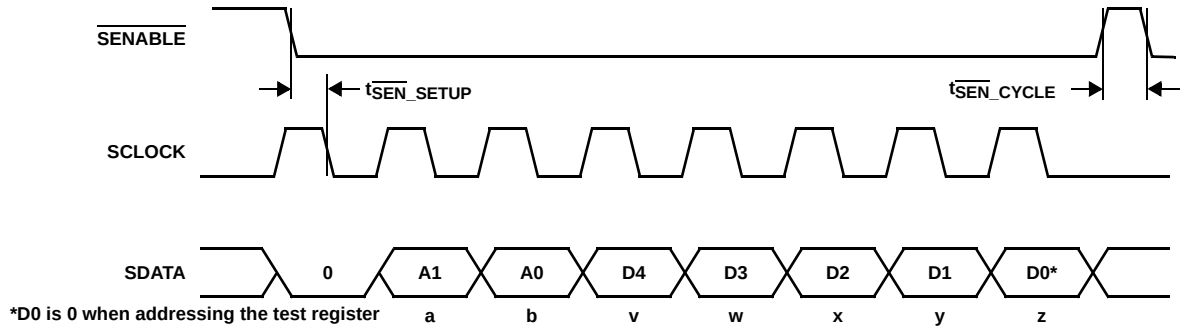


FIGURE 34. SERIAL TIMING

Figure 33 shows the ISL5992x block diagram. The 3 analog inputs are ground referenced single-ended signals. After the signal is received, the delay is introduced by switching filter blocks into the signal path. Each filter block is an all-pass filter introducing either 1, 1.5 or 2ns of delay. In addition to adding delay, each filter block also introduces some low pass filtering. As a result, the bandwidth of the signal path decreases from the 0ns delay setting to the maximum delay setting, as shown in Figures 2 through 9 of the “Typical Performance Curves”.

In operation, it is best to allocate the most delayed signal 0ns delay then increase the delay on the other channels to bring them into line. This will result in delay compensation with the lowest power and distortion.

Serial Bus Operation

The ISL5992x is programmed via 8-bit words sent through its serial interface. The first bit (MSB) of SDATA is latched on the first falling clock edge after $\overline{\text{SENABLE}}$ goes low, as shown in Figure 34. This bit should be a 0 under all conditions. The next two bits determine the color register to be written to: 01 = R, 02 = G, and 03 = B (00 is reserved for the test register). The final five bits set the delay for the specified color. After 8 bits are latched, any additional clocks are treated as a new word (data is shifted directly to the final registers as it is clocked in). This allows the user to write (for example) the 24 bits of data necessary for R, G, and B as a single 24-bit word. It is the user's responsibility to send complete multiples of 8 clock cycles. The serial state machine is reset on the falling edge of $\overline{\text{SENABLE}}$, so any data corruption that may have occurred due to too many or too few clocks can be corrected with a new word with the correct number of clocks. The initial value of all registers on power-up is 0.

TABLE 2. SERIAL BUS DATA

vwxyz	ISL59920 DELAY	ISL59921 DELAY	ISL59922 DELAY	ISL59923 DELAY
00000	0	0	0	0
00001	2	1.5	1	2
00010	4	3	2	4
00011	6	4.5	3	6

TABLE 2. SERIAL BUS DATA (Continued)

vwxyz	ISL59920 DELAY	ISL59921 DELAY	ISL59922 DELAY	ISL59923 DELAY
00100	8	6	4	8
00101	10	7.5	5	10
00110	12	9	6	12
00111	14	10.5	7	14
01000	16	12	8	16
01001	18	13.5	9	18
01010	20	15	10	20
01011	22	16.5	11	22
01100	24	18	12	24
01101	26	19.5	13	26
01110	28	21	14	28
01111	30	22.5	15	30
10000	32	24	16	N/A
10001	34	25.5	17	N/A
10010	36	27	18	N/A
10011	38	28.5	19	N/A
10100	40	30	20	N/A
10101	42	31.5	21	N/A
10110	44	33	22	N/A
10111	46	34.5	23	N/A
11000	48	36	24	N/A
11001	50	37.5	25	N/A
11010	52	39	26	N/A
11011	54	40.5	27	N/A
11100	56	42	28	N/A
11101	58	43.5	29	N/A
11110	60	45	30	N/A
11111	62	46.5	31	N/A

NOTE: Delay register word = 0abvwxyz; Red register - ab = 01; Green register - ab = 10; Blue register - ab = 11; vwxyz selects delay; ab = 00 writes to the test register to change the DAC slice level.

Offset Compensation

To counter the effects of offset, the ISL5992x incorporates an offset compensation circuit that reduces the offset to less than ±25mV. An offset correction cycle is triggered by the rising edge of the $\overline{\text{SENABLE}}$ pin after writing a delay word to any of the 3 channels. The offset calibration starts about 500ns after the $\overline{\text{SENABLE}}$ rising edge to allow the ISL5992x time to settle (electrically and thermally) to the new delay setting. It lasts about 2.5µs, for a total offset correction time of 3.0µs. During calibration, the ISL5992x's inputs are internally shorted together (however the characteristics of the ISL5992x's differential input pins stay the same), and the offset of the output stage is adjusted until it has been minimized.

In addition to automatically triggering after a delay change (or any register write), an additional offset calibration may be initiated at any time, such as:

- When the die temperature changes. Applying power to the ISL5992x will cause the die temperature to quickly increase then slowly settle over 20 to 30 seconds. Because the ISL5992x powers-down unused delay stages (to minimize power consumption), the die temp will also change and settle after a delay change. Initiating an offset 20 seconds (or longer, depending on the thermal characteristics of the system) after power-on or a delay change will minimize the offset in normal operation thereafter.
- When the ambient temperature changes. If you are monitoring the temperature, initiate a calibration every time the temperature shifts by 5 to 10 degrees. If you are not monitoring temperature, initiate a calibration periodically, as expected by the environment the device is in.
- After a CENABLE (Chip Enable) cycle. The CENABLE pin may be taken low to put the ISL5992x in a low power standby mode to conserve power when not needed. When the CENABLE pin goes high to exit this low power mode, the ISL5992x will recall the delay settings but it will *not* recall the correct offset calibration settings, so to maintain low offset, a write to the delay register is required after a CENABLE cycle. Offset errors may be as large as ±200mV coming out of standby mode - **recalibration is a necessity**. For best performance, initiate an additional calibration again once the die temperature has settled (20 to 30 seconds after coming out of standby).
- After a gain change (X2 pin changes state). The systematic offset is different for a gain of x1 vs. a gain of x2, so an offset calibration is recommended after a gain change. However in a typical application the gain is permanently fixed at x1 or x2, so this is not usually a concern.

Test Pins

Three test pins are provided (Test R, Test G, Test B). During normal operation, the test pins output pulses of current for a duration of the overlap between the inputs, as shown in Figure 35:

$TEST_R$ pulse = RED_{OUT} (A) with respect to $GREEN_{OUT}$ (B)

$TEST_G$ pulse = $GREEN_{OUT}$ with respect to $BLUE_{OUT}$

$TEST_B$ pulse = $BLUE_{OUT}$ with respect to RED_{OUT}

Averaging the current gives a direct measure of the delay between the two edges. When A precedes B, the current pulse is +50µA, and the output voltage goes up. When B precedes A, the pulse is -50µA.

For the logic to work correctly, A and B must have a period of overlap while they are high (a delay longer than the pulse width cannot be measured).

Signals A and B are derived from the video input by comparing the video signal with a slicing level, which is set by an internal DAC. This enables the delay to be measured either from the rising edges of sync-like signals encoded on top of the video or from a dedicated set-up signal. The outputs can be used to set the correct delays for the signals received.

The DAC level is set through the serial input by bits 1 through 4 directed to the test register (00).

INTERNAL DAC VOLTAGE

The slice level of the internal DAC may be programmed by writing a byte to the test register (00). Table 3 shows the values that should be written to change the DAC slice level. Please keep in mind when writing to the test register that the LSB should always be zero.

Referred to the input, the DAC slice range for the ISL5992x is cut in half for gain of 2 mode because the slicing occurs after the x1/x2 stage output amplifier. (In the EL9115, the slicing occurred before the amplifier so the range of the DAC voltage was the same for either gain of 1 or gain of 2).

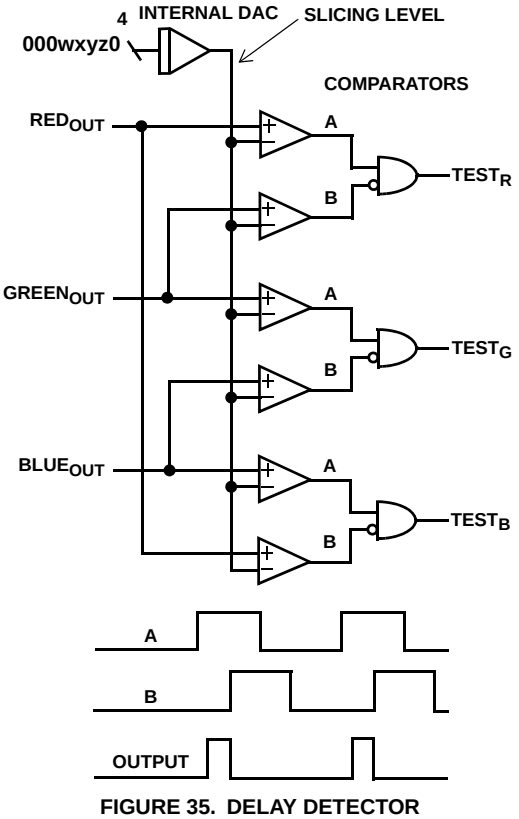


FIGURE 35. DELAY DETECTOR

TABLE 3. DAC VOLTAGE RANGE - INPUT REFERRED

wxyz	DAC RANGE [mV] (GAIN 1)	DAC RANGE [mV] (GAIN 2)
1000	-400	-200
1001	-350	-175
1010	-300	-150
1011	-250	-125
1100	-200	-100
1101	-150	-75
1110	-100	-50
1111	-50	-25
0000	0	0
0001	50	25
0010	100	50
0011	150	75
0100	200	100
0101	250	125
0110	300	150
0111	350	175

NOTE: Test Register word = 000wxyz0. wxyz fed to DAC. z is LSB

Power Dissipation

As the delay setting increases, additional filter blocks turn on and insert into the signal path. When the delay per channel increments, V_{SP} current increases by 0.9mA while V_{SM} does not change significantly. Under the extreme settings, the positive supply current reaches 141mA and the negative supply current can be 41mA. Operating at ±5V power supply, the worst-case ISL5992x power dissipation is:

$$PD = 5 \bullet 141mA + 5 \bullet 41mA = 910mW \quad \text{(EQ. 1)}$$

The minimum θ_{JA} required for long term reliable operation of the ISL5992x is calculated using Equation 2:

$$\theta_{JA} = (T_J - T_A)/PD = 55°C/W \quad \text{(EQ. 2)}$$

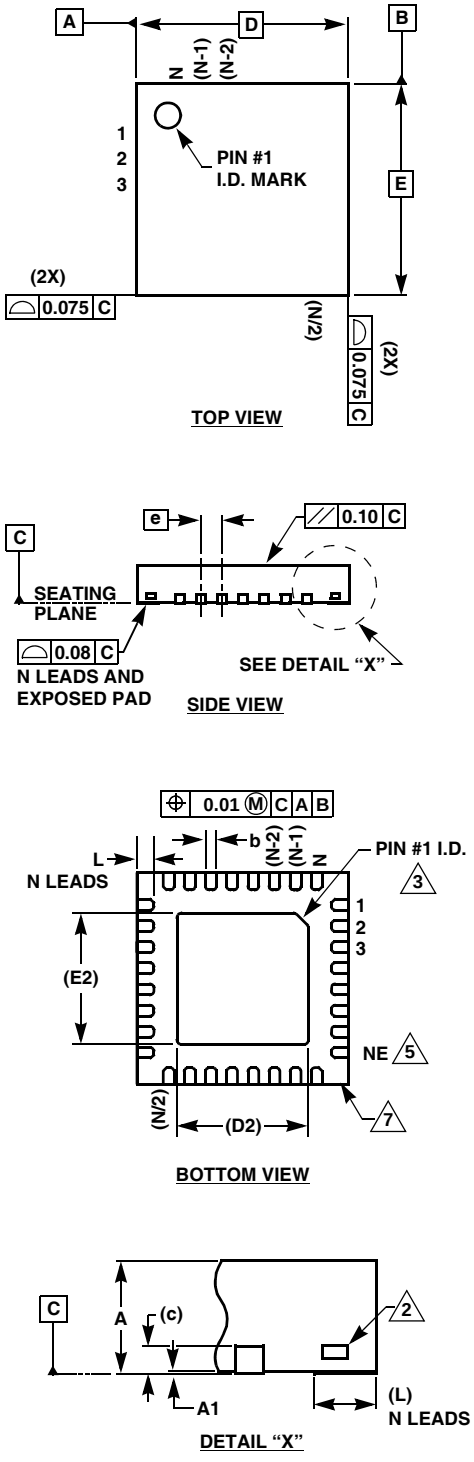
Where:

T_J is the maximum junction temperature (+135°C)

T_A is the maximum ambient temperature (+85°C)

For a 20 Ld package on a well laid-out PCB with good connectivity between the QFN's pad and the PCB copper area, 31°C/W θ_{JA} thermal resistance can be achieved. This yields a much higher power dissipation of 3.54W using Equation 2 (see Figure 32). To disperse the heat, the bottom heat spreader must be soldered to the PCB. Heat flows through the heat spreader to the circuit board copper then spreads and convects to air. Thus, the PCB copper plane becomes the heatsink (see TB389). This has proven to be a very effective technique. A separate application note, which details the 20 Ld QFN PCB design considerations, is available.

Quad Flat No-Lead Plastic Package (QFN)



L20.5x5C

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	0.00	0.02	0.05	-
b	0.28	0.30	0.32	-
c		0.20 REF		-
D		5.00 BASIC		-
D2		3.70 REF		8
E		5.00 BASIC		-
E2		3.70 REF		8
e		0.65 BASIC		-
L	0.35	0.40	0.45	-
N		20		4
ND		5 REF		6
NE		5 REF		5

Rev. 0 6/06

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.
9. One of 10 packages in MDP0046