

**EN25S80****8 Megabit 1.8V Serial Flash Memory with 4Kbyte Uniform Sector****FEATURES**

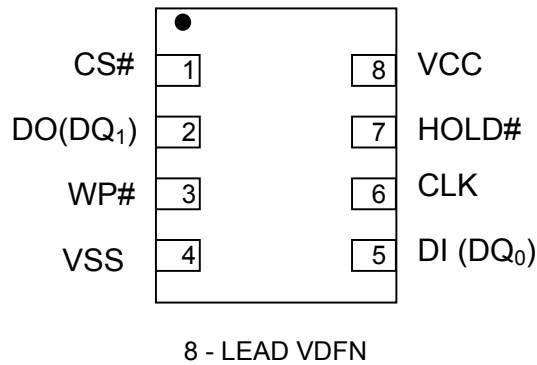
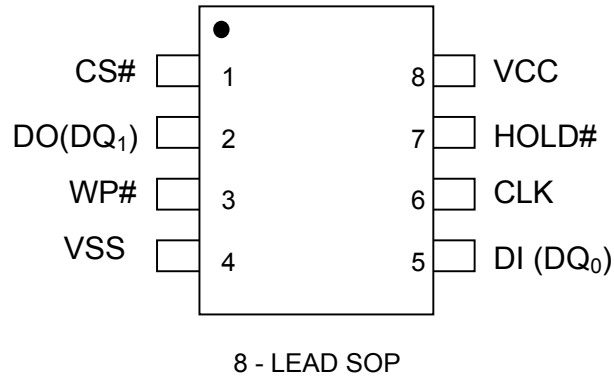
- Single power supply operation
  - Full voltage range: 1.65-1.95 volt
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- 8 M-bit Serial Flash
  - 8 M-bit/1024 K-byte/4096 pages
  - 256 bytes per programmable page
- Standard or Dual SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI: CLK, CS#, DQ<sub>0</sub>, DQ<sub>1</sub>, WP#, HOLD#
- High performance
  - 75MHz clock rate for one data bit
  - 50MHz clock rate for two data bits
- Low power consumption
  - 7 mA typical active current
  - 1  $\mu$ A typical power down current
- Uniform Sector Architecture:
  - 256 sectors of 4-Kbyte
  - 16 blocks of 64-Kbyte
  - Any sector or block can be erased individually
- Software and Hardware Write Protection:
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Page program time: 1.3ms typical
  - Sector erase time: 90ms typical
  - Block erase time 500ms typical
  - Chip erase time: 5 Seconds typical
- Lockable 256 byte OTP security sector
- Minimum 100K endurance cycle
- Package Options
  - 8 pins SOP 150mil body width
  - 8 pins SOP 200mil body width
  - 8 contact VDFN
  - All Pb-free packages are RoHS compliant
- Industrial temperature Range

**GENERAL DESCRIPTION**

The EN25S80 is an 8 Megabit (1024K-byte) Serial Flash memory, with advanced write protection mechanisms. The EN25S80 supports the standard Serial Peripheral Interface (SPI), and a high performance Dual output as well as Dual I/O using SPI pins: Serial Clock, Chip Select, Serial DQ<sub>0</sub>(DI) and DQ<sub>1</sub>(DO). SPI clock frequencies of up to 50MHz are supported allowing equivalent clock rates of 100MHz for Dual Output when using the Dual Output Fast Read instructions. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The EN25S80 also offers a sophisticated method for protecting individual blocks against erroneous or malicious program and erase operations. By providing the ability to individually protect and unprotect blocks, a system can unprotect a specific block to modify its contents while keeping the remaining blocks of the memory array securely protected. This is useful in applications where program code is patched or updated on a subroutine or module basis, or in applications where data storage segments need to be modified without running the risk of errant modifications to the program code segments.

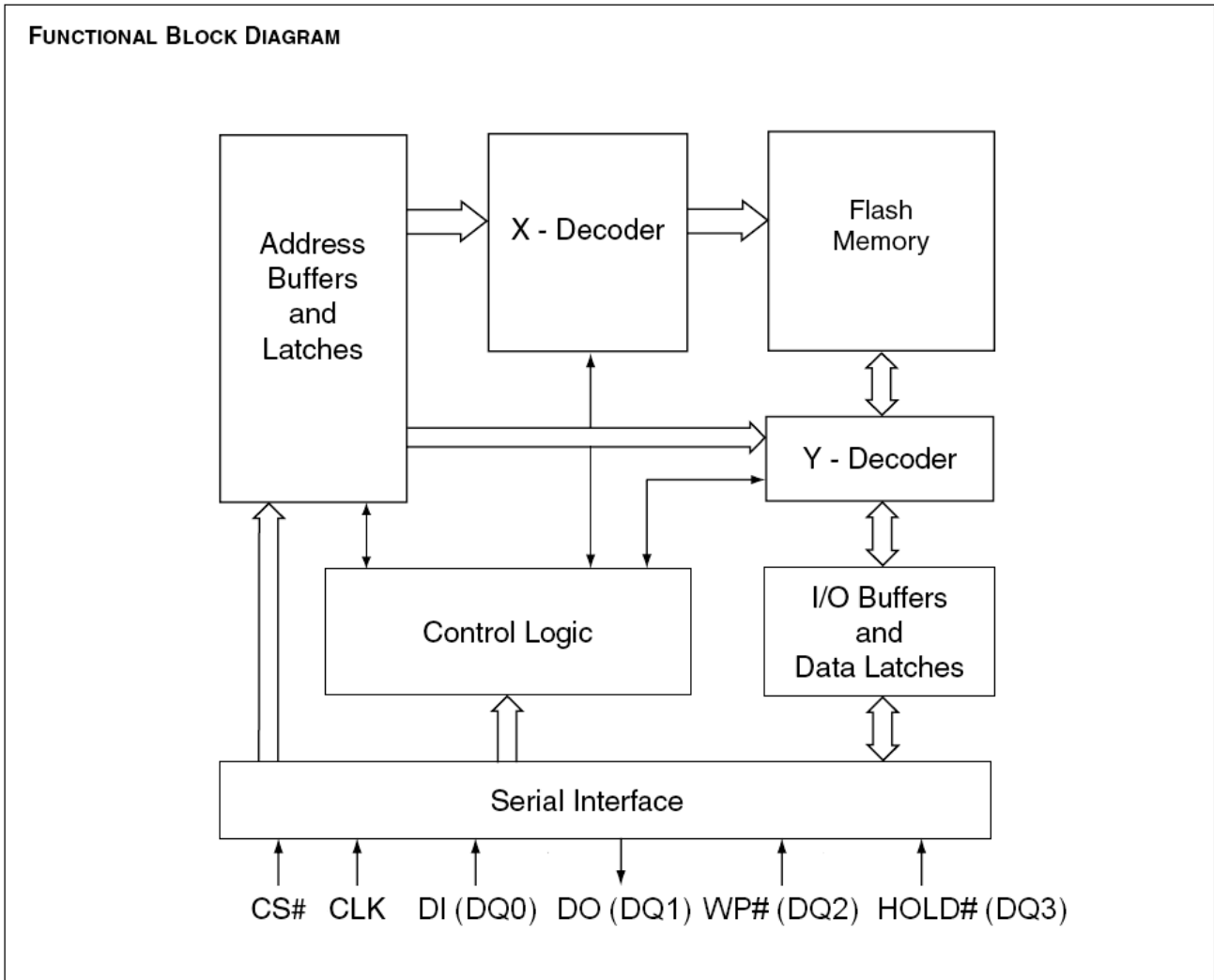
The EN25S80 is designed to allow either single Sector/Block at a time or full chip erase operation. The EN25S80 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

**Figure.1 CONNECTION DIAGRAMS**

**Table 1. Pin Names**

Symbol	Pin Name
CLK	Serial Clock Input
DI (DQ <sub>0</sub> )	Serial Data Input (Data Input Output 0) <sup>*1</sup>
DO (DQ <sub>1</sub> )	Serial Data Output (Data Input Output 1) <sup>*1</sup>
CS#	Chip Enable
WP#	Write Protect
HOLD#	Hold Input
Vcc	Supply Voltage (1.65-1.95V)
Vss	Ground
NC	No Connect

Note:

\*1. DQ<sub>0</sub> and DQ<sub>1</sub> are used for Dual instructions.

**Figure 2. BLOCK DIAGRAM**

**Note:**

1. DQ<sub>0</sub> and DQ<sub>1</sub> are used for Dual instructions.



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**SIGNAL DESCRIPTION****Serial Data Input, Output and IOs (DI, DO and DQ<sub>0</sub>, DQ<sub>1</sub>)**

The EN25S80 support standard SPI and Dual SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge CLK.

Dual SPI instruction use the bidirectional IO pins to serially write instruction, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

**Serial Clock (CLK)**

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

**Chip Select (CS#)**

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO, or DQ<sub>0</sub> and DQ<sub>1</sub>) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

**HOLD (HOLD#)**

The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). The HOLD# function can be useful when multiple devices are sharing the same SPI signals.

**Write Protect (WP#)**

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1and BP2) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected.



### MEMORY ORGANIZATION

The memory is organized as:

- 1,048,576 bytes
- Uniform Sector Architecture
  - 16 blocks of 64-Kbyte
  - 256 sectors of 4-Kbyte
- 4096 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

**Table 2. Uniform Block Sector Architecture**

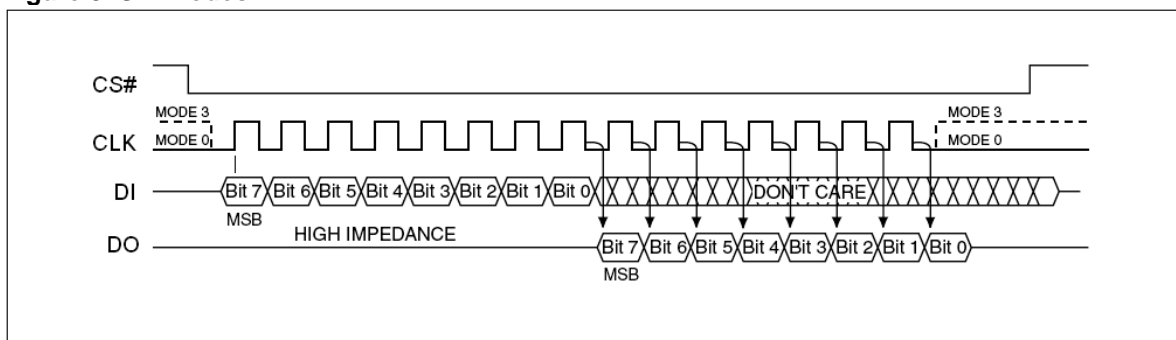
Block	Sector	Address range	
15	255	0FF000h	0FFFFFFh
	⋮	⋮	⋮
14	240	0F0000h	0F0FFFh
	239	0EF000h	0EFFFFh
13	224	0E0000h	0E0FFFh
	223	0DF000h	0DFFFFh
12	208	0D0000h	0D0FFFh
	207	0CF000h	0CFFFFh
11	192	0C0000h	0C0FFFh
	191	0BF000h	0BFFFFh
10	176	0B0000h	0B0FFFh
	175	0AF000h	0AFFFFh
9	160	0A0000h	0A0FFFh
	159	09F000h	09FFFFh
8	144	090000h	090FFFh
	143	08F000h	08FFFFh
7	128	080000h	080FFFh
	127	07F000h	07FFFFh
6	112	070000h	070FFFh
	111	06F000h	06FFFFh
5	96	060000h	060FFFh
	95	05F000h	05FFFFh
4	80	050000h	050FFFh
	79	04F000h	04FFFFh
3	64	040000h	040FFFh
	63	03F000h	03FFFFh
2	48	030000h	030FFFh
	47	02F000h	02FFFFh
1	32	020000h	020FFFh
	31	01F000h	01FFFFh
0	16	010000h	010FFFh
	15	00F000h	00FFFFh
	4	004000h	004FFFh
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

## OPERATING FEATURES

### Standard SPI Modes

The EN25S80 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3, as shown in Figure 3, concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

**Figure 3. SPI Modes**



### Dual SPI Instruction

The EN25S80 supports Dual SPI operation when using the “ Dual Output Fast Read and Dual I/ O FAST\_READ “ (3Bh and BBh) instructions. These instructions allow data to be transferred to or from the Serial Flash memory at two to three times the rate possible with the standard SPI. The Dual Read instructions are ideal for quickly downloading code from Flash to RAM upon power-up (code-shadowing) or for application that cache code-segments to RAM for execution. The Dual output feature simply allows the SPI input pin to also serve as an output during this instruction. When using Dual SPI instructions the DI and DO pins become bidirectional I/O pins; DQ<sub>0</sub> and DQ<sub>1</sub>. All other operations use the standard SPI interface with single output signal.

### Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration  $t_{PP}$ ).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0) provided that they lie in consecutive addresses on the same page of memory.

### Sector Erase, Block Erase and Chip Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration  $t_{SE}$ ,  $t_{BE}$  or  $t_{CE}$ ). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

### Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE, BE or CE ) can be achieved by not waiting for the worst case delay ( $t_W$ ,  $t_{PP}$ ,  $t_{SE}$ ,  $t_{BE}$  or  $t_{CE}$ ). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

**Active Power, Stand-by Power and Deep Power-Down Modes**

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Stand-by Power mode. The device consumption drops to  $I_{CC1}$ .

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to  $I_{CC2}$ . The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

**Status Register.** The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions.

**WIP bit.** The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

**WEL bit.** The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

**BP2, BP1, BP0 bits.** The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

**SRP bit / OTP\_LOCK bit** The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits.

In OTP mode, this bit serves as OTP\_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP\_LOCK value is equal 0, after OTP\_LOCK is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP\_LOCK bit can only be programmed once.

**Note :** In OTP mode, the WRSR command will ignore any input data and program OTP\_LOCK bit to 1, user must clear the protect bits before entering OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

**Write Protection**

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the EN25S80 provides the following data protection mechanisms:

- Power-On Reset and an internal timer ( $t_{PUW}$ ) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion or Write Status Register (WRSR) instruction completion or Page Program (PP) instruction completion or Sector Erase (SE) instruction completion or Block Erase (BE) instruction completion or Chip Erase (CE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Protect (SRP) bit to be protected. This is the Hardware Protected Mode (HPM).



- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 3. Protected Area Sizes Sector Organization

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Blocks	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	15	0F0000h-0FFFFFFh	64KB	Upper 1/16
0	1	0	14 to 15	0E0000h-0FFFFFFh	128KB	Upper 1/8
0	1	1	12 to 15	0C0000h-0FFFFFFh	256KB	Upper 1/4
1	0	0	8 to 15	080000h-0FFFFFFh	512KB	Upper 1/2
1	0	1	All	000000h-0FFFFFFh	1024KB	All
1	1	0	All	000000h-0FFFFFFh	1024KB	All
1	1	1	All	000000h-0FFFFFFh	1024KB	All

Hold Function

The Hold (HOLD#) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select (CS#) Low. The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (CLK) being Low (as shown in Figure 4.).

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (CLK) being Low.

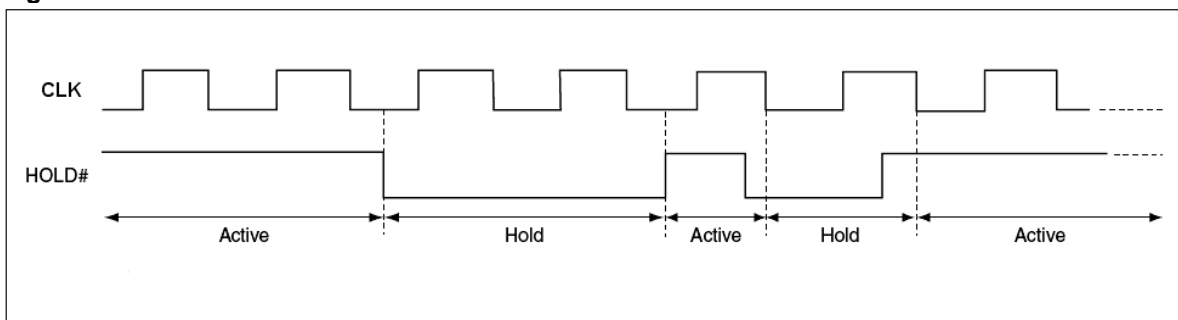
If the falling edge does not coincide with Serial Clock (CLK) being Low, the Hold condition starts after Serial Clock (CLK) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (CLK) being Low, the Hold condition ends after Serial Clock (CLK) next goes Low. (This is shown in Figure 4.).

During the Hold condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are Don't Care.

Normally, the device is kept selected, with Chip Select (CS#) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (CS#) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD#) High, and then to drive Chip Select (CS#) Low. This prevents the device from going back to the Hold condition.

Figure 4. Hold Condition Waveform







## **INSTRUCTIONS**

All instructions, addresses and data are shifted in and out of the device, most significant bit first. Serial Data Input (DI) is sampled on the first rising edge of Serial Clock (CLK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (DI), each bit being latched on the rising edges of Serial Clock (CLK).

The instruction set is listed in Table 4. Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence has been shifted in. In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast\_Read), Read Status Register (RDSR) or Release from Deep Power-down, and Read Device ID (RDI) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must be driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

**In the case of multi-byte commands of Page Program (PP), and Release from Deep Power Down (RES ) minimum number of bytes specified has to be given, without which, the command will be ignored.**

**In the case of Page Program, if the number of byte after the command is less than 4 (at least 1 data byte), it will be ignored too. In the case of SE and BE, exact 24-bit address is a must, any less or more will cause the command to be ignored.**

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.



Table 4A. Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0) <sup>(3)</sup>					continuous <sup>(4)</sup>
Write Status Register	01h	S7-S0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase / OTP erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(5)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(6)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(7)		
Enter OTP mode	3Ah						

**Notes:**

1. (BR7-BR0) : The output data of block protection register.
2. The Block Protection Registers contents will repeat continuously until CS# terminates the instruction.
3. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data being read from the device on the DO pin.
4. The Status Register contents will repeat continuously until CS# terminate the instruction.
5. The Device ID will repeat continuously until CS# terminates the instruction.
6. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction.  
00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
7. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity.

**Table 4B. Instruction Set (Read Instruction)**

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) <sup>(1)</sup>	(one byte per 4 clocks, continuous)
Dual I/O Fast Read	BBh	A23-A8 <sup>(2)</sup>	A7-A0, dummy <sup>(2)</sup>	(D7-D0, ...) <sup>(1)</sup>			(one byte per 4 clocks, continuous)

**Notes:**

## 1. Dual Output data

DQ<sub>0</sub> = (D6, D4, D2, D0)DQ<sub>1</sub> = (D7, D5, D3, D1)

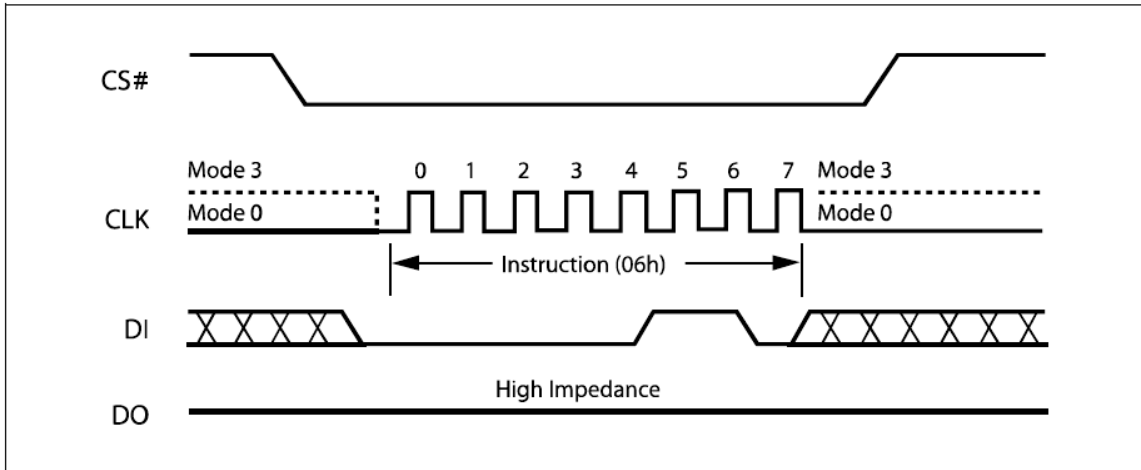
## 2. Dual Input Address

DQ<sub>0</sub> = A22, A20, A18, A16, A14, A12, A10, A8 ; A6, A4, A2, A0, dummy 6, dummy 4, dummy 2, dummy 0DQ<sub>1</sub> = A23, A21, A19, A17, A15, A13, A11, A9 ; A7, A5, A3, A1, dummy 7, dummy 5, dummy 3, dummy 1**Table 5. Manufacturer and Device Identification**

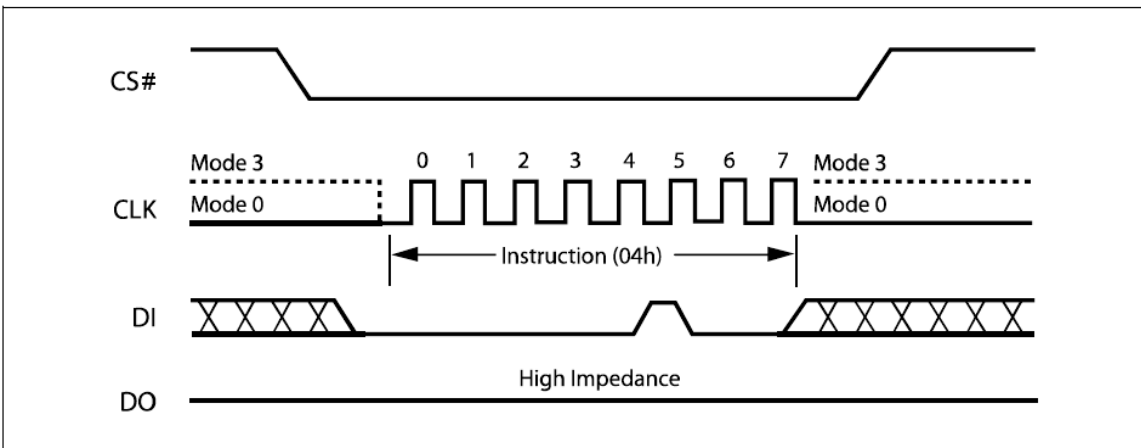
OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			73h
90h	1Ch		73h
9Fh	1Ch	3814h	

**Write Enable (WREN) (06h)**

The Write Enable (WREN) instruction (Figure 5) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) instruction. The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

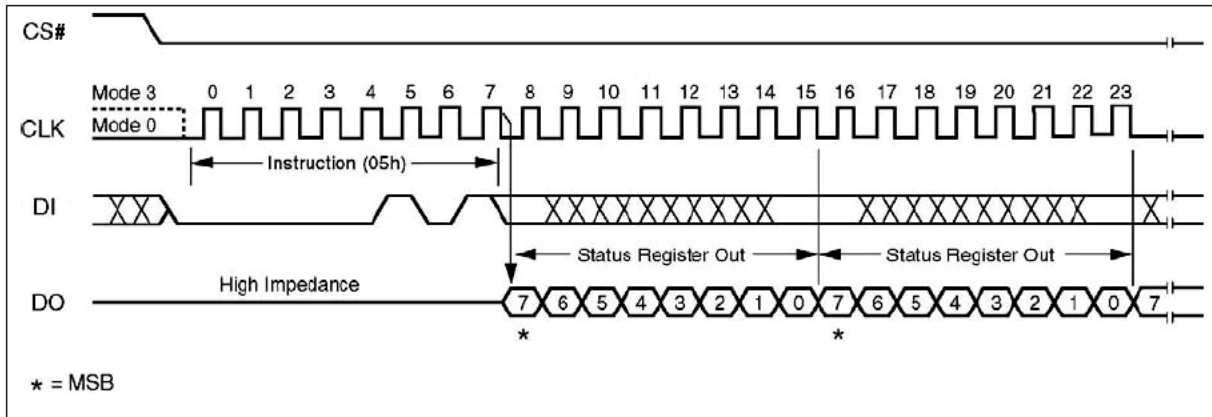

**Figure 5. Write Enable Instruction Sequence Diagram**
**Write Disable (WRDI) (04h)**

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0 or exit from OTP mode to normal mode. The Write Disable instruction is entered by driving Chip Select (CS#) low, shifting the instruction code “04h” into the DI pin and then driving Chip Select (CS#) high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase (BE) and Chip Erase instructions.


**Figure 6. Write Disable Instruction Sequence Diagram**

**Read Status Register (RDSR) (05h)**

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 7.


**Figure 7. Read Status Register Instruction Sequence Diagram**
**Table 6. Status Register Bit Locations**

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	Reserved bits	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected			(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit				Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

**Note**

- In OTP mode, SRP bit is served as OTP\_LOCK bit.
- See the table 3 "Protected Area Sizes Sector Organization".

The status and control bits of the Status Register are as follows:

**WIP bit.** The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

**WEL bit.** The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

**BP2, BP1, BP0 bits.** The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 3.) becomes protected against Page Program (PP) Sector Erase (SE) and , Block Erase (BE), instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.



**Reserved bit.** Status register bit locations 5 and 6 are reserved for future use. Current devices will read 0 for these bit locations. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

**SRP bit / OTP\_LOCK bit.** The Status Register Protect (SRP) bit is operated in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

In OTP mode, this bit is served as OTP\_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP\_LOCK value is equal 0, after OTP\_LOCK is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP\_LOCK bit can only be programmed once.

**Note :** In OTP mode, the WRSR command will ignore any input data and program OTP\_LOCK bit to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

### **Write Status Register (WRSR) (01h)**

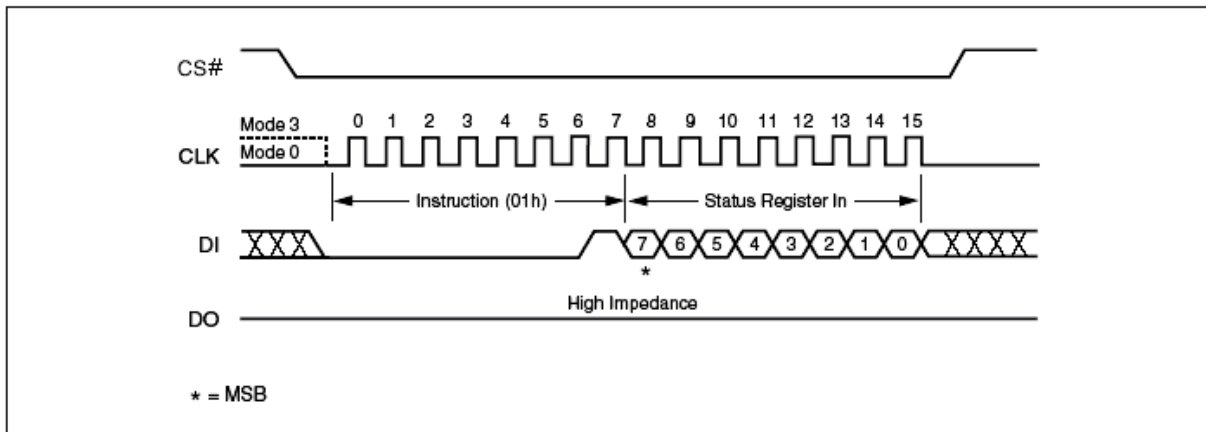
The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The instruction sequence is shown in Figure 8. The Write Status Register (WRSR) instruction has no effect on S6, S5, S1 and S0 of the Status Register. S6 and S5 are always read as 0. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is  $t_w$ ) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 3. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

**NOTE :** In the OTP mode, WRSR command will ignore input data and program OTP\_LOCK bit to 1.

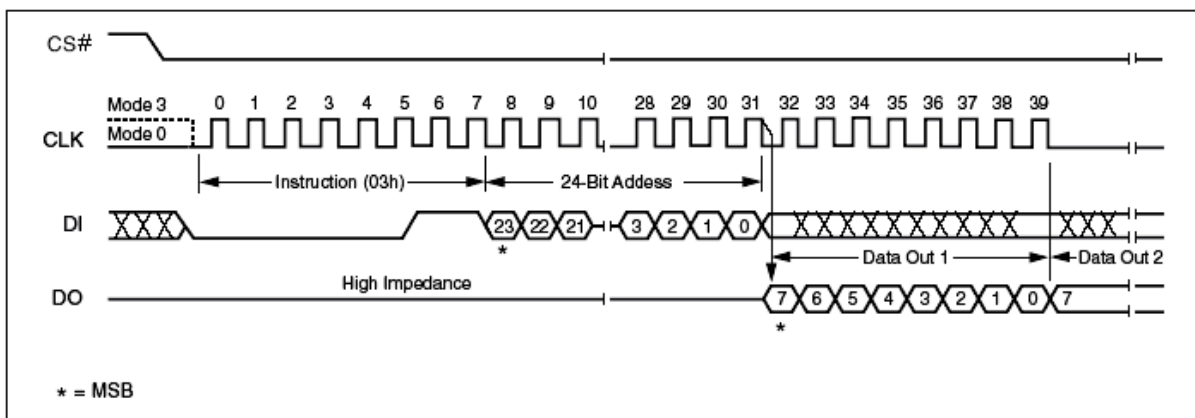

**Figure 8. Write Status Register Instruction Sequence Diagram**

### Read Data Bytes (READ) (03h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency  $f_R$ , during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

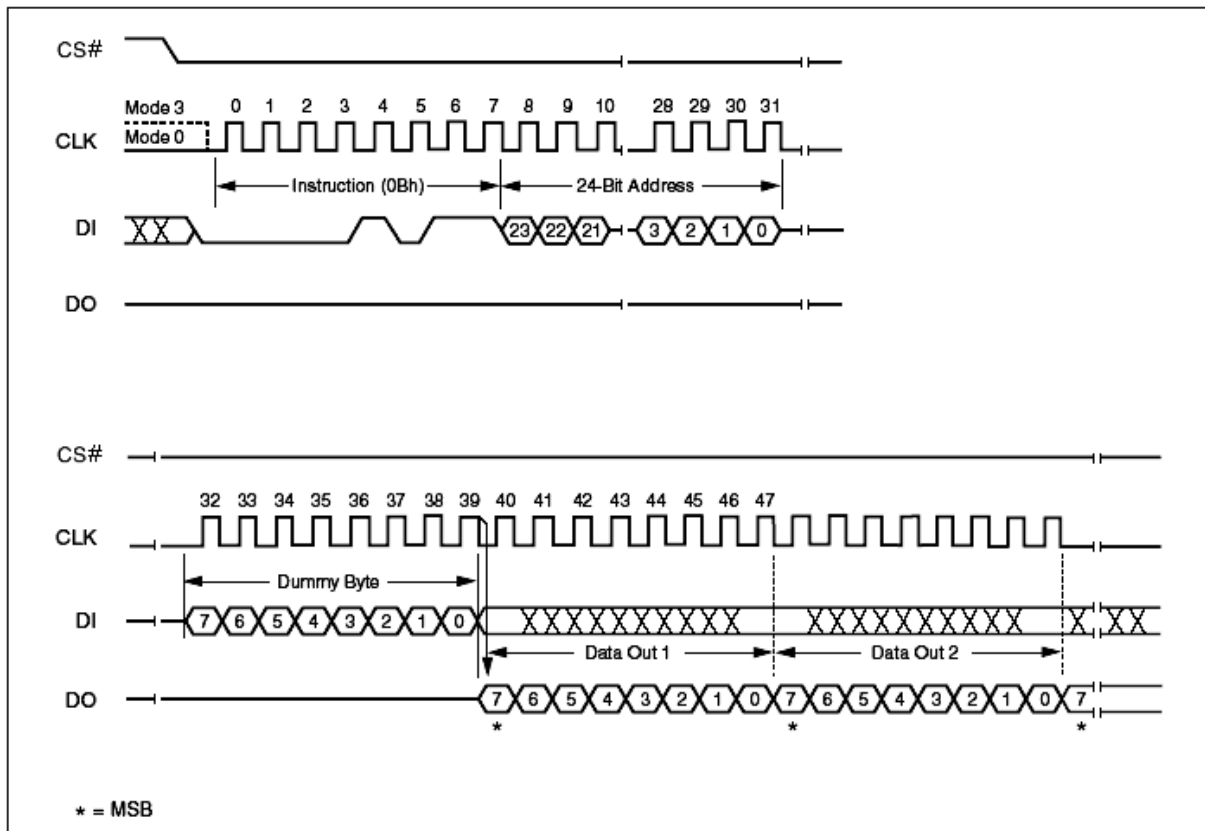

**Figure 9. Read Data Instruction Sequence Diagram**

**Read Data Bytes at Higher Speed (FAST\_READ) (0Bh)**

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST\_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency  $F_R$ , during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST\_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST\_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST\_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

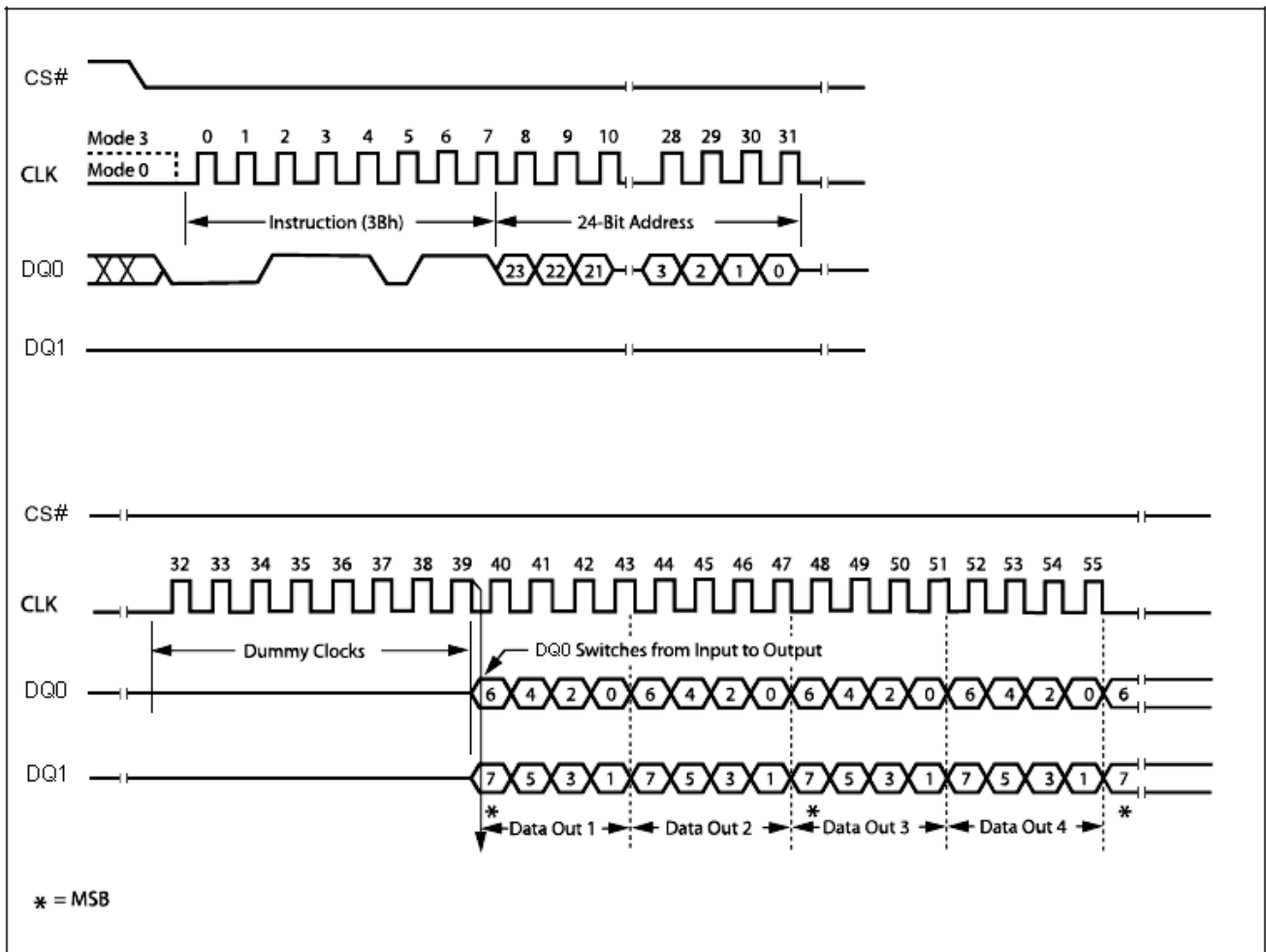

**Figure 10. Fast Read Instruction Sequence Diagram**



**Dual Output Fast Read (3Bh)**

The Dual Output Fast Read (3Bh) is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DQ<sub>0</sub> and DQ<sub>1</sub>, instead of just DQ<sub>0</sub>. This allows data to be transferred from the EN25S80 at twice the rate of standard SPI devices. The Dual Output Fast Read instruction is ideal for quickly downloading code from RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Dual Output Fast Read instruction can operation at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy clocks” after the 24-bit address as shown in figure 11. The dummy clocks allow the device’s internal circuits additional time for setting up the initial address. The input data during the dummy clock is “don’t care”. However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.

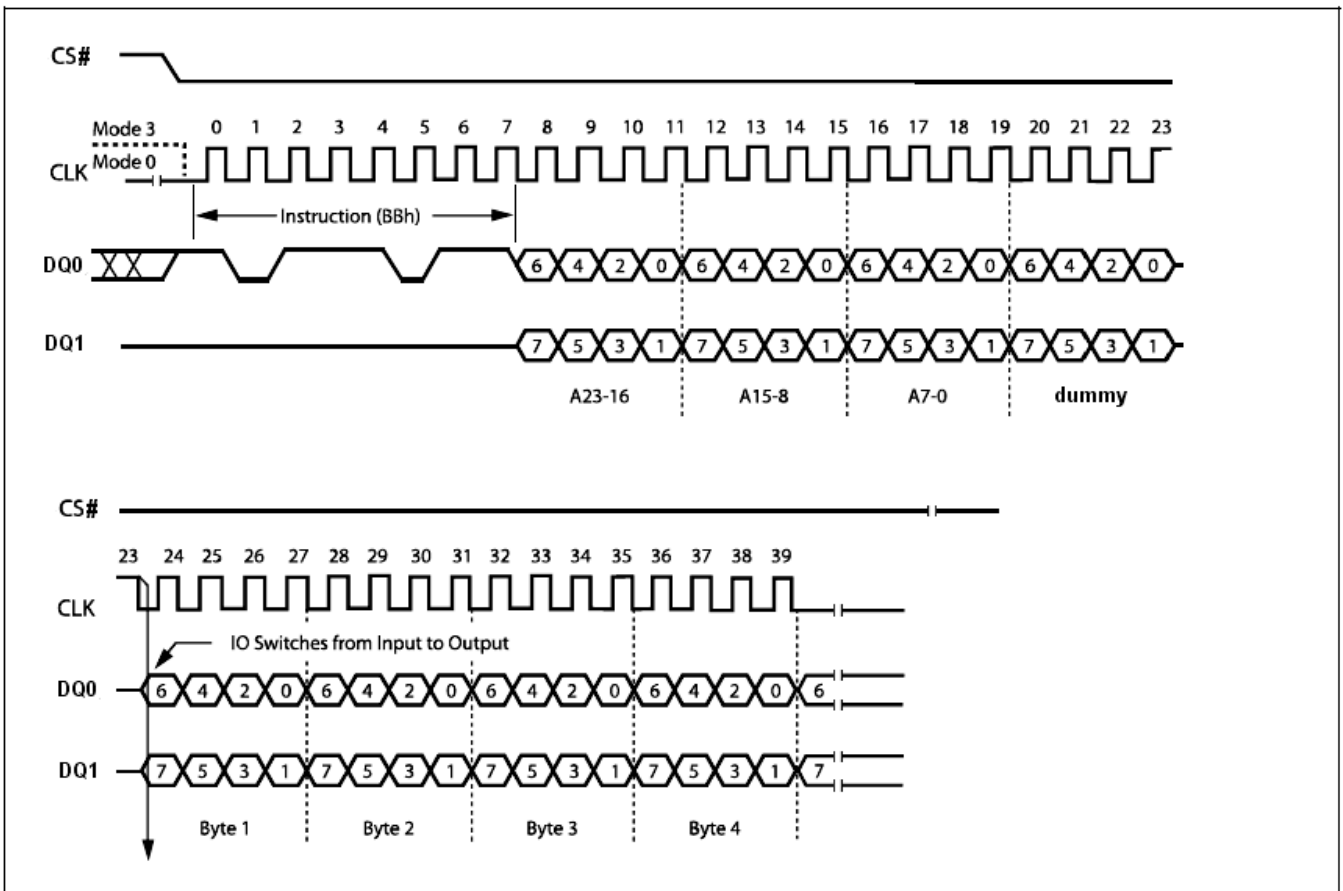


**Figure 11. Dual Output Fast Read Instruction Sequence Diagram**

**Dual Input / Output FAST\_READ (BBh)**

The Dual I/O Fast Read (BBh) instruction allows for improved random access while maintaining two IO pins, DQ<sub>0</sub> and DQ<sub>1</sub>. It is similar to the Dual Output Fast Read (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Dual I/O Fast Read instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of CLK, and data of every two bits (interleave 2 I/O pins) shift out on the falling edge of CLK at a maximum frequency. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Dual I/O Fast Read instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Dual I/O Fast Read instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit, as shown in Figure 12.



**Figure 12. Dual Input / Output Fast Read Instruction Sequence Diagram**

**Page Program (PP) (02h)**

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

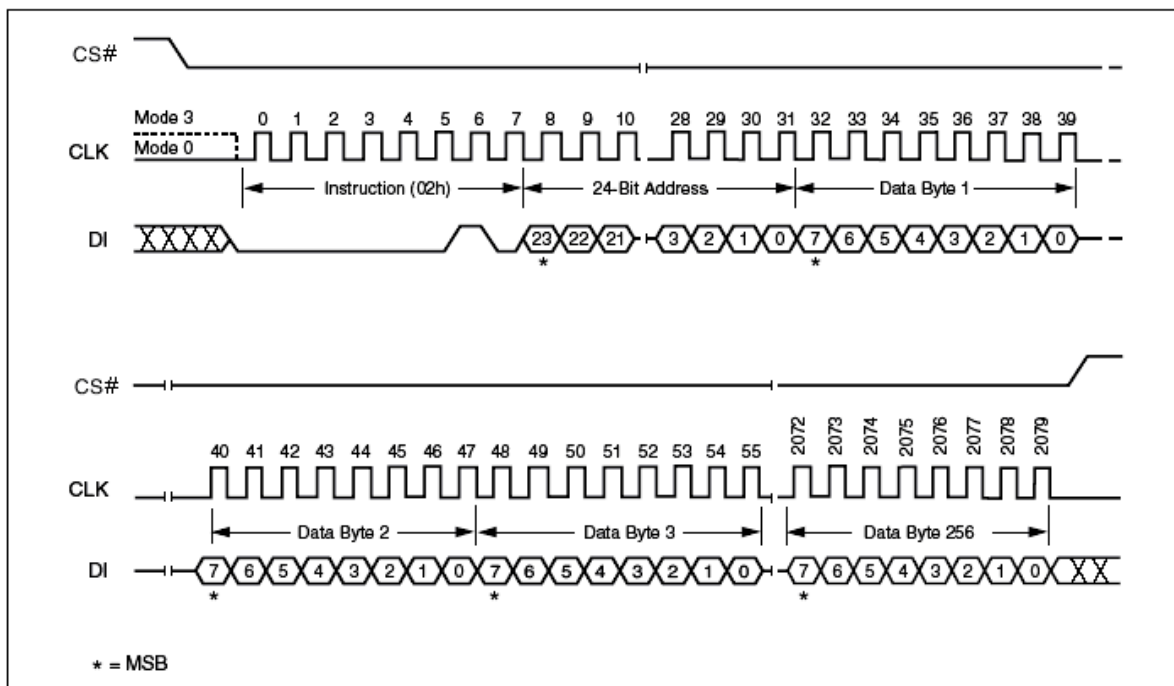
The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 13. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is  $t_{pp}$ ) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.



**Figure 13. Page Program Instruction Sequence Diagram**

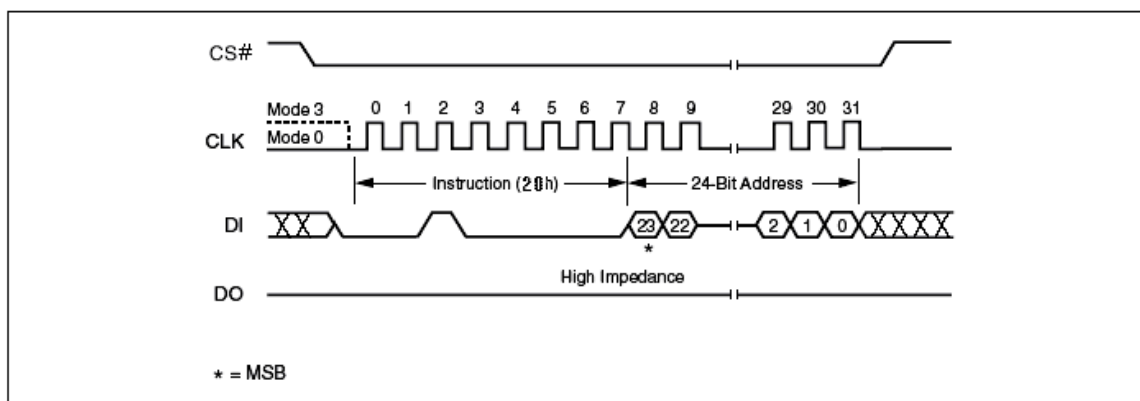
**Sector Erase (SE) (20h)**

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Sector (see Table 2) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 14. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is  $t_{SE}$ ) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a sector which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.



**Figure 14. Sector Erase Instruction Sequence Diagram**

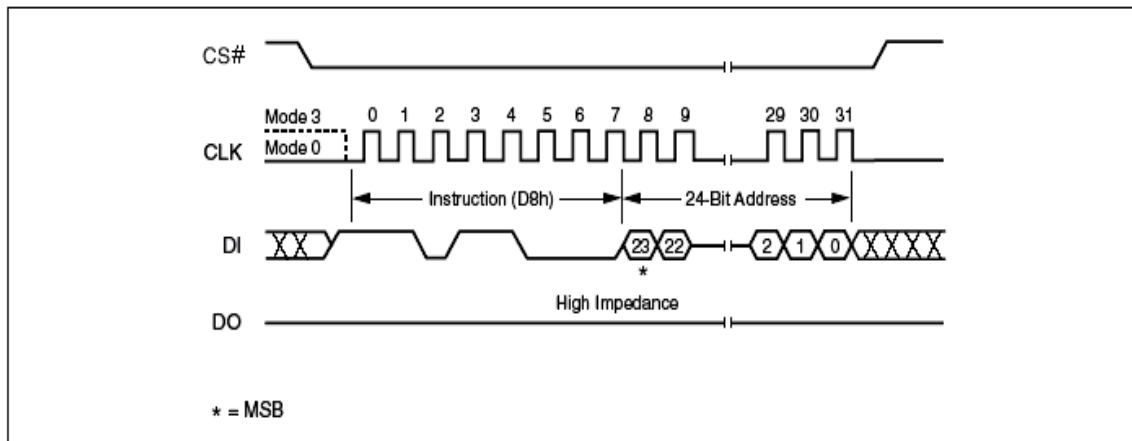
**Block Erase (BE) (D8h)**

The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Block Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Block (see Table 2) is a valid address for the Block Erase (BE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 15. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Block Erase (BE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Block Erase cycle (whose duration is  $t_{BE}$ ) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Block Erase (BE) instruction applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

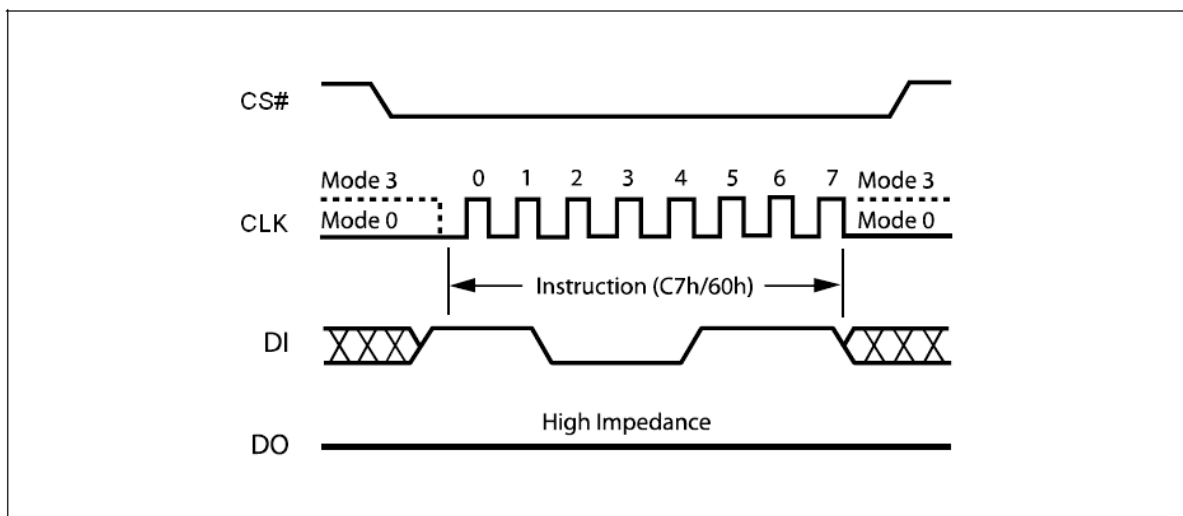

**Figure 15. Block Erase Instruction Sequence Diagram**
**Chip Erase (CE) (C7h/60h)**

The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Chip Erase (CE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 16. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Chip Erase cycle (whose duration is  $t_{CE}$ ) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) instruction is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Chip Erase (CE) instruction is ignored if one, or more blocks are protected.


**Figure 16. Chip Erase Instruction Sequence Diagram**

**Deep Power-down (DP) (B9h)**

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

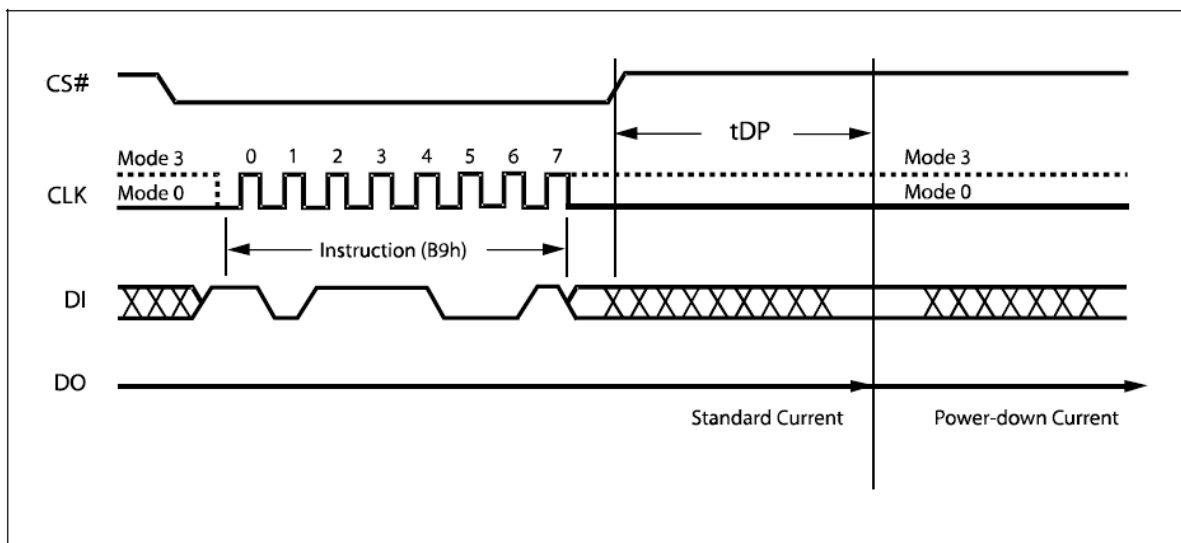
Driving Chip Select (CS#) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from  $I_{CC1}$  to  $I_{CC2}$ , as specified in Table 9.)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Device ID (RDI) instruction also allows the Device ID of the device to be output on Serial Data Output (DO).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode. The Deep Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 17. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of  $t_{DP}$  before the supply current is reduced to  $I_{CC2}$  and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.



**Figure 17. Deep Power-down Instruction Sequence Diagram**

**Release from Deep Power-down and Read Device ID (RDI)**

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identifier (RDID) instruction. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) instruction.

When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high as shown in Figure 18. After

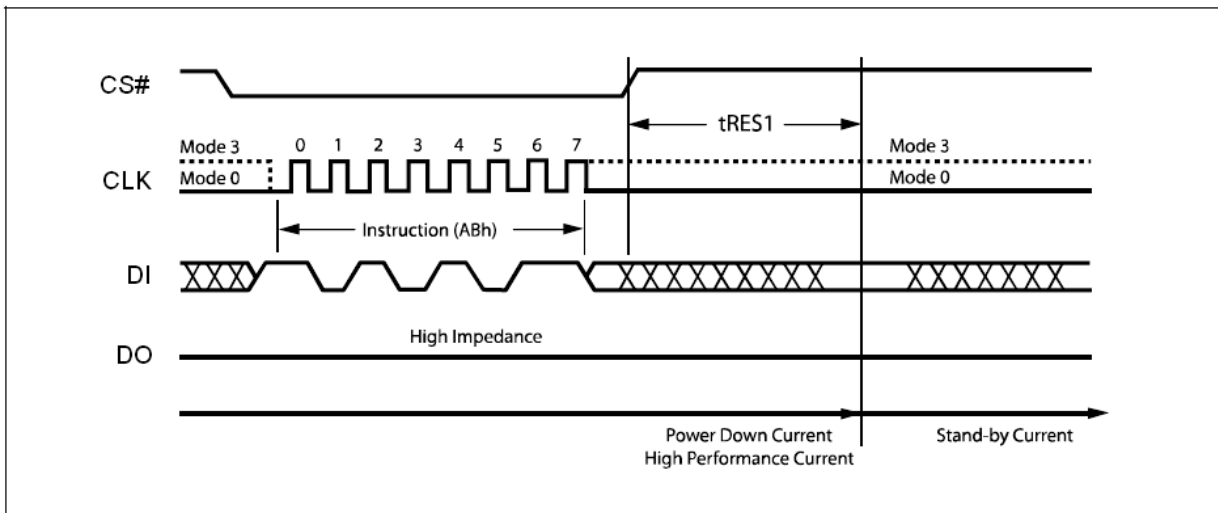
the time duration of  $t_{RES1}$  (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the  $t_{RES1}$  time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 19. The Device ID value for the EN25S80 are listed in Table 5. The Device ID can be read continuously. The instruction is completed by driving CS# high.

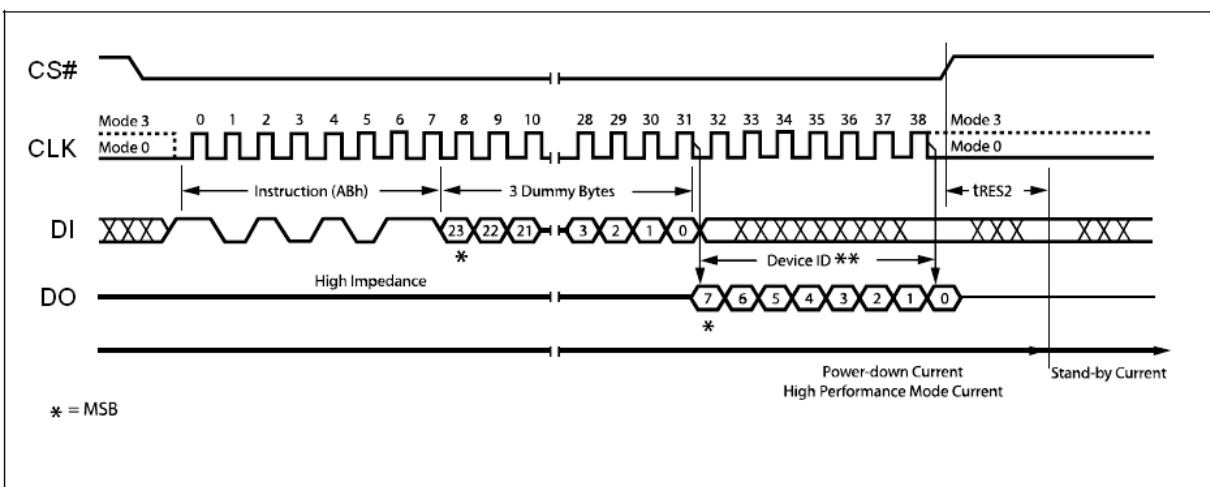
When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by  $t_{RES2}$ , and Chip Select (CS#) must remain High for at least  $t_{RES2}$  (max), as specified in Table 11. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) instruction always provides access to the 8bit Device ID of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Device ID (RDI) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.



**Figure 18. Release Power-down Instruction Sequence Diagram**

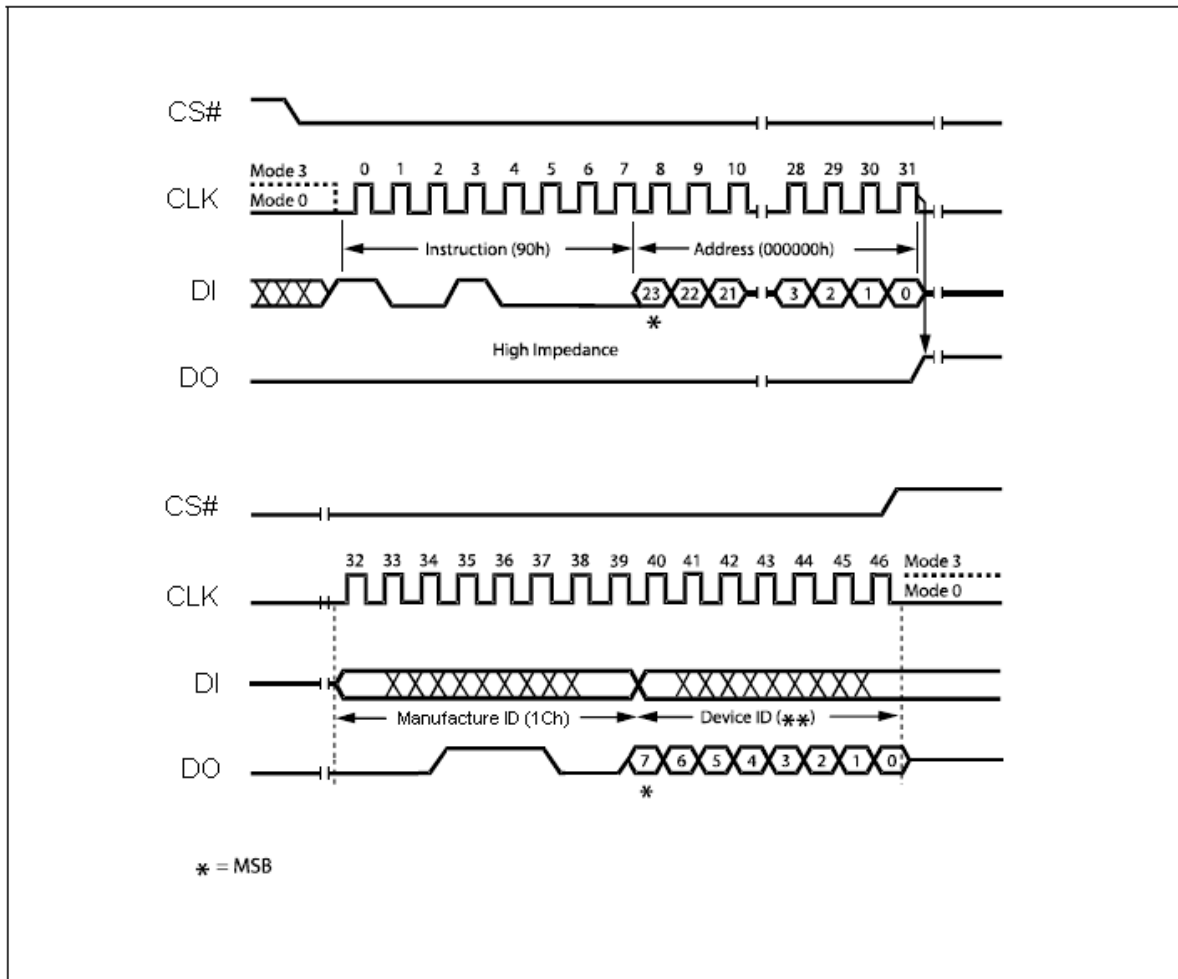


**Figure 19. Release Power-down / Device ID Instruction Sequence Diagram**

**Read Manufacturer / Device ID (90h)**

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Eon (1Ch) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 20. The Device ID values for the EN25S80 are listed in Table 5. If the 24-bit address is initially set to 000001h the Device ID will be read first



**Figure 20. Read Manufacturer / Device ID Diagram**

**Read Identification (RDID) (9Fh)**

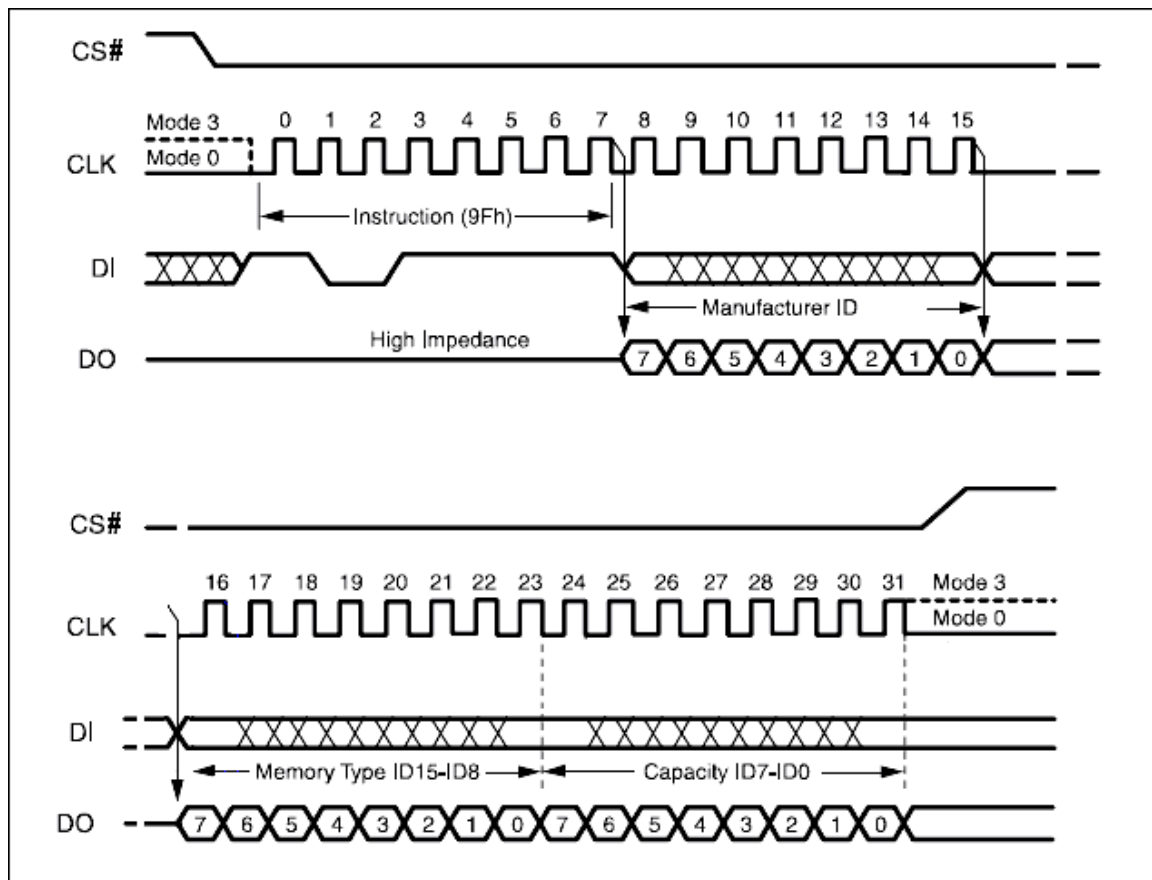
The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte.

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) instruction should not be issued while the device is in Deep Power down mode.

The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The instruction sequence is shown in Figure 21. The Read Identification (RDID) instruction is terminated by driving Chip Select High at any time during data output.



When Chip Select is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.



**Figure 21. Read Identification (RDID)**

### Enter OTP Mode (3Ah)

This Flash has an extra 256 bytes OTP sector, user must issue ENTER OTP MODE command to read, program or erase OTP sector. After entering OTP mode, the OTP sector is mapping to sector 255, **SRP bit** becomes OTP\_LOCK bit and can be read with RDSR command. Program / Erase command will be disabled when OTP\_LOCK bit is '1'

WRSR command will ignore the input data and program OTP\_LOCK bit to 1.

User must clear the protect bits before enter OTP mode.

OTP sector can only be program and erase before OTP\_LOCK bit is set to '1' and BP [2:0] = '000'. In OTP mode, user can read other sectors, but program/erase other sectors only allowed when OTP\_LOCK bit equal to '0'.

User can use WRDI (04h) command to exit OTP mode.

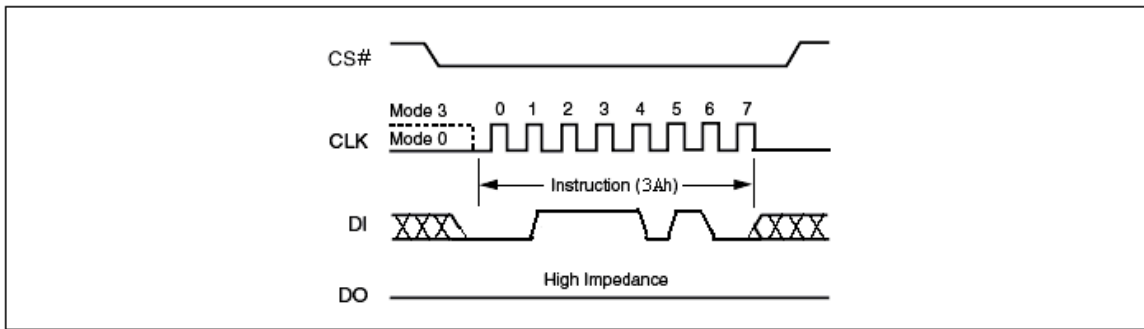
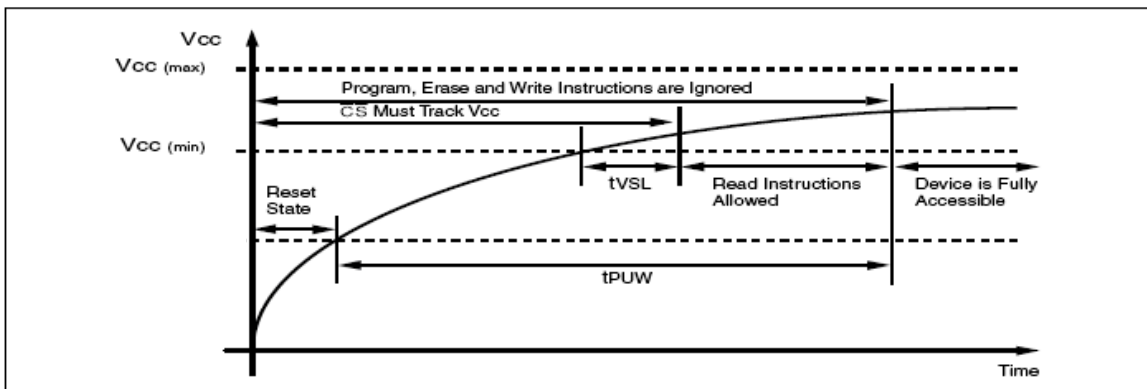
### Erase OTP Command (20h)

User can use Sector Erase (20h) command only to erase OTP data.

**Table 7. OTP Sector Address**

Sector	Sector Size	Address Range
255	256 byte	0FF000h – 0FF0FFh

Note: The OTP sector is mapping to sector 255


**Figure 22. Enter OTP Mode**
**Power-up Timing**

**Figure 23. Power-up Timing**
**Table 8. Power-Up Timing and Write Inhibit Threshold**

Symbol	Parameter	Min.	Max.	Unit
$t_{VSL}^{(1)}$	VCC(min) to CS# low	10		$\mu s$
$t_{PUW}^{(1)}$	Time delay to Write instruction	1	10	ms

**Note:**

1. The parameters are characterized only.

**INITIAL DELIVERY STATE**

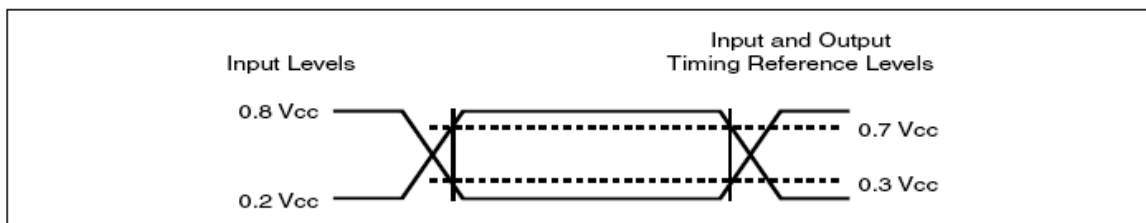
The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

**Table 9. DC Characteristics**
 $(T_a = -40^{\circ}\text{C to } 85^{\circ}\text{C}; V_{CC} = 1.65\text{-}1.95\text{V})$ 

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$I_{LI}$	Input Leakage Current			2	$\mu\text{A}$
$I_{LO}$	Output Leakage Current			2	$\mu\text{A}$
$I_{CC1}$	Standby Current	$CS\# = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$		5	$\mu\text{A}$
$I_{CC2}$	Deep Power-down Current	$CS\# = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$		5	$\mu\text{A}$
$I_{CC3}$	Operating Current (READ)	CLK = $0.1 V_{CC} / 0.9 V_{CC}$ at 75MHz, DQ = open		14	mA
		CLK = $0.1 V_{CC} / 0.9 V_{CC}$ at 30MHz, DQ = open		11	mA
$I_{CC4}$	Operating Current (PP)	$CS\# = V_{CC}$		15	mA
$I_{CC5}$	Operating Current (WRSR)	$CS\# = V_{CC}$		15	mA
$I_{CC6}$	Operating Current (SE)	$CS\# = V_{CC}$		15	mA
$I_{CC7}$	Operating Current (BE)	$CS\# = V_{CC}$		15	mA
$V_{IL}$	Input Low Voltage		-0.5	$0.2 V_{CC}$	V
$V_{IH}$	Input High Voltage		$0.7V_{CC}$	$V_{CC}+0.4$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 100 \mu\text{A}, V_{CC}=V_{CC} \text{ Min.}$		0.3	V
$V_{OH}$	Output High Voltage	$I_{OH} = -100 \mu\text{A}, V_{CC}=V_{CC} \text{ Min.}$	$V_{CC}-0.2$		V

**Table 10. AC Measurement Conditions**

Symbol	Parameter	Min.	Max.	Unit
$C_L$	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	$0.2V_{CC} \text{ to } 0.8V_{CC}$		V
	Input Timing Reference Voltages	$0.3V_{CC} \text{ to } 0.7V_{CC}$		V
	Output Timing Reference Voltages	$V_{CC} / 2$		V


**Figure 24. AC Measurement I/O Waveform**

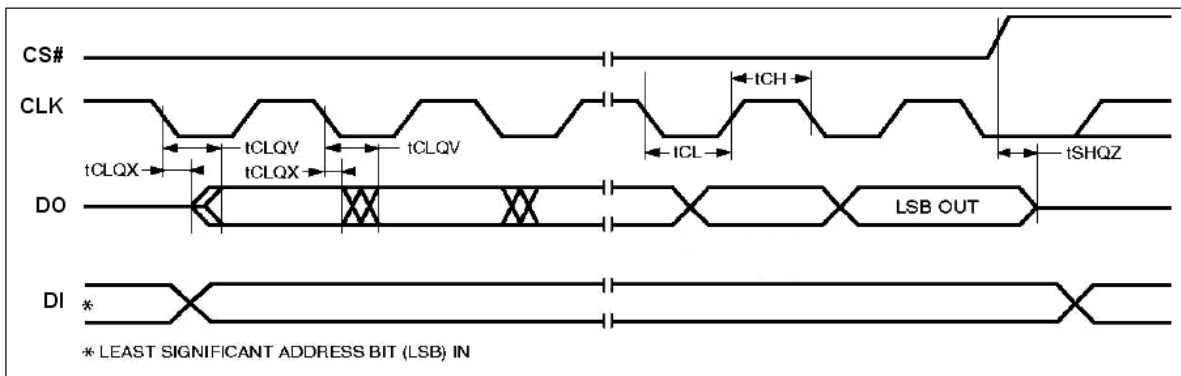
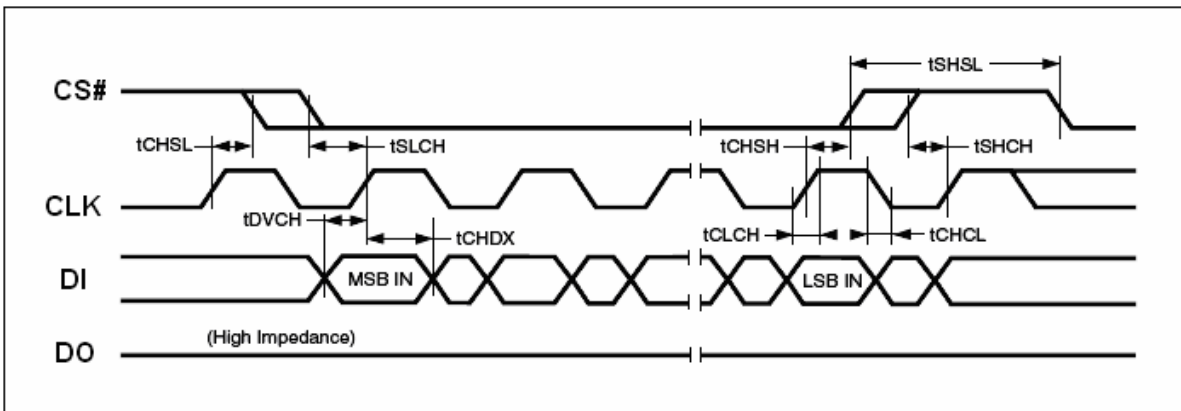
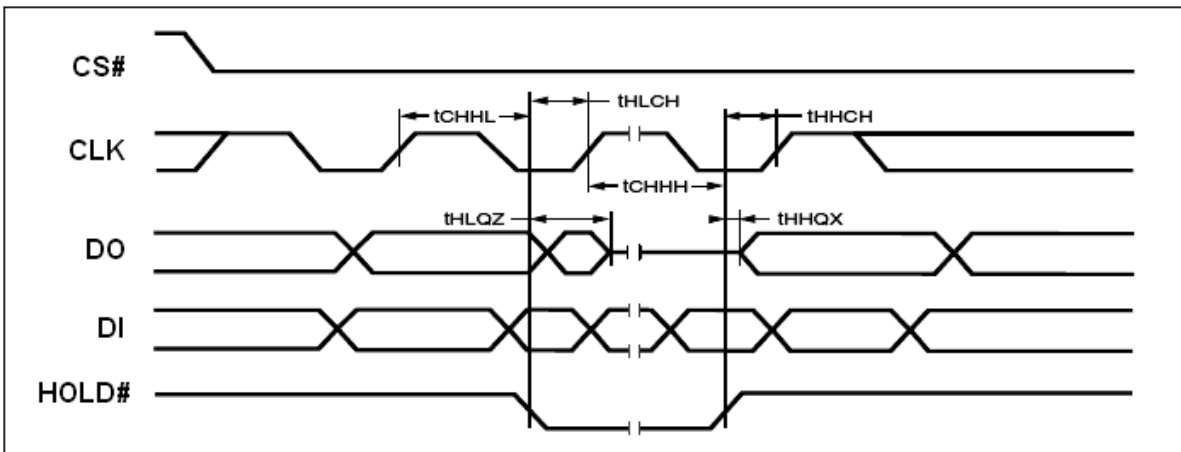


**Table 11. AC Characteristics**

( $T_a = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ;  $V_{CC} = 1.65\text{-}1.95\text{V}$ )

Symbol	Alt	Parameter	Min	Typ	Max	Unit
$F_R$	$f_C$	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR	D.C.		75	MHz
		Serial Clock Frequency for: Dual Fast Read \ Dual I/O	D.C.		50	MHz
$f_R$		Serial Clock Frequency for READ, RDSR, RDID	D.C.		33	MHz
$t_{CH}^1$		Serial Clock High Time	6			ns
$t_{CL}^1$		Serial Clock Low Time	6			ns
$t_{CLCH}^2$		Serial Clock Rise Time (Slew Rate)	0.1			V / ns
$t_{CHCL}^2$		Serial Clock Fall Time (Slew Rate)	0.1			V / ns
$t_{SLCH}$	$t_{CSS}$	CS# Active Setup Time	5			ns
$t_{CHSH}$		CS# Active Hold Time	5			ns
$t_{SHCH}$		CS# Not Active Setup Time	5			ns
$t_{CHSL}$		CS# Not Active Hold Time	5			ns
$t_{SHSL}$	$t_{CSH}$	CS# High Time	100			ns
$t_{SHQZ}^2$	$t_{DIS}$	Output Disable Time			6	ns
$t_{CLQX}$	$t_{HO}$	Output Hold Time	0			ns
$t_{DVCH}$	$t_{DSU}$	Data In Setup Time	2			ns
$t_{CHDX}$	$t_{DH}$	Data In Hold Time	5			ns
$t_{HLCH}$		HOLD# Low Setup Time ( relative to CLK )	5			ns
$t_{HHCH}$		HOLD# High Setup Time ( relative to CLK )	5			ns
$t_{CHHH}$		HOLD# Low Hold Time ( relative to CLK )	5			ns
$t_{CHHL}$		HOLD# High Hold Time ( relative to CLK )	5			ns
$t_{HLQZ}^2$	$t_{HZ}$	HOLD# Low to High-Z Output			6	ns
$t_{HHQX}^2$	$t_{LZ}$	HOLD# High to Low-Z Output			6	ns
$t_{CLQV}$	$t_V$	Output Valid from CLK ( 75 MHz Fast read)			8	ns
		Output Valid from CLK ( 50 MHz Dual fast read)			9	ns
		Output Valid from CLK ( 33 MHz Normal read)			13	ns
$t_{WHSL}^3$		Write Protect Setup Time before CS# Low	20			ns
$t_{SHWL}^3$		Write Protect Hold Time after CS# High	100			ns
$t_{DP}^2$		CS# High to Deep Power-down Mode			3	$\mu\text{s}$
$t_{RES1}^2$		CS# High to Standby Mode without Electronic Signature read			3	$\mu\text{s}$
$t_{RES2}^2$		CS# High to Standby Mode with Electronic Signature read			1.8	$\mu\text{s}$
$t_W$		Write Status Register Cycle Time		20	50	ms
$t_{PP}$		Page Programming Time		1.3	5	ms
$t_{SE}$		Sector Erase Time		0.09	0.3	s
$t_{BE}$		Block Erase Time		0.5	2	s
$t_{CE}$		Chip Erase Time		5	20	s

- Note:** 1.  $t_{CH} + t_{CL}$  must be greater than or equal to  $1/f_C$   
 2. Value guaranteed by characterization, not 100% tested in production.  
 3. Only applicable as a constraint for a Write status Register instruction when Status Register Protect Bit is set at 1.


**Figure 25. Serial Output Timing**

**Figure 26. Input Timing**

**Figure 27. Hold Timing**

## ABSOLUTE MAXIMUM RATINGS

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

Parameter	Value	Unit
Storage Temperature	-65 to +150	°C
Plastic Packages	-65 to +125	°C
Output Short Circuit Current <sup>1</sup>	200	mA
Input and Output Voltage (with respect to ground) <sup>2</sup>	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>CC</sub>	-0.5 to V <sub>CC</sub> +0.5	V

Notes:

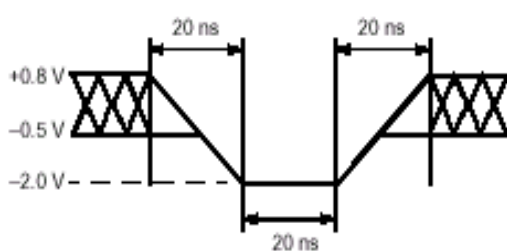
- No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
- Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, inputs may undershoot V<sub>SS</sub> to -1.0V for periods of up to 50ns and to -2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V<sub>CC</sub> + 0.5 V. During voltage transitions, outputs may overshoot to V<sub>CC</sub> + 2.0 V for periods up to 20ns. See figure below.

## RECOMMENDED OPERATING RANGES<sup>1</sup>

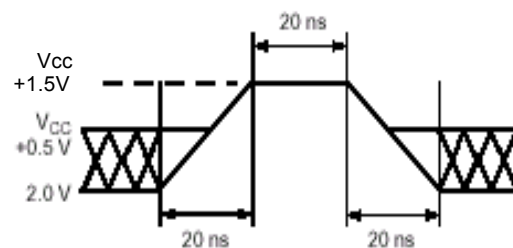
Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	°C
Operating Supply Voltage V <sub>CC</sub>	Full: 1.65 to 1.95	V

Notes:

- Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

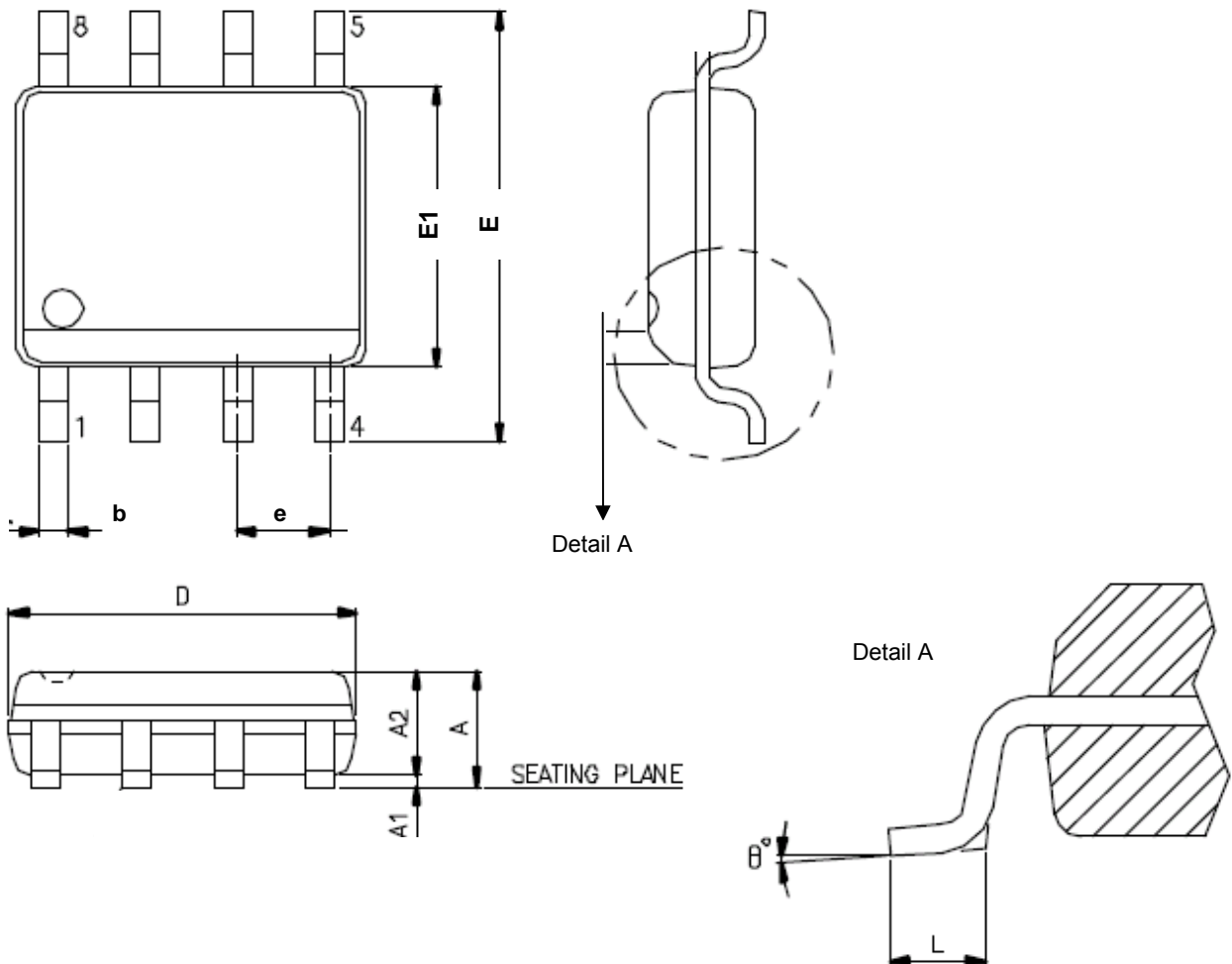
**Table 12. DATA RETENTION and ENDURANCE**

Parameter Description	Test Conditions	Min	Unit
Data Retention Time	150°C	10	Years
	125°C	20	Years
Erase/Program Endurance	-40 to 85 °C	100k	cycles

**Table 13. CAPACITANCE**(V<sub>CC</sub> = 1.65-1.95V)

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0		6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0		8	pF

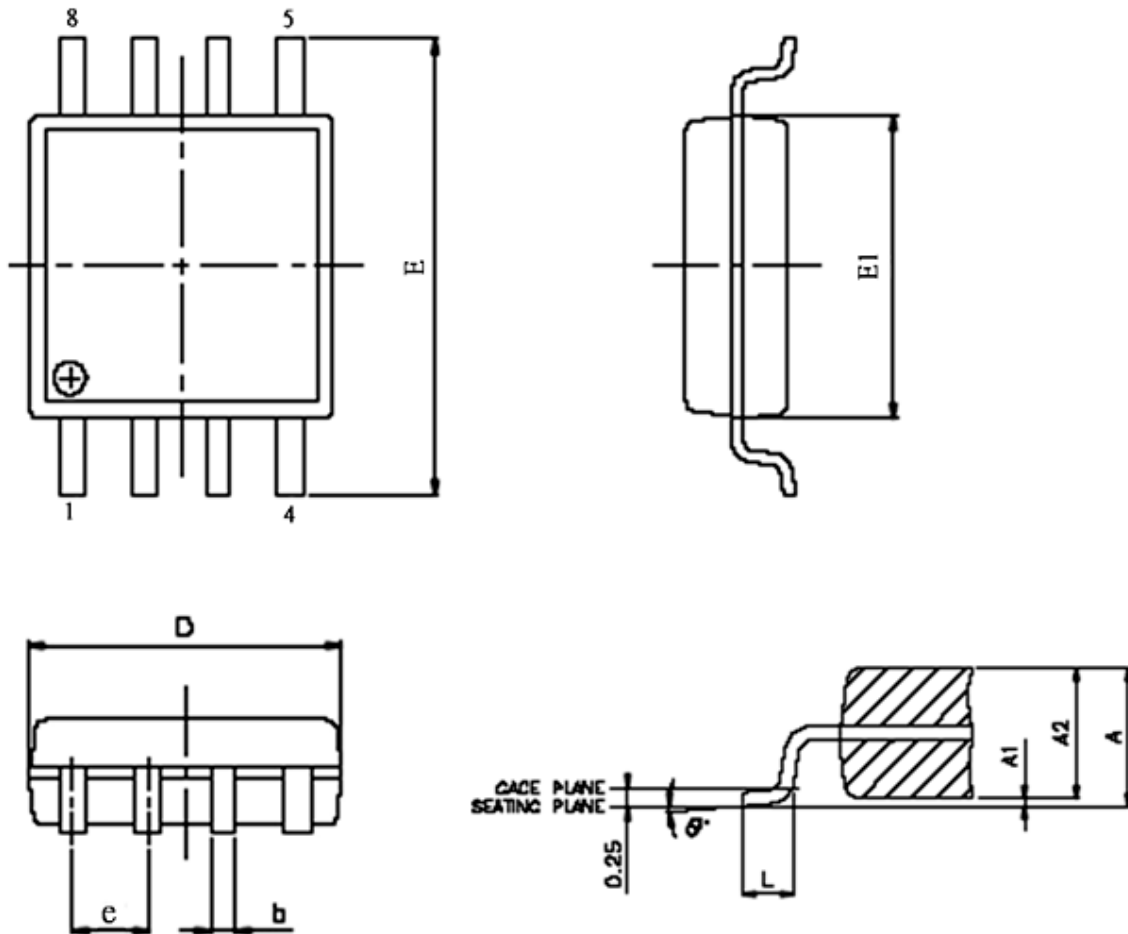
**Note** : Sampled only, not 100% tested, at T<sub>A</sub> = 25°C and a frequency of 20MHz.

**PACKAGE MECHANICAL**
**Figure 28. SOP 8 ( 150 mil )**


SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	1.35	---	1.75
A1	0.10	---	0.25
A2	---	---	1.50
D	4.80	---	5.00
E	5.80	---	6.20
E1	3.80	---	4.00
e	---	1.27	---
b	0.33	---	0.51
L	0.4	---	1.27
$\theta$	$0^\circ$	---	$8^\circ$

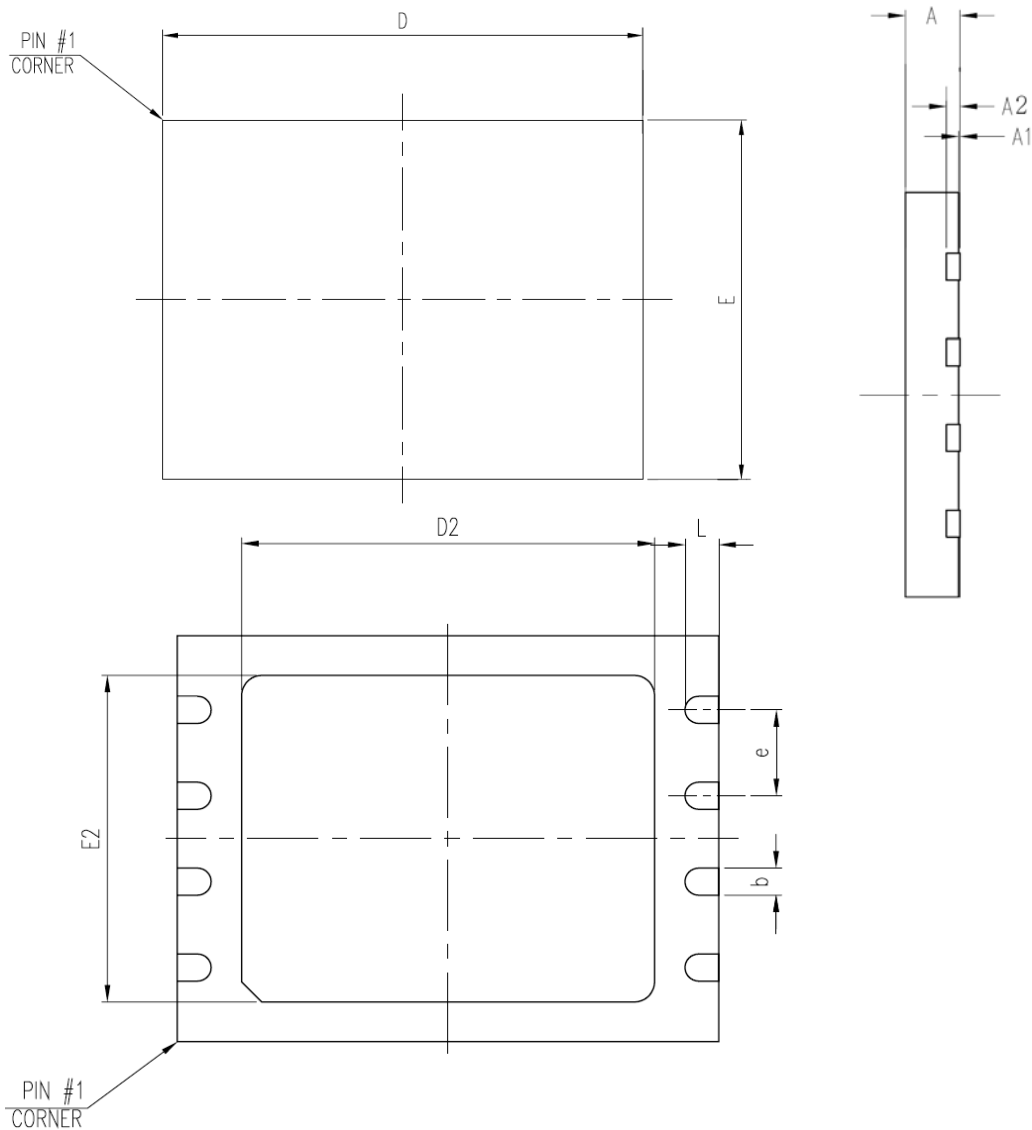
Note : 1. Coplanarity: 0.1 mm  
 2. Max. allowable mold flash is 0.15 mm  
 at the pkg ends, 0.25 mm between leads.



**Figure 29. SOP 200 mil ( Official name = 208 mil )**


SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	1.75	1.975	2.20
A1	0.05	0.15	0.25
A2	1.70	1.825	1.95
D	5.15	5.275	5.40
E	7.70	7.90	8.10
E1	5.15	5.275	5.40
e	---	1.27	---
b	0.35	0.425	0.50
L	0.5	0.65	0.80
$\theta$	$0^{\circ}$	$4^{\circ}$	$8^{\circ}$

Note : 1. Coplanarity: 0.1 mm  
 2. Max. allowable mold flash is 0.15 mm  
 at the pkg ends, 0.25 mm between leads.

**Figure 30. VDFN8 ( 5x6mm )**


SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.04
A2	---	0.20	---
D	5.90	6.00	6.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.90	4.00	4.10
e	---	1.27	---
b	0.35	0.40	0.45
L	0.55	0.60	0.65

**Note: 1. Coplanarity: 0.1 mm**



## Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

## Eon products’ New Top Marking

**cFeon**

**cFeon Top Marking Example:**

**cFeon**

**Part Number: XXXX-XXX**

**Lot Number: XXXXX**

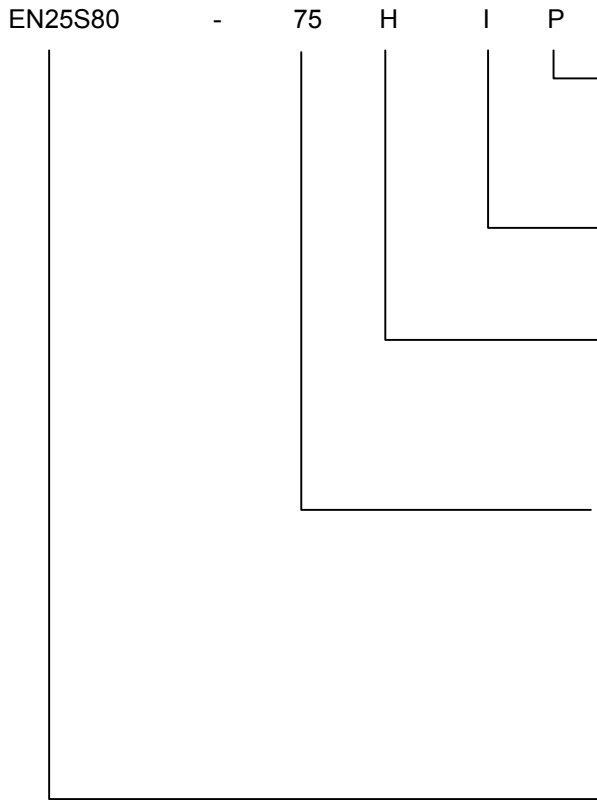
**Date Code: XXXXX**

## For More Information

Please contact your local sales office for additional information about Eon memory solutions.



**ORDERING INFORMATION**



**PACKAGING CONTENT**

(Blank) = Conventional  
P = RoHS compliant

**TEMPERATURE RANGE**

I = Industrial (-40°C to +85°C)

**PACKAGE**

G = 8-pin 150mil SOP  
H = 8-pin 200mil SOP  
W = 8-pin VDFN

**SPEED**

75 = 75 MHz

**BASE PART NUMBER**

EN = Eon Silicon Solution Inc.  
25S = 1.8V Serial Flash with 4KB Uniform-Sector  
80 = 8 Megabit (1024K x 8)

**Revisions List**

<b>Revision No</b>	<b>Description</b>	<b>Date</b>
A	Preliminary version	2008/10/03
B	1. Modify device ID in Table 5 on Page 11 2. Modify tCLQV in Table 11 on Page28 3. Add cFeon new top marking notice on Page 35	2008/12/31
C	1. Remove Quad mode spec. 2. Correction word OTP 512 to 256 byte on page 24 3. Update page program, Sector erase, Block erase time and Chip erase time on page1 and 27 4. Modify $f_R$ from 50 to 33MHz 5. Correction word $t_{CH}$ and $t_{CL}$ on page 27 6. Modify $t_W$ from Typ 10ms and Max 15ms to Typ 20ms and Max to 50ms 7. Add package 8 pins SOP 150mil body width 8. Modify $V_{OL}$ test condition and Max value to 0.3V in table 9	2009/02/18
D	1. Update Block erase: from 0.4s to 0.5s on page 1 and 28. 2. Add the description of OTP erase command on page 10 and page 25. 3. Recover the Dual Input / Output FAST_READ (BBh) spec. on page 18 4. Correction typo for mapping to sector from 1023 to 255 on page 25.	2009/05/15