Large Current External FET Controller Type Switching Regulators

Single/Dual-output High-frequency Step-down Switching Regulator(Controllertype)

BD9853AFV

No.09028EAT05

●Description

The BD9853AFV is a 2-ch synchronous DC/DC controller that can operate at a maximum switching frequency of 2MHz, enabling the use of a smaller external coil than conventional lower-frequency switching regulators. This makes the BD9853AFV a suitable choice for downsizing applications.

●Features

1) Synchronous Switching Regulator Controller 2channels
2) FET(Pch/Nch) Direct Drive
3) Adjustable Oscillator Frequency with External Resistor (Max. 2MHz)
4) Under Voltage Lockout Function (UVLO)
5) Thermal Shut Down Function (TSD)
6) Short Circuit Protection (SCP)
7) Independent ON/OFF Function in Each Channel with Soft Start Pin
8) SSOP-B16 Package

●Applications

TVSTB, PC, Portable CD・DVD,DVC etc.

●Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage (VCC-GND)	Vcc	18	V
VREGA-GND Voltage	VREGA	7	V
VCC-VREGB Voltage	VREGB	7	V
Power Dissipation	Pd	562(*1)	mW
Operating Temperature Range	Topr	-40 to +85	℃
Junction Temperature	Tjmax	+150	℃
Storage Temperature Range	Tstg	-55 to +150	℃

* Reduced by 4.49mW for each increase in Ta of 1℃ over 25℃ (When mounted on a board 70×70×1.6tmm grass-epoxy PCB)

●Recommended Operating Conditions

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Supply Voltage	Vcc	4.5	12	16	V
Oscillator Frequency	fosc	100	1000	2000	KHz

●**Electrical Characteristics** (Unless otherwise specified Ta=25℃,Vcc=12V,fosc=1000kHz,STB=3V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
【Whole Device】						
Standby Current	Iccst	—	0	5	μA	STB=0V
Circuit Current	Icc	—	3.2	5.2	mA	INV1,INV2=2.5V
【Regulator for Driver REGA】						
Output Voltage	Vrega	4.5	5.0	5.5	V	
Output Current Capability	Irega	—	—	-100	mA	Vrega > 4.5V
【Regulator for Driver REGB】						
Output Voltage	Vregb	V_{CC}-5.5	V_{CC}-5.0	V_{CC}-4.5	V	
Output Current Capability	Iregb	100	—	—	mA	Vregb < Vcc-4.5V
【Oscillator】						
Oscillator Frequency	fosc	900	1000	1100	kHz	RRT=8.2kΩ OUTH=2200pF,OUTL=1000pF
Oscillator Frequency Coefficient1	Dfosc1	-2	0	2	%	Vcc=4.5 to 5V
Oscillator Frequency Coefficient2	Dfosc2	-2	0	2	%	Vcc=5 to 18V
【Error Amplifier】						
Threshold Voltage	Vthea	0.79	0.80	0.81	V	
Input Bias Current	Ibias	-230	-115	—	nA	
Voltage Gain	Av	60	80	100	dB	DC GAIN
Max. Output Voltage	Vfbh	V_{rega}-0.85	—	—	V	
Min. Output Voltage	Vfbl	—	—	0.85	V	
Output Sink Current	Isink	2	11	-	mA	INV=2.5V, FB=2.5V
Output Source Current	Isource	-	-15	-2	mA	INV=0V, FB=2.5V
【PWM Comparator】						
0% Threshold Voltage	Vth0	1.4	1.5	1.6	V	FB Voltage
100% Threshold Voltage	Vth100	2.4	2.5	2.6	V	FB Voltage

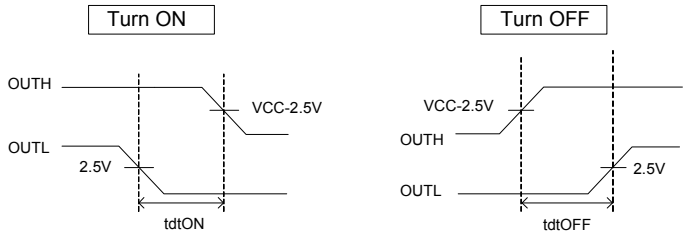
* This product is not designed for the protection against radioactive rays.

●Electrical Characteristics (Unless otherwise specified, Ta=25℃,Vcc=12V,fosc=1000kHz,STB=3V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
【FET Driver】						
On Resistance (OUT1H)	RonP	1.6	3.2	4.8	Ω	OUT=Hi
	RonN	1.7	3.4	5.1	Ω	OUT=Lo
On Resistance (OUT1L)	RonP	1.6	3.2	4.8	Ω	OUT=Hi
	RonN	1.7	3.4	5.1	Ω	OUT=Lo
On Resistance (OUT2H)	RonP	1.6	3.2	4.5	Ω	OUT=Hi
	RonN	1.7	3.4	5.1	Ω	OUT=Lo
On Resistance (OUT2L)	RonP	1.6	3.2	4.8	Ω	OUT=Hi
	RonN	1.7	3.4	5.1	Ω	OUT=Lo
Dead Time(Turn ON)	tdtON	30	70	120	ns	*OUTH,L H→L,OUTH=2200pF,OUTL=1000pF
Dead Time(Turn OFF)	tdtOFF	25	60	115	ns	*OUTH,L H→L,OUTH=2200pF,OUTL=1000pF
【Control Block】						
Threshold Voltage	Vstb	0.6	1.5	2.4	V	
Sink Current	Istb	6	15	30	μA	
【Soft Start Block】						
Soft Start Start-yo Voltage	Vstasoft	0.2	0.3	0.4	V	Output OFF when Vscp/SOFT＜Vstass
Standby Voltage	Vstsoft	—	—	40	mV	SCP/SOFT Voltage
Source Current	Isosoft	-3.2	-2.3	-1.4	μA	Vscp/SOFT=0.6V
【Short Circuit Protection (SCP)】						
Timer Start Voltage	Vtime	0.50	0.56	0.62	V	INV Voltage
Threshold Voltage	Vthscp	2.2	2.3	2.4	V	SCP/SOFT Voltage
Standby Voltage	Vstscp	1.21	1.35	1.49	V	SCP/SOFT Voltage (When soft start ends)
Source Current	Isoscp	-3.2	-2.3	-1.4	μA	SCP/SOFT=1.8V
【Under Voltage Lockout (UVLO)】						
Threshold Voltage	Vuvlo	4.0	4.15	4.30	V	Vcc sweep down
Hysteresis Voltage	DVuvlo	0.05	0.1	0.15	V	

* This product is not designed for the protection against radioactive rays.

* Measurement of dead time



●Characteristic Data

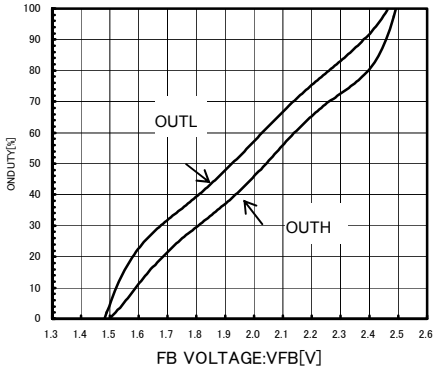


Fig.1 FB VOLTAGE VS ON DUTY

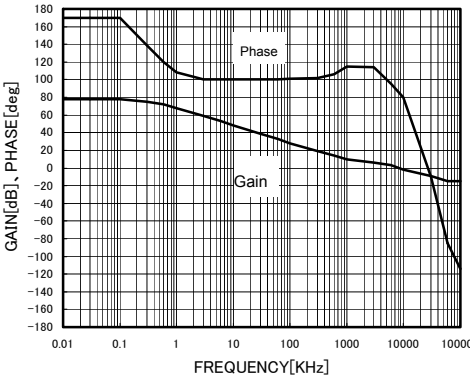


Fig.2 ERROR AMP OPEN LOOP

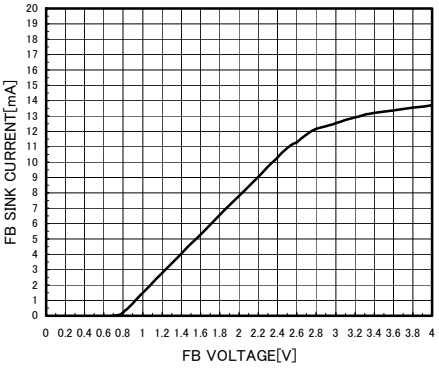


Fig.3 FB SINK CURRENT

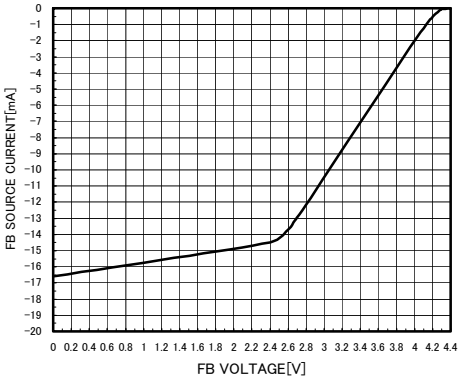


Fig.4 FB SOURCE CURRENT

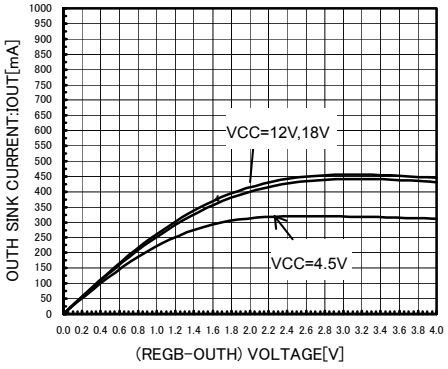


Fig.5 OUTH SINK CURRENT

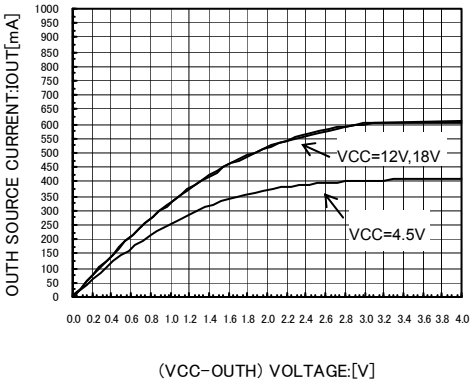


Fig.6 OUTH SOURCE CURRENT

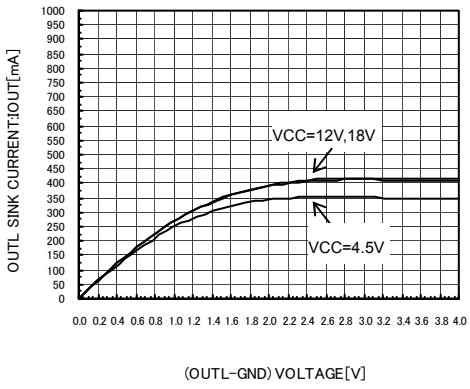


Fig.7 OUTL SINK CURRENT

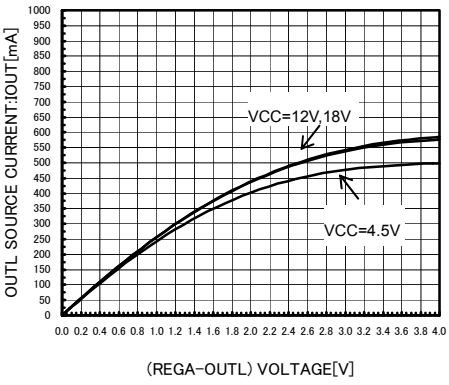


Fig.8 OUTL SOURCE CURRENT

●Block Diagram

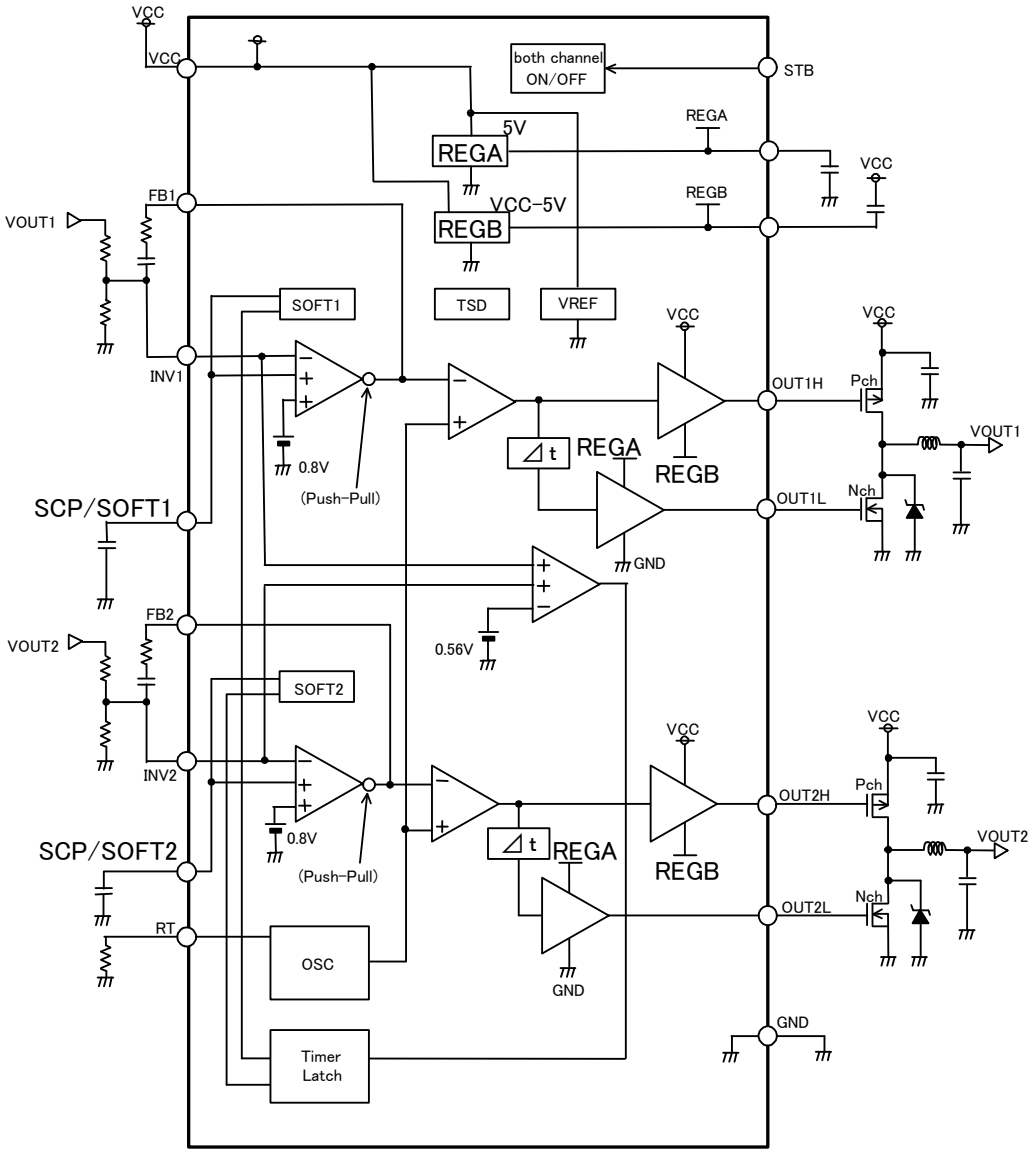


Fig. 9

●**Pin Configuration**

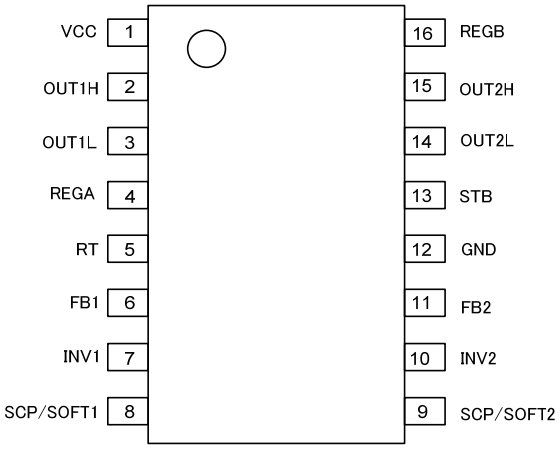


Fig. 10

●**Pin Description**

Pin Number	Pin Name	Pin Descriptions
1	VCC	Input Supply Voltage
2	OUT1H	High Side (Main) FET Driver Output Pin (CH1)
3	OUT1L	Low Side (Synchronous) FET Driver Output Pin (CH1)
4	REGA	Internal Regulator Output Pin (5V Output, 1uF Ceramic Capacitor necessary)
5	RT	Oscillator Frequency Adjustment Pin with external Resistor
6	FB1	Error Amplifier Output Pin (CH1)
7	INV1	Error Amplifer Negative Input Pin (CH1)
8	SCP/SOFT1	Short Circuit Protection・Soft Start Delay Time Setting Pin with External Capacitor (CH1)
9	SCP/SOFT2	Short Circuit Protection・Soft Start Delay Time Setting Pin with External Capacitor (CH2)
10	INV2	Error Amplifer Negative Input Pin (CH2)
11	FB2	Error Amplifier Output Pin (CH2)
12	GND	Ground Pin
13	STB	ON/OFF Control Pin
14	OUT2L	Low Side (Synchronous) FET Driver Output Pin (CH2)
15	OUT2H	High Side (Main) FET Driver Output Pin (CH2)
16	REGB	Internal Regulator Output Pin (VCC-5V Output, 1uF Ceramic Capacitor necessary)

●Block functional descriptions

・Triangular wave oscillator
Connecting the resistor that sets the triangular wave oscillation frequency at the RT terminal generates the triangular wave, which is input into the CH1 and CH2 PWM comparator.

・Error amp
The INV pin detects the output voltage, compares it to the programmed output voltage and amplifies the difference for output by the FB pin. (The 0.8V reference is the comparison voltage. The tolerance is 1.25%.)

・PWM comparator
The PWM comparator converts the error amp (FB) voltage into a pulse width modulated waveform that goes to the FET driver and turns FET output ON.

・FET driver
The push-pull FET driver directly drives the external MOSFET,providing high-side(OUT1H,OUT2H) switching at voltages between Vcc⇔REGB, and low-side switching in the 0⇔REGA voltage range. (REGA = 5V; REGB= VCC -5V internal power)

・Standby function
The standby function enables output ON/OFF control by the STB pin. Output is ON when STB voltage is HIGH.
With the STB pin set HIGH, the output ON/OFF for each channel can be independently controlled by one of the SCP/SOFT1, 2 pins.

・Soft Start/Short Circuit Protection (SCP)
Connecting the external capacitor on the SCP/SOFT1, 2 pins sets the SCP delay time and soft start time.
When STB is HIGH and the IC starts up, the capacitors on the SCP/SOFT1, 2 pins charge up at 2uA, stabilizing when the system reaches 1.3V.
If load conditions change rapidly, causing the output voltage in either channel to fall to 70% or less of the set output voltage (INV voltage 0.56 or lower), the SCP/SOFT1, 2 external capacitors will charge further until output for both channels switches OFF at 2.3V.

・Under Voltage Lockout (UVLO)
Under Voltage lockout prevents IC malfunctions that could otherwise occur due to intermittent or fluctuating power supply voltage, or insufficient voltage during start-up.When the VCC voltage falls to 4.1V or below, both channel outputs are turned OFF, while the SCP/SOFT1, 2 pins are simultaneously set LOW.
The UVLO detection voltage includes 0.1V hysteresis width to prevent malfunctions from input voltage fluctuations.

・Thermal Shutdown (TSD)
The TSD circuit protects the IC against thermal runaway and heat damage.

・The TSD thermal sensor detects junction temperature. When the temperature reaches the TSD threshold (175℃), the circuit switches the output of both channels OFF, and also switches REGA and REGB OFF. At the same time, it sets the SCP/SOFT1, 2 pins LOW. The hysteresis width (15℃) provided between the TSD function start temperature (threshold) and the stop temperature serves to prevent malfunctions from temperature fluctuations.

●Timing Chart

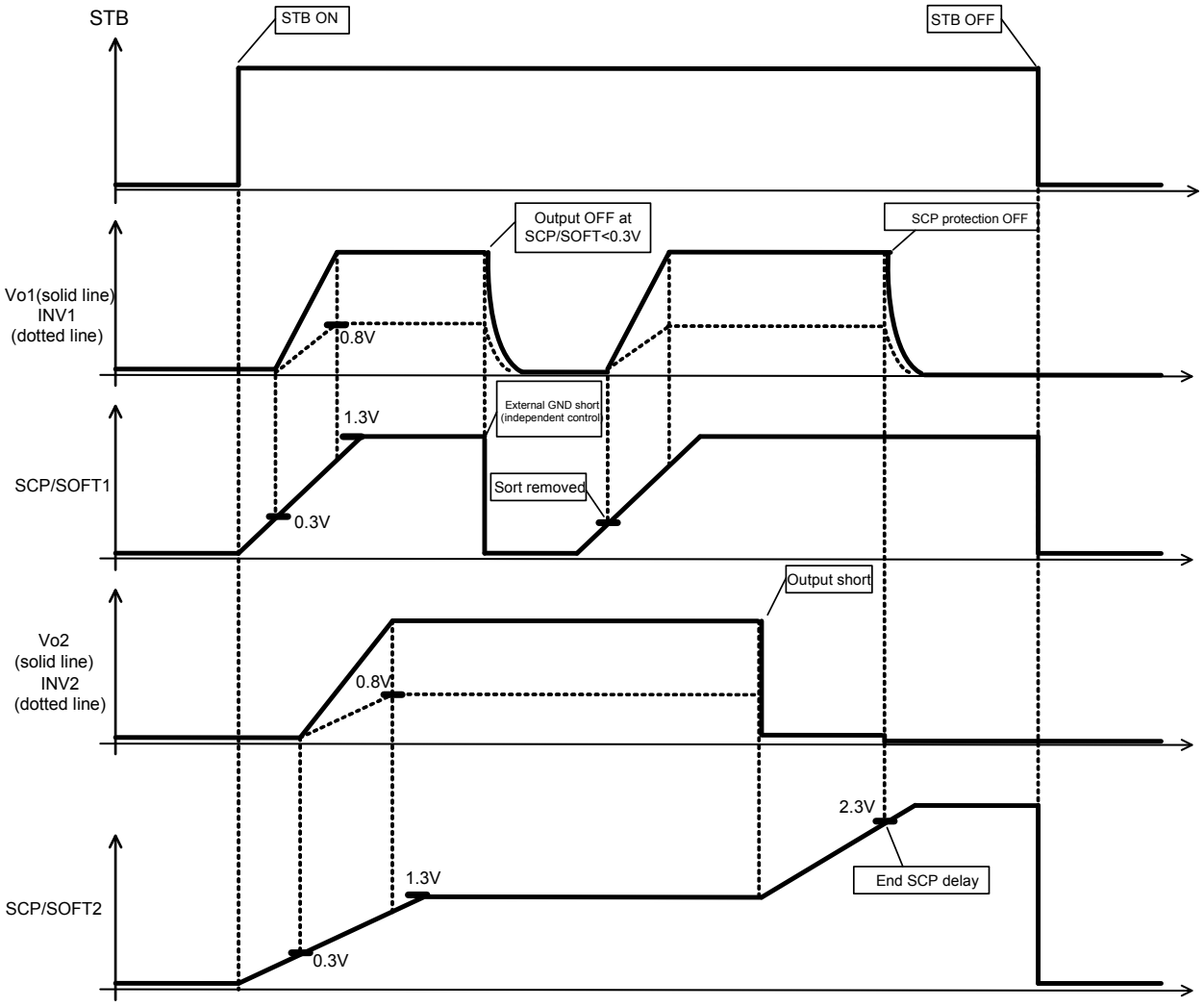


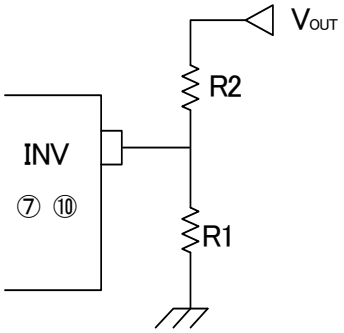
Fig. 11

●Application component selection and settings

Determining output voltage

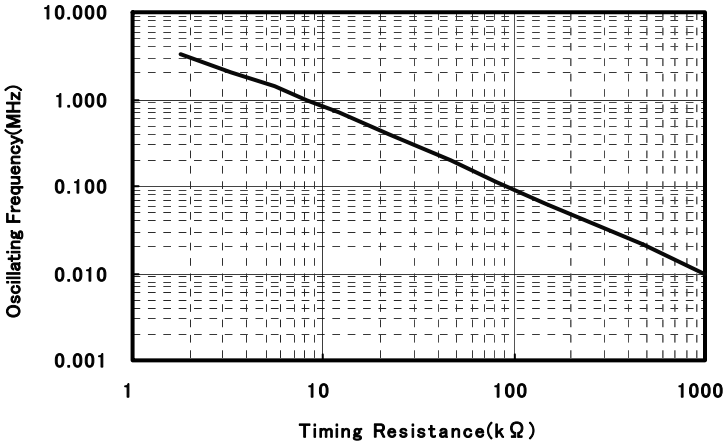
Output voltage is determined by dividing the resistance of the external resistors.

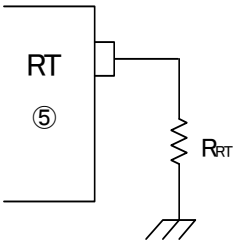
VOUT＝0.8V×(1 + R2/R1)



determining the oscillation frequency

The oscillation pin is set by the resistor connected to the RT terminal (5 PIN).





Selecting the external MOSFET

In the BD9853AFV design, the main side (OUT1H, OUT2H) is provided with an external PCH FET, while an NCH FET is used on the synchronous rectification side (OUT1L, OUT 2L) .

FET selection should be made in conformance with the following relative configurations for maximum drain voltage (VDSS), maximum gate source voltage (VGS), maximum output current, on-resistance RDS (ON) and gate capacitance (Ciss) loss:

- Maximum drain voltage (VDSS) is higher than the IC's maximum input voltage (VIN).
- Maximum gate source voltage is higher than the IC gate driving voltage (REGA, VCC-REGB).
- Maximum output current is higher than the combined maximum load current and coil ripple current (ΔI_L).
- The sum of on-resistance RDS (ON) and gate capacitance (Ciss) conduction loss, together with the switching loss, must not exceed the power dissipation (pd) for the package.

FET conduction loss Phigh and Plow are defined as follows:

Phigh=$Iout^2$×RDS(ON)×VOUT/VIN (PMOS conduction loss)

Plow=$Iout^2$×RDS(ON)×(1-VOUT/VIN) (NMOS conduction loss)

Iout：output load current, RDS(ON) : FET ON resistance value, VIN : input voltage, Vout : output voltage

FET switching loss PSW is calculated as follows:

PSW=VIN/2×(tr + tf)×fosc×Iout

VIN : input voltage, tr : drain waveform rise time, tf : drain waveform fall time, fosc : oscillation frequency, Iout : load current

In addition to the criteria for selecting individual MOSFET components, consideration must also be given to the combination of the PMOS (main side) and NMOS (synchronous side) to be used. The configuration must not generate any through current with PMOS and NMOS both ON at the same time. In order to meet this condition, the following formula must be satisfied, where PCH, NCH MOSFET turn-on delay time is represented as tdON, MOSFET turn-off delay time is tdOFF, and dead time is tdt.

tdt > tdON - tdOFF

The tdt turn-on is (OUTH,OUTL：H→L)70ns typ. Turn-off is OUTH,OUTL：L→H)70ns typ. Be sure to confirm that the process delay time does not pose problem in terms of the overall MOSFET delay.

The following MOSFETs meet all of the selection criteria outlined above, and are recommended for use. Both are manufactured by ROHM.

PCH: RSS040PO3 NCH: RSS065P03

Selecting the synchronous diode

An extremely low forward voltage Schottky barrier diode should be employed as the synchronous diode.

Selection of the specific diode to be used should be made in conformance with the following relative configurations for maximum forward current, reverse voltage and diode power dissipation.

- The maximum current rating is higher than the combined maximum load current and coil ripple current (ΔI_L).
- The reverse voltage rating is higher than the VIN value.
- Power dissipation for the selected diode must be within the rated level.

Synchronous diode power dissipation (Pdi) is expressed in the following formula:

Pdi=Iout(MAX)×tdt×fosc×Vf

Iout(MAX) : maximum load current, tdt : dead time 60ns typ,fosc : oscillation frequency, Vf : forward voltage

Selecting the output/input coil

The output coil and the output capacitor together form a second-order smoothing filter for the switch waveform and provide the DC output voltage.

If a coil's inductor value is low, its physical size is minimized, but the penalty is higher ripple current, with lowered efficiency and an increase in output noise. Conversely, a higher inductor value increases the size of the coil, but lowers the ripple current and, consequently. the output ripple current.

Generally speaking, ripple current should be between 20% and 50% of output load current. The following equation is used to calculate the inductor value that corresponds to the ripple current value being employed.

$$L=\frac{(V_{IN}-V_{OUT})}{\Delta I_L}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{f_{OSC}} \qquad \Delta I_L=(0.2 \text{ to } 0.5)\times I_{OUT}$$

L : inductor value, V_{IN} : maximum input voltage, V_{OUT} : output voltage, ΔI_L : coil ripple current value
fosc : oscillation frequency, I_{OUT} : output load current

Note that the current rating for the coil should be higher than $I_{OUT}(MAX)+\Delta I_L$.

Selecting the input capacitor

The input capacitor is the source of current that flows to the coil via the FET whenever the high side MOSFET is ON. In selecting an input capacitor, sufficient margin must be provided to accommodate capacitor pressure and the permissible ripple current.

The expression below defines the effective value of the ripple current to the input capacitor. It should be used in determining the suitability of the capacitor in providing sufficient margin for the permissible ripple current.

$$I_{RMS}=I_{OUT}\times\sqrt{(1-V_{OUT}/V_{IN})\times V_{OUT}/V_{IN}}$$

I_{RMS} : effective value of the ripple current to the input capacitor
I_{OUT} : output load current

Selecting the output capacitor

The output capacitor should confine ESR and permissible ripple current within a stable region.

Although incorporating a low-ESR capacitor will limit ripple voltage and load fluctuation, it can also hurt the stability of the feedback network. Therefore, in order to maintain a stable feedback loop when ceramic or other low-ESR capacitors are employed, special attention must be paid to providing an appropriate phase compensation scheme.

A suitable output capacitor will satisfy the following formula for ESR.

$ESR \leqq \Delta V_L/\Delta I_L$

ΔV_L : permissible ripple voltage, ΔI_L : coil ripple current

In addition, use the following formula to determine the effective value of the output capacitance permissible ripple current, and select a capacitor that allows sufficient margin to accommodate this value.

$I_{RMS}=\Delta I_L/2\sqrt{3}$

I_{RMS} : effective value of ripple current to the output condenser, ΔI_L : coil ripple current

Setting the soft start time

To prevent output voltage startup overshoot on either channel, the capacitors connected to the SCP/SOFT 1, 2 pins – in a discharged state at power-on – are gradually charged during a delay interval, thus providing a soft start. The soft start period is the time from when the standby pins go from LOW to HIGH, starting the charge, to the time that the output voltage reaches the programmed setting. The soft start time is calculated in the following equation:

$$tsoft=\frac{0.8[V]\ (typ)\times Cscp/soft\ [F]}{Isosoft\ (typ:\ 2.3\mu A)[A]}$$

tsoft : soft start time, Cscp/soft : SCP/SOFT pin connection capacitance, Isosoft : charge current

Setting the Short Circuit Protection (SCP) delay time

When the soft start is complete for each channel, the output voltage stabilizes at the set value 1.35V(typ) for the SCP/SOFT1, 2 pins.

When any type of short circuit occurs, the voltage at the point of the fault is reduced. In this case, when voltage at the INV pin falls to 0.56V(typ) or below, the SCP comparator sensor detects the short and further charges the SCP/SOFT pins for the shorted channel from the 1.35V(typ) level. When the SCP/SOFT pins are charged to 2.3V(typ), the Pch/Nch MOSFET is switched OFF.

The elapsed time from the occurrence of the output short to the point the external FET switches OFF is calculated with the following formula:

$$tscp = \frac{0.95[V](typ) \times Cscp/soft\ [F]}{Isosofc\quad (typ:\quad 2.3\mu A)[A]}$$

tscp : SCP delay time, Cscp/soft : SCP/SOFT pin connection capacitance,Isoscp : charge current

* If the current more than the capacity of power supply when the short between VOUT and GND occurs, input voltage starts to fall and under voltage lockout (UVLO) is activated at Vin < 4.15 V (typ.). The UVLO has FET driver output (OUT1H, OUT2H, OUT1L, OUT2L) off and external FETs become off. When external FETs are not operating, input voltage returns because of the short between VOUT and GND and the UVLO is canceled. But input voltage starts to fall again because the UVLO is not activated.

There is possibility that a series of behavior “output short → input voltage fall → UVLO activated → external FETs off → input voltage returns → UVLO canceled → output short”. So please make provision like inserting FUSE in input line.

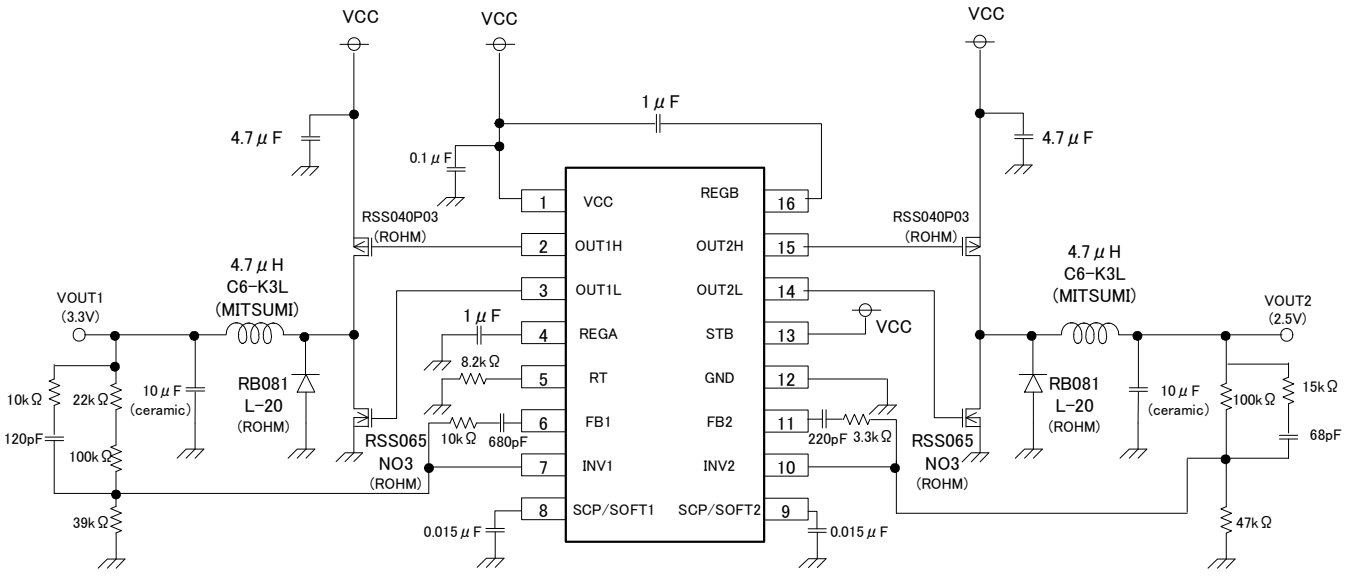
Pin conditions with the only single channel use

Pin conditions are shown in the following, when the only single channel out of 2 channels is used.

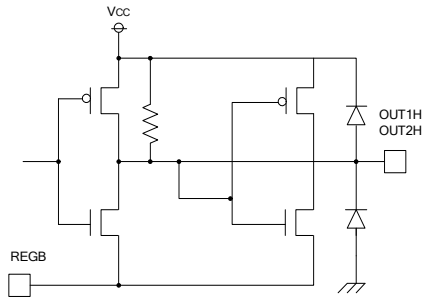
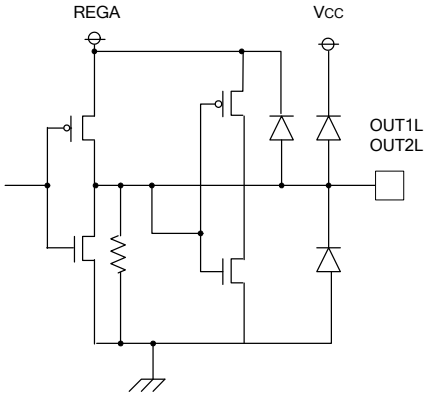
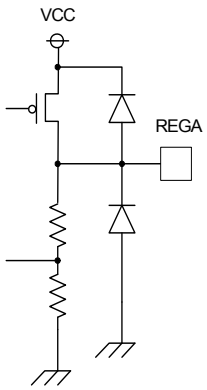
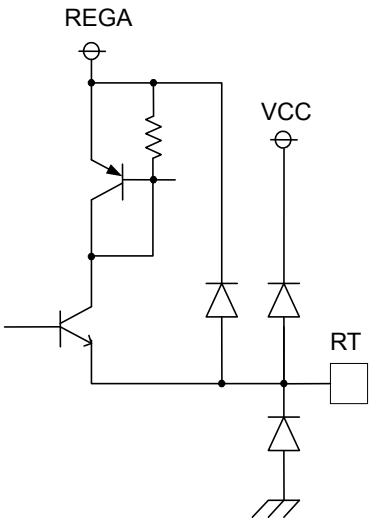
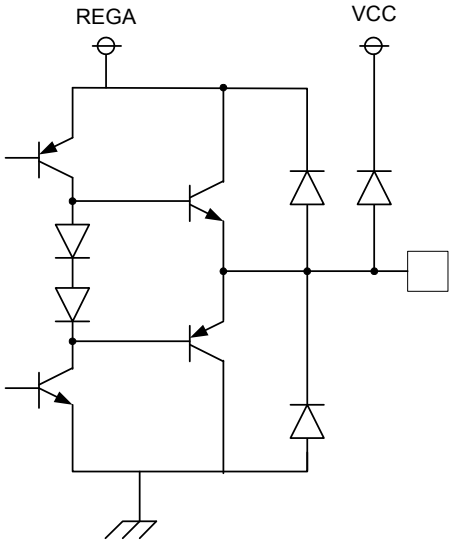
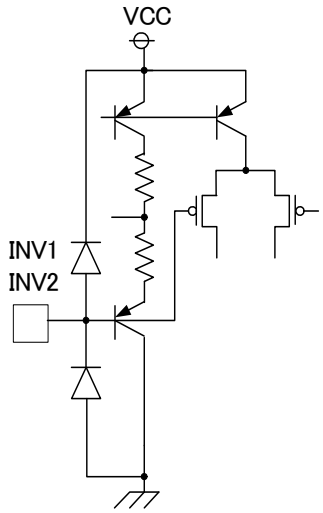
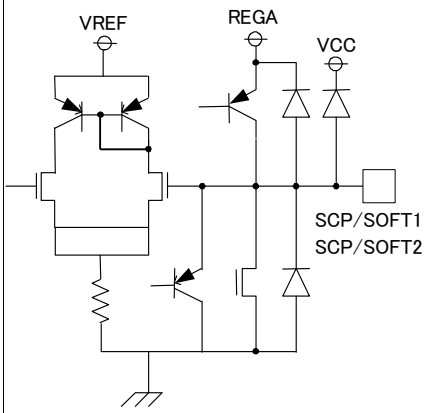
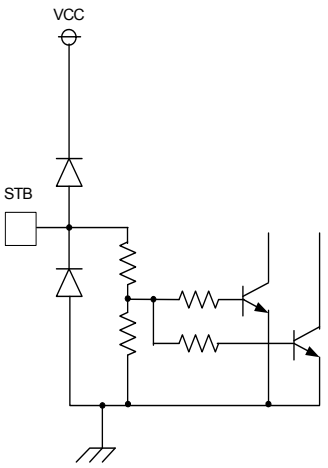
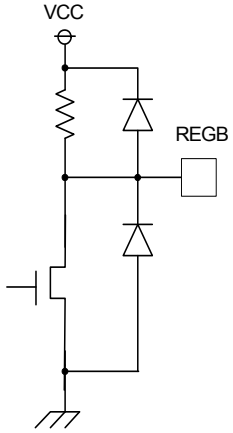
Use only CH1
- SCP/SOFT2, INV2 ⇒ GND short
- FB2, OUT2H, OUT2L ⇒ OPEN

Use only CH2
- SCP/SOFT1, INV1 ⇒ GND short
- FB1, OUT1H, OUT1L ⇒ OPEN

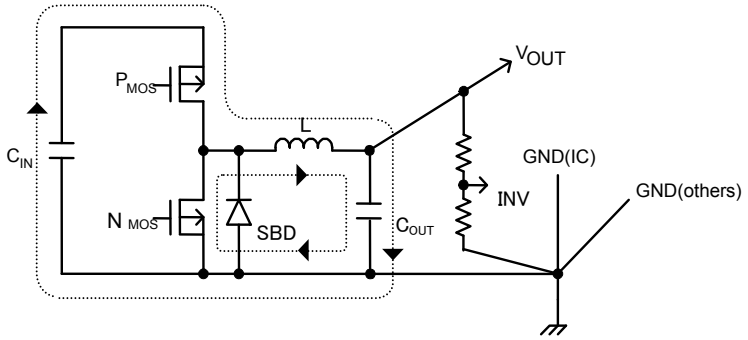
●Application example



●I/O Equivalent Circuit

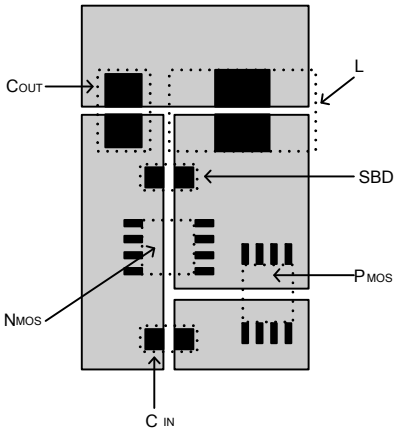
OUT1H(2),OUT2H(15)	OUT1L(3),OUT2L(14)	REGA(4)
Max ratings：7V(from VCC or REGB)	Max ratings：7V	Max ratings：7V
		
RT(5)	FB1(6),FB2(11)	INV1(7),INV2(10)
Max ratings：7V	Max ratings：7V	Max ratings：10V
		
SCP/SOFT1(8),SCP/SOFT2(9)	STB(13)	REGB(16)
Max ratings：7V	Max ratings：18V	Max ratings：7V(fromVCC)
		

●Recommended Board Patterns

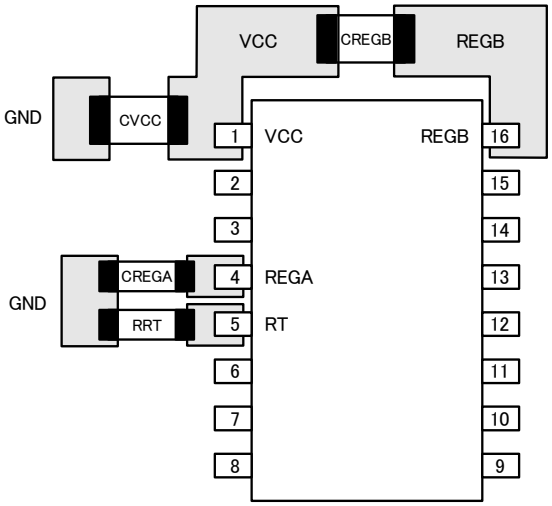


There are two current loops at the behavior of switching regulator. When laying a pattern on the board, put these elements near to minimize these current loops and make the lines as short and wide as possible. And connect all GND lines at one point to reduce effects caused by above current noise to other lines.

a pattern example of switching part



Place following parts with attention about patterns



・Place CVCC, CREGA, RRT, CREGB as near to the pin as possible.
・Pattern area has to be small enough to reduce parasitic capacitance with RT terminal.

●Notes for use

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena.

3) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.

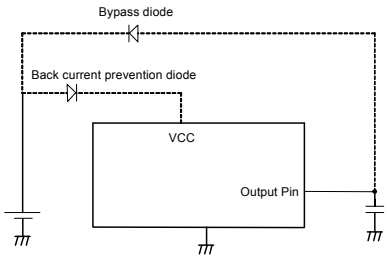
5) Operation in a strong electromagnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit (TSD circuit)
This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

7) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

8) Common impedance
Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible
(by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

9) Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits.
For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged.
It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.



10) Pin short and mistake fitting
Do not short-circuit between OUT pin and VCC pin, OUT pin and GND pin, or VCC pin and GND pin.
When soldering the IC on circuit board,
please be unusually cautious about the orientation and the position of the IC.

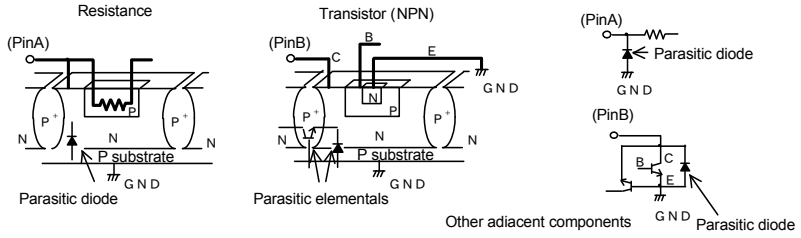
11) Timing resistor and capacitor
Timing resistor connected between RT and GND, has to be placed near RT terminal. And pattern has to be short enough.

12) IC pin input

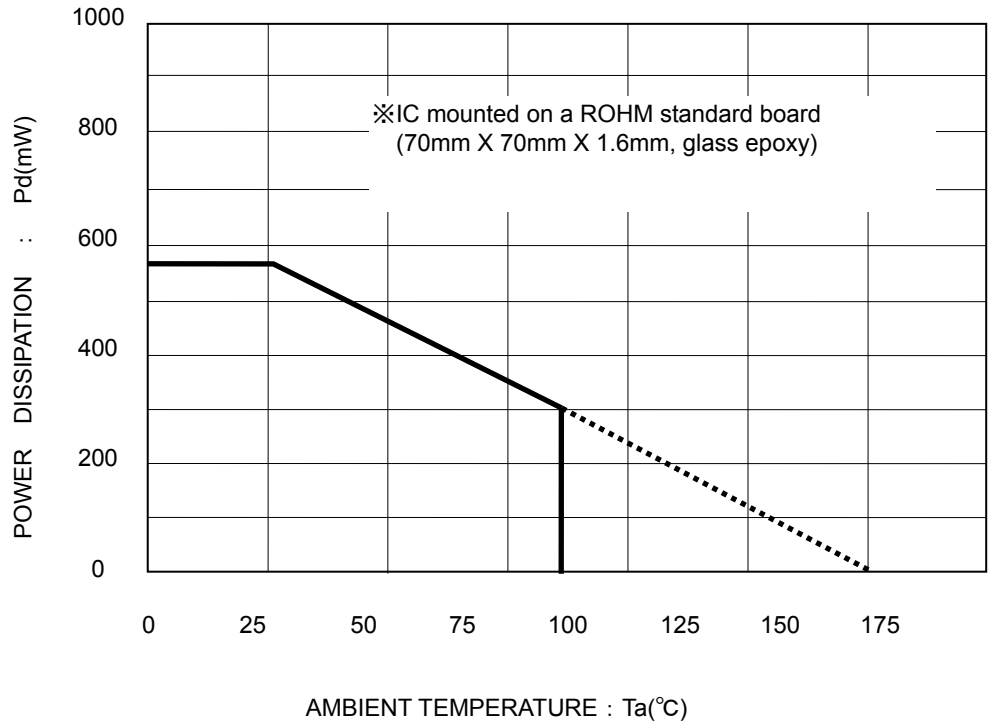
This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when a resistor and transistor are connected to pins as shown in following chart,

- ○ the P/N junction functions as a parasitic diode
  when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
- ○ Similarly, when GND > (Pin B) for the transistor (NPN),
  the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.



●Power Dissipation Reduction



●**Ordering part number**

B	D	9	8	5	3	A	F	V	-	E	2

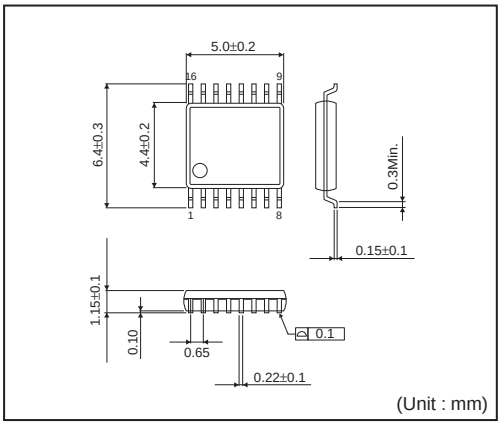
Part No.

Part No.

Package
FV: SSOP-B16

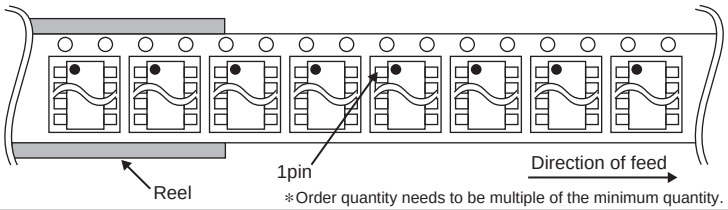
Packaging and forming specification
E2: Embossed tape and reel

SSOP-B16



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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