To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

3850 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3850 group is the 8-bit microcomputer based on the 740 family core technology.

The 3850 group is designed for the household products and office automation equipment and includes serial I/O functions, 8-bit timer, and A-D converter.

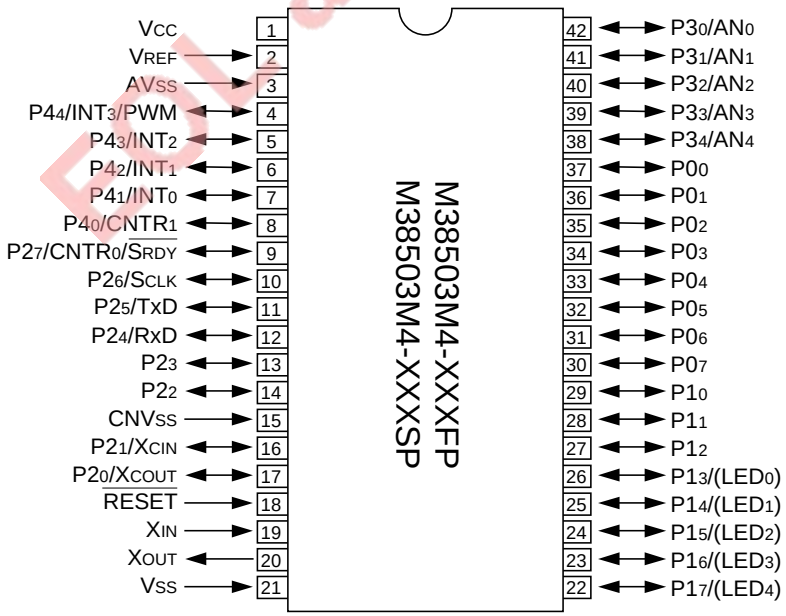
FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 0.5 µs
  (at 8 MHz oscillation frequency)
- Memory size
  ROM ..... 8K to 24K bytes
  RAM ..... 512 to 640 byte
- Programmable input/output ports 34
- Interrupts ..... 14 sources, 14 vectors
- Timers ..... 8-bit × 4
- Serial I/O ..... 8-bit × 1(UART or Clock-synchronized)
- PWM ..... 8-bit × 1
- A-D converter ..... 10-bit × 5 channels
- Watchdog timer ..... 16-bit × 1
- Clock generating circuit ..... Built-in 2 circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  In high-speed mode ..... 4.0 to 5.5 V
  (at 8 MHz oscillation frequency)
  In high-speed mode ..... 2.7 to 5.5 V
  (at 4 MHz oscillation frequency)
  In middle-speed mode ..... 2.7 to 5.5 V
  (at 8 MHz oscillation frequency)
  In low-speed mode ..... 2.7 to 5.5 V
  (at 32 kHz oscillation frequency)
- Power dissipation
  In high-speed mode ..... 34 mW
  (at 8 MHz oscillation frequency, at 5 V power source voltage)
  In low-speed mode ..... 60 µW
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... –20 to 85°C

APPLICATION

Office automation equipment, FA equipment, Household products, Consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : FP ..... 42P2R-A (42-pin plastic-molded SSOP)
Package type : SP ..... 42P4B (42-pin shrink plastic-molded DIP)

Fig. 1 M38503M4-XXXFP/SP pin configuration

FUNCTIONAL BLOCK

FUNCTIONAL BLOCK DIAGRAM

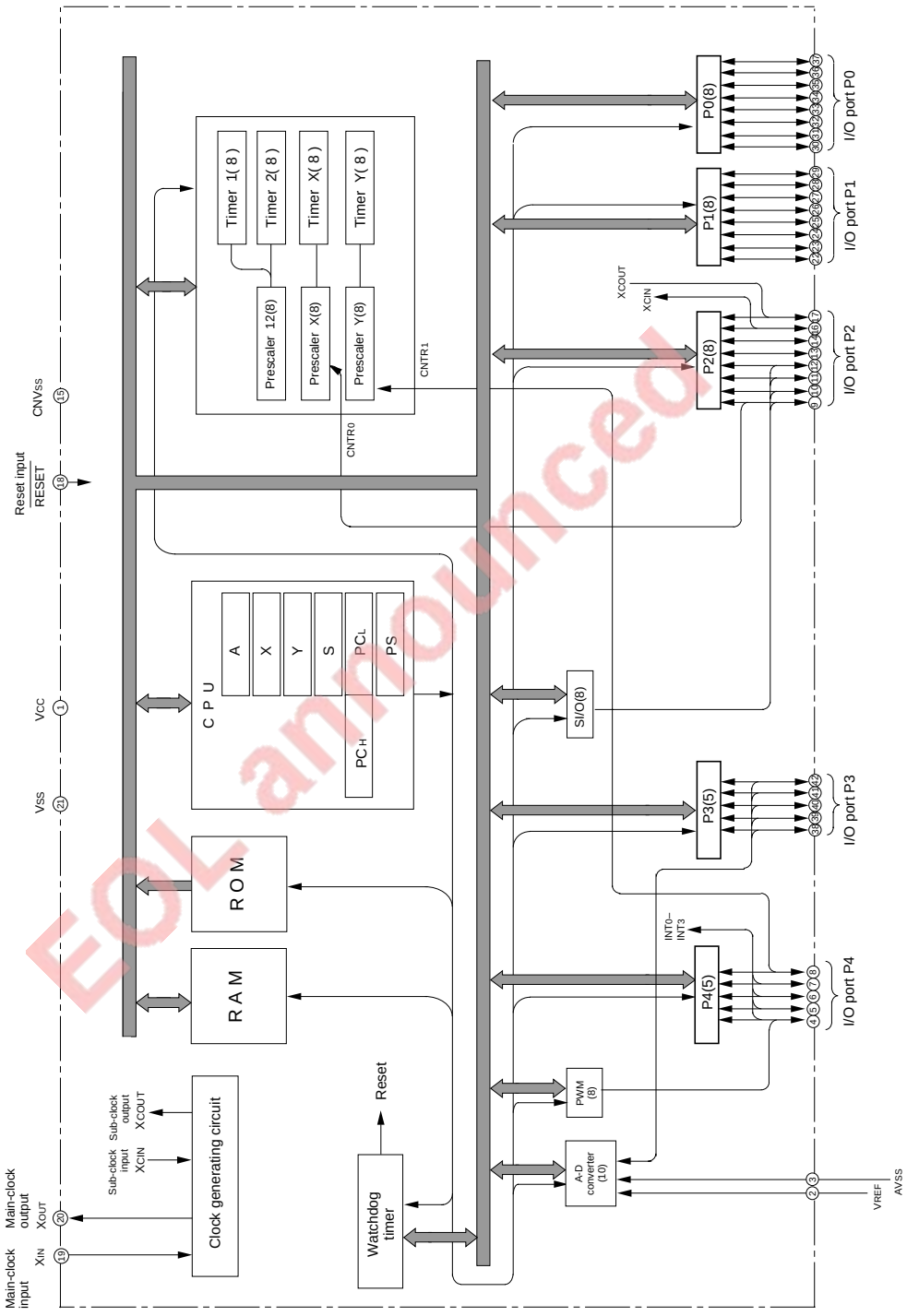


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Functions	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss.	
CNV$_{SS}$	CNV$_{SS}$ input	•This pin controls the operation mode of the chip. •Normally connected to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active "L."	
X_{IN}	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
P0$_0$–P0$_7$	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •P1$_3$ to P1$_7$ (5 bits) are enabled to output large current for LED drive.	
P1$_0$–P1$_7$	I/O port P1		
P2$_0$/X$_{COUT}$ P2$_1$/X$_{CIN}$	I/O port P2	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •P2$_0$, P2$_1$, P2$_4$ to P2$_7$: CMOS3-state output structure. •P2$_2$, P2$_3$: N-channel open-drain structure.	• Sub-clock generating circuit I/O pins (connect a resonator)
P2$_2$ P2$_3$			
P2$_4$/RxD P2$_5$/TxD			• Serial I/O function pin
P2$_6$/S$_{CLK}$			
P2$_7$/CNTR$_0$/ $\overline{S_{RDY}}$			• Serial I/O function pin/ Timer X function pin
P3$_0$/AN$_0$– P3$_4$/AN$_4$	I/O port P3	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• A-D converter input pin
P4$_0$/CNTR$_1$	I/O port P4	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• Timer Y function pin
P4$_1$/INT$_0$– P4$_3$/INT$_2$			• Interrupt input pins
P4$_4$/INT$_3$/PWM			• Interrupt input pin • PWM output pin

PART NUMBERING

Product M3850 **3 M 4 XXX FP**

Package type
FP : 42P2R-A package
SP : 42P4B package
SS : 42S1B-A package

ROM number
Omitted in some types.

ROM/PROM size

1 : 4096 bytes	9 : 36864 bytes
2 : 8192 bytes	A : 40960 bytes
3 : 12288 bytes	B : 45056 bytes
4 : 16384 bytes	C : 49152 bytes
5 : 20480 bytes	D : 53248 bytes
6 : 24576 bytes	E : 57344 bytes
7 : 28672 bytes	F : 61440 bytes
8 : 32768 bytes	

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used.

Memory type
M : Mask ROM version
E : EPROM or One Time PROM version

RAM size
0 : 192 bytes
1 : 256 bytes
2 : 384 bytes
3 : 512 bytes
4 : 640 bytes
5 : 768 bytes
6 : 896 bytes
7 : 1024 bytes
8 : 1536 bytes
9 : 2048 bytes

Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 3850 group as follows:

Memory Type

Support for mask ROM, One Time PROM, and EPROM versions.

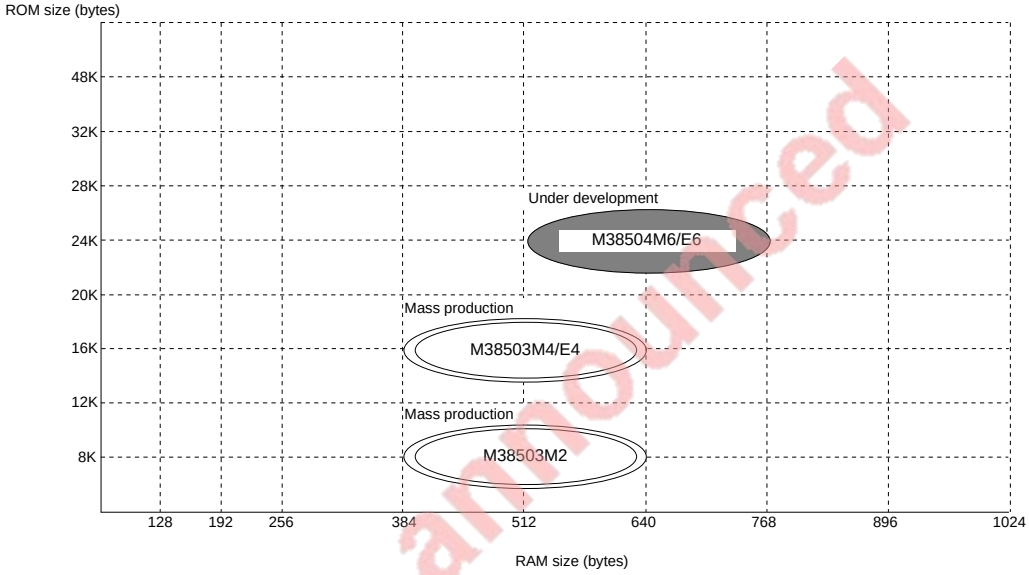
Memory Size

ROM/PROM size ..... 8K to 24K bytes
RAM size ..... 512 to 640 bytes

Packages

42P4B.....42-pin shrink plastic molded DIP
42P2R-A ..... 42-pin plastic molded SSOP
42S1B-A ..... 42-pin shrink ceramic DIP(EPROM version)

Memory Expansion Plan



Products under development or planning : the development schedule and specification may be revised without notice.
Planning products may be stopped the development.

Fig. 4 Memory expansion plan

Currently planning products are listed below.

As of August 1998

Table 2 Support products

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38503M2-XXXSP	8192 (8062)	512	42P4B	Mask ROM version
M38503M2-XXXFP			42P2R-A	Mask ROM version
M38503M4-XXXSP	16384 (16254)	512	42P4B	Mask ROM version
M38503E4-XXXSP				One Time PROM version
M38503E4SP				One Time PROM version (blank)
M38503E4SS			42S1B-A	EPROM version (stock only replaced by M38504E6SS)
M38503M4-XXXFP			42P2R-A	Mask ROM version
M38503E4-XXXFP				One Time PROM version
M38503E4FP				One Time PROM version (blank)
M38504M6-XXXSP	32768 (32638)	640	42P4B	Mask ROM version
M38504E6-XXXSP				One Time PROM version
M38504E6SP				One Time PROM version (blank)
M38504E6SS			42S1B-A	EPROM version
M38504M6-XXXFP			42P2R-A	Mask ROM version
M38504E6-XXXFP				One Time PROM version
M38504E6FP				One Time PROM version (blank)

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3850 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc.

The CPU mode register is allocated at address 003B16.

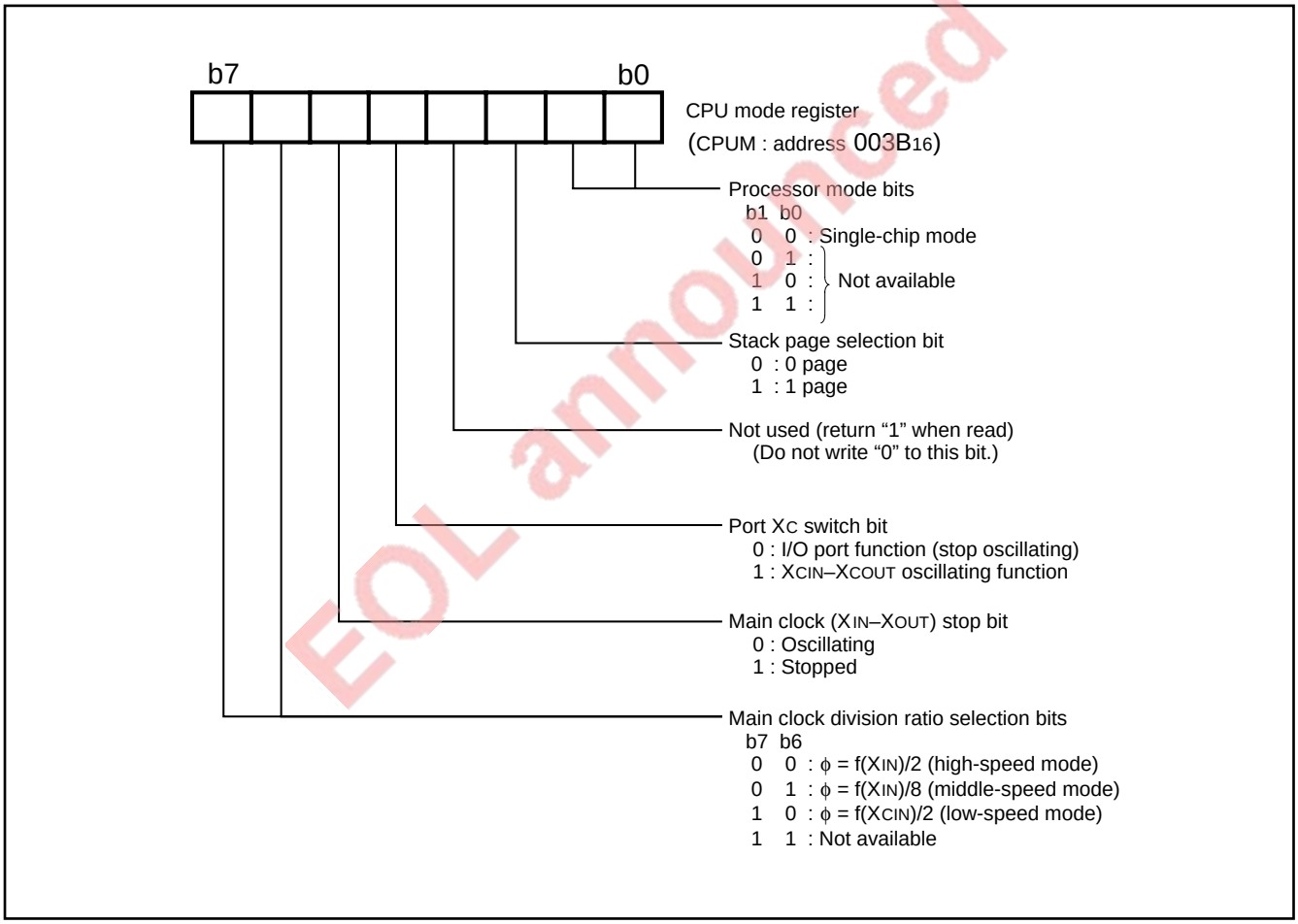


Fig. 5 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address XXXX16
192	00FF16
256	013F16
384	01BF16
512	023F16
640	02BF16
768	033F16
896	03BF16
1024	043F16
1536	063F16
2048	083F16
3072	0C3F16
4032	0FFF16

ROM area

ROM size (bytes)	Address YYYY16	Address ZZZZ16
4096	F00016	F08016
8192	E00016	E08016
12288	D00016	D08016
16384	C00016	C08016
20480	B00016	B08016
24576	A00016	A08016
28672	900016	908016
32768	800016	808016
36864	700016	708016
40960	600016	608016
45056	500016	508016
49152	400016	408016
53248	300016	308016
57344	200016	208016
61440	100016	108016

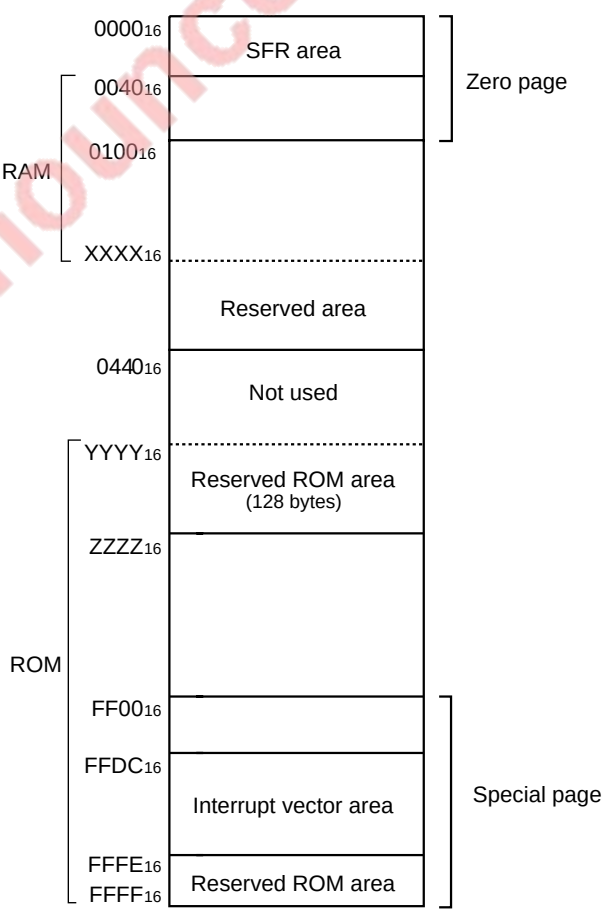


Fig. 6 Memory map diagram

0000₁₆	Port P0 (P0)
0001₁₆	Port P0 direction register (P0D)
0002₁₆	Port P1 (P1)
0003₁₆	Port P1 direction register (P1D)
0004₁₆	Port P2 (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 (P3)
0007₁₆	Port P3 direction register (P3D)
0008₁₆	Port P4 (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	
000B₁₆	
000C₁₆	
000D₁₆	
000E₁₆	
000F₁₆	
0010₁₆	
0011₁₆	
0012₁₆	
0013₁₆	
0014₁₆	
0015₁₆	Reserved ✻
0016₁₆	Reserved ✻
0017₁₆	Reserved ✻
0018₁₆	Transmit/Receive buffer register (TB/RB)
0019₁₆	Serial I/O status register (SIOSTS)
001A₁₆	Serial I/O control register (SIOCON)
001B₁₆	UART control register (UARTCON)
001C₁₆	Baud rate generator (BRG)
001D₁₆	PWM control register (PWMCON)
001E₁₆	PWM prescaler (PREPWM)
001F₁₆	PWM register (PWM)

0020₁₆	Prescaler 12 (PRE12)
0021₁₆	Timer 1 (T1)
0022₁₆	Timer 2 (T2)
0023₁₆	Timer XY mode register (TM)
0024₁₆	Prescaler X (PREX)
0025₁₆	Timer X (TX)
0026₁₆	Prescaler Y (PREY)
0027₁₆	Timer Y (TY)
0028₁₆	Timer count source selection register (TCSS)
0029₁₆	
002A₁₆	
002B₁₆	Reserved ✻
002C₁₆	Reserved ✻
002D₁₆	Reserved ✻
002E₁₆	Reserved ✻
002F₁₆	Reserved ✻
0030₁₆	Reserved ✻
0031₁₆	
0032₁₆	
0033₁₆	
0034₁₆	A-D control register (ADCON)
0035₁₆	A-D conversion low-order register (ADL)
0036₁₆	A-D conversion high-order register (ADH)
0037₁₆	
0038₁₆	MISRG
0039₁₆	Watchdog timer control register (WDTCON)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)

✻ Reserved : Do not write "1" to this address.

Fig. 7 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Table 3 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
$P0_0$–$P0_7$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output			(1)
$P1_0$–$P1_7$	Port P1					
$P2_0/X_{COUT}$ $P2_1/X_{CIN}$	Port P2			Sub-clock generating circuit	CPU mode register	(2) (3)
$P2_2$ $P2_3$			CMOS compatible input level N-channel open-drain output			(4)
$P2_4$/RxD $P2_5$/TxD			CMOS compatible input level CMOS 3-state output	Serial I/O function I/O	Serial I/O control register	(5) (6)
$P2_6/S_{CLK}$				Serial I/O function I/O	Serial I/O control register	(7)
$P2_7$/CNTR$_0$/$\overline{S_{RDY}}$				Serial I/O function I/O Timer X function I/O	Serial I/O control register Timer XY mode register	(8)
$P3_0/AN_0$– $P3_4/AN_4$	Port P3			A-D conversion input	A-D control register	(9)
$P4_0$/CNTR$_1$	Port P4			Timer Y function I/O	Timer XY mode register	(10)
$P4_1/INT_0$– $P4_3/INT_2$				External interrupt input	Interrupt edge selection register	(11)
$P4_4/INT_3$/PWM				External interrupt input PWM output	Interrupt edge selection register PWM control register	(12)

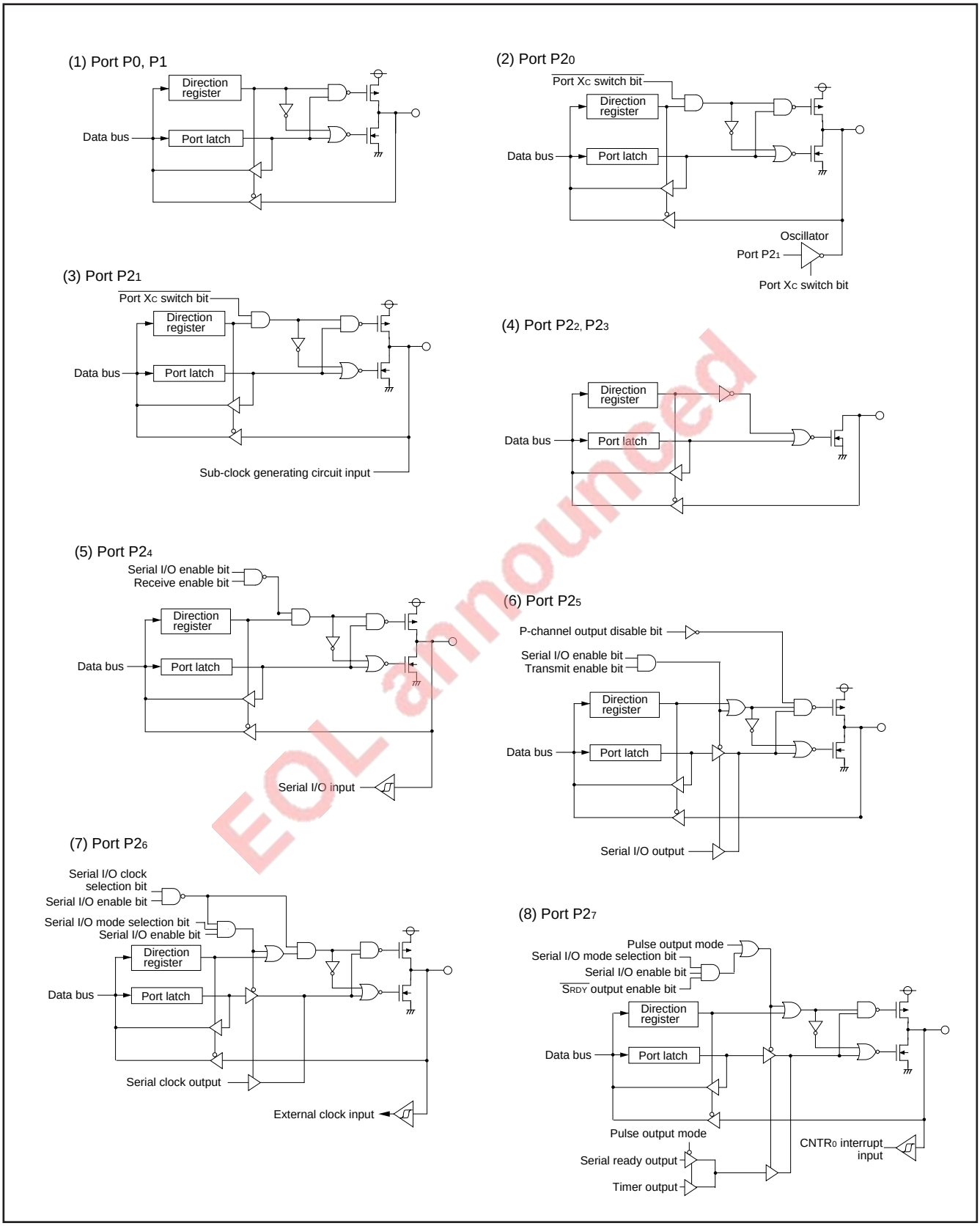


Fig. 8 Port block diagram (1)

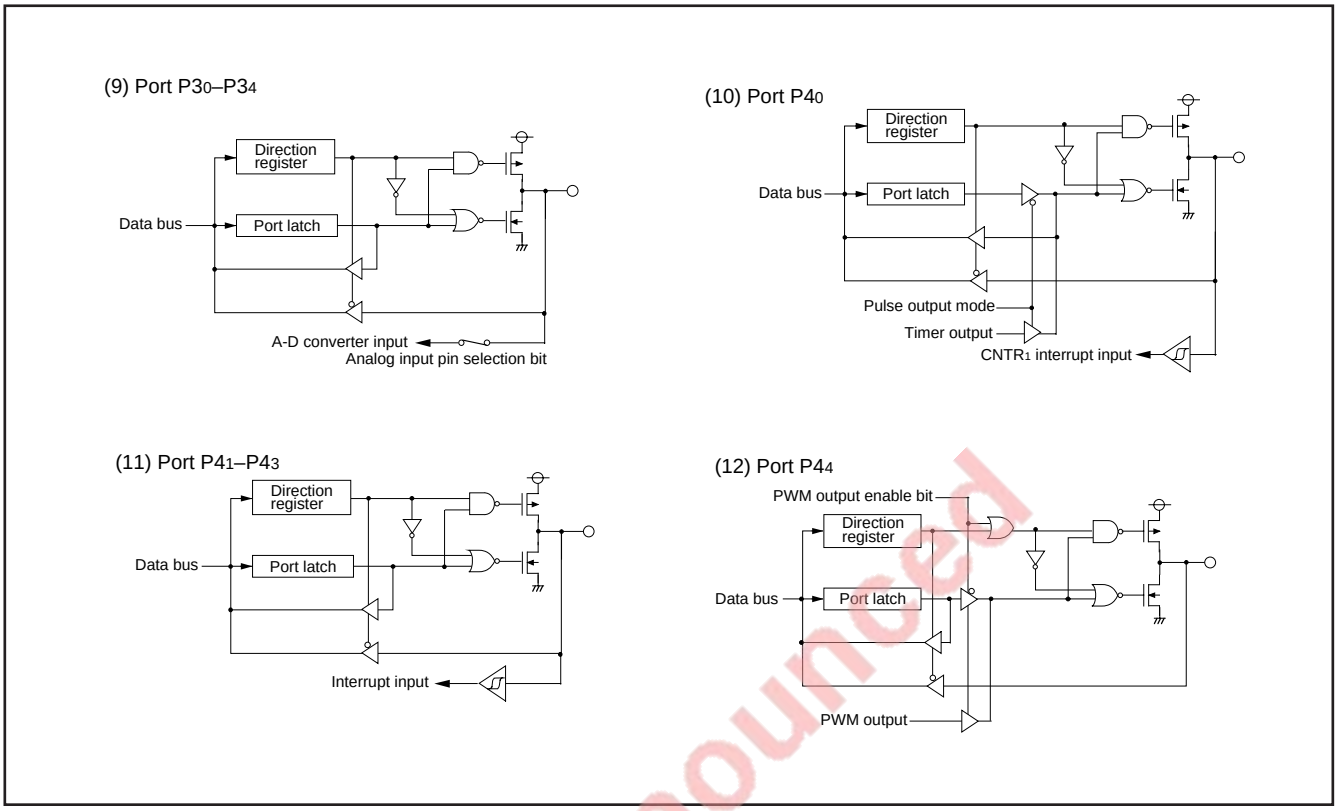


Fig. 9 Port block diagram (2)

INTERRUPTS

Interrupts occur by 14 sources among 14 sources: six external, seven internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes

When the active edge of an external interrupt (INT_0–INT_3, $CNTR_0$, $CNTR_1$) is set, the corresponding interrupt request bit may also be set. Therefore, take the following sequence:

1. Disable the interrupt
2. Change the interrupt edge selection register
   (the timer XY mode register for $CNTR_0$ and $CNTR_1$)
3. Clear the interrupt request bit to "0"
4. Accept the interrupt.

Table 4 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
Reserved	3	FFF916	FFF816	Reserved	
INT1	4	FFF716	FFF616	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
INT2	5	FFF516	FFF416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
INT3	6	FFF316	FFF216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
Reserved	7	FFF116	FFF016	Reserved	
Timer X	8	FFEF16	FFEE16	At timer X underflow	
Timer Y	9	FFED16	FFEC16	At timer Y underflow	
Timer 1	10	FFEB16	FFEA16	At timer 1 underflow	STP release timer underflow
Timer 2	11	FFE916	FFE816	At timer 2 underflow	
Serial I/O reception	12	FFE716	FFE616	At completion of serial I/O data reception	Valid when serial I/O is selected
Serial I/O Transmission	13	FFE516	FFE416	At completion of serial I/O transfer shift or when transmission buffer is empty	Valid when serial I/O is selected
CNTR0	14	FFE316	FFE216	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	15	FFE116	FFE016	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
A-D converter	16	FFDF16	FFDE16	At completion of A-D conversion	
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

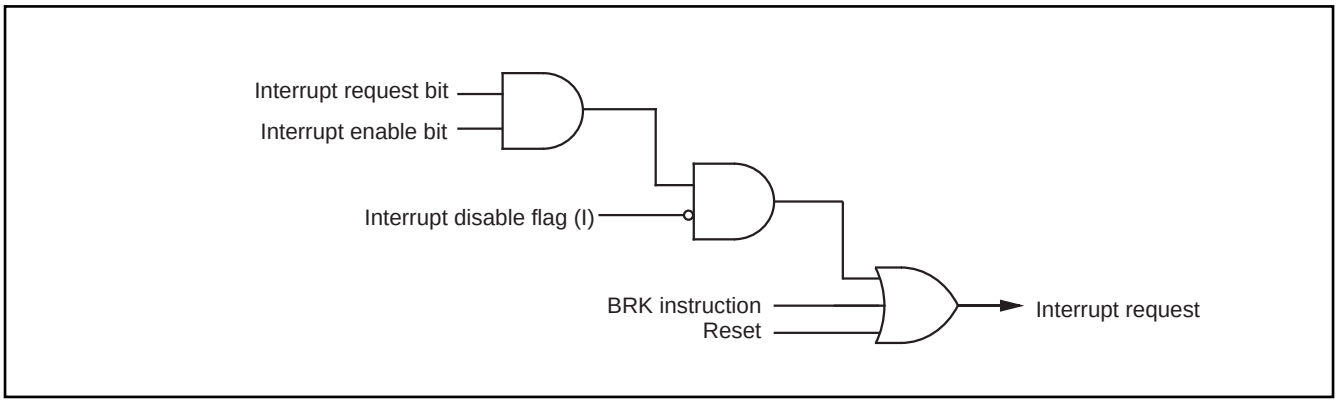


Fig. 10 Interrupt control

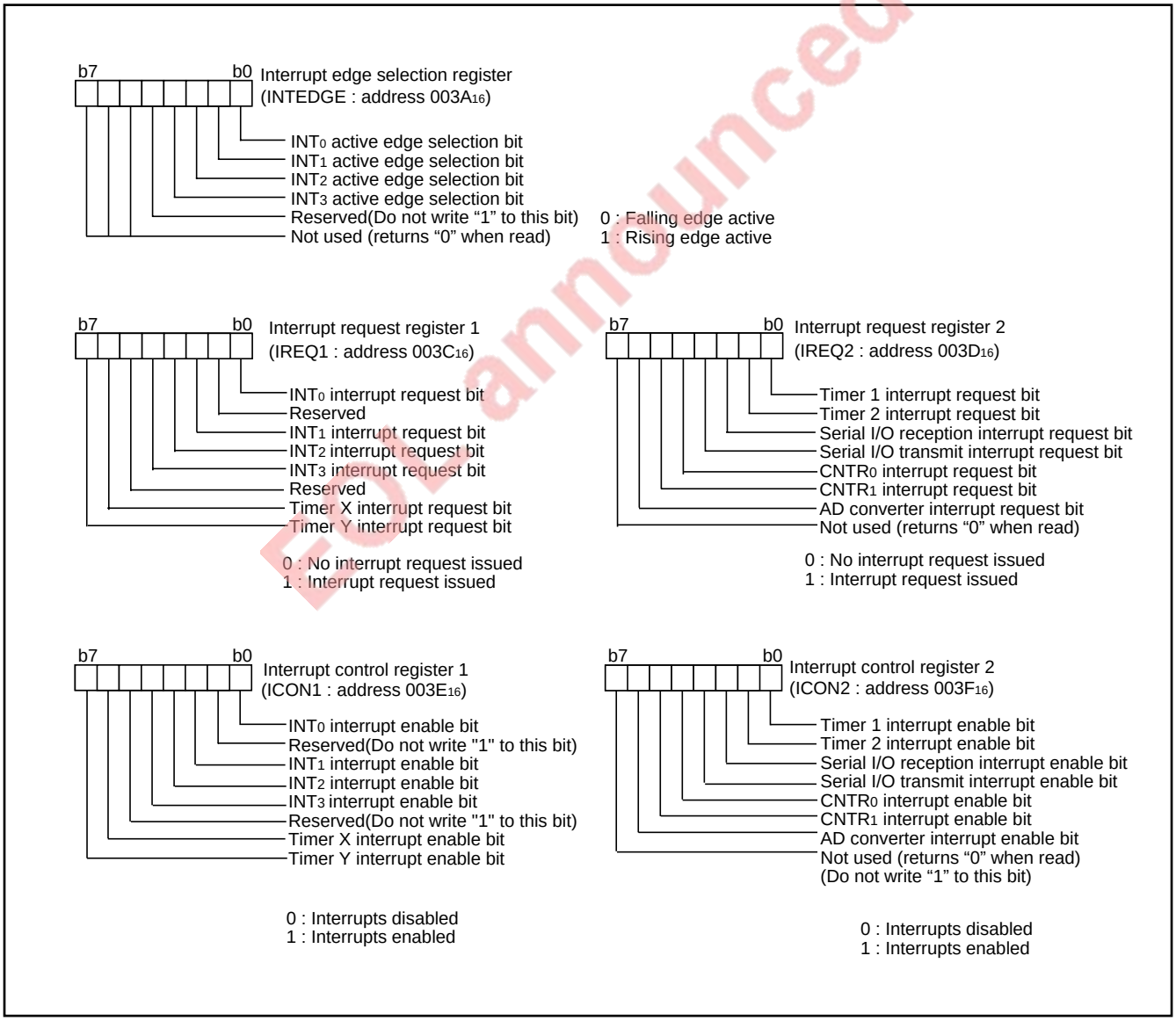


Fig. 11 Structure of interrupt-related registers (1)

TIMERS

The 3850 group has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are count down. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

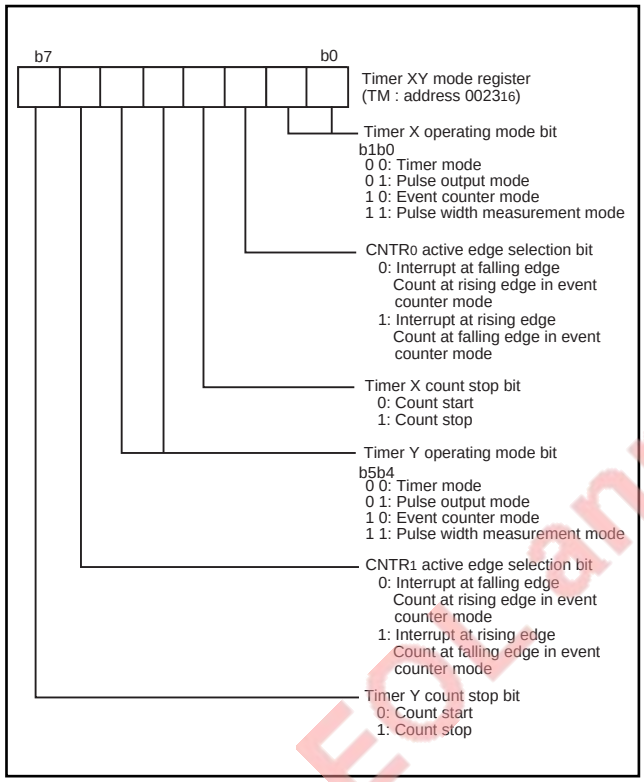


Fig. 12 Structure of timer XY mode register

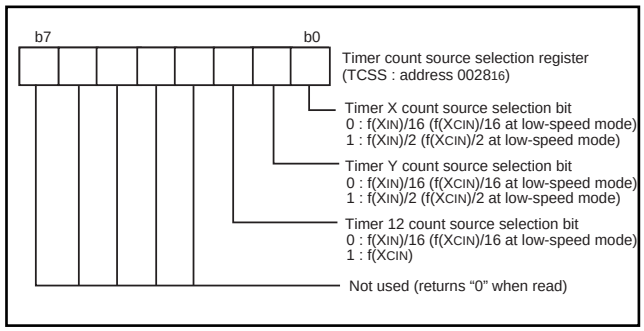


Fig. 13 Structure of timer count source selection register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency which is selected by timer 12 count source selection bit. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each select in one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts the count source selected by Timer count source selection bit.

(2) Pulse Output Mode

The timer counts the count source selected by Timer count source selection bit. Whenever the contents of the timer reach "00_{16}", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", output begins at " H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P2_7$ (or port $P4_0$) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the rising edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the falling edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

(4) Pulse Width Measurement Mode

If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the timer counts the selected signals by the count source selection bit while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the timer counts it while the $CNTR_0$ (or $CNTR_1$) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer underflows.

■Note

When switching the count source by the timer 12, X and Y count source bit, the value of timer count is altered in unconsiderable amount owing to generating of a thin pulses in the count input signals.

Therefore, select the timer count source before set the value to the prescaler and the timer.

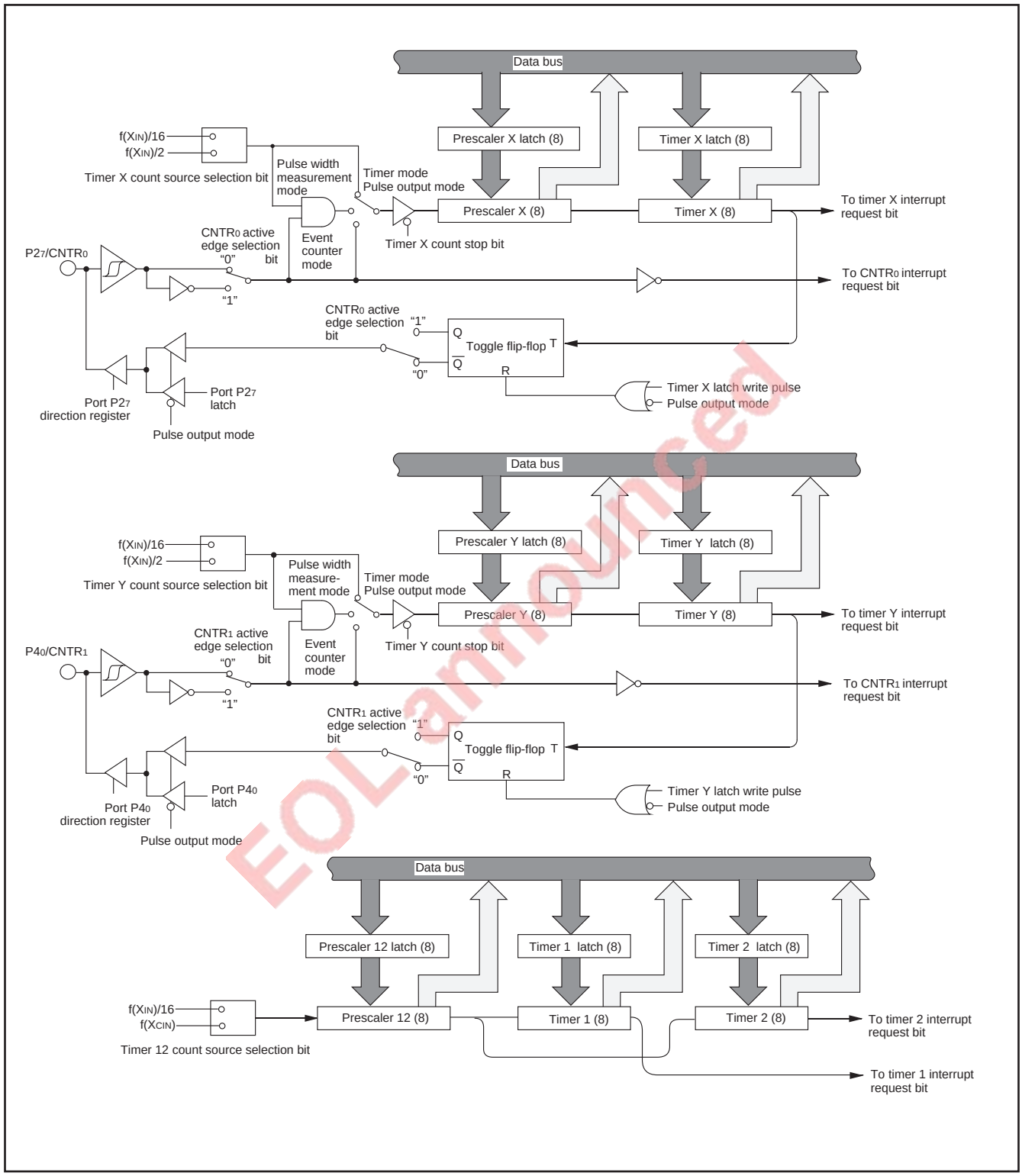


Fig. 14 Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register (bit 6 of address 001A16) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

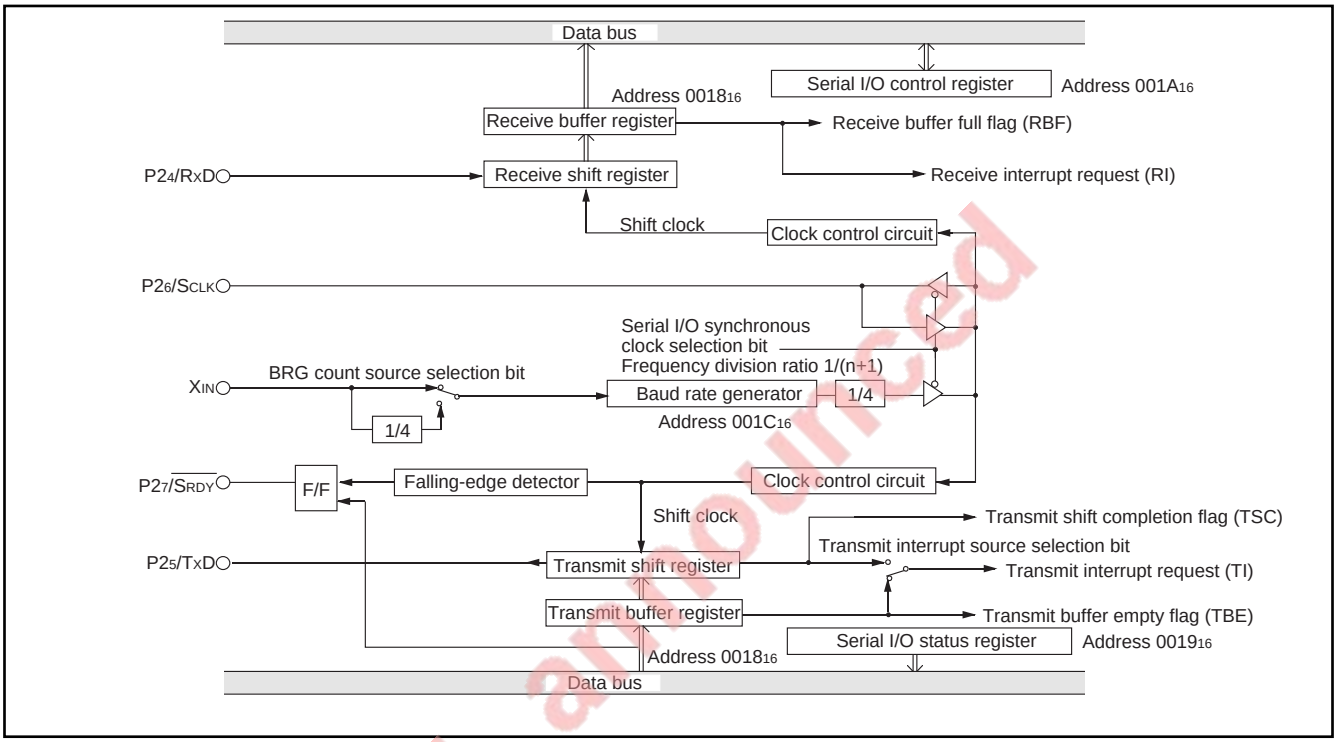
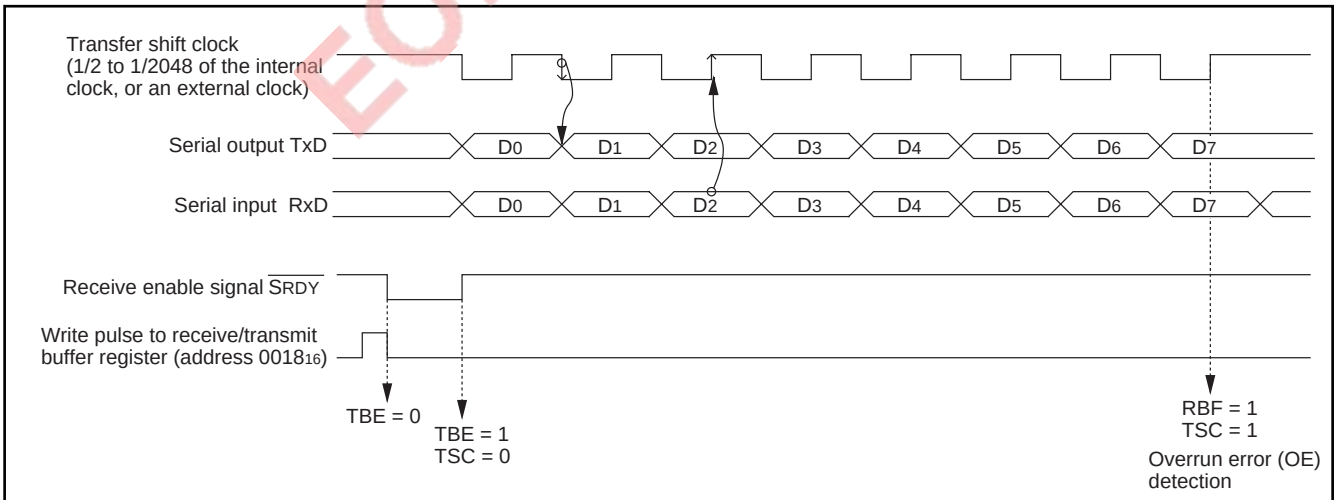


Fig. 15 Block diagram of clock synchronous serial I/O



Notes 1: As the transmit interrupt (TI), either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.
2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 16 Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit (b6) of the serial I/O control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

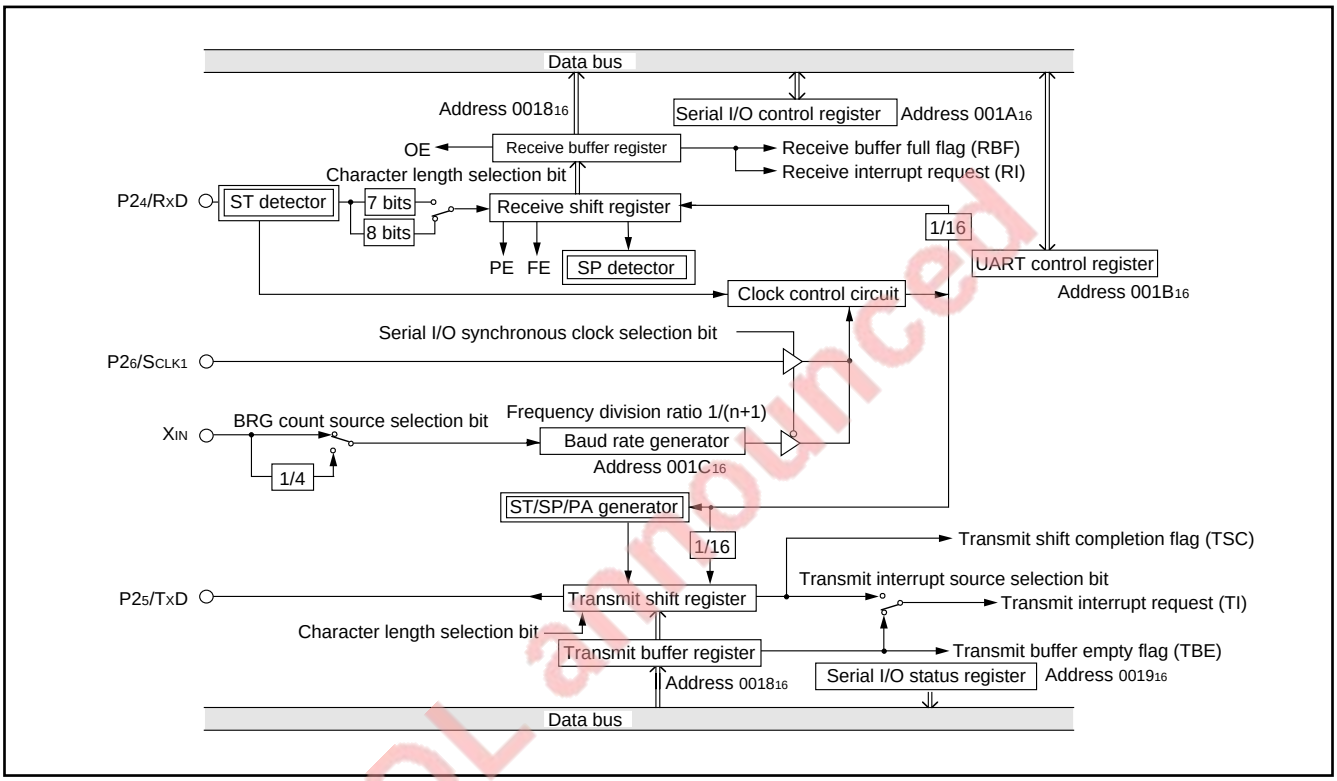
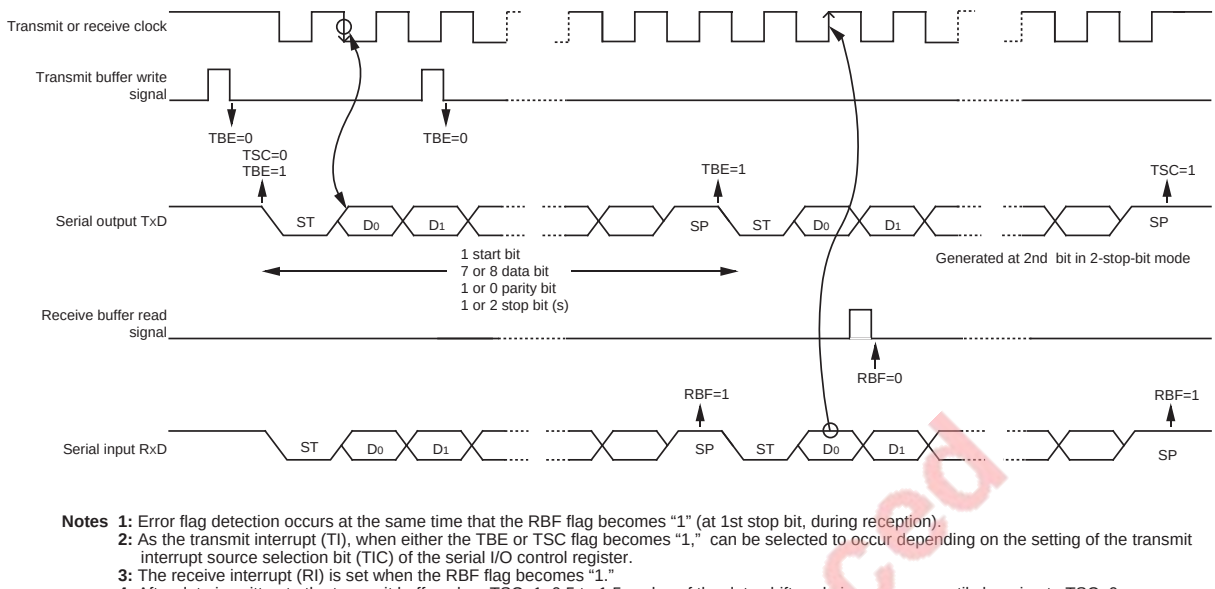


Fig.17 Block diagram of UART serial I/O



Notes **1:** Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1," can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1."
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 18 Operation of UART serial I/O function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

Serial I/O Control Register (SIOCON)] 001A$_{16}$

The serial I/O control register consists of eight control bits for the serial I/O function.

[UART Control Register (UARTCON)] 001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P25/TxD pin.

[Baud Rate Generator (BRG)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

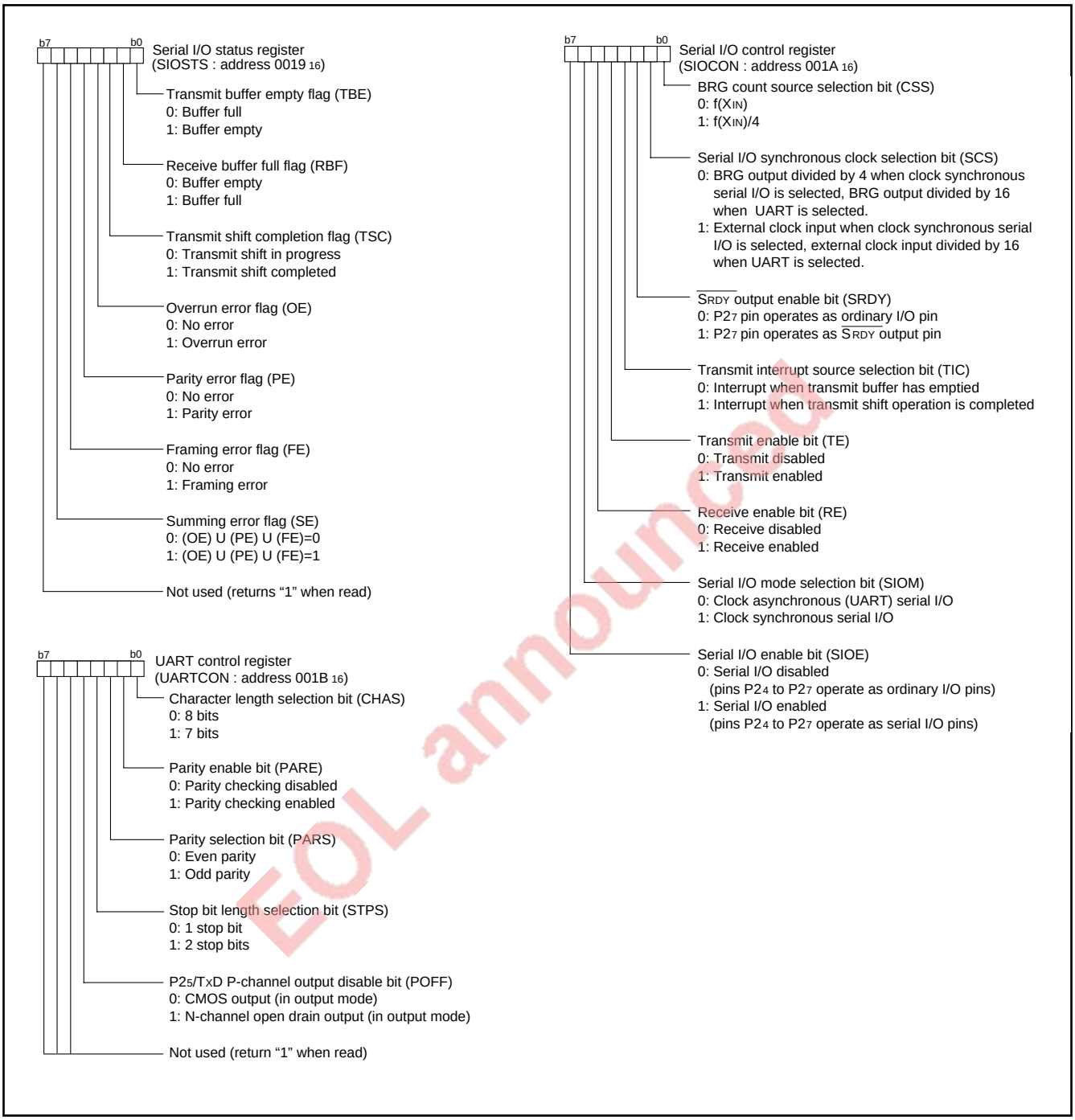


Fig. 19 Structure of serial I/O control registers

PULSE WIDTH MODULATION (PWM)

The 3850 group has a PWM function with an 8-bit resolution, based on a signal that is the clock input XIN or that clock input divided by 2.

Data Setting

The PWM output pin also functions as port P44. Set the PWM period by the PWM prescaler, and set the "H" term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

PWM period = 255 × (n+1) / f(XIN)

= 31.875 × (n+1) µs (when f(XIN) = 8 MHz)

Output pulse "H" term = PWM period × m / 255

= 0.125 × (n+1) × m µs

(when f(XIN) = 8 MHz)

PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

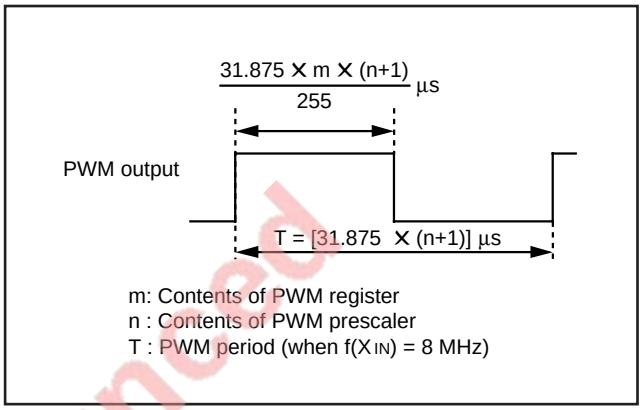


Fig. 20 Timing of PWM period

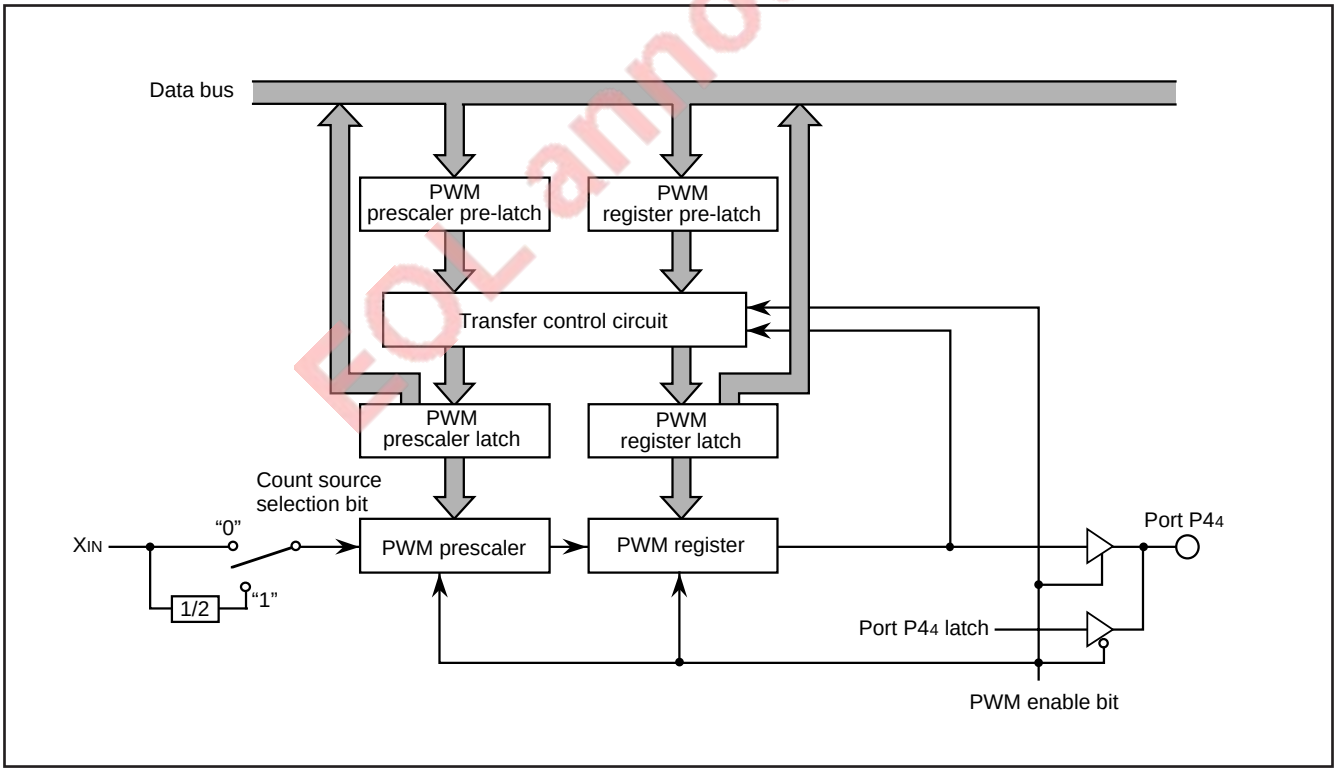


Fig. 21 Block diagram of PWM function

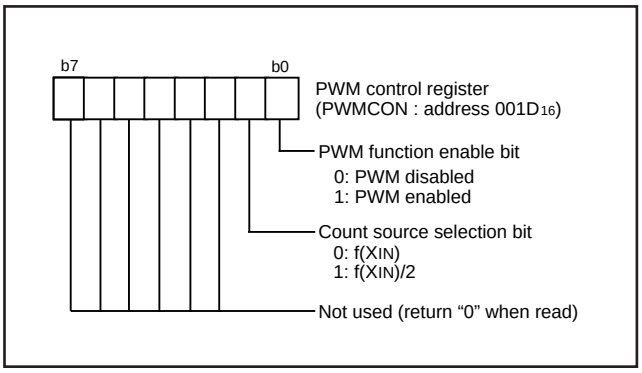


Fig. 22 Structure of PWM control register

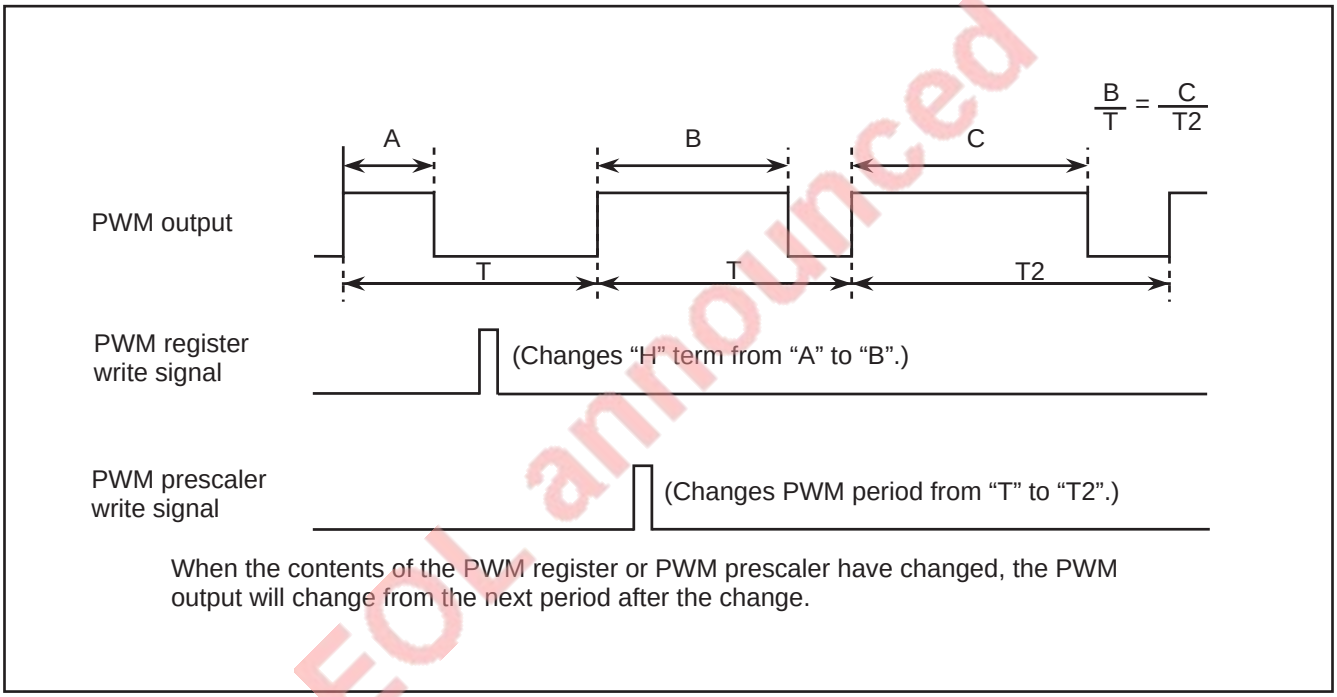


Fig. 23 PWM output timing when PWM register or PWM prescaler is changed

■Note

The PWM starts after the PWM enable bit is set to enable and "L" level is output from the PWM pin.
The length of this "L" level output is as follows:

$\frac{n+1}{2 \cdot f(X_{IN})}$ sec (Count source selection bit = 0, where n is the value set in the prescaler)

$\frac{n+1}{f(X_{IN})}$ sec (Count source selection bit = 1, where n is the value set in the prescaler)

A-D CONVERTER

[A-D Conversion Registers (ADL, ADH)] 003516, 003616

The A-D conversion registers are read-only registers that store the result of an A-D conversion. Do not read these registers during an A-D conversion

[AD Control Register (ADCON)] 003416

The AD control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 4 indicates the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF into 1024 and outputs the divided voltages.

Channel Selector

The channel selector selects one of ports P30/AN0 to P34/AN4 and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage, and the result is stored in the A-D conversion registers. When an A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A-D conversion.

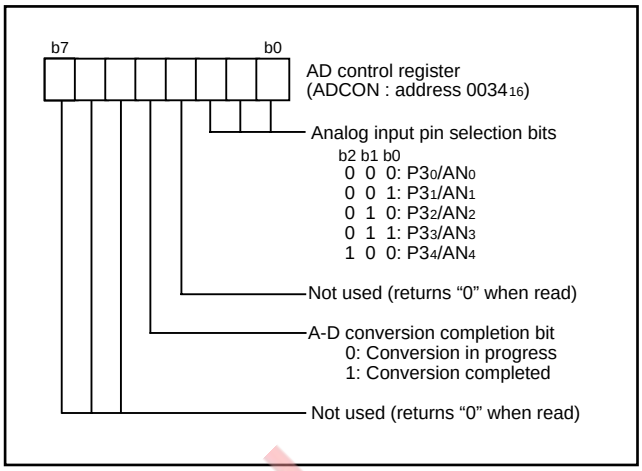


Fig. 24 Structure of AD control register

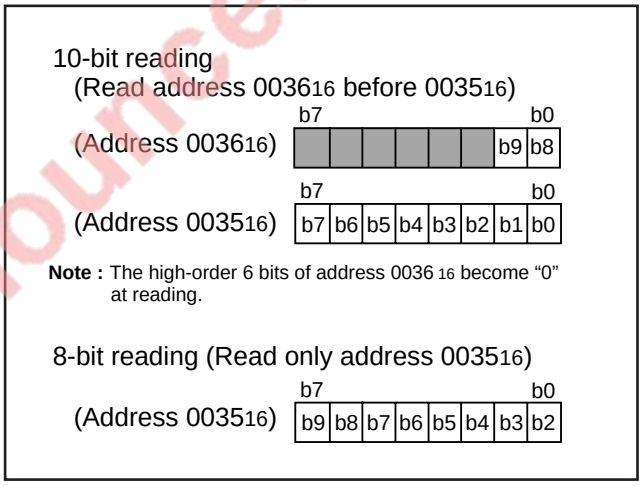


Fig. 25 Structure of A-D conversion registers

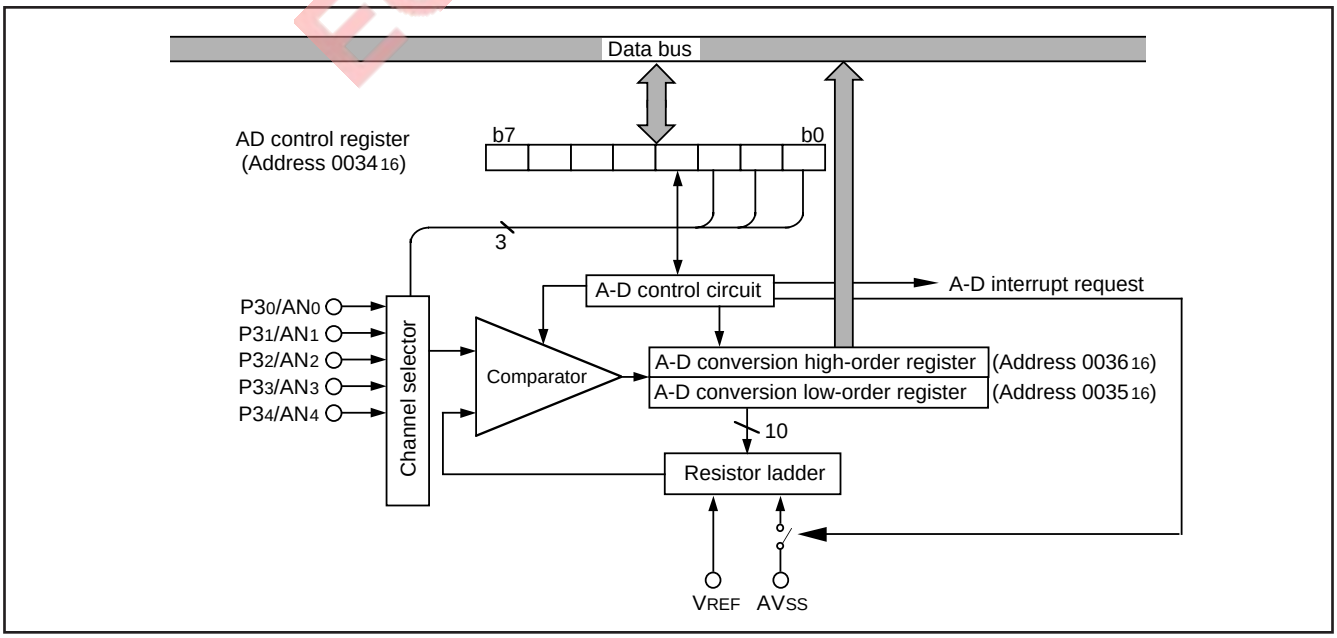


Fig. 26 Block diagram of A-D converter

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Standard Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (address 0039_{16}) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 0039_{16}) and an internal reset occurs at an underflow of the watchdog timer H.

Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0039_{16}) may be started before an underflow. When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

●Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 0039_{16}), each watchdog timer H and L is set to "FF_{16}."

●Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 0039_{16}) permits selecting a watchdog timer H count source. When this bit is set to "0", the count source becomes the underflow signal of watchdog timer L. The detection time is set to 131.072 ms at f(XIN) = 8 MHz frequency and 32.768 s at f(XCIN) = 32 kHz frequency.

When this bit is set to "1", the count source becomes the signal divided by 16 for f(XIN) (or f(XCIN)). The detection time in this case is set to 512 µs at f(XIN) = 8 MHz frequency and 128 ms at f(XCIN) = 32 kHz frequency. This bit is cleared to "0" after resetting.

●Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 0039_{16}) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, once the STP instruction is executed, an internal reset occurs. When this bit is set to "1", it cannot be rewritten to "0" by program. This bit is cleared to "0" after resetting.

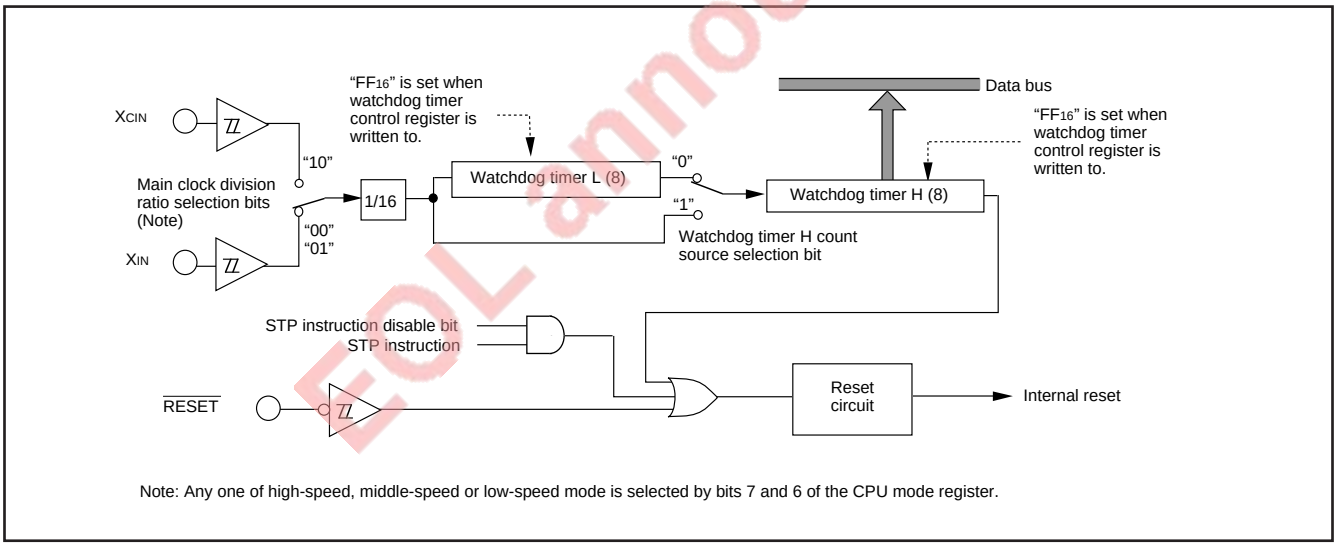


Fig. 27 Block diagram of Watchdog timer

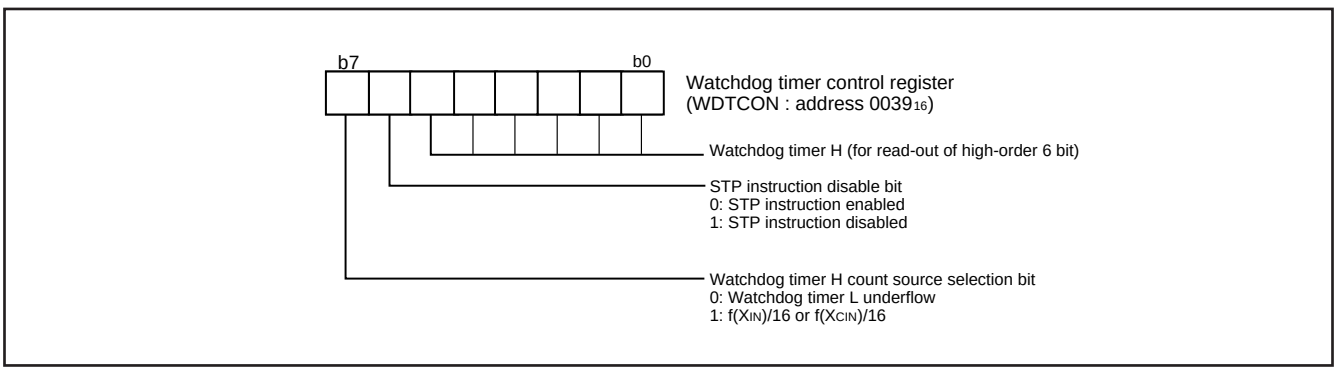


Fig. 28 Structure of Watchdog timer control register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin must be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage must be between 2.7 V and 5.5 V, and the oscillation must be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage is less than 0.54 V for V_{CC} of 2.7 V.

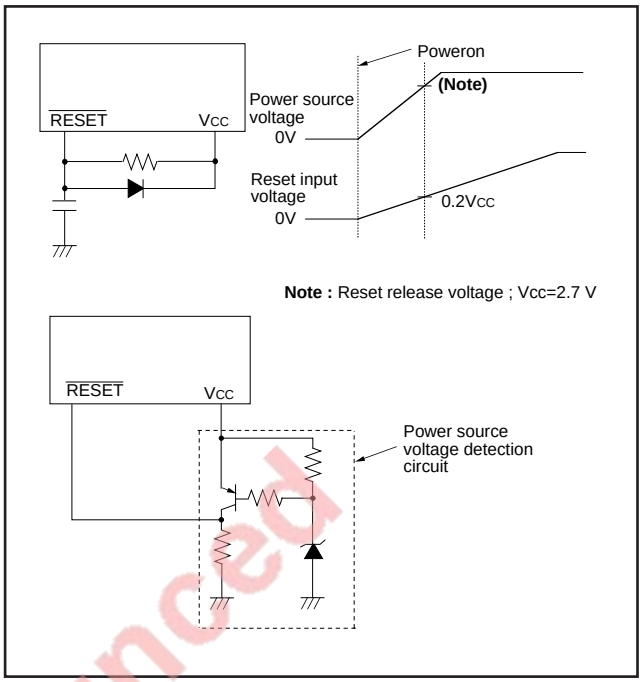


Fig. 29 Reset circuit example

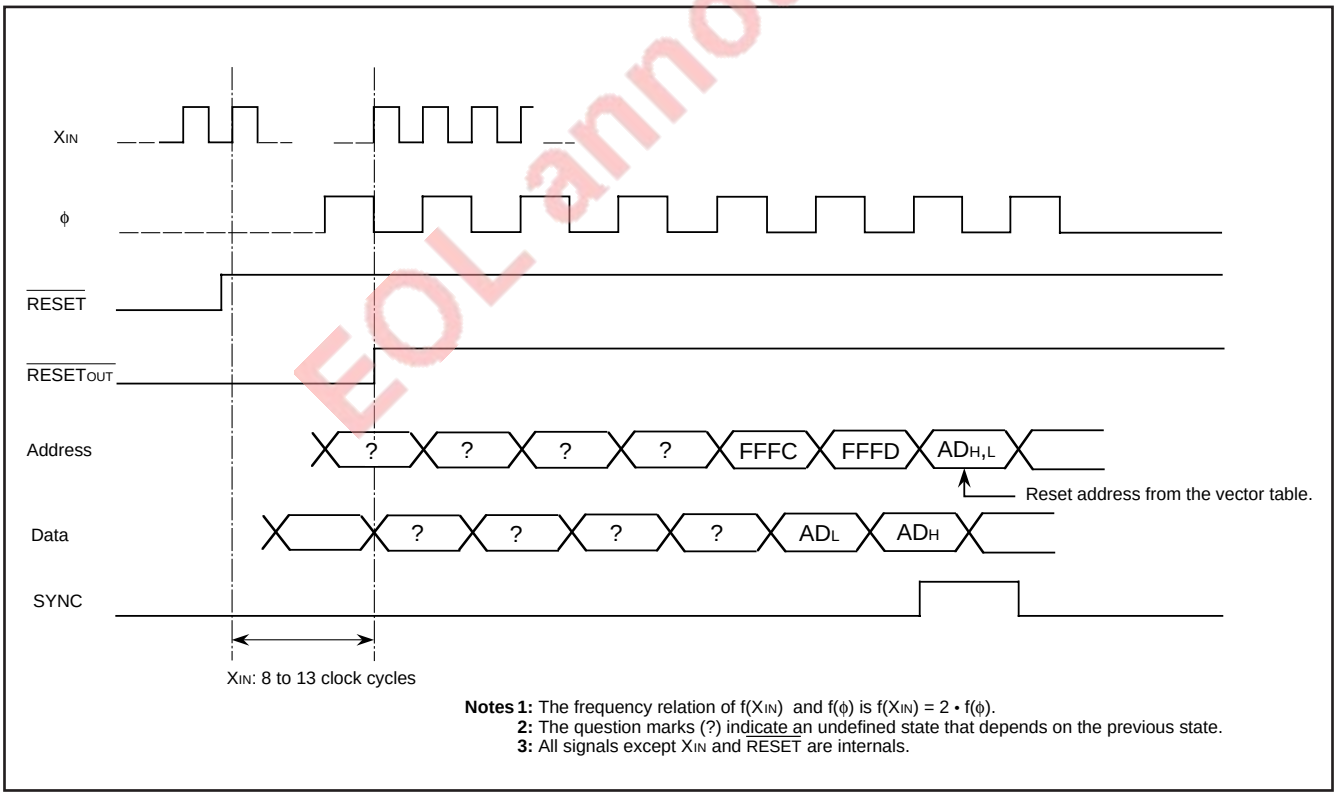


Fig. 30 Reset sequence

		Address	Register contents
(1)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(2)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(3)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(4)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(5)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(6)	Serial I/O status register (SIOSTS)	0019_{16}	1 0 0 0 0 0 0 0
(7)	Serial I/O control register (SIOCON)	$001A_{16}$	00_{16}
(8)	UART control register (UARTCON)	$001B_{16}$	1 1 1 0 0 0 0 0
(9)	PWM control register (PWMCON)	$001D_{16}$	00_{16}
(10)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(11)	Timer 1 (T1)	0021_{16}	01_{16}
(12)	Timer 2 (T2)	0022_{16}	00_{16}
(13)	Timer XY mode register (TM)	0023_{16}	00_{16}
(14)	Prescaler X (PREX)	0024_{16}	FF_{16}
(15)	Timer X (TX)	0025_{16}	FF_{16}
(16)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(17)	Timer Y (TY)	0027_{16}	FF_{16}
(18)	Timer count source select register	0028_{16}	00_{16}
(19)	Reserved	$002C_{16}$	Not fixed
(20)	Reserved	$002D_{16}$	Not fixed
(21)	Reserved	$002E_{16}$	Not fixed
(22)	Reserved	$002F_{16}$	Not fixed
(23)	Reserved	0030_{16}	Not fixed
(24)	AD control register (ADCON)	0034_{16}	0 0 0 1 0 0 0 0
(25)	MISRG	0038_{16}	00_{16}
(26)	Watchdog timer control register (WDTCON)	0039_{16}	0 0 1 1 1 1 1 1
(27)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(28)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(29)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(30)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(31)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(32)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(33)	Processor status register	(PS)	X X X X X 1 X X
(34)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X indicates Not fixed .

Fig. 31 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3850 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power on and at returning from the stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3•f(XCIN).

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1." When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

The sub-clock XCIN-XCOUT oscillating circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

Oscillation Control
(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillation stops. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116." When the oscillation stabilizing time set after STP instruction released bit is "1," set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

Either XIN or XCIN divided by 16 is input to the prescaler 12 as count source. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized. When the oscillator is restarted by reset, apply "L" level to the RESET pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.

When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

■Note

When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.

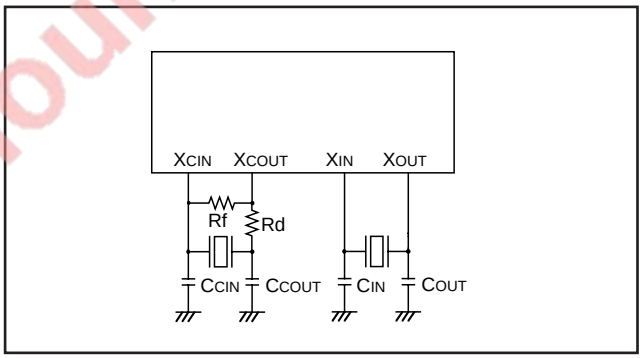


Fig. 32 Ceramic resonator circuit

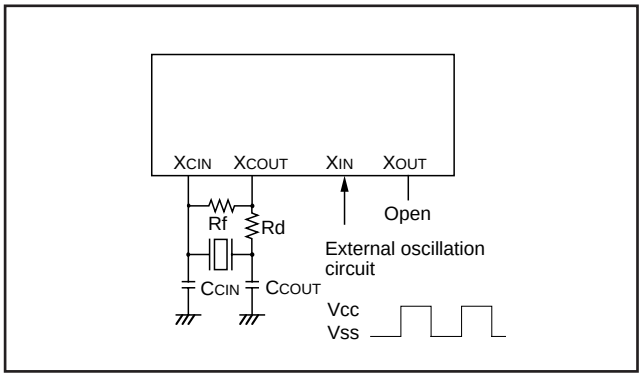


Fig. 33 External clock input circuit

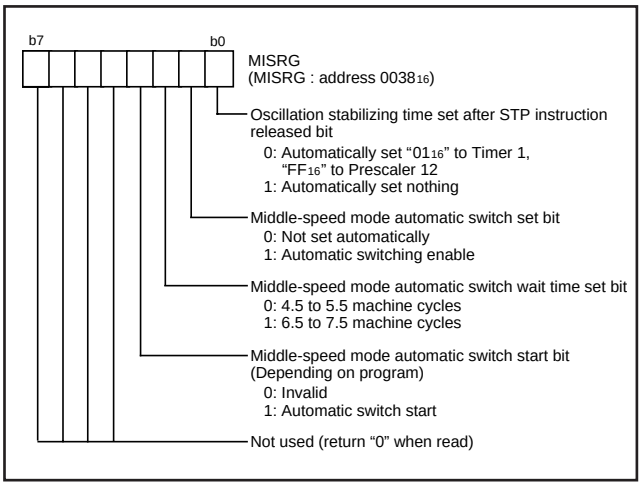
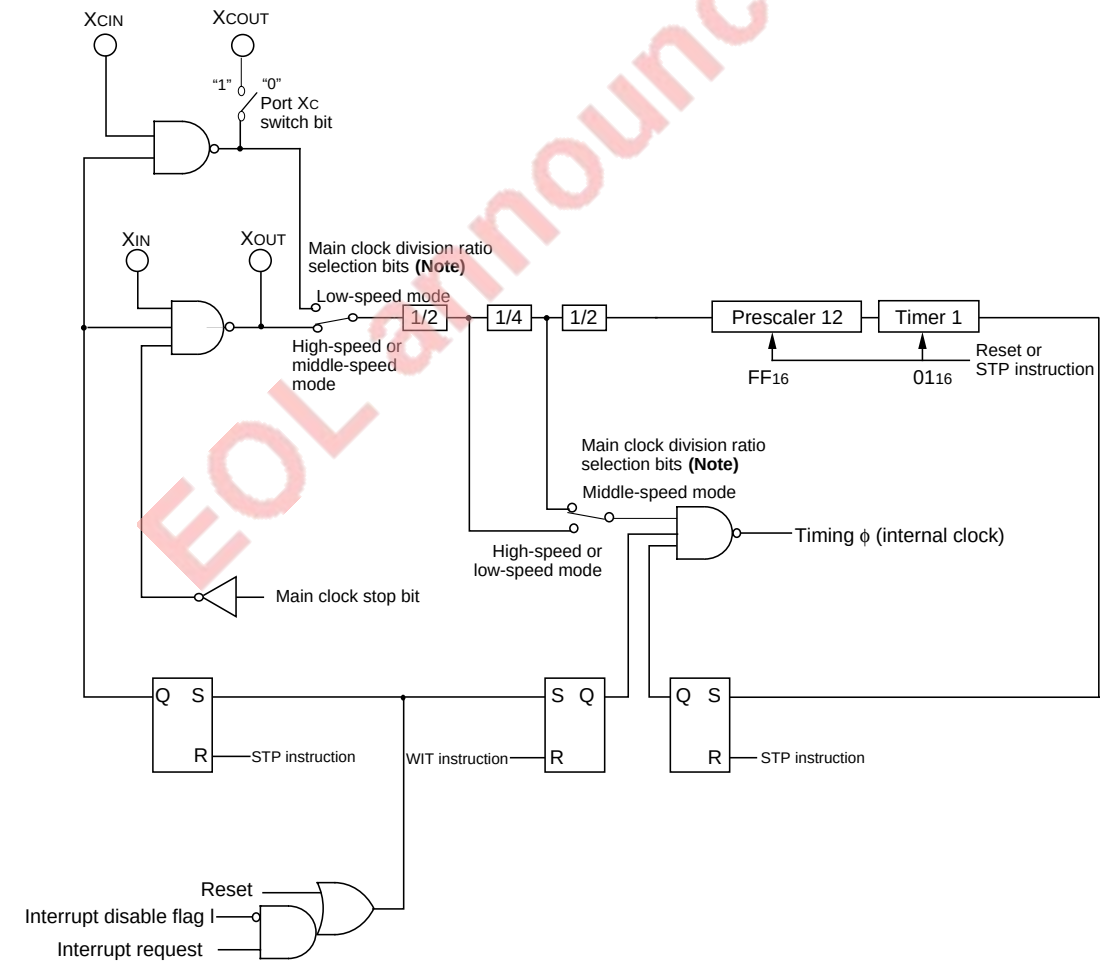


Fig. 34 Structure of MISRG

Middle-speed mode automatic switch set bit

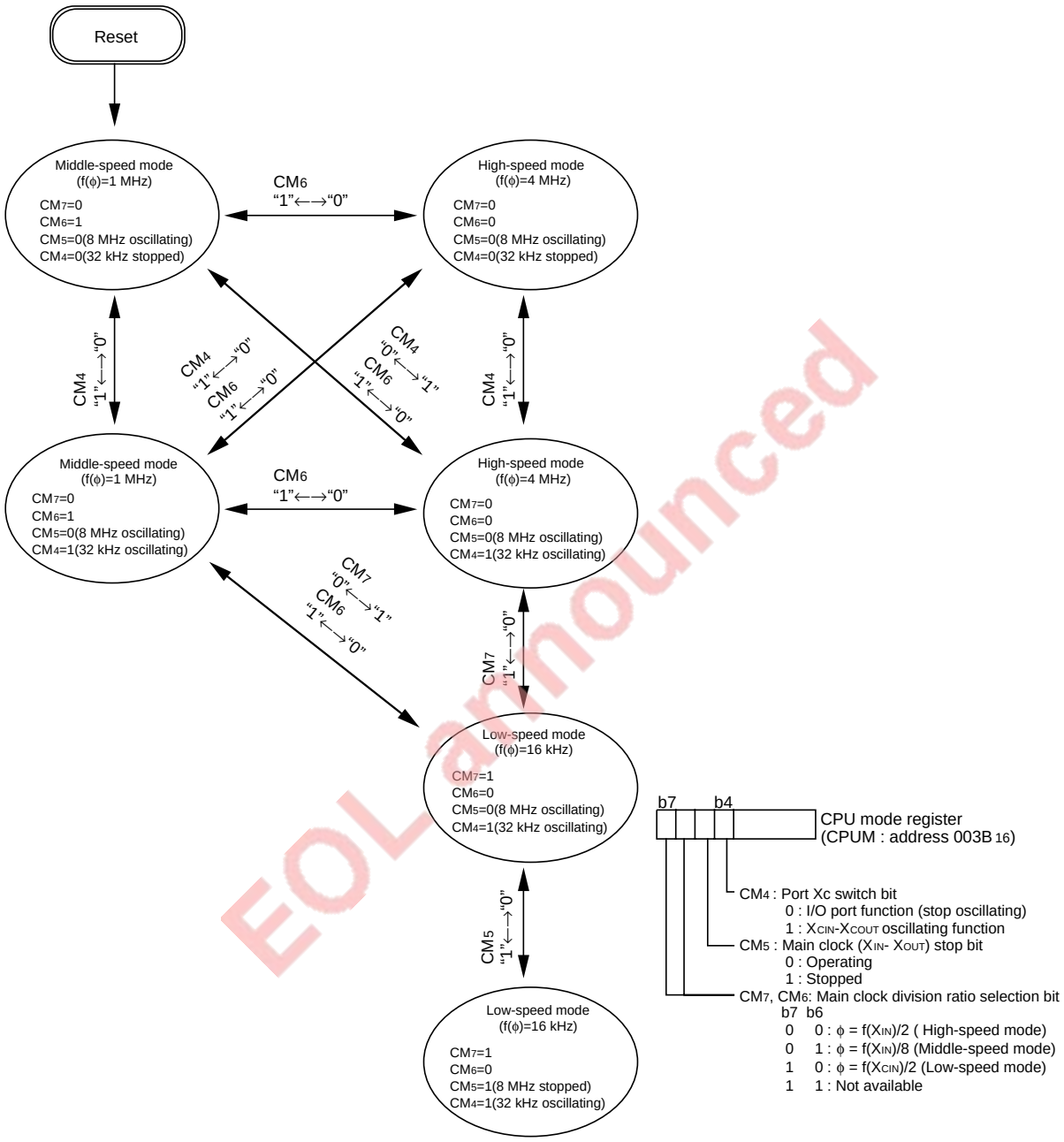
By setting the middle-speed mode automatic switch set bit to "1" while operating in the low-speed mode, XIN oscillation automatically starts and the mode is automatically switched to the middle-speed mode when defecting a rising/falling edge of the SCL or SDA pin. The middle-speed automatic switch wait time set bit can select the switch timing from the low-speed to the middle-speed mode; either 4.5 to 5.5 machine cycles or 6.5 to 7.5 machine cycles in the low-speed mode. Select it according to oscillation start characteristics of used XIN oscillator.

The middle-speed mode automatic switch start bit is used to automatically make to XIN oscillation start and switch to the middle-speed mode by setting this bit to "1" while operating in the low-speed mode.



Note: Any one of high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register. When low-speed mode is selected, set port Xc switch bit (b1) to "1".

Fig. 35 System clock generating circuit block diagram (Single-chip mode)



Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3 : Timer operates in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs by connecting prescaler 12 in middle/high-speed mode.
5 : When the stop mode is ended, a delay of approximately 16 ms occurs by Timer 1 and Timer 2 in low-speed mode.
6 : Wait until oscillation stabilizes after oscillating the main clock X IN before the switching from the low-speed mode to middle/high-speed mode.
7 : The example assumes that 8 MHz is being applied to the X IN pin and 32 kHz to the X CIN pin. ϕ indicates the internal clock.

Fig. 36 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1."

Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

When an external clock is used as synchronous clock in serial I/O, write transmission data to the transmit buffer register while the transfer clock is "H."

A-D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that f(XIN) is at least on 500 kHz during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the XIN frequency in high-speed mode.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

DATA REQUIRED FOR ROM WRITING ORDERS

The following are necessary when ordering a ROM writing:

1. ROM Writing Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 5 Programming adapter

Package	Name of Programming Adapter
42P2R-A	PCA4738F-42A
42P4B	PCA4738S-42A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 49 is recommended to verify programming.

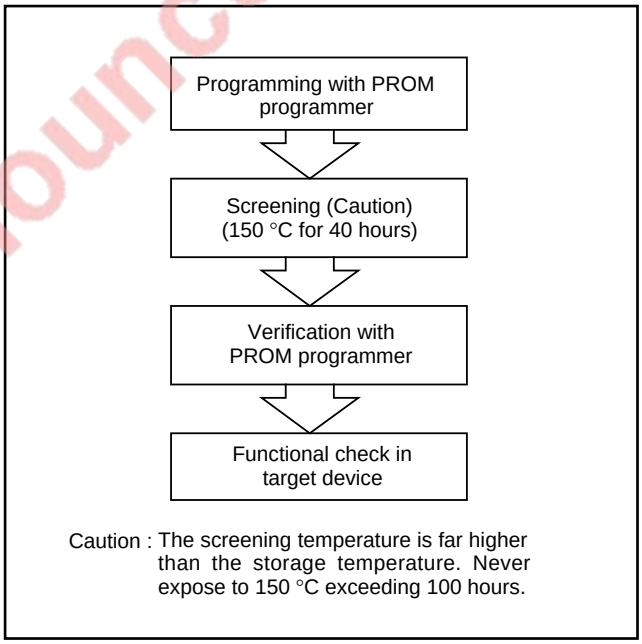


Fig. 37 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Table 6 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$, V_{REF}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P2_2$, $P2_3$		–0.3 to 5.8	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV$_{SS}$		–0.3 to 13	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P2_2$, $P2_3$		–0.3 to 5.8	V
P_d	Power dissipation	T_a = 25 °C	300	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Table 7 Recommended operating conditions (1)
(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (At 8 MHz)		4.0	5.0	5.5	V
	Power source voltage (At 4 MHz)		2.7	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{REF}	A-D convert reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage	AN_0–AN_4	AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$, X_{IN}, CNV$_{SS}$	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$	0		0.2V_{CC}	V
V_{IL}	“L” input voltage	$\overline{RESET}$, CNV$_{SS}$	0		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	“H” total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_4$ (Note)			–80	mA
$\Sigma I_{OH(peak)}$	“H” total peak output current	$P2_0$, $P2_1$, $P2_4$–$P2_7$, $P4_0$–$P4_4$ (Note)			–80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_2$, $P3_0$–$P3_4$ (Note)			80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current	$P1_3$–$P1_7$ (Note)			80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current	$P2_0$–$P2_7$,$P4_0$–$P4_4$ (Note)			80	mA
$\Sigma I_{OH(avg)}$	“H” total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_4$ (Note)			–40	mA
$\Sigma I_{OH(avg)}$	“H” total average output current	$P2_0$, $P2_1$, $P2_4$–$P2_7$, $P4_0$–$P4_4$ (Note)			–40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_2$, $P3_0$–$P3_4$ (Note)			40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current	$P1_3$–$P1_7$ (Note)			40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current	$P2_0$–$P2_7$,$P4_0$–$P4_4$ (Note)			40	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 8 Recommended operating conditions (2)
(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ (Note 1)			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_2$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ (Note 1)			10	mA
$I_{OL(peak)}$	"L" peak output current	$P1_3$–$P1_7$ (Note 1)			20	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ (Note 2)			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_2$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ (Note 2)			5	mA
$I_{OL(avg)}$	"L" peak output current	$P1_3$–$P1_7$ (Note 2)			15	mA
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC} = 4.0 to 5.5V) (Note 3)				8	MHz
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC} = 2.7 to 5.5V) (Note 3)				4	kHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50%.

Table 9 Electrical characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ **(Note)**	I_{OH} = –10 mA V_{CC} = 4.0–5.5 V	V_{CC}–2.0			V
		I_{OH} = –1.0 mA V_{CC} = 2.7–5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_2$, $P2_0$–$P2_7$ $P3_0$–$P3_4$, $P4_0$–$P4_4$	I_{OL} = 10 mA V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 1.0 mA V_{CC} = 2.7–5.5 V			1.0	V
V_{OL}	"L" output voltage $P1_3$–$P1_7$	I_{OL} = 20 mA V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 10 mA V_{CC} = 2.7–5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0–INT_3			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD, SCLK			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_4$, $P4_0$–$P4_4$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$,CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4		µA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V

Note: $P2_5$ is measured when the $P2_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".

Table 10 Electrical characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			6.8	13	mA
		High-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			1.6		mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			60	200	µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			20	40	µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			20	55	µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			5.0	10.0	µA
		Middle-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = stopped Output transistors “off”			4.0	7.0	mA
		Middle-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”			1.5		mA
		Increment when A-D conversion is executed $f(X_{IN})$ = 8 MHz			800		µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Table 11 A-D converter characteristics

(V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 8 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				10	bit
–	Absolute accuracy (excluding quantization error)				±4	LSB
t_{CONV}	Conversion time				61	tc(ϕ)
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	μA
$I_{I(AD)}$	A-D port input current			0.5	5.0	μA

TIMING REQUIREMENTS

Table 12 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0–INT_3 input “H” pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0–INT_3 input “L” pulse width	80			ns
$t_{C(SCLK)}$	Serial I/O clock input cycle time (Note)	800			ns
$t_{WH(SCLK)}$	Serial I/O clock input “H” pulse width (Note)	370			ns
$t_{WL(SCLK)}$	Serial I/O clock input “L” pulse width (Note)	370			ns
$t_{su(RxD-SCLK)}$	Serial I/O input setup time	220			ns
$t_{h(SCLK-RxD)}$	Serial I/O input hold time	100			ns

Note : When $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

Table 13 Timing requirements (2)

(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0–INT_3 input “H” pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0–INT_3 input “L” pulse width	230			ns
$t_{C(SCLK)}$	Serial I/O clock input cycle time (Note)	2000			ns
$t_{WH(SCLK)}$	Serial I/O clock input “H” pulse width (Note)	950			ns
$t_{WL(SCLK)}$	Serial I/O clock input “L” pulse width (Note)	950			ns
$t_{su(RxD-SCLK)}$	Serial I/O input setup time	400			ns
$t_{h(SCLK-RxD)}$	Serial I/O input hold time	200			ns

Note : When $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

Table 14 Switching characteristics 1
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH} (SCLK)	Serial I/O clock output "H" pulse width	t_C(SCLK)/2–30			ns
t_{WL} (SCLK)	Serial I/O clock output "L" pulse width	t_C(SCLK)/2–30			ns
t_d (SCLK-TxD)	Serial I/O output delay time (Note 1)			140	ns
t_v (SCLK-TxD)	Serial I/O output valid time (Note 1)	–30			ns
t_r (SCLK)	Serial I/O clock output rising time			30	ns
t_f (SCLK)	Serial I/O clock output falling time			30	ns
t_r (CMOS)	CMOS output rising time (Note 2)		10	30	ns
t_f (CMOS)	CMOS output falling time (Note 2)		10	30	ns

Notes 1: For t_{WH}(SCLK), t_{WL}(SCLK), when the P51/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: The X_{OUT} pin is excluded.

Table 15 Switching characteristics 2
(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH} (SCLK)	Serial I/O clock output "H" pulse width	t_C(SCLK)/2–50			ns
t_{WL} (SCLK)	Serial I/O clock output "L" pulse width	t_C(SCLK)/2–50			ns
t_d (SCLK-TxD)	Serial I/O output delay time (Note 1)			350	ns
t_v (SCLK-TxD)	Serial I/O output valid time (Note 1)	–30			ns
t_r (SCLK)	Serial I/O clock output rising time			50	ns
t_f (SCLK)	Serial I/O clock output falling time			50	ns
t_r (CMOS)	CMOS output rising time (Note 2)		20	50	ns
t_f (CMOS)	CMOS output falling time (Note 2)		20	50	ns

Notes 1: For t_{WH}(SCLK), t_{WL}(SCLK), when the P51/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: The X_{OUT} pin is excluded.

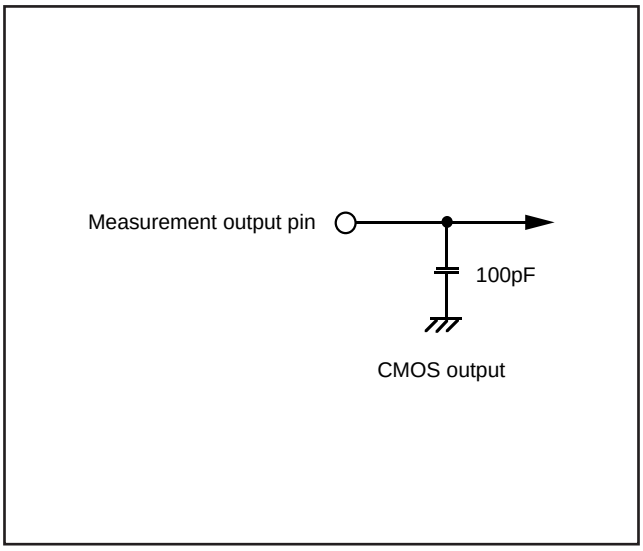


Fig. 38 Circuit for measuring output switching characteristics (1)

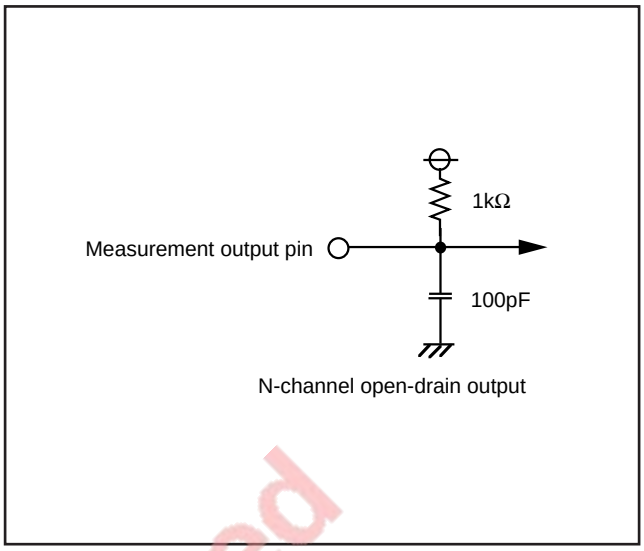


Fig. 39 Circuit for measuring output switching characteristics (2)

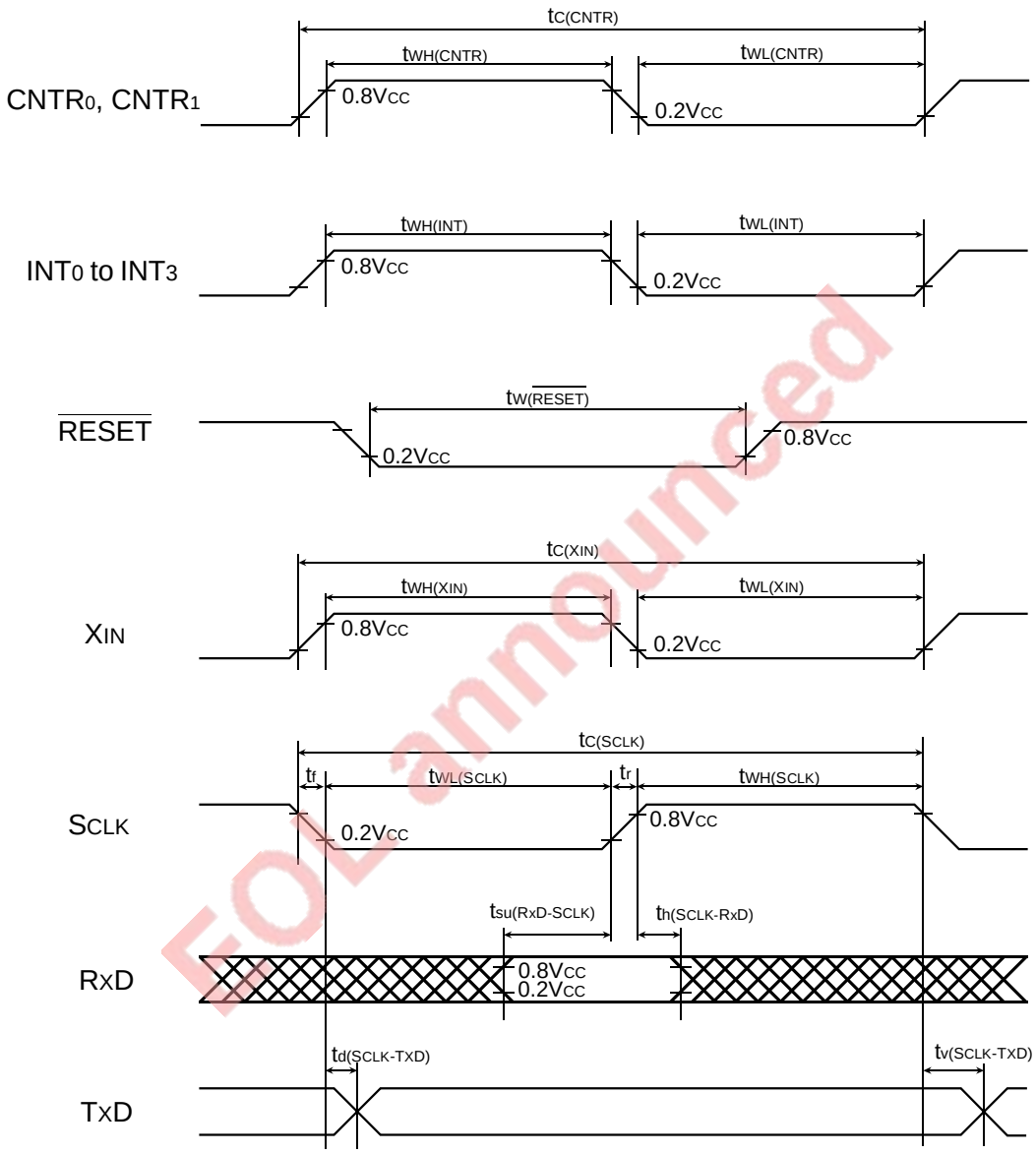


Fig. 40 Timing diagram

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MASK ROM CONFIRMATION FORM

GZZ-SH53-11B<86A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38503M2-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

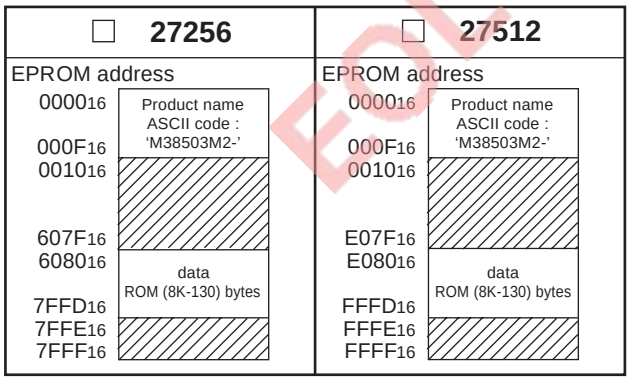
✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data.
We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name: ☐ M38503M2-XXXSP ☐ M38503M2-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address 6080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
(2) The ASCII codes of the product name "M38503M2–" must be entered in addresses 0000₁₆ to 0008₁₆. And set the data "FF₁₆" in addresses 0009₁₆ to 000F₁₆.
The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address	
0000₁₆	'M' = 4D₁₆
0001₁₆	'3' = 33₁₆
0002₁₆	'8' = 38₁₆
0003₁₆	'5' = 35₁₆
0004₁₆	'0' = 30₁₆
0005₁₆	'3' = 33₁₆
0006₁₆	'M' = 4D₁₆
0007₁₆	'2' = 32₁₆

Address	
0008₁₆	'–' = 2D₁₆
0009₁₆	FF₁₆
000A₁₆	FF₁₆
000B₁₆	FF₁₆
000C₁₆	FF₁₆
000D₁₆	FF₁₆
000E₁₆	FF₁₆
000F₁₆	FF₁₆

GZZ-SH53-11B<86A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38503M2-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program because ASCII codes of the product name are written to addresses 000016 to 000816 of EPROM.

EPROM type	27256	27512
The pseudo-command	*= △$8000 .BYTE △'M38503M2–'	*= △$0000 .BYTE △'M38503M2–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

✺ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (42P4B for M38503M2-XXXSP, 42P2R-A for M38503M2-XXXFP) and attach it to the mask ROM confirmation form.

✺ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the XIN-XOUT oscillator?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other ( )

At what frequency? f(XIN) = ☐ MHz

(2) Which function will you use the pins P21/XCIN and P20/XCOUT as P21 and P20, or XCIN and XCOUT ?

☐ Ports P21 and P20 function ☐ XCIN and XCOUT function (external resonator)

✺ 4. Comments

MASK ROM CONFIRMATION FORM

GZZ-SH11-40A<6YA0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38503M4-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

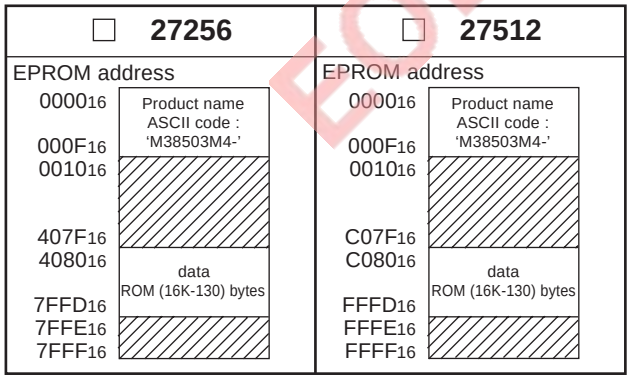
✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data.
We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name: ☐ M38503M4-XXXSP ☐ M38503M4-XXXFP

Checksum code for entire EPROM [ ][ ][ ][ ] (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address C080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
(2) The ASCII codes of the product name "M38503M4–" must be entered in addresses 0000₁₆ to 0008₁₆. And set the data "FF₁₆" in addresses 0009₁₆ to 000F₁₆.
The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address	
0000₁₆	'M' = 4D₁₆
0001₁₆	'3' = 33₁₆
0002₁₆	'8' = 38₁₆
0003₁₆	'5' = 35₁₆
0004₁₆	'0' = 30₁₆
0005₁₆	'3' = 33₁₆
0006₁₆	'M' = 4D₁₆
0007₁₆	'4' = 34₁₆

Address	
0008₁₆	'–' = 2D₁₆
0009₁₆	FF₁₆
000A₁₆	FF₁₆
000B₁₆	FF₁₆
000C₁₆	FF₁₆
000D₁₆	FF₁₆
000E₁₆	FF₁₆
000F₁₆	FF₁₆

GZZ-SH11-40A<6YA0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38503M4-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program because ASCII codes of the product name are written to addresses 0000_{16} to 0008_{16} of EPROM.

EPROM type	27256	27512
The pseudo-command	*= △$8000 .BYTE △'M38503M4–'	*= △$0000 .BYTE △'M38503M4–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (42P4B for M38503M4-XXXSP, 42P2R-A for M38503M4-XXXFP) and attach it to the mask ROM confirmation form.

✵ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the XIN-XOUT oscillator?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other ( )

At what frequency? f(XIN) = ☐ MHz

(2) Which function will you use the pins P21/XCIN and P20/XCOUT as P21 and P20, or XCIN and XCOUT ?

☐ Ports P21 and P20 function ☐ XCIN and XCOUT function (external resonator)

✵ 4. Comments

ROM PROGRAMMING CONFIRMATION FORM

GZZ-SH11-41A<6YA0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38503E4-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

✵ 1. Confirmation

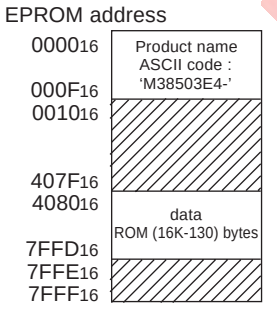
Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the programming data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name: ☐ M38503E4-XXXSP ☐ M38503E4-XXXFP

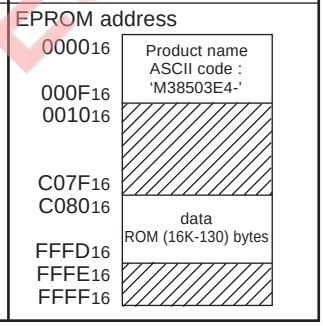
Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ **27256**



☐ **27512**



In the address space of the microcomputer, the internal ROM area is from address C08016 to FFFD16. The reset vector is stored in addresses FFFC16 and FFFD16.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF16".
(2) The ASCII codes of the product name "M38503E4–" must be entered in addresses 000016 to 000816. And set the data "FF16" in addresses 000916 to 000F16. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address	
000016	'M' = 4D16
000116	'3' = 3316
000216	'8' = 3816
000316	'5' = 3516
000416	'0' = 3016
000516	'3' = 3316
000616	'E' = 4516
000716	'4' = 3416

Address	
000816	'–' = 2D16
000916	FF16
000A16	FF16
000B16	FF16
000C16	FF16
000D16	FF16
000E16	FF16
000F16	FF16

GZZ-SH11-41A<6YA0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38503E4-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program because ASCII codes of the product name are written to addresses 0000_{16} to 0008_{16} of EPROM.

EPROM type	27256	27512
The pseudo-command	*= △$8000 .BYTE △'M38503E4–'	*= △$0000 .BYTE △'M38503E4–'

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM will not be processed.

✺ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form; 42P2R-A for the M38503E4-XXXFP, the shrink DIP package Mark Specification Form (only for built-in One Time PROM microcomputer) for the M38503E4-XXXSP; and attach it to the ROM programming confirmation form.

✺ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other ( )

At what frequency? $f(X_{IN})$ = ☐ MHz

(2) Which function will you use the pins $P2_1/X_{CIN}$ and $P2_0/X_{COUT}$ as $P2_1$ and $P2_0$, or X_{CIN} and X_{COUT} ?

☐ Ports $P2_1$ and $P2_0$ function ☐ X_{CIN} and X_{COUT} function (external resonator)

✺ 4. Comments

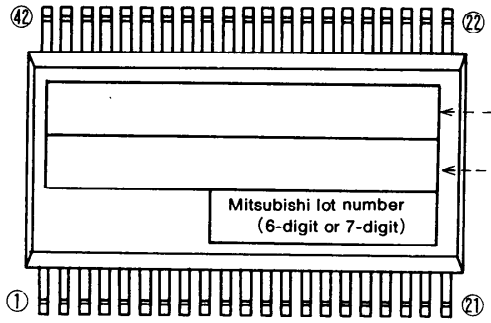
MARK SPECIFICATION FORM

42P2R-A (42-PIN SHRINK SOP) MARK SPECIFICATION FORM

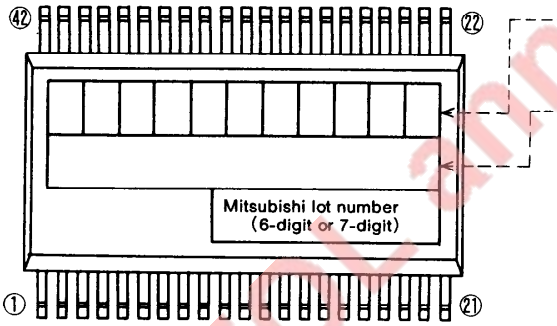
Mitsubishi ICcatalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi catalog name



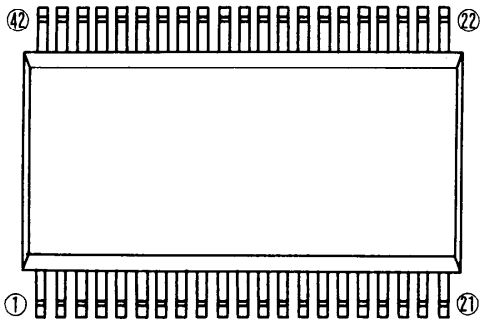
Customer's Parts Number

Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's Parts Number can be up to 11 characters : Only 0~9, A~Z, +, −, /, (,), &, ©, ・ (periods), , (commas) are usable.

C. Special Mark Required



Note1 : If the Special Mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the Special Mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

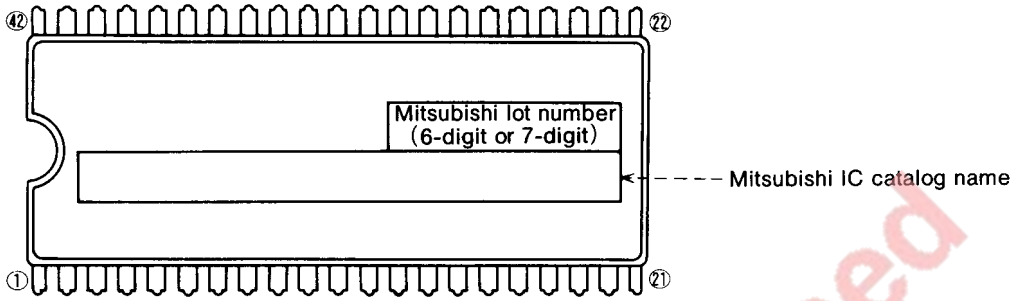
3 : The standard Mitsubishi font is used for all characters except for a logo.

42P4B (42-PIN SHRINK DIP) MARK SPECIFICATION FORM

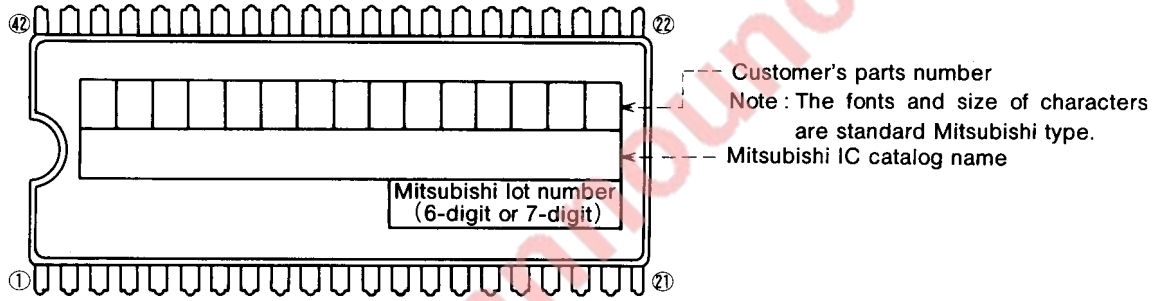
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

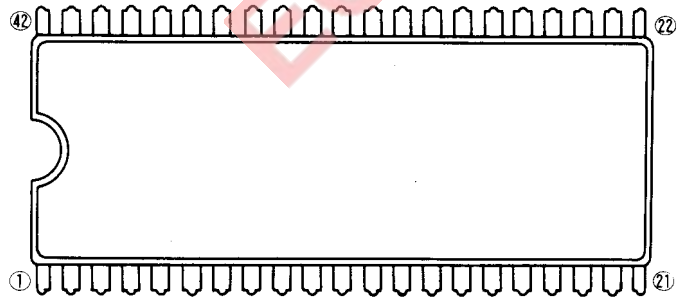


B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 15 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, . (period), and , (comma) are usable.

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

The standard Mitsubishi font is used for all characters except for a logo.

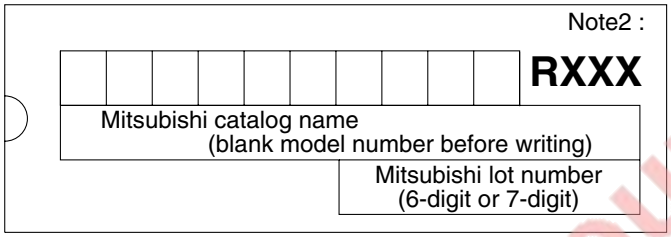
SHRINK DIP MARK SPECIFICATION FORM
for One Time PROM version microcomputers

Enter the catalog number of the microcomputer for which this mark specification is intended. (If you do not know the ROM code number, enter XXX in its place.)

The catalog number of the microcomputer **M**

A. Standard Mitsubishi Mark

Customer specified part number will be printed together with the ROM code number on the top line.
Enter the desired part number left aligned in the box below. (up to 10 characters)



Note1 : The following characters can be used in the part number :
Uppercase alphabet, numbers, ampersand, hyphen, period, comma, +, /, (,), ©
(© will be printed at 1.5 × character width)
2 : XXX is the ROM code number.

B. Special Mark Required

If you desire anything other than the standard Mitsubishi mark, it will be treated as a special mark.
Special marks will take longer to produce and should be avoided if possible.
If a special mark is to be printed, indicate the desired layout of the mark in the figure below. The layout will be duplicated as closely as possible.

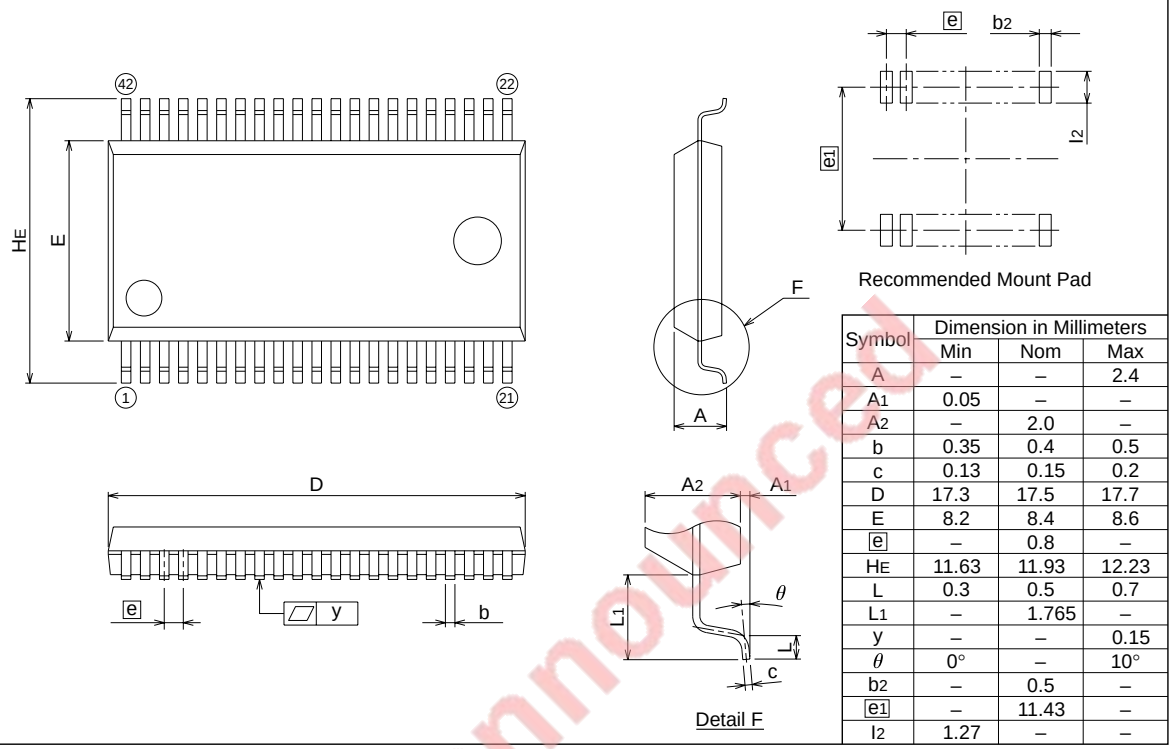
Note1 : If the customer's trademark logo must be used in the Special Mark, please submit a clean original logo.
Note that special marks require extra cost and time to produce.

PACKAGE OUTLINE

42P2R-A

Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	–	0.63	Alloy 42/Cu Alloy

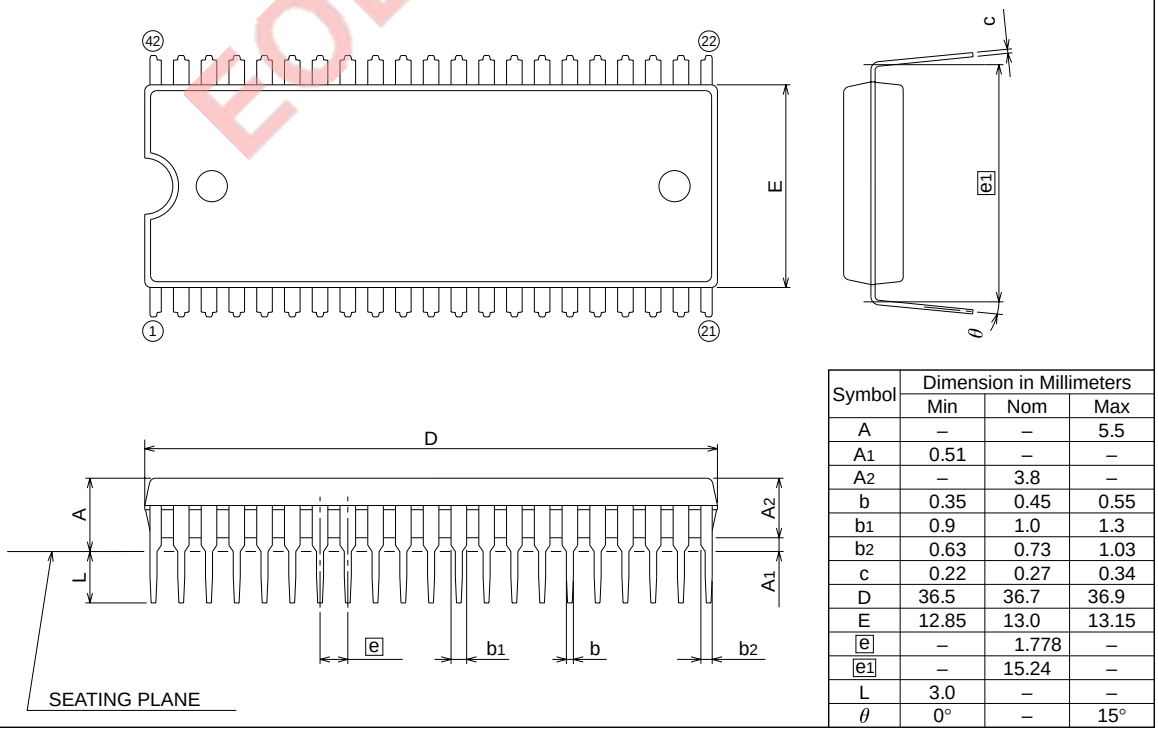


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A1	0.05	–	–
A2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	–	0.8	–
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	–	1.765	–
y	–	–	0.15
θ	0°	–	10°
b2	–	0.5	–
e1	–	11.43	–
l2	1.27	–	–

42P4B

Plastic 42pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP42-P-600-1.78	–	4.1	Alloy 42/Cu Alloy

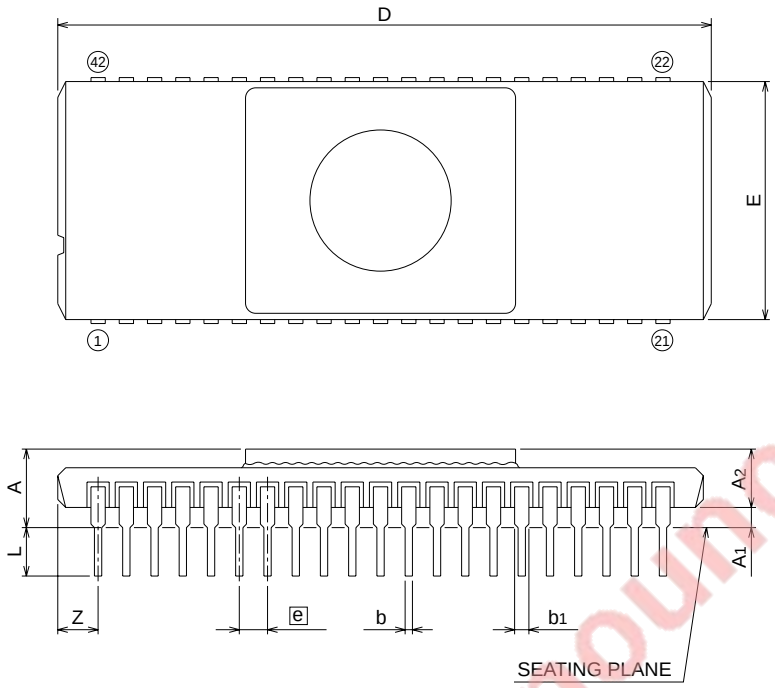


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A1	0.51	–	–
A2	–	3.8	–
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
b2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	–	1.778	–
e1	–	15.24	–
L	3.0	–	–
θ	0°	–	15°

42S1B-A

Metal seal 42pin 600mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
WDIP42-C-600-1.78	–	



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.0
A_1	1.0	–	–
A_2	–	–	3.44
b	0.38	0.46	0.54
b_1	0.7	0.8	0.9
c	0.17	0.25	0.33
D	–	–	41.1
E	–	–	15.8
e	–	1.778	–
e_1	–	15.24	–
L	3.05	–	–
Z	–	–	3.05

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

New publication, effective Aug. 1998.
Specifications subject to change without notice.

REVISION DESCRIPTION LIST	3850 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980817