TJA1054

Fault-tolerant CAN transceiver

Rev. 04 — 24 September 2009 Product data sheet

1. General description

The TJA1054 is the interface between the protocol controller and the physical bus wires in a Controller Area Network (CAN). It is primarily intended for low-speed applications up to 125 kBd in passenger cars. The device provides differential receive and transmit capability but will switch to single-wire transmitter and/or receiver in error conditions.

The TJA1054T is pin and downwards compatible with the PCA82C252T and the TJA1053T. This means that these two devices can be replaced by the TJA1054T with retention of all functions.

The most important improvements of the TJA1054 with respect to the PCA82C252 and TJA1053 are:

- Very low EME due to a very good matching of the CANL and CANH output signals
- Good EMI, especially in low power modes
- Full wake-up capability during bus failures
- Extended bus failure management including short-circuit of the CANH bus line to V_{CC}
- Support for easy system fault diagnosis
- Two-edge sensitive wake-up input signal via pin $\overline{WAKE}$

2. Features

2.1 Optimized for in-car low-speed communication

- Baud rate up to 125 kBd
- Up to 32 nodes can be connected
- Supports unshielded bus wires
- Very low ElectroMagnetic Emission (EME) due to built-in slope control function and a very good matching of the CANL and CANH bus outputs
- Very high ElectroMagnetic Immunity (EMI) in normal and low power operating modes
- Fully integrated receiver filters
- Transmit Data (TxD) dominant time-out function

2.2 Bus failure management

- Supports single-wire transmission modes with ground offset voltages up to 1.5 V
- Automatic switching to single-wire mode in the event of bus failures, even when the CANH bus wire is short-circuited to V_{CC}
- Automatic reset to differential mode if bus failure is removed
- Full wake-up capability during failure modes

NXP founded by Philips

2.3 Protections

- Bus pins short-circuit safe to battery and to ground
- Thermally protected
- Bus lines protected against transients in an automotive environment
- An unpowered node does not disturb the bus lines

2.4 Support for low power modes

- Low current sleep mode and standby mode with wake-up via the bus lines
- Power-on reset flag on the output

3. Quick reference data

Table 1. Quick reference data

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 27 V; V_{STB} = V_{CC}; T_{vj} = –40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[1][2]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			4.75	-	5.25	V
V_{BAT}	battery supply voltage on pin BAT	no time limit		–0.3	-	+40	V
		operating mode	[3]	5.0	-	27	V
		load dump		-	-	40	V
I_{BAT}	battery supply current on pin BAT	sleep mode; V_{CC} = 0 V; V_{BAT} = 12 V		-	30	50	µA
V_{CANH}	voltage on pin CANH	V_{CC} = 0 V to 5.0 V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin		–40	-	+40	V
V_{CANL}	voltage on pin CANL	V_{CC} = 0 V to 5.0 V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin		–40	-	+40	V
ΔV_{CANH}	voltage drop on pin CANH	I_{CANH} = –40 mA		-	-	1.4	V
ΔV_{CANL}	voltage drop on pin CANL	I_{CANL} = 40 mA		-	-	1.4	V
$t_{PD(L)}$	propagation delay TXD (LOW) to RXD (LOW)			-	1	-	µs
t_r	bus line output rise time	between 10 % and 90 %; C1 = 10 nF; see Figure 5		-	0.6	-	µs
t_f	bus line output fall time	between 10 % and 90 %; C1 = 1 nF; see Figure 5		-	0.3	-	µs
T_{vj}	virtual junction temperature		[4]	–40	-	+150	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design, but only 100 % tested at T_{amb} = 125 °C for dies on wafer level, and above this for cased products 100 % tested at T_{amb} = 25 °C, unless otherwise specified.

[2] For bare die, all parameters are only guaranteed if the back side of the die is connected to ground.

[3] A local or remote wake-up event will be signalled at the transceiver pins RXD and $\overline{ERR}$ if V_{BAT} = 5.3 V to 27 V see Table 5.

© NXP B.V. 2009. All rights reserved.

[4] Junction temperature in accordance with *"IEC 60747-1"*. An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$ where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1054T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1054T/S900	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1054U	-	bare die; 1990 × 2700 × 375 µm	-

5. Block diagram

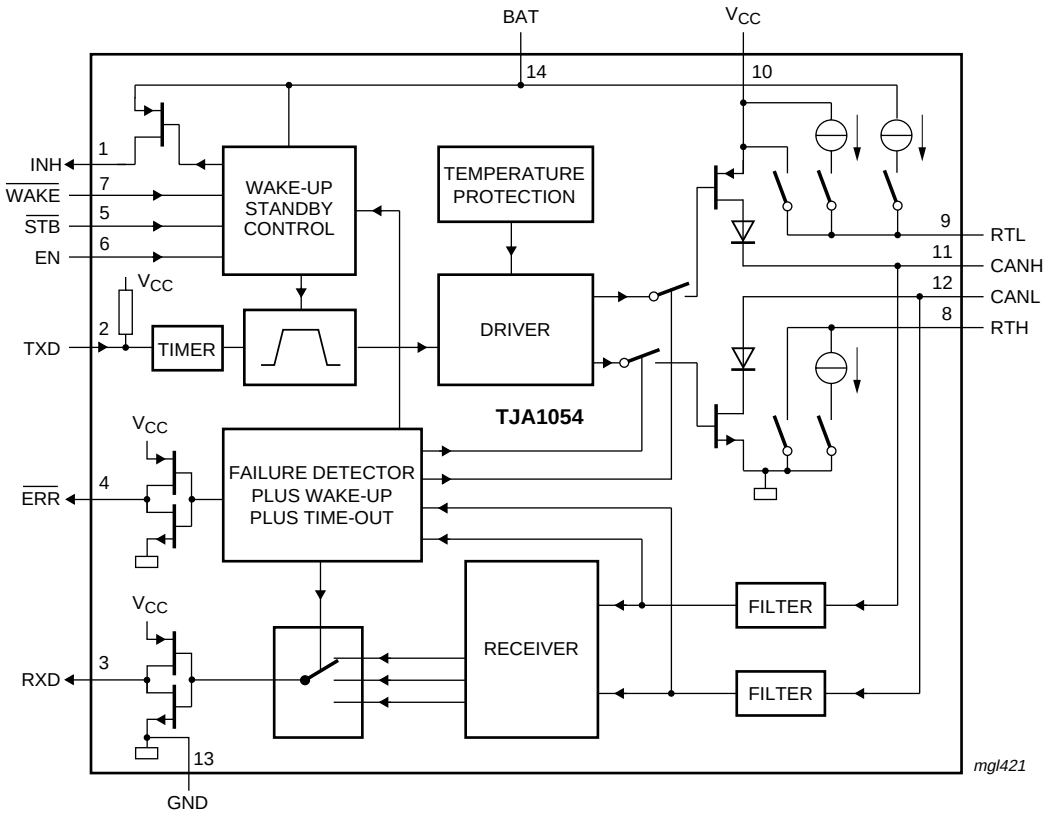


Fig 1. Block diagram

© NXP B.V. 2009. All rights reserved.

6. Pinning information

6.1 Pinning

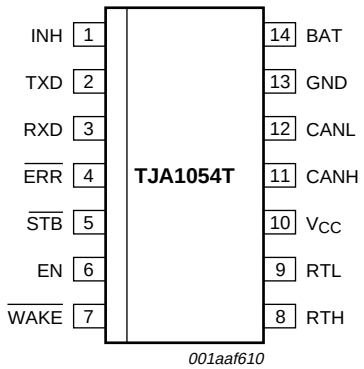


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
INH	1	inhibit output for switching an external voltage regulator if a wake-up signal occurs
TXD	2	transmit data input for activating the driver to the bus lines
RXD	3	receive data output for reading out the data from the bus lines
$\overline{ERR}$	4	error, wake-up and power-on indication output; active LOW in normal operating mode when a bus failure is detected; active LOW in standby and sleep mode when a wake-up is detected; active LOW in power-on standby when a V_{BAT} power-on event is detected
$\overline{STB}$	5	standby digital control signal input; together with the input signal on pin EN this input determines the state of the transceiver; see Table 5 and Figure 3
EN	6	enable digital control signal input; together with the input signal on pin $\overline{STB}$ this input determines the state of the transceiver; see Table 5 and Figure 3
$\overline{WAKE}$	7	local wake-up signal input (active LOW); both falling and rising edges are detected
RTH	8	termination resistor connection; in case of a CANH bus wire error the line is terminated with a predefined impedance
RTL	9	termination resistor connection; in case of a CANL bus wire error the line is terminated with a predefined impedance
V_{CC}	10	supply voltage
CANH	11	HIGH-level CAN bus line
CANL	12	LOW-level CAN bus line
GND	13	ground
BAT	14	battery supply voltage

© NXP B.V. 2009. All rights reserved.

7. Functional description

The TJA1054 is the interface between the CAN protocol controller and the physical wires of the CAN bus (see Figure 7). It is primarily intended for low-speed applications, up to 125 kBd, in passenger cars. The device provides differential transmit capability to the CAN bus and differential receive capability to the CAN controller.

To reduce EME, the rise and fall slopes are limited. This allows the use of an unshielded twisted pair or a parallel pair of wires for the bus lines. Moreover, the device supports transmission capability on either bus line if one of the wires is corrupted. The failure detection logic automatically selects a suitable transmission mode.

In normal operating mode (no wiring failures) the differential receiver is output on pin RXD (see Figure 1). The differential receiver inputs are connected to pins CANH and CANL through integrated filters. The filtered input signals are also used for the single-wire receivers. The receivers connected to pins CANH and CANL have threshold voltages that ensure a maximum noise margin in single-wire mode.

A timer function (TxD dominant time-out function) has been integrated to prevent the bus lines from being driven into a permanent dominant state (thus blocking the entire network communication) due to a situation in which pin TXD is permanently forced to a LOW level, caused by a hardware and/or software application failure.

If the duration of the LOW level on pin TXD exceeds a certain time, the transmitter will be disabled. The timer will be reset by a HIGH level on pin TXD.

7.1 Failure detector

The failure detector is fully active in the normal operating mode. After the detection of a single bus failure the detector switches to the appropriate mode (see Table 4). The differential receiver threshold voltage is set at –3.2 V typical (V_{CC} = 5 V). This ensures correct reception with a noise margin as high as possible in the normal operating mode and in the event of failures 1, 2, 5 and 6a. These failures, or recovery from them, do not destroy ongoing transmissions. The output drivers remain active, the termination does not change and the receiver remains in differential mode (see Table 4).

Failures 3, 3a and 6 are detected by comparators connected to the CANH and CANL bus lines. Failures 3 and 3a are detected in a two-step approach. If the CANH bus line exceeds a certain voltage level, the differential comparator signals a continuous dominant condition. Because of inter operability reasons with the predecessor products PCA82C252 and TJA1053, after a first time-out the transceiver switches to single-wire operation through CANH. If the CANH bus line is still exceeding the CANH detection voltage for a second time-out, the TJA1054 switches to CANL operation; the CANH driver is switched off and the RTH bias changes to the pull-down current source. The time-outs (delays) are needed to avoid false triggering by external RF fields.

© NXP B.V. 2009. All rights reserved.

Table 4. Bus failures

Failure	Description	Termination CANH (RTH)	Termination CANL (RTL)	CANH driver	CANL driver	Receiver mode
1	CANH wire interrupted	on	on	on	on	differential
2	CANL wire interrupted	on	on	on	on	differential
3	CANH short-circuited to battery	weak[1]	on	off	on	CANL
3a	CANH short-circuited to V_{CC}	weak[1]	on	off	on	CANL
4	CANL short-circuited to ground	on	weak[2]	on	off	CANH
5	CANH short-circuited to ground	on	on	on	on	differential
6	CANL short-circuited to battery	on	weak[2]	on	off	CANH
6a	CANL short-circuited to V_{CC}	on	on	on	on	differential
7	CANL and CANH mutually short-circuited	on	weak[2]	on	off	CANH

[1] A weak termination implies a pull-down current source behavior of 75 µA typical.

[2] A weak termination implies a pull-up current source behavior of 75 µA typical.

Failure 6 is detected if the CANL bus line exceeds its comparator threshold for a certain period of time. This delay is needed to avoid false triggering by external RF fields. After detection of failure 6, the reception is switched to the single-wire mode through CANH; the CANL driver is switched off and the RTL bias changes to the pull-up current source.

Recovery from failures 3, 3a and 6 is detected automatically after reading a consecutive recessive level by corresponding comparators for a certain period of time.

Failures 4 and 7 initially result in a permanent dominant level on pin RXD. After a time-out the CANL driver is switched off and the RTL bias changes to the pull-up current source. Reception continues by switching to the single-wire mode via pins CANH or CANL. When failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold level for a certain period of time, reception and transmission switch back to the differential mode.

If any of the wiring failure occurs, the output signal on pin $\overline{ERR}$ will be set to LOW. On error recovery, the output signal on pin $\overline{ERR}$ will be set to HIGH again. In case of an interrupted open bus wire, this failure will be detected and signalled only if there is an open wire between the transmitting and receiving node(s). Thus, during open wire failures, pin $\overline{ERR}$ typically toggles.

During all single-wire transmissions, EMC performance (both immunity and emission) is worse than in the differential mode. The integrated receiver filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In single-wire mode, LF noise cannot be distinguished from the required signal.

© NXP B.V. 2009. All rights reserved.

7.2 Low power modes

The transceiver provides three low power modes which can be entered and exited via $\overline{STB}$ and EN (see Table 5 and Figure 3).

The sleep mode is the mode with the lowest power consumption. Pin INH is switched to HIGH-impedance for deactivation of the external voltage regulator. Pin CANL is biased to the battery voltage via pin RTL. If the supply voltage is provided, pins RXD and $\overline{ERR}$ will signal the wake-up interrupt.

The standby mode operates in the same way as the sleep mode but with a HIGH level on pin INH.

The power-on standby mode is the same as the standby mode, however, in this mode the battery power-on flag is shown on pin $\overline{ERR}$ instead of the wake-up interrupt signal. The output on pin RXD will show the wake-up interrupt. This mode is only for reading out the power-on flag.

Table 5. Normal operating and low power modes

Mode	Pin $\overline{STB}$	Pin EN	Pin $\overline{ERR}$		Pin RXD		Pin RTL switched to
			LOW	HIGH	LOW	HIGH	
Goto-sleep command	LOW	HIGH	wake-up interrupt signal[1][2][3]		wake-up interrupt signal[1][2][3]		V_{BAT}
Sleep	LOW	LOW[4]					
Standby	LOW	LOW					
Power-on standby	HIGH	LOW	V_{BAT} power-on flag[1][5]		wake-up interrupt signal[1][2][3]		V_{BAT}
Normal operating	HIGH	HIGH	error flag	no error flag	dominant received data	recessive received data	V_{CC}

[1] If the supply voltage V_{CC} is present

[2] Wake-up interrupts are released when entering normal operating mode.

[3] A local or remote wake-up event will be signalled at the transceiver pins RXD and $\overline{ERR}$ if V_{BAT} = 5.3 V to 27 V.

[4] In case the goto-sleep command was used before. When V_{CC} drops, pin EN will become LOW, but due to the fail-safe functionality this does not effect the internal functions.

[5] V_{BAT} power-on flag will be reset when entering normal operating mode.

Wake-up requests are recognized by the transceiver through two possible channels:

- The bus lines for remote wake-up
- Pin $\overline{WAKE}$ for local wake-up

In order to wake-up the transceiver remotely through the bus lines, a filter mechanism is integrated. This mechanism makes sure that noise and any present bus failure conditions do not result into an erroneous wake-up. Because of this mechanism it is not sufficient to simply pull the CANH or CANL bus lines to a dominant level for a certain time. To guarantee a successful remote wake-up under all conditions, a message frame with a dominant phase of at least the maximum specified $t_{(CANH)}$ or $t_{(CANL)}$ in it is required.

© NXP B.V. 2009. All rights reserved.

A local wake-up through pin $\overline{\text{WAKE}}$ is detected by a rising or falling edge with a consecutive level exceeding the maximum specified t_{WAKE}.

On a wake-up request the transceiver will set the output on pin INH to HIGH which can be used to activate the external supply voltage regulator.

If V_{CC} is provided the wake-up request can be read on the $\overline{\text{ERR}}$ or RXD outputs, so the external microcontroller can activate the transceiver (switch to normal operating mode) via pins $\overline{\text{STB}}$ and EN.

To prevent a false remote wake-up due to transients or RF fields, the wake-up voltage levels have to be maintained for a certain period of time. In the low power modes the failure detection circuit remains partly active to prevent an increased power consumption in the event of failures 3, 3a, 4 and 7.

To prevent a false local wake-up during an open wire at pin $\overline{\text{WAKE}}$, this pin has a weak pull-up current source towards V_{BAT}. However, in order to prevent EMC issues, it is recommended to connect a not used pin $\overline{\text{WAKE}}$ to pin BAT. INH is set to floating only if the goto-sleep command is entered successfully. To enter a successful goto-sleep command under all conditions, this command must be kept stable for the maximum specified $t_{h(sleep)}$.

Pin INH will be set to a HIGH level again by the following events only:

- V_{BAT} power-on (cold start)
- Rising or falling edge on pin $\overline{\text{WAKE}}$
- A message frame with a dominant phase of at least the maximum specified $t_{(CANH)}$ or $t_{(CANL)}$, while pin EN or pin $\overline{\text{STB}}$ is at a LOW level
- Pin $\overline{\text{STB}}$ goes to a HIGH level with V_{CC} active

To provide fail-safe functionality, the signals on pins $\overline{\text{STB}}$ and EN will internally be set to LOW when V_{CC} is below a certain threshold voltage ($V_{CC(stb)}$).

7.3 Power-on

After power-on (V_{BAT} switched on) the signal on pin INH will become HIGH and an internal power-on flag will be set. This flag can be read in the power-on standby mode through pin $\overline{\text{ERR}}$ ($\overline{\text{STB}}$ = 1; EN = 0) and will be reset by entering the normal operating mode.

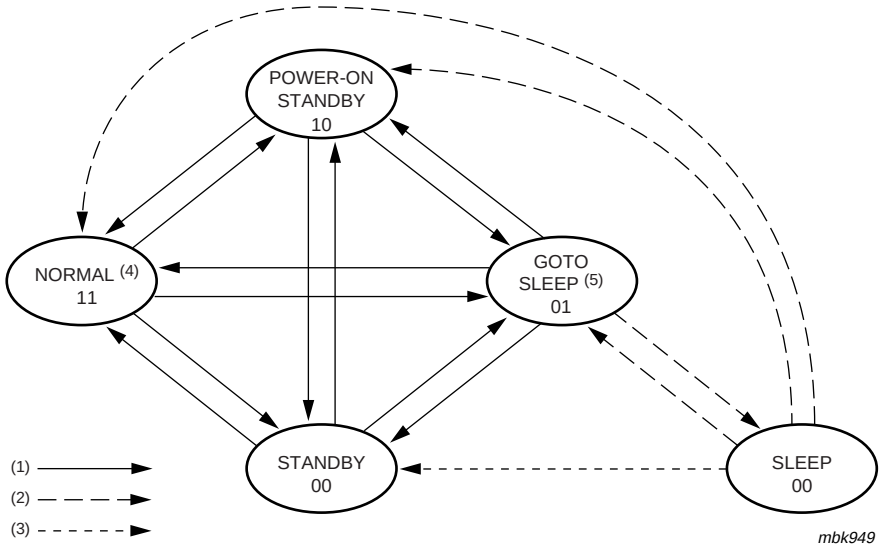
7.4 Protections

A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage.

If the junction temperature exceeds the typical value of 165 °C, the transmitter output stages are disabled. Because the transmitter is responsible for the major part of the power dissipation, this will result in a reduced power dissipation and hence a lower chip temperature. All other parts of the device will continue to operate.

The pins CANH and CANL are protected against electrical transients which may occur in an automotive environment.

© NXP B.V. 2009. All rights reserved.



Mode 10 stands for: Pin $\overline{STB}$ = HIGH and pin EN = LOW.

(1) Mode change via input pins $\overline{STB}$ and EN.

(2) Mode change via input pins $\overline{STB}$ and EN; it should be noted that in the sleep mode pin INH is inactive and possibly there is no V_{CC}. Mode control is only possible if V_{CC} of the transceiver is active.

(3) Pin INH is activated after wake-up via bus input pin $\overline{WAKE}$.

(4) Transitions to normal mode clear the internal wake-up: interrupt and battery fail flag are cleared.

(5) Transitions to sleep mode: pin INH is deactivated.

Fig 3. Mode control

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+6	V
V_{BAT}	battery supply voltage		–0.3	+40	V
V_{TXD}	voltage on pin TXD		–0.3	V_{CC} + 0.3	V
V_{RXD}	voltage on pin RXD		–0.3	V_{CC} + 0.3	V
V_{ERR}	voltage on pin $\overline{ERR}$		–0.3	V_{CC} + 0.3	V
V_{STB}	voltage on pin $\overline{STB}$		–0.3	V_{CC} + 0.3	V
V_{EN}	voltage on pin EN		–0.3	V_{CC} + 0.3	V
V_{CANH}	voltage on pin CANH	with respect to any other pin	–40	+40	V
V_{CANL}	voltage on pin CANL	with respect to any other pin	–40	+40	V
$V_{trt(n)}$	transient voltage on pins CANH and CANL	see Figure 6	–150	+100	V

© NXP B.V. 2009. All rights reserved.

Table 6. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{I(WAKE)}$	input voltage on pin $\overline{WAKE}$	with respect to any other pin		–	V_{BAT} + 0.3	V
$I_{I(WAKE)}$	input current on pin $\overline{WAKE}$		[2]	–15	-	mA
V_{INH}	voltage on pin INH			–0.3	V_{BAT} + 0.3	V
V_{RTH}	voltage on pin RTH	with respect to any other pin		–0.3	V_{BAT} + 1.2	V
V_{RTL}	voltage on pin RTL	with respect to any other pin		–0.3	V_{BAT} + 1.2	V
R_{RTH}	termination resistance on pin RTH			500	16000	Ω
R_{RTL}	termination resistance on pin RTL			500	16000	Ω
T_{vj}	virtual junction temperature		[3]	–40	+150	°C
T_{stg}	storage temperature			–55	+150	°C
V_{ESD}	electrostatic discharge voltage	human body model	[4]	–2	+2	kV
		machine model	[5]	–100	+100	V

[1] All voltages are defined with respect to pin GND, unless otherwise specified. Positive current flows into the device.

[2] Only relevant if $V_{WAKE} < V_{GND} - 0.3$ V; current will flow into pin GND.

[3] Junction temperature in accordance with *"IEC 60747-1"*. An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$ where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[4] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

[5] Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 µH coil.

9. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	120	K/W
$R_{th(j-s)}$	thermal resistance from junction to substrate bare die	in free air	40	K/W

© NXP B.V. 2009. All rights reserved.

10. Static characteristics

Table 8. Static characteristics

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 27 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies (pins V_{CC} and BAT)						
V_{CC}	supply voltage		4.75	-	5.25	V
$V_{CC(stb)}$	supply voltage for forced standby mode (fail-safe)		2.75	-	4.5	V
I_{CC}	supply current	normal operating mode; V_{TXD} = V_{CC} (recessive)	4	7	11	mA
		normal operating mode; V_{TXD} = 0 V (dominant); no load	10	17	27	mA
		low power modes at V_{TXD} = V_{CC}	0	0	10	µA
V_{BAT}	battery supply voltage on pin BAT	no time limit	−0.3	-	+40	V
		operating mode	5.0	-	27	V
		load dump	-	-	40	V
I_{BAT}	battery supply current on pin BAT	all modes and in low power modes at V_{RTL} = V_{WAKE} = V_{INH} = V_{BAT}				
		V_{BAT} = 12 V	10	30	50	µA
		V_{BAT} = 5 V to 27 V	5	30	125	µA
		V_{BAT} = 3.5 V	5	20	30	µA
		V_{BAT} = 1 V	0	0	10	µA
		sleep mode; V_{CC} = 0 V;				
		V_{BAT} = 12 V	-	30	50	µA
$V_{BAT(Pwon)}$	power-on flag voltage on pin BAT	low power modes				
		power-on flag set	-	-	1	V
		power-on flag not set	3.5	-	-	V
I_{tot}	supply current plus battery current	low power modes; V_{CC} = 5 V; V_{BAT} = V_{WAKE} = V_{INH} = 12 V	-	30	60	µA
Pins $\overline{STB}$, EN and TXD						
V_{IH}	HIGH-level input voltage		0.7V_{CC}	-	V_{CC} +0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	0.3V_{CC}	V
I_{IH}	HIGH-level input current					
	pins $\overline{STB}$ and EN	V_I = 4 V	-	9	20	µA
	pin TXD	V_I = 4 V	−200	−80	−25	µA
I_{IL}	LOW-level input current					
	pins $\overline{STB}$ and EN	V_I = 1 V	4	8	-	µA
	pin TXD	V_I = 1 V	−800	−320	−100	µA

© NXP B.V. 2009. All rights reserved.

Table 8. Static characteristics *...continued*

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 27 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pins RXD and $\overline{ERR}$						
$V_{OH)}$	HIGH-level output voltage					
	on pin $\overline{ERR}$	I_O = −100 µA	V_{CC} − 0.9	-	V_{CC}	V
	on pin RXD	I_O = −1 mA	V_{CC} − 0.9	-	V_{CC}	V
V_{OL}	LOW-level output voltage					
	on pin $\overline{ERR}$	I_O = 1.6 mA	0	-	0.4	V
	on pin RXD	I_O = 7.5 mA	0	-	1.5	V
Pin $\overline{WAKE}$						
I_{IL}	LOW-level input current	V_{WAKE} = 0 V; V_{BAT} = 27 V	−10	−4	−1	µA
$V_{th(wake)}$	wake-up threshold voltage	V_{STB} = 0 V	2.5	3.2	3.9	V
Pin INH						
ΔV_H	HIGH-level voltage drop	I_{INH} = −0.18 mA	-	-	0.8	V
I_L	leakage current	sleep mode; V_{INH} = 0 V	-	-	5	µA
Pins CANH and CANL						
V_{CANH}	voltage on pin CANH	V_{CC} = 0 V to 5.0 V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	−40	-	+40	V
V_{CANL}	voltage on pin CANL	V_{CC} = 0 V to 5.0 V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	−40	-	+40	V
ΔV_{CANH}	voltage drop on pin CANH	I_{CANH} = −40 mA	-	-	1.4	V
ΔV_{CANL}	voltage drop on pin CANL	I_{CANL} = 40 mA	-	-	1.4	V
$V_{th(dif)}$	differential receiver threshold voltage	no failures and bus failures 1, 2, 5 and 6a; see Figure 4				
		V_{CC} = 5 V	−3.5	−3.2	−2.9	V
		V_{CC} = 4.75 V to 5.25 V	$-0.70V_{CC}$	$-0.64V_{CC}$	$-0.58V_{CC}$	V
$V_{O(reces)}$	recessive output voltage	V_{TXD} = V_{CC}				
	on pin CANH	R_{RTH} < 4 kΩ	-	-	0.2	V
	on pin CANL	R_{RTL} < 4 kΩ	V_{CC} − 0.2	-	-	V
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; V_{EN} = V_{CC}				
	on pin CANH	I_{CANH} = −40 mA	V_{CC} − 1.4	-	-	V
	on pin CANL	I_{CANL} = 40 mA	-	-	1.4	V
$I_{O(CANH)}$	output current on pin CANH	normal operating mode; V_{CANH} = 0 V; V_{TXD} = 0 V	−110	−80	−45	mA
		low power modes; V_{CANH} = 0 V; V_{CC} = 5 V	-	−0.25	-	µA

© NXP B.V. 2009. All rights reserved.

Table 8. Static characteristics *…continued*

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 27 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{O(CANL)}$	output current on pin CANL	normal operating mode; V_{CANL} = 14 V; V_{TXD} = 0 V	45	70	100	mA
		low power modes; V_{CANL} = 12 V; V_{BAT} = 12 V	-	0	-	µA
$V_{d(CANH)(sc)}$	detection voltage for short-circuit to battery voltage on pin CANH	normal operating mode; V_{CC} = 5 V	1.5	1.7	1.85	V
		low power modes	1.1	1.8	2.5	V
$V_{d(CANL)(sc)}$	detection voltage for short-circuit to battery voltage on pin CANL	normal operating mode				
		V_{CC} = 5 V	6.6	7.2	7.8	V
		V_{CC} = 4.75 V to 5.25 V	$1.32V_{CC}$	$1.44V_{CC}$	$1.56V_{CC}$	V
$V_{th(wake)}$	wake-up threshold voltage					
	on pin CANL	low power modes	2.5	3.2	3.9	V
	on pin CANH	low power modes	1.1	1.8	2.5	V
$\Delta V_{th(wake)}$	difference of wake-up threshold voltages	low power modes	0.8	1.4	-	V
$V_{th(CANH)(sc)}$	single-ended receiver threshold voltage on pin CANH	normal operating mode and failures 4, 6 and 7				
		V_{CC} = 5 V	1.5	1.7	1.85	V
		V_{CC} = 4.75 V to 5.25 V	$0.30V_{CC}$	$0.34V_{CC}$	$0.37V_{CC}$	V
$V_{th(CANL)(sc)}$	single-ended receiver threshold voltage on pin CANL	normal operating mode and failures 3 and 3a				
		V_{CC} = 5 V	3.15	3.3	3.45	V
		V_{CC} = 4.75 V to 5.25 V	$0.63V_{CC}$	$0.66V_{CC}$	$0.69V_{CC}$	V
$R_{i(CANH)(sc)}$	single-ended input resistance on pin CANH	normal operating mode	110	165	270	kΩ
$R_{i(CANL)(sc)}$	single-ended input resistance on pin CANL	normal operating mode	110	165	270	kΩ
$R_{i(dif)}$	differential input resistance	normal operating mode	220	330	540	kΩ
Pins RTH and RTL						
$R_{sw(RTL)}$	switch-on resistance on pin RTL and V_{CC}	normal operating mode; $\|I_O\|$ < 10 mA	-	50	100	Ω
$R_{sw(RTH)}$	switch-on resistance on pin RTH and ground	normal operating mode; $\|I_O\|$ < 10 mA	-	50	100	Ω
$V_{O(RTH)}$	output voltage on pin RTH	low power modes; I_O = 1 mA	-	0.7	1.0	V
$I_{O(RTL)}$	output current on pin RTL	low power modes; V_{RTL} = 0 V	−1.25	−0.65	−0.3	mA
$I_{pu(RTL)}$	pull-up current on pin RTL	normal operating mode and failures 4, 6 and 7	-	75	-	µA

© NXP B.V. 2009. All rights reserved.

Table 8. Static characteristics *...continued*

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 27 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{pd(RTH)}$	pull-down current on pin RTH	normal operating mode and failures 3 and 3a	-	75	-	µA
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature		155	165	180	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design, but only 100 % tested at T_{amb} = 125 °C for dies on wafer level, and above this for cased products 100 % tested at T_{amb} = 25 °C, unless otherwise specified.

[2] For bare die, all parameters are only guaranteed if the back side of the die is connected to ground.

[3] A local or remote wake-up event will be signalled at the transceiver pins RXD and $\overline{ERR}$ if V_{BAT} = 5.3 V to 27 V (see Table 5).

11. Dynamic characteristics

Table 9. Dynamic characteristics

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 27 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{t(r-d)}$	transition time for recessive to dominant (on pins CANL and CANH)	between 10 % and 90 %; R1 = 100 Ω; C1 = 10 nF; C2 = not present; see Figure 5	0.35	0.65	-	µs
$t_{t(d-r))}$	transition time for dominant to recessive (on pins CANL and CANH)	between 10 % and 90 %; R1 = 100 Ω; C1 = 10 nF; C2 = not present; see Figure 5	0.2	0.3	-	µs
$t_{PD(L)}$	propagation delay TXD (LOW) to RXD (LOW)	no failures and failures 1, 2, 5 and 6a; R1 = 100 Ω; see Figure 4 and Figure 5				
		C1 = 1 nF; C2 = not present	-	0.75	1.5	µs
		C1 = C2 = 3.3 nF	-	1	1.75	µs
		failures 3, 3a, 4, 6 and 7; R1 = 100 Ω; see Figure 4 and Figure 5				
		C1 = 1 nF; C2 = not present	-	0.85	1.4	µs
		C1 = C2 = 3.3 nF	-	1.1	1.7	µs
$t_{PD(H)}$	propagation delay TXD (HIGH) to RXD (HIGH)	no failures and failures 1, 2, 5 and 6a; R1 = 100 Ω; see Figure 4 and Figure 5				
		C1 = 1 nF; C2 = not present	-	1.2	1.9	µs
		C1 = C2 = 3.3 nF	-	2.5	3.3	µs
		failures 3, 3a, 4, 6 and 7; R1 = 100 Ω; see Figure 4 and Figure 5				
		C1 = 1 nF; C2 = not present	-	1.1	1.7	µs
		C1 = C2 = 3.3 nF	-	1.5	2.2	µs
t_r	bus line output rise time	between 10 % and 90 %; C1 = 10 nF; see Figure 5	-	0.6	-	µs
t_f	bus line output fall time	between 10 % and 90 %; C1 = 1 nF; see Figure 5	-	0.3	-	µs
$t_{react(sleep)}$	reaction time of goto sleep command	[4]	5	-	50	µs

© NXP B.V. 2009. All rights reserved.

Table 9. Dynamic characteristics *…continued*

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 27 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{dis(TxD)}$	disable time of TxD permanent dominant timer	normal operating mode; V_{TXD} = 0 V		0.75	-	4	ms
t_{CANH}	dominant time for remote wake-up on pin CANH	low power modes; V_{BAT} = 12 V	[4]	7	-	38	µs
t_{CANL}	dominant time for remote wake-up on pin CANL	low power modes; V_{BAT} = 12 V	[4]	7	-	38	µs
t_{WAKE}	required time on pin $\overline{WAKE}$ for local wake-up	low power modes; V_{BAT} = 12 V; for wake-up after receiving a falling or rising edge	[4]	7	-	38	µs
t_{det}	failure detection time	normal operating mode					
		failures 3 and 3a		1.6	-	8.0	ms
		failures 4, 6 and 7		0.3	-	1.6	ms
		low power modes; V_{BAT} = 12 V					
		failures 3 and 3a		1.6	-	8.0	ms
		failures 4 and 7		0.1	-	1.6	ms
t_{rec}	failure recovery time	normal operating mode					
		failures 3 and 3a		0.3	-	1.6	ms
		failures 4 and 7		7	-	38	µs
		failure 6		125	-	750	µs
		low power modes; V_{BAT} = 12 V					
		failures 3, 3a, 4 and 7		0.3	-	1.6	ms
n_{det}	pulse-count difference between CANH and CANL for failure detection	normal operating mode and failures 1, 2, 5 and 6a; pin $\overline{ERR}$ becomes LOW		-	4	-	
n_{rec}	number of consecutive pulses on CANH and CANL simultaneously for failure recovery	failures 1, 2, 5 and 6a		-	4	-	

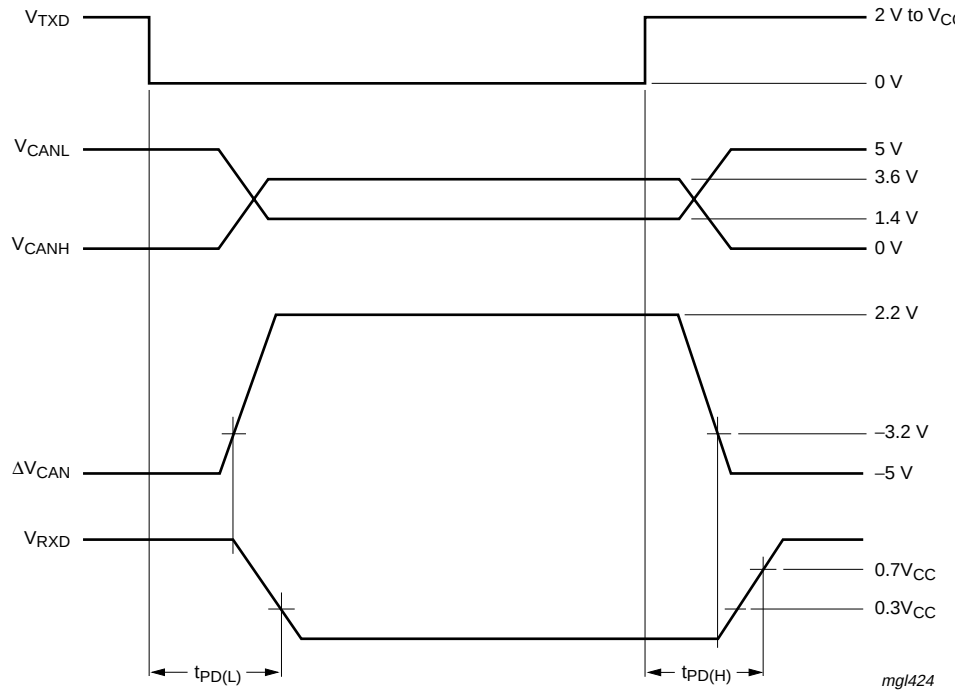
[1] All parameters are guaranteed over the virtual junction temperature range by design, but only 100 % tested at T_{amb} = 125 °C for dies on wafer level, and above this for cased products 100 % tested at T_{amb} = 25 °C, unless otherwise specified.

[2] For bare die, all parameters are only guaranteed if the back side of the die is connected to ground.

[3] A local or remote wake-up event will be signalled at the transceiver pins RXD and $\overline{ERR}$ if V_{BAT} = 5.3 V to 27 V (see Table 5).

[4] To guarantee a successful mode transition under all conditions, the maximum specified time must be applied.

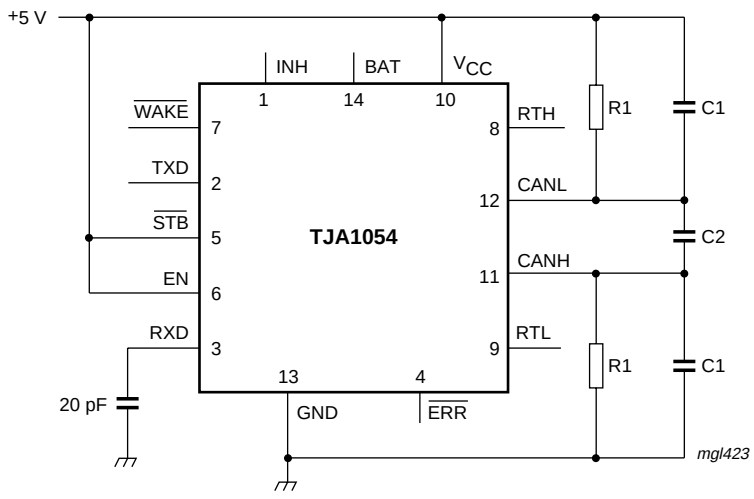
© NXP B.V. 2009. All rights reserved.



$V_{diff} = V_{CANH} - V_{CANL}$

Fig 4. Timing diagram for dynamic characteristics

12. Test information

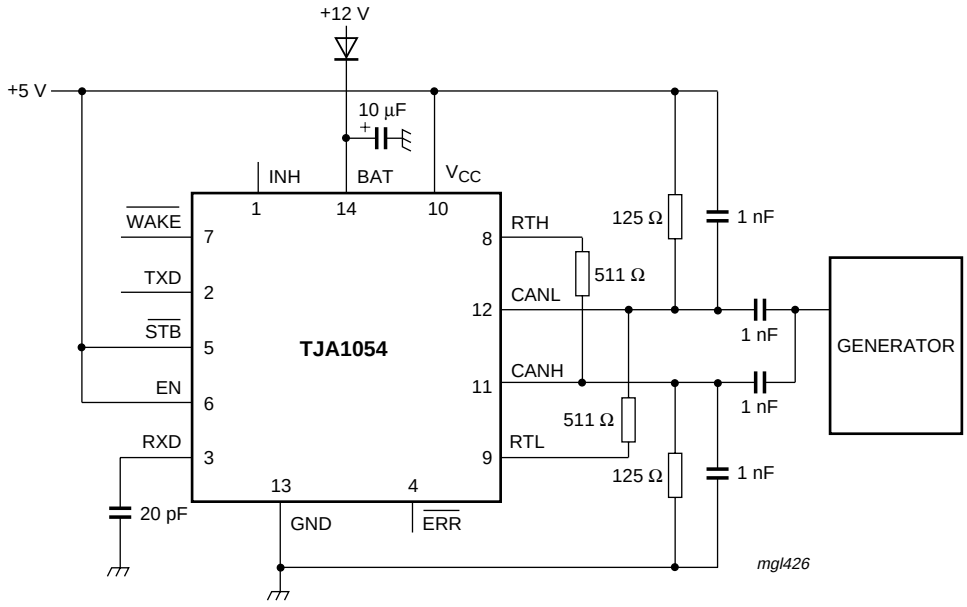


Termination resistors R1 (100 Ω) are not connected to pin RTH or pin RTL for testing purposes because the minimum load allowed on the CAN bus lines is 500 Ω per transceiver.

The capacitive bus load of 10 nF is split into 3 equal capacitors (3.3 nF) to simulate the bus cable.

Fig 5. Test circuit for dynamic characteristics

© NXP B.V. 2009. All rights reserved.



The waveforms of the applied transients on pins CANH and CANL will be in accordance with ISO 7637 part 1: test pulses 1, 2, 3a and 3b.

Fig 6. Test circuit for automotive transients

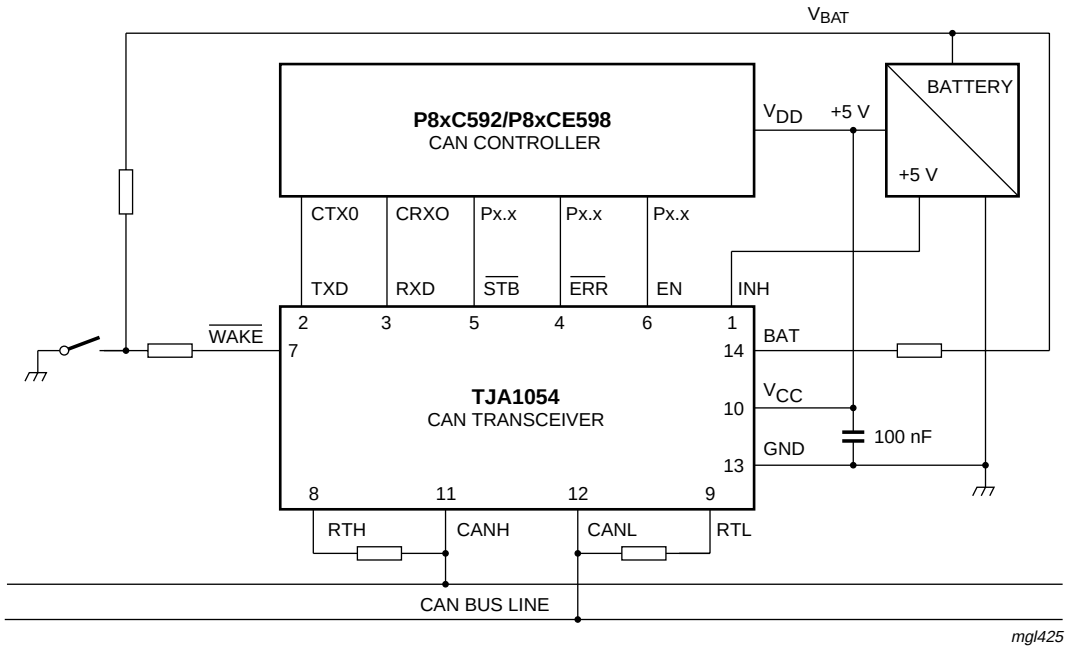


Fig 7. Application diagram

12.1 Quality information

This product has been qualified to the appropriate Automotive Electronics Council (AEC) standard Q100 or Q101 and is suitable for use in automotive applications.

© NXP B.V. 2009. All rights reserved.

13. Bare die information

Table 10. Bonding pad locations

Symbol	Pad	Coordinates[1]	
		x	y
INH	1	106	317
TXD	2	111	169
RXD	3	750	111
$\overline{ERR}$	4	1347	111
$\overline{STB}$	5	2248	103
EN	6	2521	240
$\overline{WAKE}$	7	2521	381
RTH	8	2550	1269
RTL	9	2359	1840
V_{CC}	10	1886	1809
CANH	11	872	1840
CANL	12	437	1840
GND	13a	80	1356
GND	13b	80	1241
BAT	14	106	772

[1] All coordinates (µm) represent the position of the center of each pad with respect to the bottom left-hand corner of the top aluminium layer (see Figure 8).

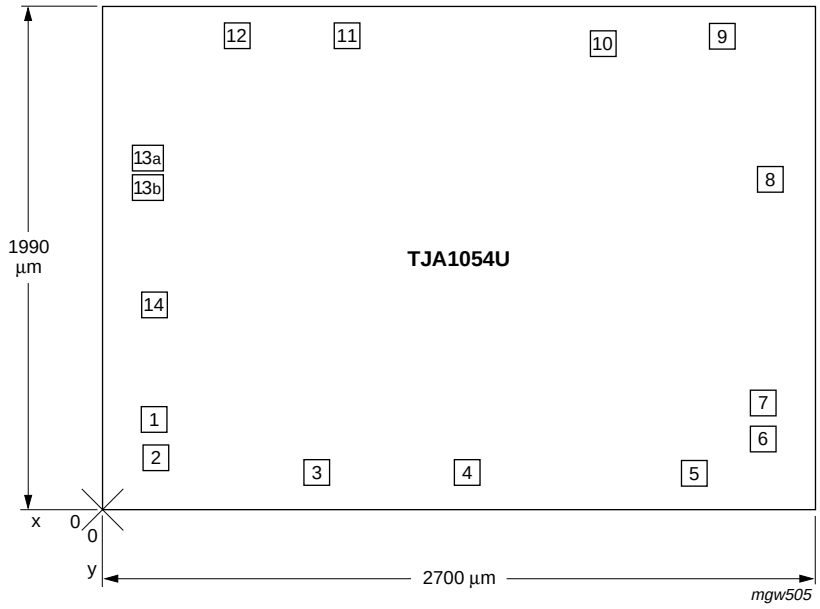
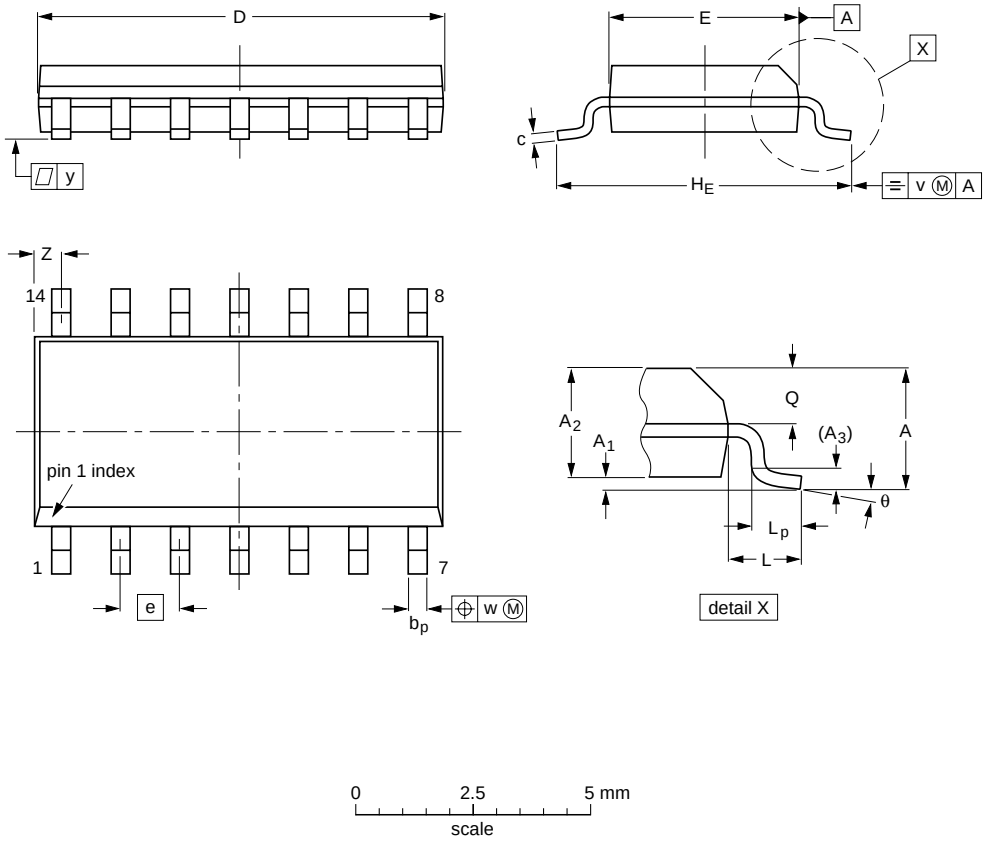


Fig 8. Bonding pad locations

© NXP B.V. 2009. All rights reserved.

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

© NXP B.V. 2009. All rights reserved.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

© NXP B.V. 2009. All rights reserved.

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

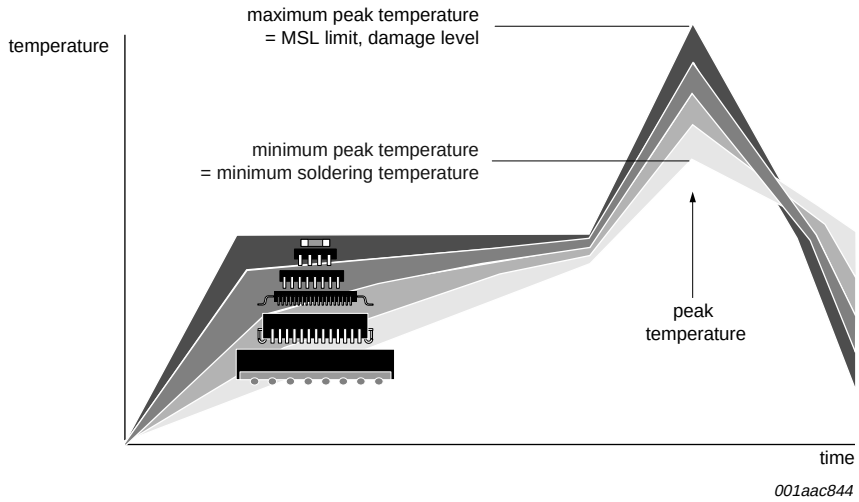
Table 12. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.

© NXP B.V. 2009. All rights reserved.



MSL: Moisture Sensitivity Level

Fig 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1054_4	20090924	Product data sheet	-	TJA1054_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Value of parameter V_{ESD} (machine model) changed in Table 6.			
TJA1054_3 (9397 750 11721)	20040323	Product specification	-	TJA1054_2
TJA1054_2 (9397 750 08965)	20011120	Product specification	-	TJA1054_1
TJA1054_1 (9397 750 03636)	19990211	Preliminary specification	-	-

© NXP B.V. 2009. All rights reserved.

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

17.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Bare die — All die are tested on compliance with their related technical specifications as stated in this data sheet up to the point of wafer sawing and are handled in accordance with the NXP Semiconductors storage and transportation conditions. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post-packing tests performed on individual die or wafers.

NXP Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, NXP Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

All die sales are conditioned upon and subject to the customer entering into a written die sale agreement with NXP Semiconductors through its legal department.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

© NXP B.V. 2009. All rights reserved.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2009. All rights reserved.

19. Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2009. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 24 September 2009
Document identifier: TJA1054_4

founded by

PHILIPS