Document Title
4Bank x 2M x 16bits Synchronous DRAM

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	Jul. 2009	Preliminary
1.0	Release	Aug. 2009	

DESCRIPTION

The Hynix H57V1262GFR series is a 134,217,728bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. H57V1262GFR series is organized as 4banks of 2,097,152 x 16.

H57V1262GFR is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a '2N' rule)

FEATURES

- Voltage: VDD and VDDQ 3.3V supply voltage
- All device pins are compatible with LVTTL interface
- 54 Ball FBGA (Lead or Lead Free Package)
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM, LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 Refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{CAS}$ Latency; 2, 3 Clocks
- Burst Read Single Write operation
- Operation temperature
  HY5V26F(L)F(P)-XX Series: 0 ~ 70°C
  HY5V26F(L)F(P)-X(I) Series: -40 ~ 85°C

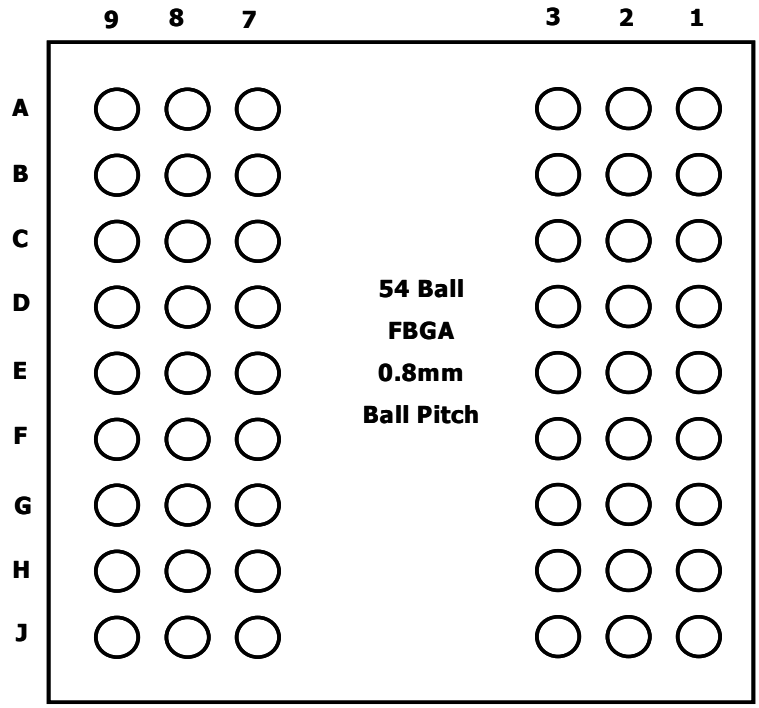
● **This product is in compliance with the directive pertaining of RoHS.**

ORDERING INFORMATION

Part No.	Clock Frequency	Organization	Interface	Package
H57V1262GFR-50X	200MHz	4Banks x 2Mbits x16	LVTTL	54 Ball FBGA
H57V1262GFR-60X	166MHz			
H57V1262GFR-70X	143MHz			
H57V1262GFR-75X	133MHz			

1. H57V1262GFR-XXC Series: Normal power, Commercial Temp.(0°C to 70°C)
2. H57V1262GFR-XXI Series: Normal power, Industrial Temp. (-40°C to 85°C)
3. H57V1262GFR-XXL Series: Low power, Commercial Temp.(0°C to 70°C)
4. H57V1262GFR-XXJ Series: Low power, Industrial Temp. (-40°C to 85°C)

BALL CONFIGURATION



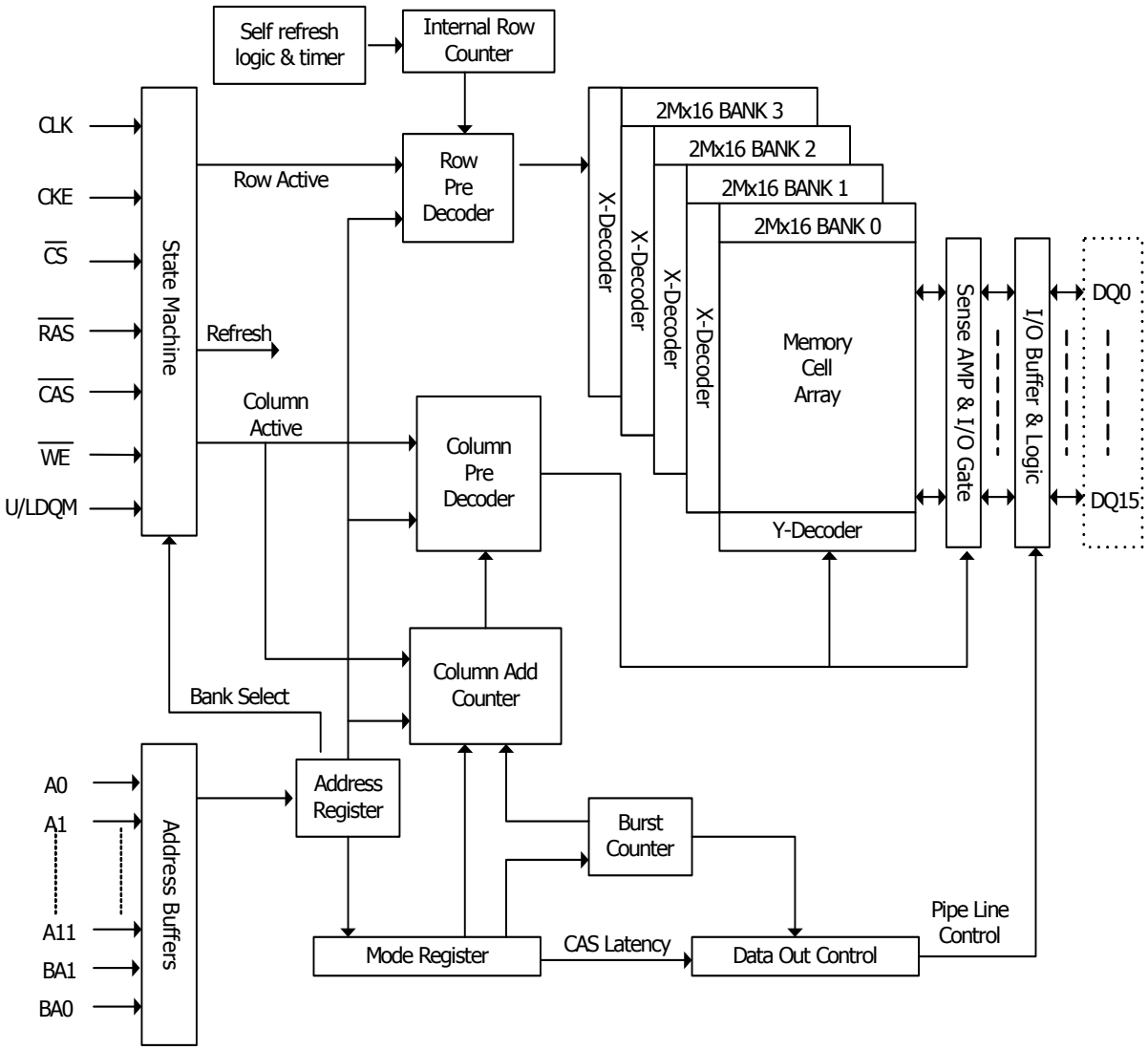
<Bottom View>

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	/CAS	/RAS	/WE
NC	A11	A9	G	BA0	BA1	/CS
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

< Top View >

FUNCTIONAL BLOCK DIAGRAM

2Mbit x 4banks x 16 I/O Synchronous DRAM



BASIC FUNCTIONAL DESCRIPTION

Mode Register

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	OP Code	0	0	CAS Latency			BT	Burst Length		

OP Code

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit	Note
Ambient Temperature	TA	0 ~ 70°C	°C	1
		-40 ~ 85°C	°C	2
Storage Temperature	TSTG	-55 ~ 125	°C	
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V	
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V	
Short Circuit Output Current	IOS	50	mA	
Power Dissipation	PD	1	W	
Soldering Temperature / Time	TSOLDER	260 / 10	°C / Sec	

Notes:
1. Commercial (0 ~ 70°C)
2. Industrial (-40 ~ 85°C)

DC OPERATING CONDITION

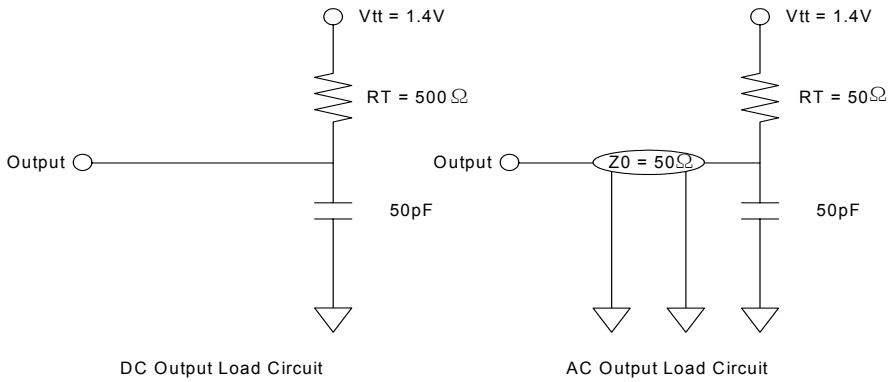
Parameter	Symbol	Min.	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High Voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1, 2
Input Low Voltage	VIL	-0.3	-	0.8	V	1, 3

Notes:
1. All voltages are referenced to VSS = 0V
2. VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
3. VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration

AC OPERATING TEST CONDITION (VDD=3.3±0.3V, VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4 / 0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note: 1.



DC Output Load Circuit AC Output Load Circuit

CAPACITANCE (f=1MHz, VDD=3.3V)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	2.0	4.0	pF
	A0 ~ A11, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, UDQM	CI2	2.0	4.0	pF
Data input / output capacitance	DQ0 ~ DQ15	CI/O	3.0	5.5	pF

DC CHARACTERISTICS I

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -2mA
Output Low Voltage	VOL	-	0.4	V	IOL = +2mA

Notes:

1. VIN = 0 to 3.3V, All other balls are not tested under VIN =0V
2. DOUT is disabled, VOUT=0 to 3.6

DC CHARACTERISTICS II

Parameter	Symbol	Test Condition		Speed				Unit	Note
				5	6	7	H		
Operating Current	I_{DD1}	Burst length=1, One bank active $t_{RC} \geq t_{RC}(min)$, I_{OL}=0mA		100	80	70	70	mA	1
Precharge Standby Current in Power Down Mode	I_{DD2P}	CKE ≤ V_{IL}(max), t_{CK} = 15ns		2				mA	
	I_{DD2PS}	CKE ≤ V_{IL}(max), t_{CK} = ∞		2				mA	
Precharge Standby Current in Non Power Down Mode	I_{DD2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CK} = 15ns Input signals are changed one time during 2clks. All other pins ≥ V_{DD}-0.2V or ≤ 0.2V		18				mA	
	I_{DD2NS}	CKE ≥ V_{IH}(min), t_{CK} = ∞ Input signals are stable.		15					
Active Standby Current in Power Down Mode	I_{DD3P}	CKE ≤ V_{IL}(max), t_{CK} = 15ns		5				mA	
	I_{DD3PS}	CKE ≤ V_{IL}(max), t_{CK} = ∞		5					
Active Standby Current in Non Power Down Mode	I_{DD3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CK} = 15ns Input signals are changed one time during 2clks. All other pins ≥ V_{DD}-0.2V or ≤ 0.2V		40				mA	
	I_{DD3NS}	CKE ≥ V_{IH}(min), t_{CK} = ∞ Input signals are stable.		35					
Burst Mode Operating Current	I_{DD4}	$t_{CK} \geq t_{CK}$(min), I_{OL}=0mA All banks active		120	100	100	100	mA	1
Auto Refresh Current	I_{DD5}	$t_{RC} \geq t_{RC}$(min), All banks active		210	200	190	190	mA	2
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V	Normal	2				mA	3
			Low power	800				uA	

Notes:

1. I_{DD1} and I_{DD4} depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II
3. H57V1262GTR-XXC Series: Normal Power
   H57V1262GTR-XXL Series: Low Power

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Sym-bol	5		6		7		H		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CL = 3	tCK3	5.0	1000	6.0	1000	7.0	1000	7.5	1000	ns	
	CL = 2	tCK2	-		-		-		10		ns	
Clock High Pulse Width		tCHW	1.75	-	2.0	-	2.0	-	2.5	-	ns	1
Clock Low Pulse Width		tCLW	1.75	-	2.0	-	2.0	-	2.5	-	ns	1
Access Time From Clock	CL = 3	tAC3	-	4.5	-	5.4	-	5.4	-	5.4	ns	2
	CL = 2	tAC2	-	-	-	-	-	-	-	6.0	ns	
Data-out Hold Time		tOH	2.0	-	2.0	-	2.5	-	2.7	-	ns	
Data-Input Setup Time		tDS	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
Data-Input Hold Time		tDH	0.8	-	0.8	-	0.8	-	0.8	-	ns	1
Address Setup Time		tAS	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
Address Hold Time		tAH	0.8	-	0.8	-	0.8	-	0.8	-	ns	1
CKE Setup Time		tCKS	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
CKE Hold Time		tCKH	0.8	-	0.8	-	0.8	-	0.8	-	ns	1
Command Setup Time		tCS	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
Command Hold Time		tCH	0.8	-	0.8	-	0.8	-	0.8	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1.0	-	1.0	-	1.5	-	1.5	-	ns	
CLK to Data Output in High-Z Time	CL = 3	tOHZ3	-	4.5	-	5.4	-	5.4	-	5.4	ns	
	CL = 2	tOHZ2	-	-	-	-	-	-	-	6.0	ns	

Notes:

1. Assume t_R / t_F (input rise and fall time) is 1ns. If t_R & t_F > 1ns, then [(t_R+t_F)/2-1]ns should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If t_R > 1ns, then (t_R/2-0.5)ns should be added to the parameter.

AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Symbol	5		6		7		H		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	55	-	60	-	63	-	63	-	ns	
$\overline{RAS}$ Cycle Time	Auto Refresh	tRRC	55	-	60	-	63	-	63	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	15	-	18	-	20	-	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	38.7	100K	42	100K	42	100K	42	120K	ns	
$\overline{RAS}$ Precharge Time		tRP	15	-	18	-	20	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	10	-	12	-	14	-	15	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	0	-	CLK	
Data-in to Precharge Command		tDPL	2	-	2	-	2	-	2	-	CLK	
Data-In to Active Command		tDAL	tDPL + tRP									
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	2	-	CLK	
Precharge to Data Output High-Z	CL = 3	tPROZ3	3	-	3	-	3	-	3	-	CLK	
	CL = 2	tPROZ2	-	-	-	-	-	-	2	-	CLK	
Power Down Exit Time		tDPE	1	-	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	ms	

Note:

1. A new command can be given tRRC after self refresh exit.

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Burst-Read-Single-WRITE		H	X	L	L	L	L	X	A9 ball High (Other balls OP code)			MRS Mode
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

PACKAGE INFORMATION

54 Ball FBGA 8.0mm x 8.0mm