

# Low-Noise Synchronous PWM Step-Down DC/DC Converter

### FEATURES

- Greater than 95% efficiency.
- Guaranteed output current of 800mA.
- 100% duty cycle in dropout.
- Fixed 500 KHz or adjustable frequency sychronous PWM operation.
- Very low quiescent current of 35µA (typ.).
- Adjustable output voltage from 0.75V to VIN, ranging from 2.5V to 5.5V.
- Accurate reference: 0.75V (±1.2%).
- Synchronizable external switching frequency up to 1MHz.
- Small 8-Pin MSOP package.

## APPLICATIONS

- PDAs.
- Handy-terminals.
- WLAN cards
- Cellular phones.
- CPU I/O supplies.
- Cordless phones.
- Notebook chipset supplies.
- Battery-operated devices (3 or 1 Li-Ion/NiMH/ NiCd Cells).

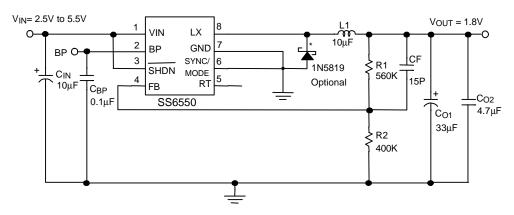
# TYPICAL APPLICATION CIRCUIT

### DESCRIPTION

The SS6550 is a low-noise pulse-widthmodulated (PWM) DC/DC step-down converter, which can power logic circuits and transmitters in small wireless systems such as communicating PDAs, cellular phones and handy-terminals.

The device features an internal synchronous rectifier for high conversion efficiency. Excellent noise characteristics and fixed-frequency operation provide easy post-filtering. The SS6550 is ideally suited for Li-Ion battery applications. It is also suitable for +3V or +5V fixed input applications. The device operates in one of the following four modes. Forced PWM mode operates at a fixed frequency regardless of the load. Synchronizable PWM mode allows the synchronization of an external switching frequency and minimizes harmonics. PWM/PFM Mode extends battery life by switching to a PFM pulse-skipping mode under light loads. Shutdown mode places the device in standby, reducing supply current to under 0.1µA.

The SS6550 can deliver over 800mA of output current. The output voltage can be adjusted from 0.75V to VIN with the input range of +2.5Vto +5.5V. Other features of the SS6550 include low quiescent current, low dropout voltage, and a  $\pm 1.2\%$  accuracy 0.75V reference. It is available in a space-saving 8-pin MSOP package.





## **ORDERING INFORMATION**

SS6550CX<u>XX</u>

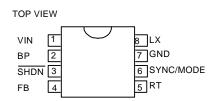
– PACKING TYPE TR: TAPE & REEL TB: TUBE

PACKAGE TYPE
 O: MSOP8

Example: SS6550COTR

→ in MSOP package in tape & reel

## **PIN CONFIGURATION**



## ABSOLUTE MAXIMUM RATINGS

VIN, BP, SHDN, SYNC/MODE, RT to GND	-0.3 to +6V
BP to VIN	0.3 to 0.3V
LX to GND	-0.3 to (V <sub>IN</sub> +0.3V)
FB to GND	-0.3 to (V <sub>BP</sub> +0.3V)
Operating Temperature Range	4000 0500
Storage Temperature Range	- 40°C ~ 150°C



# **ELECTRICAL CHARACTERISTICS** (V<sub>IN</sub>=+3.6V, T<sub>A</sub>=+25°C, SYNC/MODE =GND,

SHDN =IN, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V <sub>IN</sub>			2.5		5.5	
Output Adjustment Range	V <sub>OUT</sub>	(Note 1)		V <sub>REF</sub>		V <sub>IN</sub>	V
Feedback Voltage	$V_{FB}$			0.735	0.75	0.765	V
Line Regulation		Duty Cycle = 10	0% to 23%		+1		%
Load Regulation		I <sub>OUT</sub> = 0 to 800mA			-1.3		%/A
FB Input Current	I <sub>FB</sub>	V <sub>FB</sub> = 1.4V,		-50	0.01	50	nA
D sharrel On Desistance	<b>D</b>	I <sub>LX</sub> = 100mA	V <sub>IN</sub> = 3.6V		0.32	0.65	Ω
P-channel On-Resistance	P <sub>RDS(ON)</sub>		V <sub>IN</sub> = 2.5V		0.38		
N-channel On-Resistance	N <sub>RDS(ON)</sub>	I <sub>LX</sub> = 100mA	V <sub>IN</sub> = 3.6V		0.32	0.65	Ω
			$V_{IN} = 2.5V$		0.38		
P-channel Current-Limit Threshold				0.85	1.2	1.55	A
Quiescent Current		SYNC/MODE = GND, V <sub>FB</sub> = 1.4V, LX unconnected			35	70	μΑ
Shutdown Supply Current		SHDN       = LX = GND, includes LX       Ieakage current			0.1	1	μΑ
LX Leakage Current		$V_{IN} = 5.5V, V_{LX} = 0 \text{ or } 5.5V$		-20	0.1	20	μΑ
Oscillator Frequency	fosc			400	500	600	KHz
SYNC Capture Range				500		1000	KHz
Maximum Duty Cycle	duty <sub>MAX</sub>			100			%
Undervoltage Lockout Threshold	UVLO	V <sub>IN</sub> rising, typical hysteresis is 85mV		2.0	2.2	2.4	V
Logic Input High	VIH	SHDN , SYNC/MODE, LIM		2			V
Logic Input Low	V <sub>IL</sub>	SHDN , SYNC/MODE, LIM				0.4	V
Logic Input Current		SHDN, SYNC/MODE, LIM		-1	0.1	1	μA
SYNC/MODE Minimum Pulse Width		High or low		500			ns

Note 1: Specifications to -40°C are guaranteed by design, not production tested.



## **TYPICAL PERFORMANCE CHARACTERISTICS**

(T<sub>A</sub>=25°C, V<sub>IN</sub>=3.6V, SYNC/MODE=GND, L = Coilcraft DS1608C-103, unless otherwise noted.)

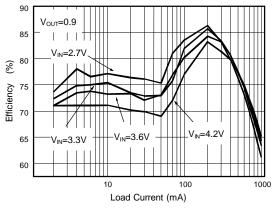
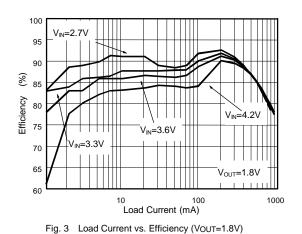


Fig. 1 Load Current vs. Efficiency (VOUT=0.9V)



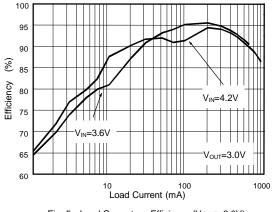
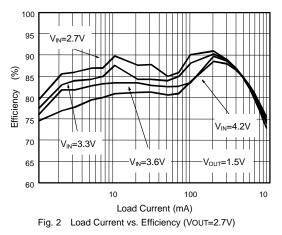
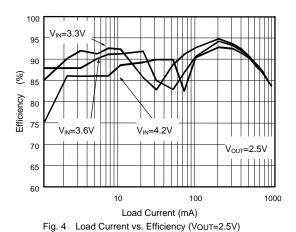
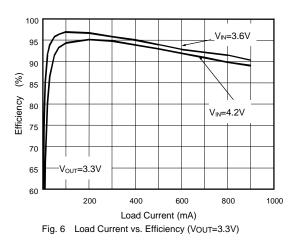


Fig. 5 Load Current vs. Efficiency (Vout=3.0V)









## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

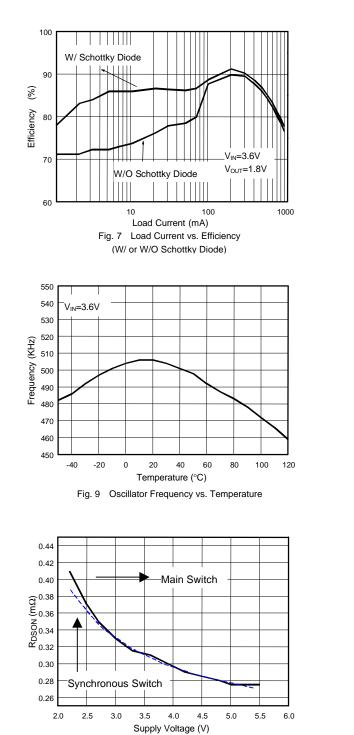
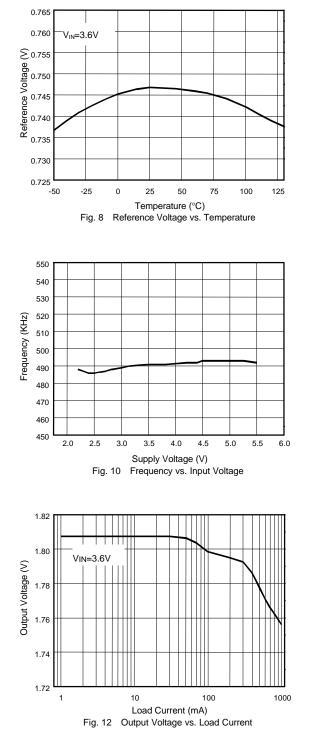


Fig. 11 RDSON vs. Supply Voltage





## **TYPICAL PERFORMANCE CHARACTERISTICS** (continued)

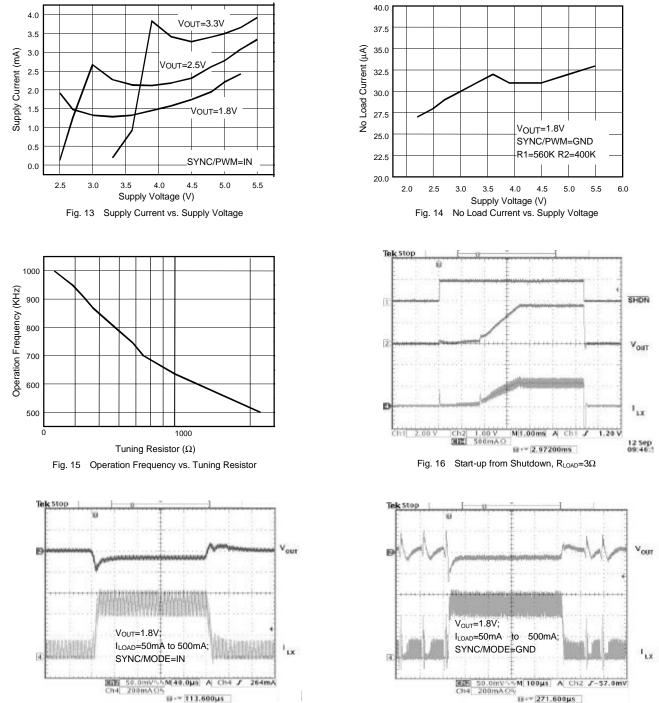
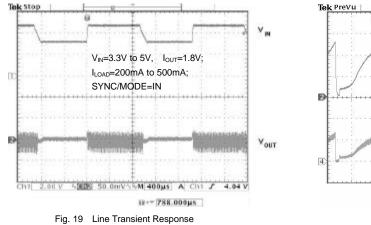


Fig. 17 Load Transient Response

Fig. 18 Load Transient Response



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)



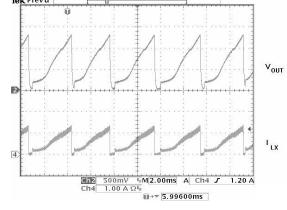
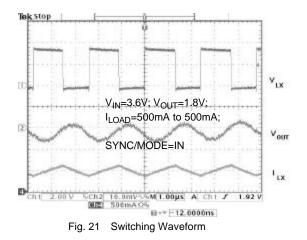
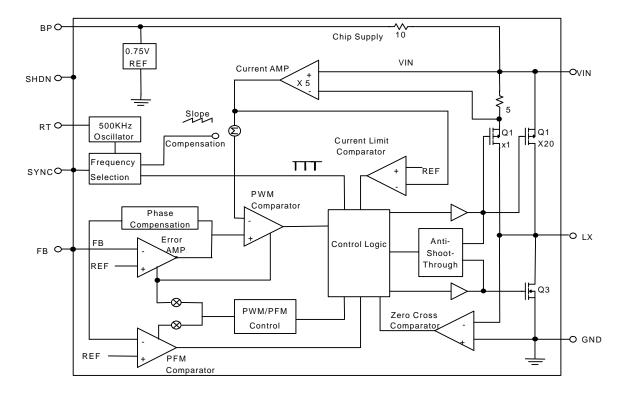


Fig. 20 Short Circuit Protection





## **BLOCK DIAGRAM**



### **PIN DESCRIPTIONS**

- PIN 1: VIN- Supply voltage input. Input range from +2.5V to +5.5V. Bypass with a 10µF capacitor.
- PIN 2: BP-Supply bypass pin, internally connected to VIN. Bypass with a 0.1µF capacitor. Do not connect to an external power source other than VIN.
- PIN 3: SHDN Active-low, shutdown-control input. Reduces supply current to 0.1µA in shutdown.
- PIN 4: FB- Feedback input.
- PIN 5: RT- Frequency adjustable pin. Connect a resistor from this pin to GND to decrease the frequency.

PIN 6: SYNC/M	ODE- Oscillator sync and low-noise, mode-control Input.
	SYNC/MODE = VIN (Forced PWM mode)
	SYNC/MODE = GND (PWM/PFM mode)
	An external clock signal connected to this pin allows for LX switching synchronization.
PIN 7: GND-	•

Inductor connection to the drains of

the internal power MOSFETs

PIN 8: LX-



## APPLICATION INFORMATION

#### Introduction

The SS6550 is a low-noise, pulse-width-modulated (PWM), DC/DC step-down converter. It features an internal synchronous rectifier, which eliminates the external Schottky diode. The SS6550 is suitable for Li-lon battery applications, or can be used with 3V or 5V fixed input voltages. It operates in one of the following four modes

- 1. The SS6550 can operate in PWM mode with a fixed frequency, regardless of its load.
- In synchronizable PWM mode, it allows an external switching frequency to control and minimize harmonics.
- In idle mode (PWM/PFM), it can extend battery life by switching to PFM pulseskipping mode during light loads.
- 4. In shutdown mode, the device will stop working and the supply current will reduce to  $0.1\mu A$  or less.

The continuous output current of the SS6550 can be up to 800mA and the output voltage can be adjusted from 0.75V to VIN with an input range from 2.5V to 5.5V using a voltage divider. The SS6550 also features high efficiency, low dropout voltage, and a 0.75V reference with  $\pm$ 1.2% accuracy. It is available in a space-saving 8-pin MSOP package.

#### Operation

When powered on, the control logic block detects whether the SYNC/MODE pin is connected to VIN or GND to determine the operation function and gives a signal to the PWM/PFM control block to determine the proper comparator (ref. Block Diagram). The SS6550 works with an internal synchronous rectifier Q3, to increase efficiency. When the control logic block turns Q2 on, Q3 will turn off through the anti-shortthrough block. Similarly, when Q3 is on, Q2 will turn off.

The SS6550 provides a current limit function by using a  $5\Omega$  resistor. When Q1 turns on, current flows through the  $5\Omega$  resistor and the current amplifier senses the voltage across the resistor and amplifies it. When the sensed voltage gets bigger than the reference voltage, the control logic shuts the device off.

#### **PWM/PFM Function**

When connecting the SYNC/MODE pin to VIN, the device is forced into the PWM (Pulse-Width-Modulated) mode with constant frequency. The advantage of constant frequency is that noise can be reduced easily without complex post-filtering. However, it has the disadvantage of low efficiency at light loading. Therefore, the SS6550 provides a function to solve this problem. When connecting the SYNC/MODE pin to GND, the device is able to get into PWM/PFM (Pulse-Frequency-Modulated) modes. Under a light load condition, the device shifts to PFM mode, which results in a higher efficiency. PWM mode is on under heavy loading and the noise is reduced.

#### **Frequency Synchronization**

Connecting an external clock signal to the SNYC/MODE pin can control the switching frequency. The acceptable range is from 500 kHz to 1 MHz. This mode exhibits low output ripple as well as low audio noise and reduces RF interference, while providing reasonable low current efficiency.

#### Adjustable Switching Frequency

The decrease of the switching frequency can also be controlled by connecting an external resistor from the RT pin to ground (ref. Fig. 15). In this mode, the PFM mode is disabled and the device operates with the adjusted frequency. This function is helpful in reducing high frequency harmonics and a post-filter can be easily designed for this function. However, there will be an increase in ripple voltage.



## **APPLICATION INFORMATION (cont.)**

#### 100% Duty Cycle Operation

When the input voltage approaches the output voltage, the converter continuously turns Q1 on. In this mode, the output voltage is equal to the input voltage minus the voltage-drop across Q1.

#### **Components Selection**

#### Inductor

The inductor selection depends on the operating frequency of the SS6550. The internal switching frequency is 500 kHz, and the external synchronized frequency ranges from 500 kHz to 1 MHz. A higher frequency allows the use of smaller inductor and capacitor values. However, higher frequency also results in lower efficiency due to the internal switching loss.

The ripple current  $\Delta I_L$  is related to the inductor value. A lower inductor value creates a higher ripple current. A higher V<sub>IN</sub> or V<sub>OUT</sub> can also create the same result. The inductor value can be calculated from the following formula:

$$= \frac{1}{(f)(\Delta I_L)} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \qquad \dots (1)$$

Users can define the acceptable ripple current to obtain a suitable inductor value.

#### **Output Capacitor**

The selection of output capacitor depends on the acceptable ripple voltage. Lower ripple voltage corresponds to lower ESR (equivalent-series-resistance) of the output capacitor. Typically, once the ESR is determined from the ripple voltage, the value of the capacitor is adequate for filtering. The formula for ripple voltage is:

$$\Delta V_{OUT} = \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

For more reduction in the ripple voltage, a 15pF ceramic capacitor can be used in parallel with the output capacitor.

#### **External Schottky Diode**

The SS6550 has an internal synchronous rectifier, instead of the Schottky diode usually found in a buck converter. However, a blank period occurs at each switching cycle when both the main switch, Q2, and the synchronous rectifier, Q3, are off. This results in a decrease in efficiency. Therefore, an external Schottky diode is needed to reinforce the efficiency.

Since the diode conducts during the off time, the peak current and voltage of the converter must not exceed the diode ratings. The ratings of the diode can be calculated from the following formulae:

$$\begin{split} V_{D,MAX(OFF)} &= V_{IN} \\ I_{D,MAX(ON)} &= I_{OUT,MAX} + \frac{\Delta I_L}{2} \\ I_{D,avg(ON)} &= I_{OUT} - I_{IN} = I_{OUT} - D \times I_{OUT} \\ &= (1 - D) \times I_{OUT} \end{split}$$

#### Adjustable Output Voltage

The SS6550 presents a 0.75V reference voltage at the FB pin. The output voltage, ranging from 0.75V to  $V_{IN}$ , can be set by connecting two external resistors, R1 and R2.  $V_{OUT}$  can be calculated as:

$$V_{OUT} = 0.75 V \times (1 + \frac{R1}{R2})$$

Applying a  $15\mu$ F capacitor in parallel with R1 can prevent stray pickup. This should sit as close to the SS6550 as possible. However, the load transient response is degraded by this capacitor.



## **APPLICATION INFORMATION (cont.)**

#### **Layout Consideration**

To ensure proper operation of the SS6550, the following points should be considered:

- 1. The input capacitor and VIN should be placed as close as possible to each other to avoid the AC current flow into the internal MOSFET.
- The output loop, which consists of the inductor, Schottky diode and output capacitor, should be kept as small as possible.
- 3. The routes carrying large currents should be kept short and wide.
- 4. Logically the large current of the converter, when SS6550 is on or off, should flow in the same direction.
- 5. The FB pin should connect to the feedback resistors directly, and the route should be away from any noise source, such as the inductance of the LX line.
- Grounding all components at the same point may effectively reduce the occurrence of loops. A stable ground plane is very important to obtain higher efficiency. When a ground plane is cut apart, it may cause disturbed signals and noise. If possible, two or three through-holes can ensure the stability of grounding. Fig.2 to 4 shows the layout diagrams of the SS6550.

#### Example

Here is an example to illustrate the components selection guide lines above. Let's assume the SS6550 is to be used for a mobile phone application, which uses a 1-cell Li-Ion battery with 2.7V to 4.2V input voltage for the power source. The required load current is 800mA, and the output voltage is 1.8V. Substituting  $V_{OUT}$ =1.8V,  $V_{IN}$ =4.2V, ripp1e=250mA, and f=500 kHz to equation (1)

$$L = \frac{1.8V}{500 \text{kHz} \times 250 \text{mA}} \left( 1 - \frac{1.8V}{4.2V} \right) = 8.23 \mu \text{H}$$

Therefore,  $10\mu$ H is appropriate for the inductor. The inductor, series number SLF6025-100M1R0 from TDK, with 57.3m $\Omega$  series resistance is recommended for the best efficiency.

For the output capacitor, the ESR is more important than its capacitance. Assuming ripple voltage of 100mV, then the ESR can be calculated as:

$$\mathsf{ESR} = \frac{\Delta \mathsf{V}}{\Delta \mathsf{I}} = \frac{100 \mathsf{mV}}{250 \mathsf{mA}} = 0.4 \Omega$$

Therefore, a  $33\mu$ F/10V capacitor, MCM series from NIPPON, is recommended.

Schottky selection is calculated as following.

$$V_{D,MAX(OFF)} = V_{IN} = 4.2V$$

$$I_{D,MAX(ON)} = I_{OUT,MAX} + \frac{\Delta I_{L}}{2}$$

$$= 800mA + \frac{250mA}{2}$$

$$= 925mA$$

I<sub>D,avg(ON)</sub>

$$= (1-D) \times I_{OUT}$$
  
=  $(1-\frac{1.8}{4.2}) \times 800$ mA  
= 457.14mA

According to the data above, the Schottky diode, SS12, from GS is recommended.

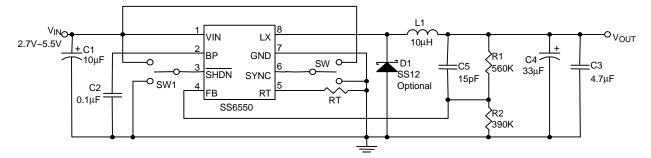
For feedback resistors, choose R2=390k $\Omega$ , and then R1 can be calculated as follow:

$$R1 = \left(\frac{1.8V}{0.75} - 1\right) \times 390k\Omega = 546k\Omega \text{ ; use } 560k\Omega$$

Fig. 22 shows this application circuit for the SS6550.



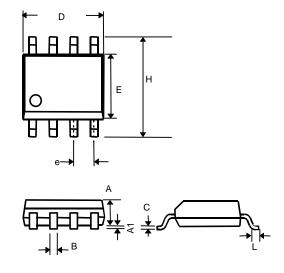
## APPLICATION INFORMATION (cont.)





### PHYSICAL DIMENSIONS

• MSOP 8 (unit: mm)



SYMBOL	MIN	MAX	
А	0.76	0.97	
A1		0.20	
В	0.28	0.38	
С	0.13	0.23	
D	2.90	3.10	
E	2.90	3.10	
е	0.65		
Н	4.80	5.00	
L	0.40	0.66	

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, express or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.