YAMAR Electronics Ltd
Preliminary *Data Sheet*

SIG40 for DC-LIN Asynchronous Communication Over Noisy Lines

This information is preliminary and may be changed without notice

1 GENERAL

The SIG40 is an innovative VLSI solution for digital communication over a single wire or a battery-powered line for asynchronous LIN and UART protocols, using original multiplex digital signaling technology. It provides a new economical physical communication layer for asynchronous protocols.

Since the SIG40 consists of CMOS technology, it can be economically integrated with other CMOS applications such as micro controllers.

When implemented in a LIN network, the SIG40 replaces the LIN transceiver and the LIN Data wire. Its 57.6Kbps data rate triples the LIN transfer rate. The SIG40 saves node costs and increases the network capacity. A sleep mode enables power saving. Wakeup messages on the DC line awaken remote devices as required by the LIN protocol.

The SIG40 capability of communicating over battery-powered line as a new physical layer of the LIN protocol is useful for a wide range of vehicular applications, such as doors, seats, mirrors, climate control, lights etc. The SIG40 contains a host and LIN interface, modem, line driver and ceramic filter interface.

The device features a unique Signaling technology to overcome the hostile communication conditions of a vehicle battery line. It consists of a Signaling Modem, Signaling Coder/Decoder and a Communication Controller overcoming the hostile environment over vehicle battery lines. Sleep mode reduces the power consumption when there is no bus activity.

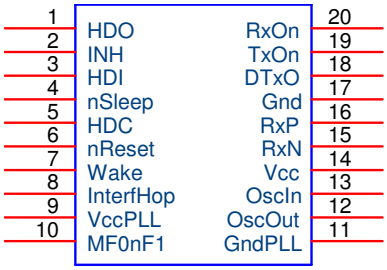

Figure 1.1 - SIG40 Pin Diagram

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2 OVERVIEW

2.1 Signaling System

The SIG40 device is based on a patented Signaling technology. The device transmits and receives a special signaling carrier, which can be differentiated from noise. The receiver receives the signaling patterns, extracting them into the original bits. The rest of the spectrum is reserved for additional communication channels over the same DC noisy lines.

2.2 Channels and Network

The SIG40 operates over one of two preset selectable channels (frequencies) using a single line such as the vehicle's battery power line. Up to 16 devices can be connected to each of the channels over the same line. Each of them can broadcast asynchronous data messages to other devices on the bus according to the LIN protocol. The device is controlled by its host microprocessor through its UART.

Channel frequencies: 3.58MHz to 6.5MHz
Data transfer rate: 19.2Kbps to 57.6Kbps.
Cable length: See 3.3.9.

2.3 The SIG40 Device

The SIG40 device is responsible to transfer messages to all devices over the line. The device handles the communication physical layer and Interference detection. The device communicates with its host via an asynchronous serial port for data transfer and device control. Figure 2.1 outlines the building blocks of the SIG40 device.

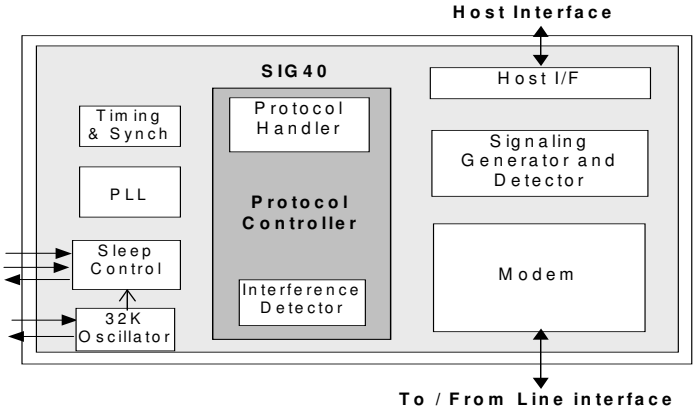


Figure 2.1 - SIG40 logical blocks

2.4 Protocol

The LIN protocol is based on a master device communicating with up to 15 slaves using half-duplex UART data. The device is transparent to the LIN host while providing additional services for the link and application layers with a built-in Interference detector and frequency management.

2.5 Power Management

Sleep Mode, controlled by the host, saves power by disabling most of the circuits.
During Sleep Mode, the device is switched On for a short period to detect wakeup messages from other devices on the bus. If no activity is detected, the device is switched back to Sleep.

3 SIG40 SIGNALS

The SIG40 Signals are divided into three main functions:

- Host input / output
- Line interface
- Sleep mechanism

Figure 3.1 describes the interconnections between SIG40 its host, the ceramic filters and the DC line.

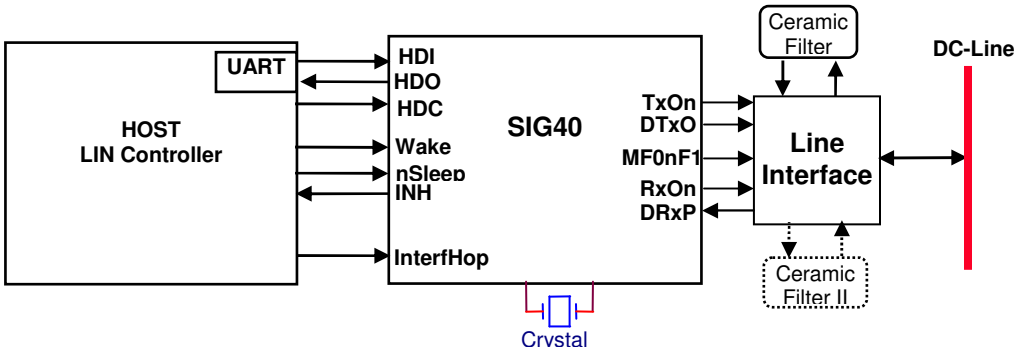


Figure 3.1 - Interfacing the SIG40

Device signals are defined in table 3.1.

Table 3.1 - Device signals

Host I/O signals

HDO	Data Output	1
INH	Inhibit operation Output	2
HDI	Data Input	3
nSleep	Sleep Input	4
HDC	Data/Command Input	5
nReset	Reset Input	6
Wake	Wakeup Input	7
InterfHop	Allow Interference hopping Input	8

Line Interface signals

MF0nF1	F0/F1 selected Output	10
OscOut	Crystal Output	12
OscIn	Crystal Input	13
RxN	Rx Analog - Input	15
RxP	Rx Analog + Input	16
DTxO	Transmit data Output	18
TxOn	Transmit On Output	19
RxOn	Receive On Output	20

Power signals

Vcc	Power	14
Gnd	Power	17
GndPLL	Ground for PLL	11
VccPLL	Vcc for PLL	9

3.1 Host interface

Three lines are dedicated for Host data input / output and for command.

3.1.1 HDI

Data input signal to the SIG40. Transfer data from host to SIG40. When not in use should be pulled Up.

3.1.2 HDO

Data output signal from SIG40. Transfers received data to host.

3.1.3 HDC

Data/Command mode. When Low, enables read and write to internal registers. When not in use should be pulled Up.

3.2 Sleep Mechanism

Three signals are dedicated for Sleep wakeup mechanism

3.2.1 nSleep

Sleep control input from the host. This pin is high for normal operation, and low for Sleep Mode. When not in use, this pin should be pulled Up.

3.2.2 Wake

Local wakeup input. Negative or positive edge wakes up the device. When not in use, this pin should be pulled Up or Down.

3.2.3 INH

Inhibit output for enabling the host (or an external voltage regulator powering the host. This output is LOW when in Sleep Mode, and HIGH in normal operation and after a wakeup event.

3.3 Line interface

Whenever a dual channel F0/F1 is required, the line interface is described in figure 3.2. It requires addition analog switch such as FSA157 and two transistors for Tx and Rx drivers.

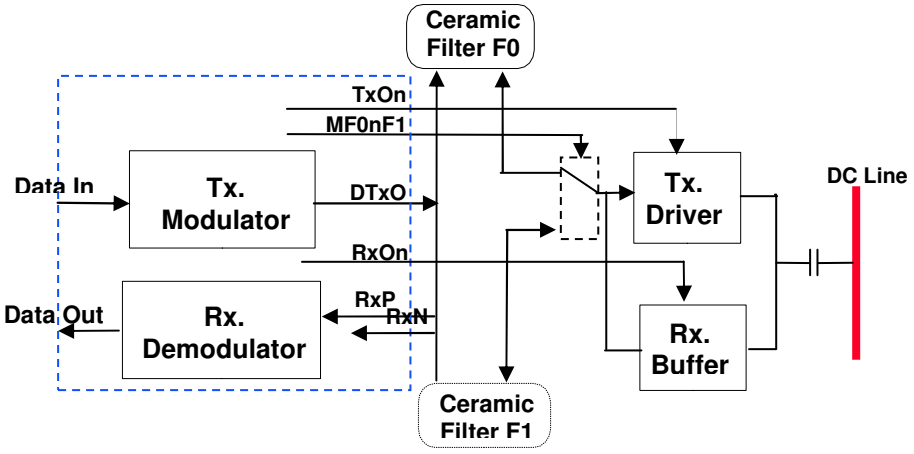


Figure 3.2 – DC - line interface block diagram

The line interface signals are:

3.3.1 DTxO

Modulated transmit signal output

3.3.2 TxOn

High when the device is transmitting

3.3.3 MF0nF1

Output signal indicates the selected channel. F0=”High”, F1= “Low”.

3.3.4 RxP

Comparator’s positive pin input signal. It swings around RxN.

3.3.5 RxN

Comparator’s negative pin input signal. Its value should be about Vcc/2.

3.3.6 RxOn

High when the device is in receive mode.

3.3.7 Power Signals

There are two sets of power signals, Vcc, Gnd and VccPLL, GndPLL. See 3.6

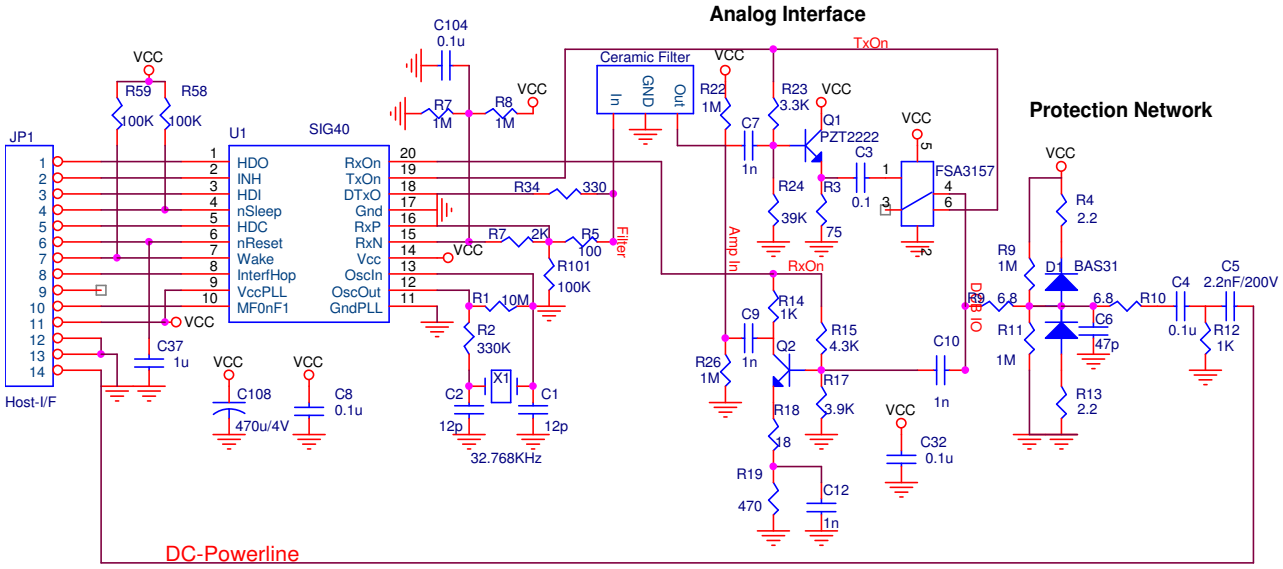


Figure 3.3 - Single channel line interface example

Notes: A SPST analog switch can replace FSA157.

3.3.8 Ceramic Filter Considerations

The SIG40 is designed to operate with one ceramic filter for transmission and reception. However, if switching between two channels is desired, two ceramic filters are required. The minimum allowable bandwidth of the ceramic filters is +/-70 kHz @ 3dB. Narrower bandwidth limits the maximal bit rate.

The SIG40 selectable frequencies are designed according to the market available ceramic filters.

Nominal freq.	3 db BW	20db BW	Insertion loss	Stop band attenuation	In/Out imped.	Murata part #	Oscilent part #
MHz	KHz min.	KHz max.	dB max.	dB min.	Ohm		
*3.58	+/-40	530	6.0	25	530	SFSH3.58MCB	
4.5	+/-70	750	6.0	30	1000	SFSL4.5MDB	773-0045
5.5	+/-80	750	6.0	30	600	SFSL5.5MDB	773-0055
6.0	+/-80	750	6.0	30	470	SFSL6.0MDB	773-0060
6.5	+/-80	800	6.0	30	470	SFSL6.5MDB	773-0065

* The 3.58MHz frequency can be operated at 19.2Kbps only.

3.3.9 Communication performance

The maximal cable length between extreme devices depends mainly on the AC impedance of loads connected to that line and number of nodes. The DC cable length has less effect on communication. The SIG40 needs at least 20mVpp for proper reception. Good communication should be achieved if the transmitted signal can be seen on an oscilloscope at the receiving side within the line noise.

3.4 Frequency Control

The device is designed for operation in two selectable carrier frequencies (channels).
Presence of an interference signal can be read from the device internal register.

3.4.1 Operating Frequency

Bit 0 in control register 0 determines the operating channel F1 or F0.

3.4.2 InterfHop

When high, the device switches its channel automatically whenever an interference signal is detected in the operating frequency. If the device did not receive any data in the new channel it will return to the previous channel after 2Sec. if, again, no data has been received for 2Sec. and the interference has stopped, it will switch frequency once more and will stay at the new channel.

3.4.3 MF0nF1

Output signal indicates the selected channel. F0="High", F1= "Low".

3.5 Crystal Oscillator

The SIG40 is designed to operate with a low cost 32.768KHz crystal connected between OscIn and OscOut pins. This type of crystal has the advantage of very low power consumption and low cost. However there are also drawbacks. It is very sensitive to noise and has a temperature dependency that should be carefully considered when selecting the crystal.

The following guidelines should be used when designing the PCB:

1. Design the trace length as short as possible.
2. Avoid thin line on resonator traces (< 0.010"), keep them as wide as possible.
3. To avoid noise, protect these signals with Ground shields.

The values of C1, C2 in Figure 3.3 oscillator circuitry should be determined according to the crystal manufacturer recommendations.

3.5.1 Recommended 32.768KHz Crystal Specifications

Type	Value
Nominal Frequency:	32.768KHz
Frequency tolerance @25ºC	+/-20 ppm
Load capacitance	12.5 pF
Serial resistance	50K Ohm (max.)
Drive level	1uW (max.)
Quality factor	50,000 (max.)
Turnover temperature	+25ºC +/- 5ºC
Parabolic constant	-0.04 ppm/ºC² (max.)
Aging	+/-3 ppm in first year (max.)
Operating temperature	-40ºC to + 85ºC
Storage temperature	-55ºC to + 125ºC

The overall frequency tolerance should not exceed 200ppm.

3.6 PLL Power Pins

VccPLL should be connected to Vcc. GndPLL should be connected to ground. The PLL supply has to be sufficiently powered, to avoid any fluctuations of power supply. A capacitor of at least 47uF should be connected as close as possible to these pins. It is recommended to keep the lines between 3.3V power supply and the Vcc pins as short as possible with wide PCB traces.

4 OPERATION

4.1 Message Construction

The host constructs a message from bytes of data sent to its UART. The device receives this data on its HDI data-In line. The 1st low input bit (start bit) starts the signaling transmission, and the 10th high bit (stop bit) stops the transmission. If all bits, including the 10th bit, are low, the transmission continues until a bit becomes high, but no more than 31-bit duration. It is considered as the Synch_Break Field of the LIN protocol. The stop bit stops the transmission unless a new byte is received from host. The total byte length does not change. The data latency between transmitter and receiver is about four bits.

4.1.1 LIN Protocol Messages

In order to comply with the LIN protocol, transmission of two kinds of bytes are allowed:

1. Bytes beginning with a start bit, followed by 8 bits and ending with a stop bit.
2. Bytes beginning with a start bit followed by a number of zeros ranging from 9 to 30 bits and ending with a stop bit.

4.1.2 Commanding the SIG40

Writing and reading to/from the internal Control registers (See 4.2) using write and read commands set the device behavior.

The registers are set by power-up Reset to operate at 19.2KBps, F0 = 5.5Mhz and F1 = 6.5Mhz. Writing into the registers allows changing the selectable frequencies, the bit rate, and the operating frequency. It also allows activating the automatic sleep feature and the automatic response to received bytes feature.

4.1.3 Transmit

Upon detection of a start bit in HDI, the SIG40 starts to transmit modulated signal to the DC line according to the set-up channel frequency and bit rate.

Note: *After transmission, it takes duration of 2 bits before the device starts to listen to the DC-line.*

4.1.4 Receive

When not transmitting, the SIG40 listens to the DC line in order to:

- Detect and decode a legal signaling pattern according to the setup channel and bit rate.
- In Sleep mode, the device detects wakeup messages.
- Detects Interference signals.

Note: *After transmission, it takes duration of 2 bits before the device starts to listen to the DC-line.*

4.2 Control Registers

4.2.1 Device operating parameters and statuses

The internal control registers shown in table 4.1 contain the device parameters and statuses:

Register 0

7	6	5	4	3	2	1	0
Interference			Sleep (“0”)				~F0/F1

Register 1

7	6	5	4	3	2	1	0
“1”	“1”	Bit rate		Select frequency (table 4.2)			

Table 4.1 - Device Control Registers

Address	Register Name	dir	bits	Description	Default
0[0]	F1/~F0	R/W	1	1 = F1, 0 = F0.	F0
0[1]	Remote loopback	R/W	1	Transmits back the last received byte	0
0[3:2]	For future use				00

0[4]	nAuto sleep	R/W	1	0 = Automatically enters into Sleep Mode when no reception from the DC line for 8 Sec.	1
0[6:5]	For future use				00
0[7]	Interference	R	1	Interference Detected indication	-
1[5:0]	F0, F1, bit rate select	R/W	6	See Tables 4.2 and 4.3	"FF"H
1[7:6]	For future use			Should be "11"	11

4.3 SIG40 Configuration

The SIG40 operates at default with the following parameters:
Bit rate: 19.2 kbps
F0=5.5MHz, F1=6.5MHz
The following configuration bits set the operating frequencies according to table 4.2.

Table 4.2 – F0, F1 select

Control_register1 (3:0)	F0	F1
0000	3.58Mhz	4.5Mhz
0001	3.58Mhz	5.5Mhz
0010	3.58Mhz	6Mhz
0011	3.58Mhz	6.5Mhz
0100	4.5Mhz	5.5Mhz
0101	4.5Mhz	6Mhz
0110	4.5Mhz	6.5Mhz
0111	4.5Mhz	Reserved
1000	Reserved	Reserved
1001	5.5Mhz	Reserved
1010	5.5Mhz	Reserved
1011	6Mhz	Reserved
1100	6Mhz	Reserved
1101	6.5Mhz	Reserved
1110	6.5Mhz	Reserved
1111	5.5Mhz	6.5Mhz

Table 4.3 – bit rates select

Control_register_1 (5:4)	01 = 57.6Kbps 10 = Reserved	00 = 38.4Kbps 11 = 19.2Kbps

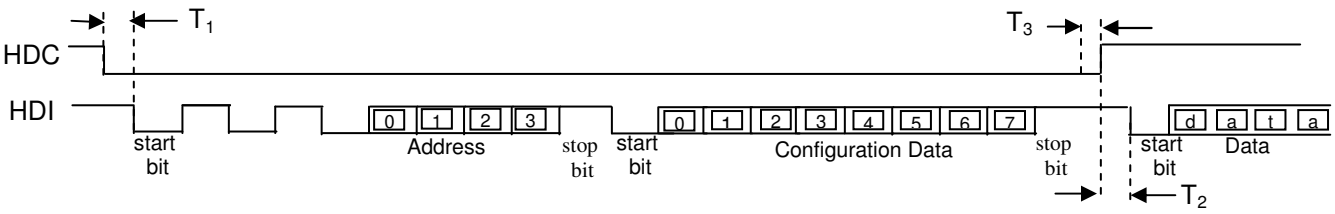
4.3.1 Command Mode

When in command mode, the host can configure the device according to the desired operating parameters. The device enters command mode when pin HDC is lowered to zero. When in command mode, data on the HDI pin is not transmitted to the bus, but is used to configure the SIG40. The command can be written in any of the allowed Bit Rates.
In order to write to a control register, the host sends two bytes. The first byte begins with the address of the register followed by 5(hex), and the second byte is the configuration data, as shown in figure 4.2. The bytes should be sent more than 200nSec after lowering HDC.

	Higher nibble [7:4]	**Lower nibble [3:0]**
First Byte	Register Address	5(hex)
Second Byte	Configuration Data	Configuration Data

Table 4.4 - Write Command

Figure 4.3 shows the pins involved in the writing process:



T_3>1/half bit rate

Figure 4.3 - Writing to a Control Register

In order to read from a control register, the host sends one byte. The byte should be sent more than 200nSec after lowering HDC. The byte begins with the address of the register followed by ”D”H. The SIG40 will then output the content of the register to pin HDO.

Read Command	Register Address[3:0]	D(hex)

Read Command

Figure 4.4 shows the pins involved in the reading process:

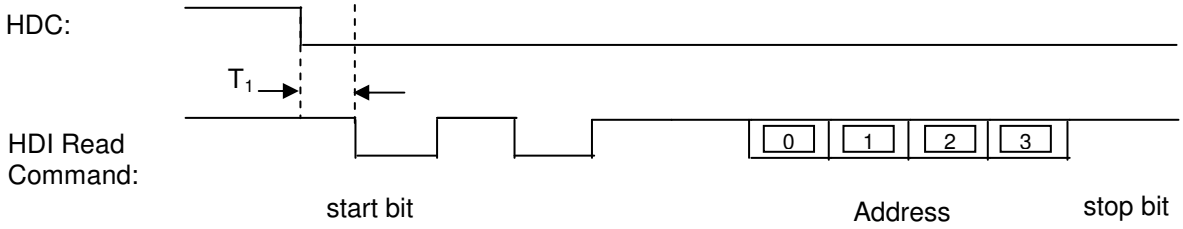


Figure 4.4 - Reading from a Control register

Note: Writing to Register 1

Writing a change frequencies command to register 1 is not always interpreted correctly by the device. The device will switch to the correct frequencies pair however, it will not function properly, resulting a communication lost.

Workaround: When changing frequencies by writing to register 1, use the following procedure:

Lower the H_DC.

Send a command to register 1 containing the require frequencies pair and a false bit rate.

Raise the H_DC

Lower the H_DC

Send a command to register 1 containing the require frequencies pair and the required bit rate.

Raise the H_DC.

For example, when wanting to work with frequencies 3.58MHz and 4.5MHz at 19.2Kbps the correct way to program the device is described in Figure 4.4.1

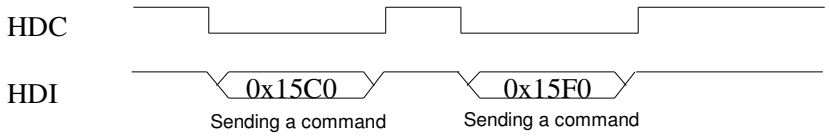


Figure 4.4.1 – Writing to Register

Note: Changing only the bit rate can be done with a single write, as described above.

4.4 Loopback

The device operates like a transceiver, therefor while transmitting or writing a command the HDI signal is looped back to the HDO pin.

4.5 Reset and Power-up

The device has internal Power-up reset. It takes 6mS until a stable operation is achieved from power-up, or from raising the nReset signal to high.

4.6 Sleep Mode

The device has three operation modes: Normal mode (normal transmitting and receiving), Sleep mode (power saving mode), and Standby mode (after waking up, while pin nSleep is low). Transitions between the modes are done via dedicated pins, or remotely, due to bus activity.

4.6.1 Entering Sleep mode

Host can move the device into Sleep mode from Normal mode either by a lowering to "0" (falling edge) pin nSleep or enabling the AutoSleep option (Setting Register 0 bit 4 to “0”). The device enters to Sleep mode and lowers output pin INH.
When AutoSleep option is enabled the device will enter Sleep mode if there was no reception from the bus for a period of 8 Sec. EVEN if the device is currently transmitting. The device must receive data from the bus in order to reset its internal autosleep timer. There are three ways to wakeup the device from Sleep mode.

4.6.2 Wakeup from pin nSleep

In this case, the host raises pin nSleep. The device then enters Normal mode and raises pin INH. The device automatically transmits a wakeup message to wakeup all other devices on the bus. While transmitting this wakeup message to the bus, the device lowers pin HDO. After the transmission is complete the device raises pin HDO (can be used to signal/interrupt the host). After the transmission is completed and pin nSleep is high, the device enters Normal mode. See Figure 4.5 for signals description.

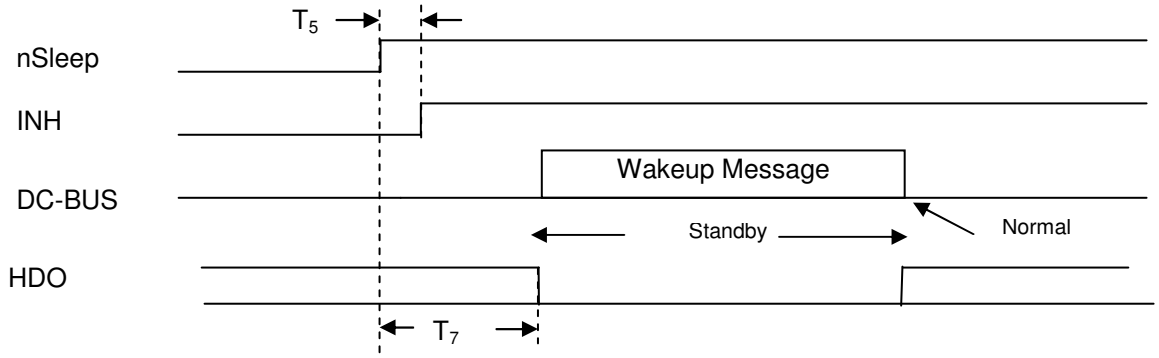


Figure 4.5 - Wakeup from nSleep

4.6.3 Wakeup from pin Wake

In this case, a transition on pin Wake (caused by an external switch of the application) is used to wake the device. The device then enters Standby mode, raises pin INH, and transmits a wakeup message to the bus. While transmitting the wakeup message to the bus, the device lowers pin HDO. After the transmission is complete the device raises pin HDO (can be used to signal/interrupt the host). After the transmission is completed and pin nSleep is high, the device enters Normal mode. The host has to raise the nSleep pin (otherwise the device will remain in Standby mode).

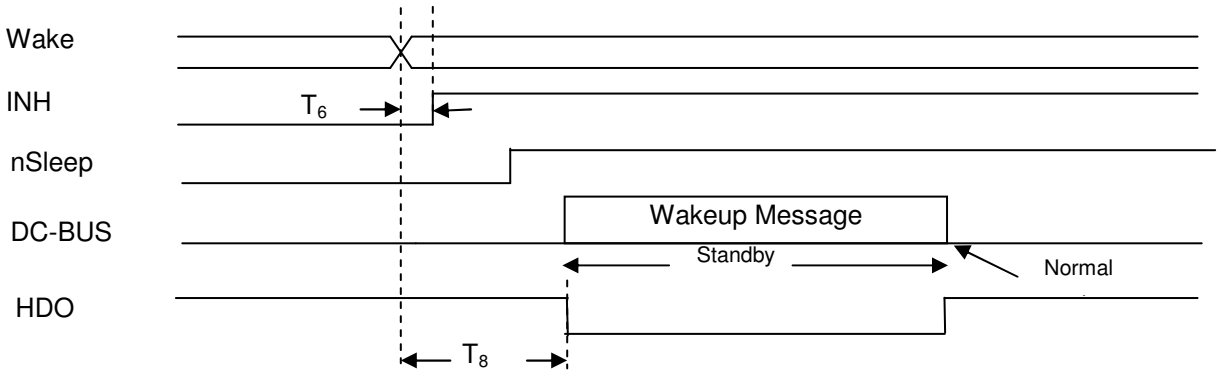


Figure 4.6 - Wakeup from Wake

4.6.4 Wakeup from bus message

During Sleep mode, the device wakes up periodically to check for activity on the bus every 32 mSec. If a wakeup message is detected, the device enters Standby mode and raises pin INH. The device then signals the host by lowering pin HDO for a minimal duration of 8 bits, and a maximal duration of about 150mSec. The host has to raise nSleep pin (otherwise the device will remain in Standby mode). After completing the reception, the device enters Normal mode. See Figure 4.7 for signals description.

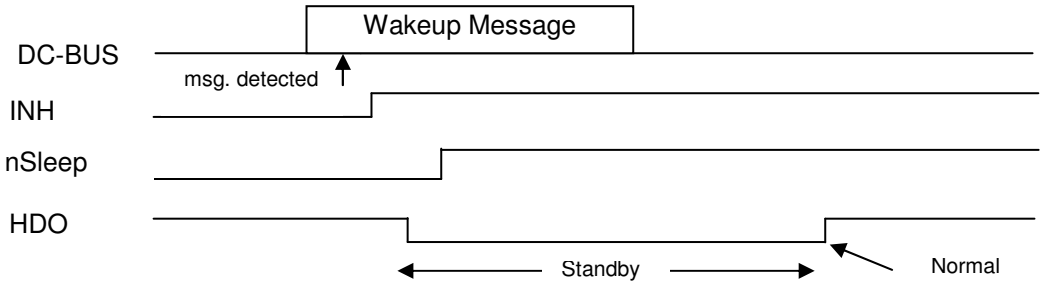


Figure 4.7 - Wakeup from bus message

4.7 Timing Characteristic

Symbol	Figure	Characteristics	Min	Max
T_1	4.3,4.4	Drop of HDC to drop of HDI	200nS	
T_2	4.3	Raise of HDC to drop of HDI	200nS	
T_3	4.3	Command stop bit to raise of HDC	Half bit rate	
T_4		Drop of nSleep to drop of INH	30uS	62uS
T_5	4.5	Raise of nSleep to raise of INH	30uS	62uS
T_6	4.6	Transact on Wake to raise of INH	30uS	62uS
T_7	4.5	Raise of nSleep to drop of HDO	92uS	124uS
T_8	4.6	Transact on Wake to drop of HDO	92uS	124uS
		Power Up or Reset to Normal mode		6mS

5 ELECTRICAL PARAMETERS

5.1 Absolute Maximal Rating

Ambient Temperature under bias	-40°C to 125°C
Storage Temperature	-55°C to 150°C
Input Voltage	-0.6V to Vcc+0.3V
Vcc Supply voltage	-0.3V to 4V

5.2 Electrical Operating Conditions

Symbol	Characteristics	Min	Typ	Max	Units	Conditions
Vcc	Supply Voltage	3.0	3.3	3.6	V	
Icc	Supply Current		35		mA	
Ipd	Power in Sleep mode			80	uA	

5.3 DC Electrical Characteristics

Symbol	Characteristics	Vcc	Typ	Units	Conditions
V_{IH}	Minimum high level input voltage	3.0	2.1	V	
V_{IL}	Maximum low level input voltage	3.0	0.9	V	
V_{OH}	Minimum high level output voltage	3.0	2.4	V	
V_{OL}	Minimum low level output voltage	3.0	0.4	V	
I_{IN}	Maximum input current	3.3	+/- 10	uA	

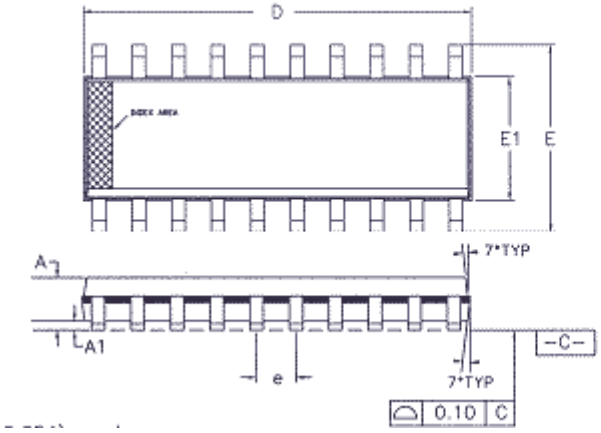
5.4 Operating Temperature

Commercial: 0°C to 70°C

Industrial: -40°C to 85°C

5.5 Package

20 lead SOP



SYMBOL	LEADS / TOL.	20 LEAD
A	MAX	2.65
A_1	MIN \ MAX	0.10 \ 0.30
D	MIN \ MAX	12.60 \ 13.00
E	MIN \ MAX	10.00 \ 10.65
E1	MIN \ MAX	7.44 \ 7.62
L	MIN \ MAX	0.40 \ 1.27
b	MIN \ MAX	0.33 \ 0.50
e	BASIC	1.27
ccc	MAX	0.25
JEDEC REF #		MS-013