Timing-Safe™ Peak EMI reduction IC

General Features

- Clock distribution with Timing-Safe™ Peak EMI Reduction
- Input frequency range: 20MHz - 50MHz
- Zero input - output propagation delay
- Low-skew outputs
  - Output-output skew less than 250pS
  - Device-device skew less than 700pS
- Less than 200pS cycle-to-cycle jitter
- Available in 16pin, 150mil SOIC, 4.4mm TSSOP (PCS5P23Z09B), and in 8pin, 150 mil SOIC, 4.4mm TSSOP Packages (PCS5P23Z05B)
- 3.3V Operation
- Industrial temperature range
- Advanced CMOS technology
- The First True Drop-in Solution

Functional Description

PCS5P23Z05B/09B is a versatile, 3.3V zero-delay buffer designed to distribute high-speed Timing-Safe™ clocks with Peak EMI Reduction. PCS5P23Z09B accepts one reference input and drives out nine low-skew clocks. It is available in a 16pin Package. The PCS5P23Z05B is the eight-pin version and accepts one reference input and drives out five low-skew clocks.

All parts have on-chip PLLs that lock to an input clock on the CLKIN pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad, internal to the device.

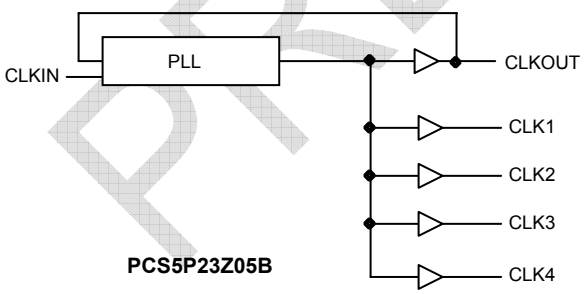
Multiple PCS5P23Z05B/09B devices can accept the same input clock and distribute it. In this case, the skew between the outputs of the two devices is guaranteed to be less than 700pS.

All outputs have less than 200pS of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than ±350pS, and the output-to-output skew is guaranteed to be less than 250pS.

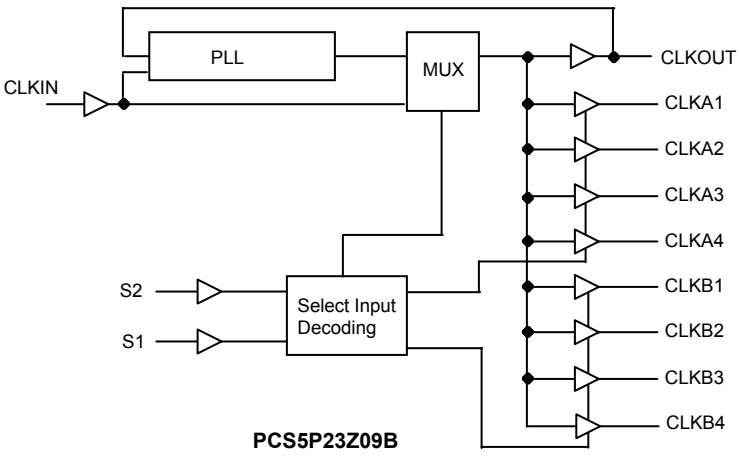
Refer "Spread Spectrum Control and Input-Output Skew Table" for deviations and Input-Output Skew for PCS5P23Z05B and PCS5P23Z09B devices

The PCS5P23Z05B and PCS5P23Z09B are available in two different packages, as shown in the ordering information table.

Block Diagram



PCS5P23Z05B



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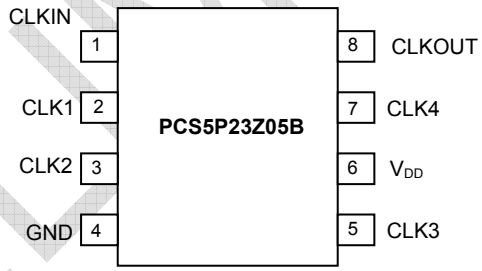
Spread Spectrum Frequency Generation

The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi-layer PCBs etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The PCS5P23Z05B/09B uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation

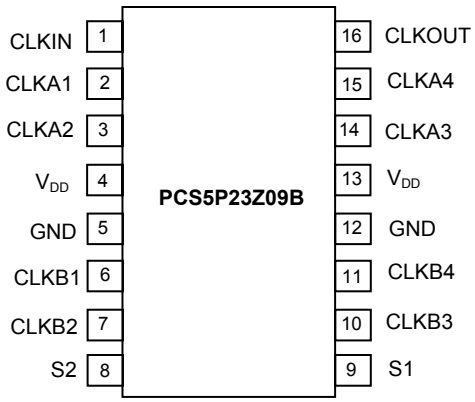
Timing-Safe™ technology

Timing-Safe™ technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Pin Configuration (8 Pin Device)



Pin Configuration (16 Pin Device)



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Pin Description for PCS5P23Z05B

Pin #	Pin Name	Description
1	CLKIN	Input reference frequency, 5V-tolerant input
2	CLK1[1]	Buffered clock output
3	CLK2[1]	Buffered clock output
4	GND	Ground
5	CLK3[1]	Buffered clock output
6	V_{DD}	3.3V supply
7	CLK4[1]	Buffered clock output
8	CLKOUT[1,2]	Buffered clock output, internal feedback on this pin

Notes: 1. Weak pull-down on these outputs.
2. This output is driven and has an internal feedback for the PLL.
3. All Buffered clock outputs are Timing-Safe™.

Pin Description for PCS5P23Z09B

Pin #	Pin Name	Description
1	CLKIN	Input reference frequency, 5V tolerant input
2	CLKA1[1]	Buffered clock output
3	CLKA2[1]	Buffered clock output
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1[1]	Buffered clock output
7	CLKB2[1]	Buffered clock output
8	S2[2]	Select Input, bit 2
9	S1[2]	Select Input, bit 1
10	CLKB3[1]	Buffered clock output
11	CLKB4[1]	Buffered clock output
12	GND	Ground
13	V_{DD}	3.3V supply
14	CLKA3[1]	Buffered clock output
15	CLKA4 [1]	Buffered clock output
16	CLKOUT[1,3]	Buffered output, Internal feedback on this pin

Notes: 1. Weak pull-down on all outputs.
2. Weak pull-up on these Inputs.
3. This output is driven and has an internal feedback for the PLL.
4. All Buffered clock outputs are Timing-Safe™.

Spread Spectrum Control and Input-Output Skew Table

(Note: The values given in the table are for an input frequency of 32MHz)

Device	Deviation	Input-Output Skew($\pm T_{SKEW}$)
PCS5P23Z05B	±0.25 %	0.125
PCS5P23Z09B	±0.25 %	0.125

Note: T_{SKEW} is measured in units of the Clock Period

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions for PCS5P23Z05B and PCS5P23Z09B Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	+85	°C
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for PCS5P23Z05B and PCS5P23Z09B

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage[1]				0.8	V
V_{IH}	Input HIGH Voltage[1]		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V			50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}			100	µA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8mA			0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = -8mA	2.4			V
I_{DD}	Supply Current	Unloaded outputs		15		mA
Z_o	Output Impedance			23		Ω

Note: 1. CLKIN input has a threshold voltage of $V_{DD}/2$
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

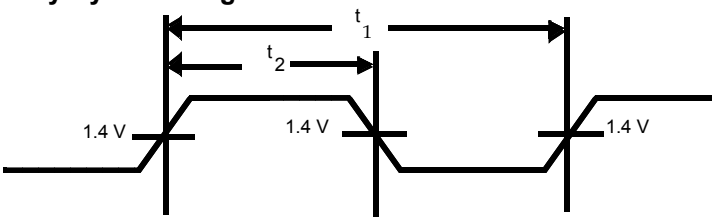
Switching Characteristics for PCS5P23Z05B and PCS5P23Z09B

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Output Frequency	30pF load	20		50	MHz
	Duty Cycle [2] = (t_2 / t_1) * 100	Measured at $V_{DD}/2$	40	50	60	%
t_3	Output Rise Time[1, 2]	Measured between 0.8V and 2.0V			2.5	nS
t_4	Output Fall Time[1, 2]	Measured between 2.0V and 0.8V			2.5	nS
t_5	Output-to-output skew [2]	All outputs equally loaded			250	pS
t_6	Delay, CLKIN Rising Edge to CLKOUT Rising Edge [2]	Measured at V_{DD} /2			±350	pS
t_7	Device-to-Device Skew [2]	Measured at $V_{DD}/2$ on the CLKOUT pins of the device			700	pS
t_J	Cycle-to-cycle jitter [2]	Loaded outputs			200	pS
t_{LOCK}	PLL Lock Time [2]	Stable power supply, valid clock presented on CLKIN pin			1.0	mS

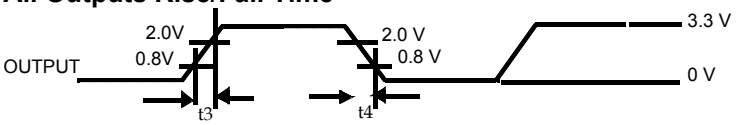
Note: 1. The parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

Switching Waveforms

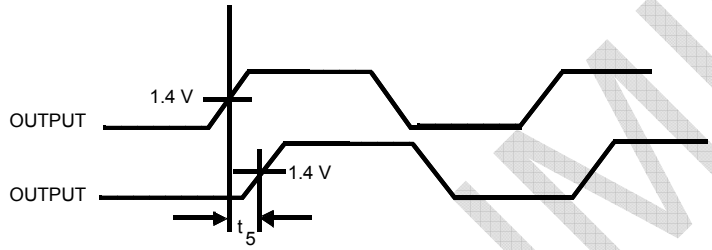
Duty Cycle Timing



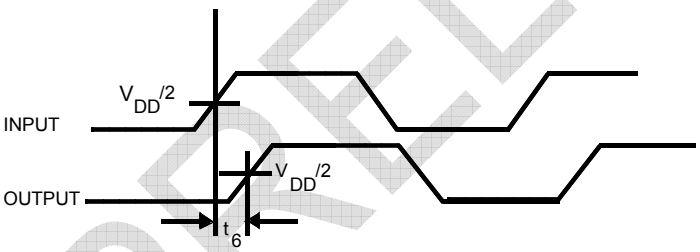
All Outputs Rise/Fall Time



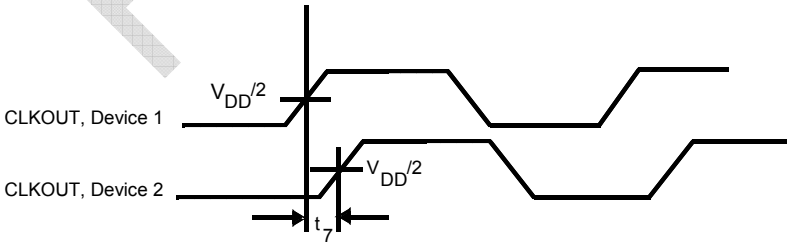
Output - Output Skew



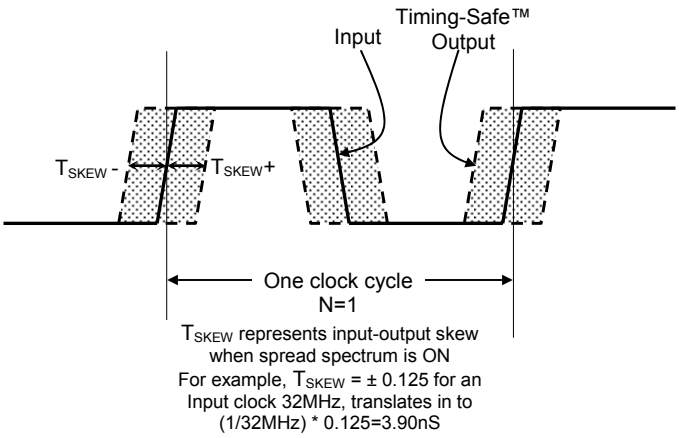
Input - Output Propagation Delay



Device - Device Skew

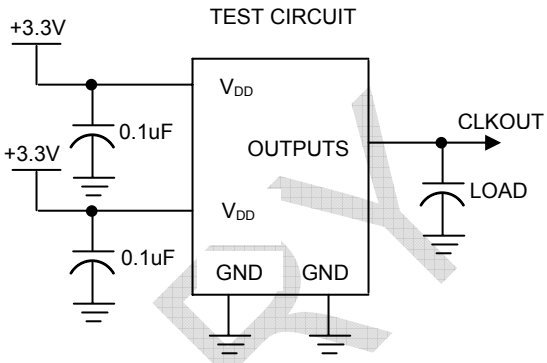


Input-Output Skew

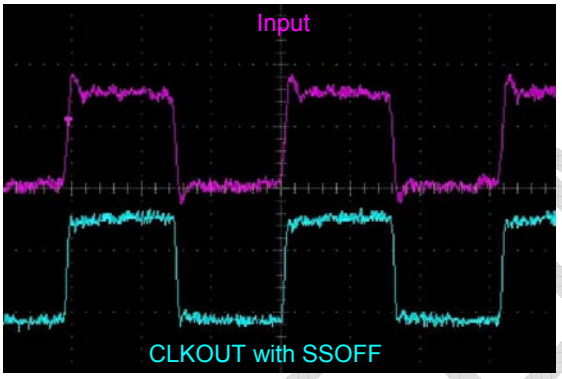


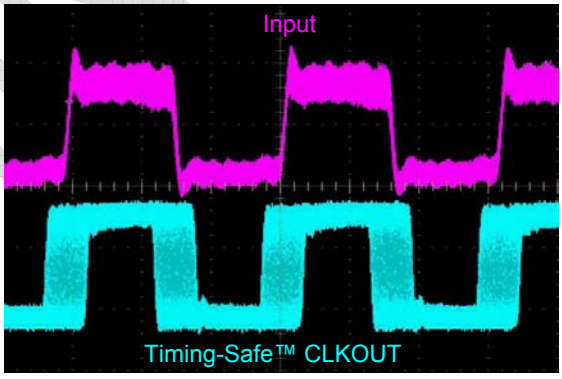
T_{SKEW} represents input-output skew when spread spectrum is ON
For example, T_{SKEW} = ± 0.125 for an Input clock 32MHz, translates in to (1/32MHz) * 0.125=3.90nS

Test Circuit



A Typical example of Timing-Safe™ waveform





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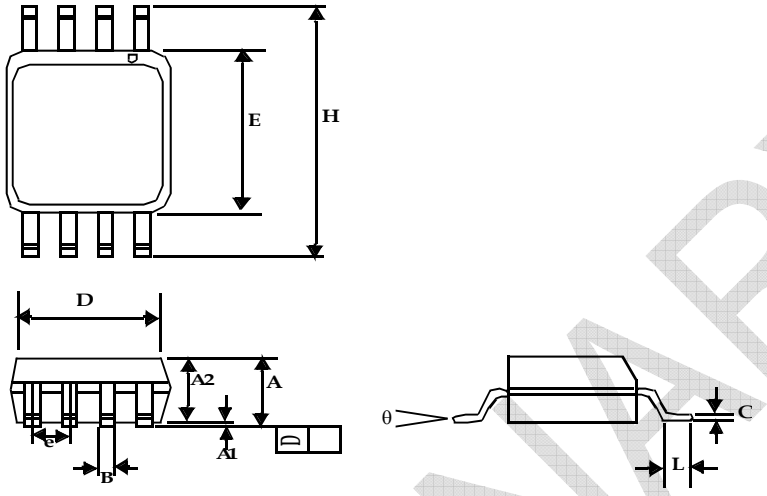
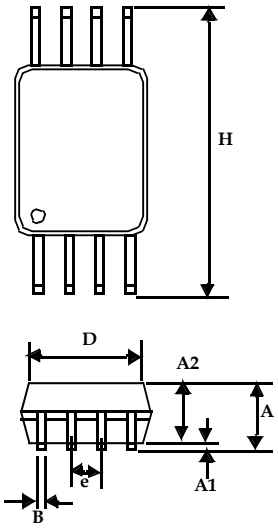
Package Information

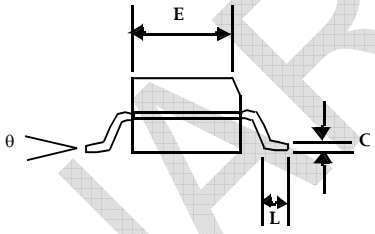
8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

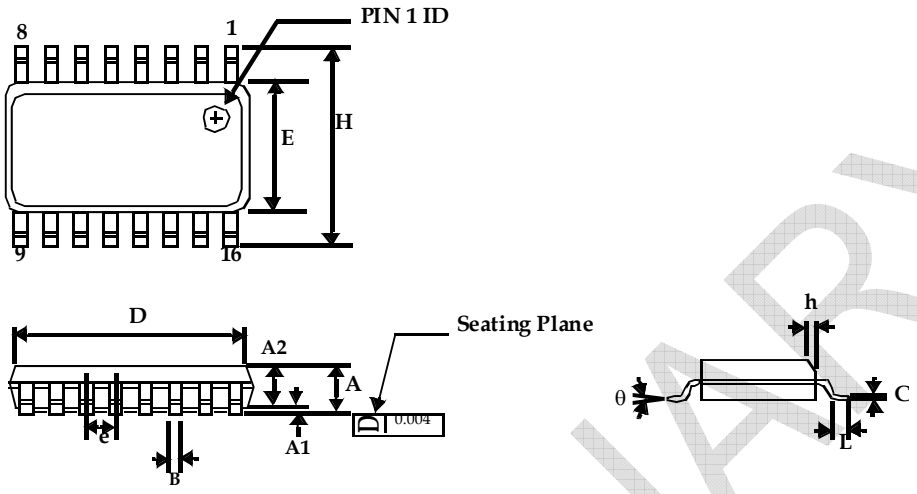
8-lead TSSOP (4.40-MM Body)





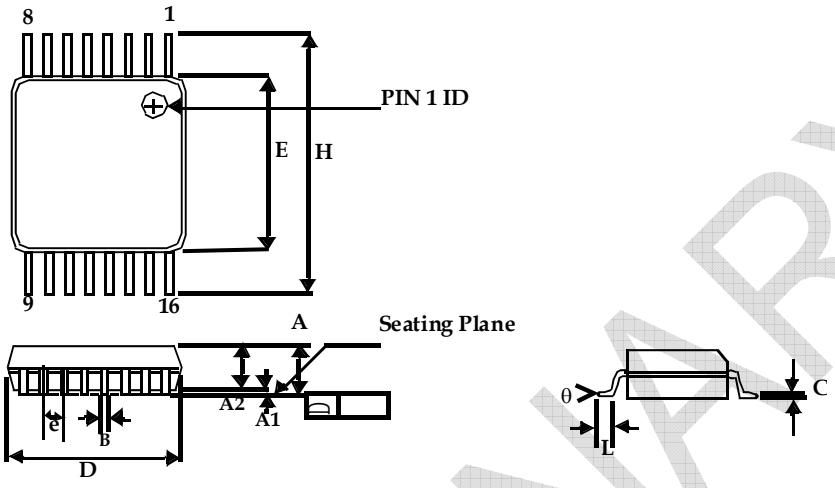
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

16-lead (150 Mil) Molded SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.013	0.022	0.33	0.53
C	0.008	0.012	0.19	0.27
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.40	0.89
θ	0°	8°	0°	8°

16-lead TSSOP (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.030	0.50	0.75
θ	0°	8°	0°	8°

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Ordering Codes

Ordering Code	Marking	Package Type	Temperature
PCS5P23Z09BF-16-ST	5P23Z09BF	16-pin 150-mil SOIC-TUBE, Pb Free	Commercial
PCS5I23Z09BF-16-ST	5I23Z09BF	16-pin 150-mil SOIC-TUBE, Pb Free	Industrial
PCS5P23Z09BF-16-SR	5P23Z09BF	16-pin 150-mil SOIC-TAPE & REEL, Pb Free	Commercial
PCS5I23Z09BF-16-SR	5I23Z09BF	16-pin 150-mil SOIC-TAPE & REEL, Pb Free	Industrial
PCS5P23Z09BF-16-TT	5P23Z09BF	16-pin 4.4-mm TSSOP - TUBE, Pb Free	Commercial
PCS5I23Z09BF-16-TT	5I23Z09BF	16-pin 4.4-mm TSSOP - TUBE, Pb Free	Industrial
PCS5P23Z09BF-16-TR	5P23Z09BF	16-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Commercial
PCS5I23Z09BF-16-TR	5I23Z09BF	16-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Industrial
PCS5P23Z05BF-08-ST	5P23Z05BF	8-pin 150-mil SOIC-TUBE, Pb Free	Commercial
PCS5I23Z05BF-08-ST	5I23Z05BF	8-pin 150-mil SOIC-TUBE, Pb Free	Industrial
PCS5P23Z05BF-08-SR	5P23Z05BF	8-pin 150-mil SOIC-TAPE & REEL, Pb Free	Commercial
PCS5I23Z05BF-08-SR	5I23Z05BF	8-pin 150-mil SOIC-TAPE & REEL, Pb Free	Industrial
PCS5P23Z05BF-08-TT	5P23Z05BF	8-pin 4.4-mm TSSOP - TUBE, Pb Free	Commercial
PCS5I23Z05BF-08-TT	5I23Z05BF	8-pin 4.4-mm TSSOP - TUBE, Pb Free	Industrial
PCS5P23Z05BF-08-TR	5P23Z05BF	8-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Commercial
PCS5I23Z05BF-08-TR	5I23Z05BF	8-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Industrial
PCS5P23Z09BG-16-ST	5P23Z09BG	16-pin 150-mil SOIC-TUBE, Green	Commercial
PCS5I23Z09BG-16-ST	5I23Z09BG	16-pin 150-mil SOIC-TUBE, Green	Industrial
PCS5P23Z09BG-16-SR	5P23Z09BG	16-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
PCS5I23Z09BG-16-SR	5I23Z09BG	16-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
PCS5P23Z09BG-16-TT	5P23Z09BG	16-pin 4.4-mm TSSOP - TUBE, Green	Commercial
PCS5I23Z09BG-16-TT	5I23Z09BG	16-pin 4.4-mm TSSOP - TUBE, Green	Industrial
PCS5P23Z09BG-16-TR	5P23Z09BG	16-pin 4.4-mm TSSOP - TAPE & REEL, Green	Commercial
PCS5I23Z09BG-16-TR	5I23Z09BG	16-pin 4.4-mm TSSOP - TAPE & REEL, Green	Industrial
PCS5P23Z05BG-08-ST	5P23Z05BG	8-pin 150-mil SOIC-TUBE, Green	Commercial
PCS5I23Z05BG-08-ST	5I23Z05BG	8-pin 150-mil SOIC-TUBE, Green	Industrial
PCS5P23Z05BG-08-SR	5P23Z05BG	8-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
PCS5I23Z05BG-08-SR	5I23Z05BG	8-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
PCS5P23Z05BG-08-TT	5P23Z05BG	8-pin 4.4-mm TSSOP - TUBE, Green	Commercial
PCS5I23Z05BG-08-TT	I23Z05BG	8-pin 4.4-mm TSSOP - TUBE, Green	Industrial
PCS5P23Z05BG-08-TR	5P23Z05BG	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	Commercial
PCS5I23Z05BG-08-TR	5I23Z05BG	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	Industrial

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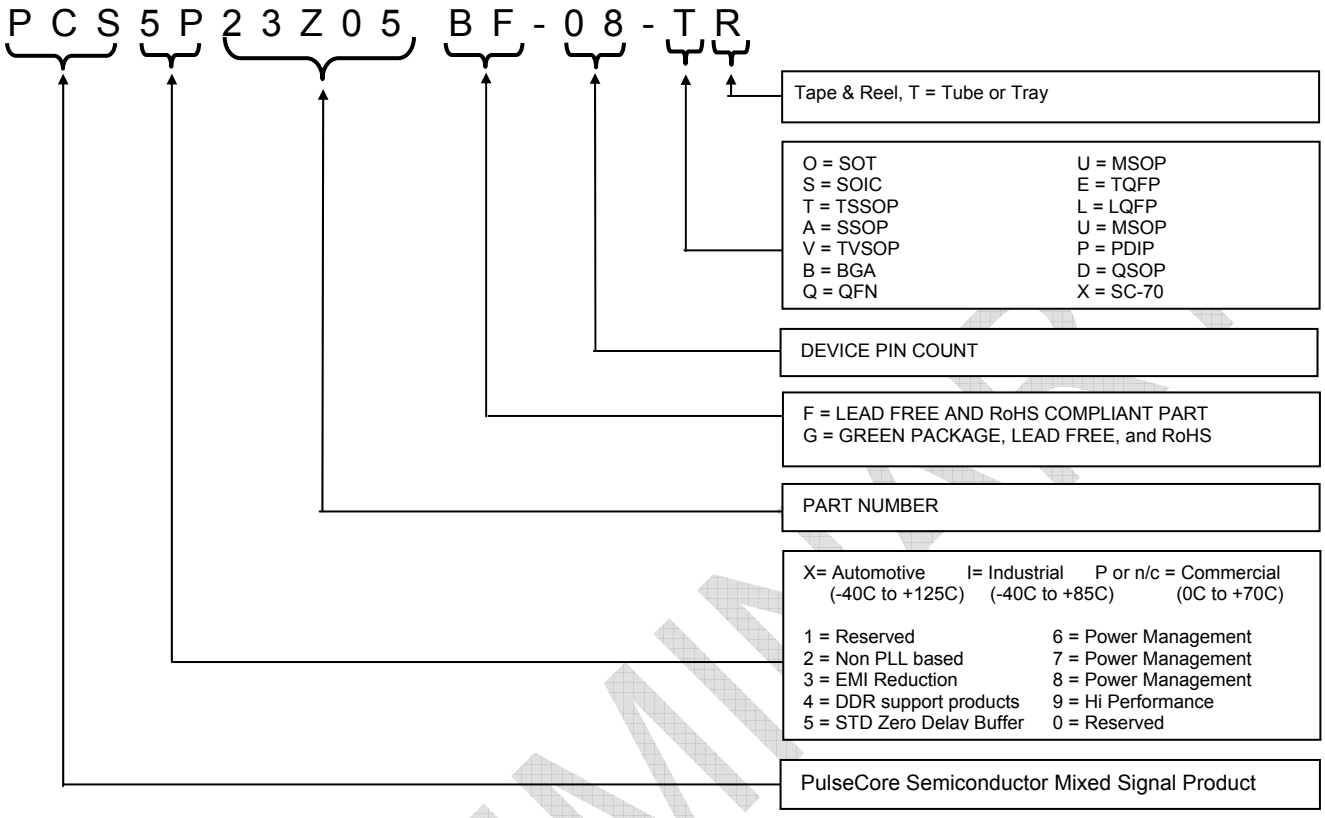
Device Ordering Information



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Preliminary Information
Part Number: PCS5P23Z05B/09B
Document Version: 0.2

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Timing-Safe™ US Patent Pending.