

September 2006 Giving you the edge PCS2P5T915A

rev 0.2

Low Voltage (2.5V) High Accuracy 1:5 Clock Fan-Out Buffer

Features

- Very low Output Skew: < 25 pS (max)
- Very low Duty Cycle Distortion: 300 pS (max)
- Low Propagation delays : 2nS (max)
- DC to 250MHz Operating Range
- Very low Power Consumption
- Hot insertable
- Over-Voltage Tolerant Inputs
- Very Low Cycle to cycle Jitter
- 2.5V Supply Voltage
- Isolated Output Power (VDDQ)
- 3 level inputs for selectable interface
- Selectable Inputs: HSTL, eHSTL, 1.8V/2.5V LVTTL or LVPECL
- Available in Standard 48 pin TSSOP Package
- Lead Free Option

Product Description

The PCS2P5T915A is a versatile user configurable/selectable 2.5V differential buffer for fanout and distribution of a high accuracy clock reference source. Accepting either a single ended or a differential

input, the PCS2P5T915A replicates the input to 10 outputs organised as output pairs for differential signalling.

The PCS2P5T915A performs as a translator or converter for a differential HSTL, eHSTL, 1.8V/2.5V LVTTL or CMOS, LVPECL or single ended 1.8V/2.5V LVTTL or CMOS inputs to HSTL, eHSTL, 1.8V/2.5V LVTTL outputs A user interface for configuration/selection is controlled via a three level input that can be wired or conditioned for the appropriate low-mid-high levels. In addition, the PCS2P5T915A true or complementary outputs may be asynchronously enabled and/or disabled. Multiple power pins for power and and returns guarantee the low skews and high accuracy.

Applications

- High Accuracy Clock Signal Fan-out and Distribution
- Specialty Synchronous Memory Clock Support
- Data Communications

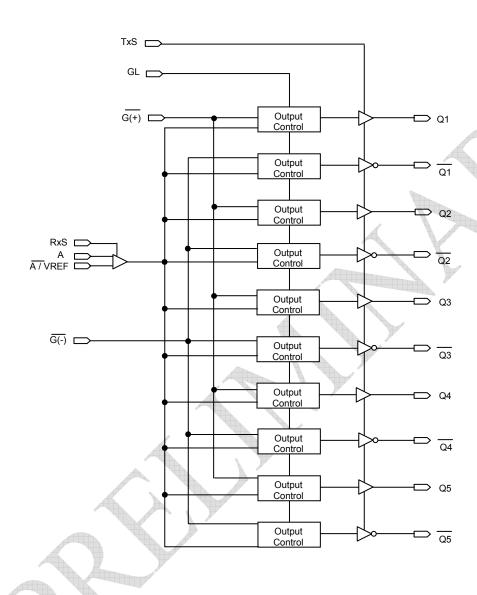
Switches

Routers

Hubs.

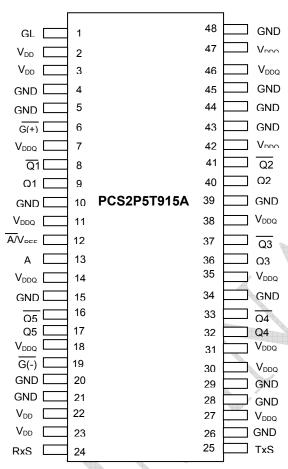


PCS2P5T915A Functional Block Diagram





Pin Configuration



Absolute Maximum Ratings¹

Notes: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. V_{DDQ} and V_{DD} internally operate independently. No power sequencing requirements need to be met.

3. Not to exceed 3.6V.

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage ²	-0.5 to +3.6	V
V_{DDQ}	Output Power Supply ²	-0.5 to +3.6	V
Vı	Input Voltage	-0.5 to +3.6	V
Vo	Output Voltage ³	-0.5 to V _{DDQ} +0.5	V
V_{REF}	Reference Voltage ³	-0.5 to +3.6	V
T _{STG}	Storage Temperature	-65 to +165	° C
TJ	Junction Temperature	150	° C

Capacitance^{1,2} (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Тур	Max	Unit
C _{IN}	Input Capacitance		3.5		pF

Notes: 1. This parameter is measured at characterization but not tested.

2. Capacitance applies to all inputs except RxS and TxS.



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Recommended Operating Range

Symbol	Description	Min	Тур	Max	Unit
T _A	Ambient Operating Temperature	-40	+25	+85	° C
V_{DD}^{1}	Internal Power Supply Voltage	2.4	2.5	2.6	V
	HSTL Output Power Supply Voltage	1.4	1.5	1.6	V
V_{DDQ}^{1}	Extended HSTL and 1.8V LVTTL Output Power Supply Voltage	1.65	1.8	1.95	V
	2.5V LVTTL Output Power Supply Voltage		V_{DD}		V
V_T	Termination Voltage		V _{DDQ} / 2		V

Note: 1. All power supplies should operate in tandem. If V_{DD} or V_{DDQ} is at maximum, then V_{DDQ} or V_{DD} (respectively) should be at maximum, and vice-versa.

Pin Description

Pin Descr	iptioi	1	
Symbol	I/O	Туре	Description
Α	I	Adjustable ¹	Clock input. A is the "true" side of the differential clock input. If operating in single-ended mode, A is the clock input.
ĀV _{REF}	1	Adjustable ¹	Complementary clock input. \overline{A}/V_{REF} is the "complementary" side of A if the input is in differential mode. If operating in single-ended mode, \overline{A}/V_{REF} is connected to GND. For single-ended operation in differential mode, \overline{A}/V_{REF} should be set to the desired toggle voltage for A: 2.5V LVTTL $V_{REF} = 1250 \text{mV}$ 1.8V LVTTL, eHSTL $V_{REF} = 900 \text{mV}$ HSTL $V_{REF} = 750 \text{mV}$ LVEPECL , $V_{REF} = 1082 \text{mV}$
G(+)	I	LVTTL ⁵	Gate control for "true", Qn, outputs. When $\overline{G(+)}$ is LOW, the "true" outputs are enabled. When $\overline{G(+)}$ is HIGH, the "true" outputs are asynchronously disabled to the level designated by GL^4 .
G (-)	ı	LVTTL ⁵	Gate control for "complementary", \overline{Qn} , outputs. When $\overline{G(-)}$ is LOW, the "complementary" outputs are enabled. When $\overline{G(-)}$ is HIGH, the "complementary" outputs are asynchronously disabled to the opposite level as GL^4 .
GL	1	LVTTL ⁵	Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH.
Qn	0	Adjustable ²	Clock outputs
Qn	0	Adjustable ²	Complementary clock outputs
RxS	I	3 Level ³	Selects single-ended 2.5V LVTTL (HIGH), 1.8V LVTTL (MID) clock input or differential (LOW) clock input
TxS	I	3 Level ³	Sets the drive strength of the output drivers to be 2.5V LVTTL (HIGH), 1.8V LVTTL (MID) or HSTL (LOW) compatible. Used in conjuction with V_{DDQ} to set the interface levels.
V_{DD}	4	PWR	Power supply for the device core and inputs
V_{DDQ}		PWR	Power supply for the device outputs. When utilizing 2.5V LVTTL outputs, V_{DDQ} should be connected to V_{DD} .
GND		PWR	Power supply return for all power

Notes: 1. Inputs are capable of translating the following interface standards. User can select between:
Single-ended 2.5V LVTTL levels

Single-ended 1.8V LVTTL levels

or Differential 2.5V/1.8V LVTTL levels

Differential HSTL and eHSTL levels

- Differential LVEPECL levels 2. Outputs are user selectable to drive 2.5V, 1.8V LVTTL, eHSTL, or HSTL interface levels when used with the appropriate VDDQ voltage.
- 3. 3-level inputs are static inputs and must be tied to VDD or GND or left floating. These inputs are not hot-insertable or over voltage tolerant.
- 4. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
- 5. Pins listed as LVTTL inputs will accept 2.5V signals when RxS = HIGH or 1.8V signals when RxS = LOW or MID.



Input/Output Selection¹

Input/Output Selection					
Input	Output				
2.5V LVTTL SE					
1.8V LVTTL SE					
2.5V LVTTL DSE					
1.8V LVTTL DSE					
LVEPECL DSE					
eHSTL DSE	2.5V LVTTL				
HSTL DSE	2.50 LVIIL				
2.5V LVTTL DIF					
1.8V LVTTL DIF					
LVEPECL DIF					
eHSTL DIF					
HSTL DIF					
2.5V LVTTL SE					
1.8V LVTTL SE					
2.5V LVTTL DSE					
1.8V LVTTL DSE					
LVEPECL DSE					
eHSTL DSE	1.8V LVTTL				
HSTL DSE	1.8V LVIIL				
2.5V LVTTL DIF					
1.8V LVTTL DIF	\				
LVEPECL DIF					
eHSTL DIF					
HSTL DIF					
	The second secon				

Input	Output
2.5V LVTTL SE	
1.8V LVTTL SE	
2.5V LVTTL DSE	
1.8V LVTTL DSE	A
LVEPECL DSE	
eHSTL DSE	eHSTL
HSTL DSE	CHOIL
2.5V LVTTL DIF	
1.8V LVTTL DIF	
LVEPECL DIF	N. C.
eHSTL DIF	
HSTL DIF	
2.5V LVTTL SE	
1.8V LVTTL SE	
2.5V LVTTL DSE	
1.8V LVTTL DSE	
LVEPECL DSE	
eHSTL DSE	HSTL
HSTL DSE	HOIL
2.5V LVTTL DIF	
1.8V LVTTL DIF	
LVEPECL DIF	
eHSTL DIF	
HSTL DIF	

Note: 1. The INPUT/OUTPUT SELECTION Table describes the total possible combinations of input and output interfaces. Single-Ended (SE) inputs in a single-ended mode require the ΔIV_{REF} pin to be connected to GND. Differential Single-Ended (DSE) is for single-ended operation in differential mode, requiring a V_{REF} . Differential (DIF) inputs are used only in differential mode.

DC Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Co	onditions	Min	Max	Unit
V _{IHH}	Input HIGH Voltage Level ¹	3-Level I	nputs Only	V _{DD -} 0.4		V
V _{IMM}	Input MID Voltage Level ¹	3-Level I	nputs Only	V _{DD} /2 - 0.2	$V_{DD}/2 + 0.2$	V
V_{ILL}	Input LOW Voltage Level ¹	3-Level Inputs Only			0.4	V
		V _{IN} = V _{DD}	HIGH Level		200	
l ₃	3-Level Input DC Current (RxS, TxS)	V _{IN} = V _{DD} /2	MID Level	-50	+50	μA
A		V _{IN} = GND	LOW Level	-200		

Note: 1. These inputs are normally wired to V_{DD} , GND, or left floating. Internal termination resistors bias unconnected inputs to $V_{DD}/2$.



DC Electrical Characteristics Over Operating Range for HSTL¹

Symbol	Parameter	Test Conditions	Min	Typ ⁷	Max	Unit
Input Cha	racteristics		•			
I _{IH}	Input HIGH Current ⁹	V_{DD} = 2.6V V_{I} = V_{DDQ} /GND			±5	
I _{IL}	Input LOW Current ⁹	V_{DD} = 2.6V V_{I} = GND/ V_{DDQ}			±5	μA
V_{IK}	Clamp Diode Voltage	V _{DD} = 2.4V, I _{IN} = - 18mA		-0.7	- 1.2	V
V_{IN}	DC Input Voltage		-0.3		+3.6	V
V_{DIF}	DC Differential Voltage ^{2,8}		0.2	A		V
V_{CM}	DC Common Mode Input Voltage ^{3,8}		680	750	900	mV
V_{IH}	DC Input HIGH ^{4,5,8}		V _{REF} + 100			mV
V_{IL}	DC Input LOW ^{4,6,8}				V _{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage ^{4,8}			750		mV
Output C	haracteristics					
1/	Outrout I II CI I Voltage	I _{OH} = -8mA	V _{DDQ} - 0.4			V
V_{OH}	Output HIGH Voltage	I _{OH} = -100μA	V _{DDQ} - 0.1			V
	0.1.1100000000	I _{OL} = 8mA			0.4	V
V_{OL}	Output LOW Voltage	I _{OL} = 100μA			0.1	V

Notes: 1. See RECOMMENDED OPERATING RANGE table.

- interface table should be referenced.

 9. For differential mode (RxS = LOW), A and A/V_{REF} must be at the opposite rail.

Power Supply Characteristics for HSTL Outputs¹

Symbol	Parameter	Test Conditions ²	Тур	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	20	30	mA
I_{DDQQ}	Quiescent V _{DDQ} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	0.1	0.3	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	20	30	μΑ/MHz
I _{DDDQ}	Dynamic V _{DDQ} Power Supply Current per Output	V _{DD} = Max., V _{DDQ} = Max., C _L = 0pF	30	50	μΑ/MHz
	Total Power V _{DD} Supply	V _{DDQ} = 1.5V, F _{REFERENCE} CLOCK= 100MHz,C _L = 15pF	20	40	m Λ
I _{TOT}	Current	V _{DDQ} = 1.5V, F _{REFERENCE} CLOCK= 250MHz, C _L = 15pF	35	50	mA
I _{TOTQ}	Total Power V _{DDQ} Supply	V _{DDQ} = 1.5V, F _{REFERENCE CLOCK} = 100MHz, C _L = 15pF	35	70	mA
ITOTQ	Current	V _{DDO} = 1.5V, F _{REFERENCE} CLOCK= 250MHz, C _I = 15pF	60	120	1 '''

Note: 1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.

- 2. The termination resistors are excluded from these measurements.
- 3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

See RECOMMENDED OPERATING RANGE table.
 V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
 V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
 For single-ended operation, in differential mode, AV_{REF} is tied to the DC voltage V_{REF}.
 Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
 Voltage required to maintain a logic LOW, single-ended operation in differential mode.
 Typical values are at V_{DD} = 2.5V, V_{DDQ} = 1.5V, +25°C ambient.
 The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.

Differential Input AC Test Conditions for HSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ¹	1	V
V _X	Differential Input Signal Crossing Point ²	750	mV
V_{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t _R , t _F	Input Signal Edge Rate ⁴	1	V/nS

Notes: 1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment.

Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.

2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices

- must meet the \dot{V}_X specification under actual use conditions.
- 3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
- 4. The input signal edge rate of 1V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.

DC Electrical Characteristics Over Operating Range for eHSTL¹

De Electrical Characteristics Over Operating Range for endit							
ol Parameter	Test Conditions	Min	Typ ⁷	Max	Unit		
haracteristics				7			
Input HIGH Current ⁹	V_{DD} = 2.6V $V_{I} = V_{DDQ}/GND$	4 \ \		±5	μΑ		
Input LOW Current ⁹	V_{DD} = 2.6V V_{I} = GND/ V_{DDQ}			±5			
Clamp Diode Voltage	V _{DD} = 2.4V, I _{IN} = -18mA		- 0.7	- 1.2	V		
DC Input Voltage		-0.3		+3.6	V		
DC Differential Voltage ^{2,8}		0.2			V		
DC Common Mode Input Voltage ^{3,8}		800	900	1000	mV		
DC Input HIGH ^{4,5,8}		V _{REF} + 100			mV		
DC Input LOW ^{4,6,8}				V _{REF} - 100	mV		
Single-Ended Reference Voltage ^{4,8}	4 74		900		mV		
Characteristics							
Output IIICI I Valtaga	I _{OH} = -8mA	V _{DDQ} - 0.4			V		
Output HIGH Voltage	I _{OH} = -100μA	V _{DDQ} - 0.1			V		
Output LOW/Voltage	I _{OL} = 8mA			0.4	V		
Output LOW Voltage	I _{OL} = 100μA			0.1	V		
	Input HIGH Current ⁹ Input LOW Current ⁹ Clamp Diode Voltage DC Input Voltage DC Differential Voltage ^{2,8} DC Common Mode Input Voltage ^{3,8} DC Input HIGH ^{4,5,8} DC Input LOW ^{4,6,8}	Parameter Test Conditions haracteristics Input HIGH Current ⁹ V _{DD} = 2.6V V _I = V _{DDQ} /GND Input LOW Current ⁹ V _{DD} = 2.6V V _I = GND/V _{DDQ} Clamp Diode Voltage V _{DD} = 2.4V, I _{IN} = -18mA DC Input Voltage DC Differential Voltage ^{2,8} DC Common Mode Input Voltage ^{3,8} DC Input HIGH ^{4,5,8} DC Input LOW ^{4,6,8} Single-Ended Reference Voltage ^{4,8} Characteristics Output HIGH Voltage I _{OH} = -8mA I _{OH} = -100µA	Parameter Test Conditions Min	Parameter Test Conditions Min Typ	Parameter Test Conditions Min Typ Max		

- 2. V_{DIF} specifies the minimum input differential voltage (V_{TR} V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- 3. V_{CM} specifies the maximum allowable range of $(V_{TR} + V_{CP})$ /2. Differential mode only.
- 4. For single-ended operation, in a differential mode, A/V_{REF} is tied to the DC voltage V_{REF}.
- 5. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- 6. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
- 7. Typical values are at V_{DD} = 2.5V, V_{DDQ} = 1.8V, +25°C ambient.
- 8. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.
- 9. For differential mode (RxS = LOW), A and A/ V_{REF} must be at the opposite rail.



Power Supply Characteristics for eHSTL Outputs¹

Symbol	Parameter	Test Conditions ²	Тур	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	20	30	mA
I _{DDQQ}	Quiescent V _{DDQ} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	0.1	0.3	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	20	30	μΑ/MHz
I _{DDDQ}	Dynamic V _{DDQ} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	40	60	μΑ/MHz
I _{TOT}	Total Power V _{DD} Supply Current	V _{DDQ} = 1.8V, F _{REFERENCE CLOCK} = 100MHz, C _L = 15pF	20	40	mA
101		V_{DDQ} = 1.8V, $F_{REFERENCE\ CLOCK}$ = 250MHz, C_L = 15pF	35	50 🗸	
I _{TOTQ}	Total Power V _{DDQ} Supply Current	V _{DDQ} = 1.8V, F _{REFERENCE CLOCK} = 100MHz, C _L = 15pF V _{DDQ} = 1.8V, F _{REFERENCE CLOCK} = 250MHz, C _L = 15pF	40 80	80 160	mA

Notes: 1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.

Differential Input AC Test Conditions for eHSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ¹	1	V
V _X	Differential Input Signal Crossing Point ²	900	mV
V_{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t _R , t _F	Input Signal Edge Rate⁴	1	V/nS

Notes: 1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.

DC Electrical Characteristics Over Operating Range for LVEPECL¹

Symbol	Parameter	Test (Conditions	Min	Typ ²	Max	Unit
Input Ch	aracteristics			•	•	•	
I _{IH}	Input HIGH Current ⁶	V _{DD} = 2.6V	$V_I = V_{DDQ}/GND$			±5	μA
I _{IL}	Input LOW Current ⁶	V _{DD} = 2.6V	$V_I = GND/V_{DDQ}$			±5	μΛ
V _{IK}	Clamp Diode Voltage	V _{DD} = 2.4	V, I _{IN} = -18mA		-0.7	- 1.2	V
V _{IN}	DC Input Voltage			- 0.3		3.6	V
V _{СМ}	DC Common Mode Input Voltage ^{3,5}			915	1082	1248	mV
V_{REF}	Single-Ended Reference Voltage ^{4,5}				1082		mV
V _{IH}	DC Input HIGH			1275		1620	mV
V _{IL}	DC Input LOW			555		875	mV

- 2. Typical values are at V_{DD} = 2.5V, +25°C ambient.

- 3. V_{CM} specifies the maximum allowable range of (V_{TR} + VCP) /2. Differential mode only.
 4. For single-ended operation while in differential mode, A/V_{REF} is tied to the DC Voltage V_{REF}.
 5. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.
- 6. For differential mode (RxS = LOW), A and A/ V_{REF} must be at the opposite rail.

^{2.} The termination resistors are excluded from these measurements.

^{3.} If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

^{2.} A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.

In all cases, input waveform timing is marked at the differential cross-point of the input signals.
 The input signal edge rate of 1V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.



Differential Input AC Test Conditions for LVEPECL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ¹	732	mV
V _X	Differential Input Signal Crossing Point ²	1082	mV
V_{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t _R , t _F	Input Signal Edge Rate⁴	1	V/nS

Notes: 1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.

- 2. A 1082mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_x specification under actual use conditions.
- 3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
- 4. The input signal edge rate of 1V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.

DC Electrical Characteristics Over Operating Range for 2.5V LVTTL¹

Parameter Test Conditions Min Typ8 Max Unit	DC Electi	C Electrical Characteristics Over Operating Range for 2.5v Lv i i L							
IIH	Symbol	Parameter	Test Conditions	Min	Typ ⁸	Max	Unit		
IIIL Input LOW Current 10	Input Ch	naracteristics)				
Input LOW Current V V E S V E S V E S V E S V E S V E S V E S V E S V E S V E S V E S V E S V E S V E S V E S E S V E S E	I _{IH}	Input HIGH Current ¹⁰	V_{DD} = 2.6V V_{I} = V_{DDQ} /GND			±5			
Vin DC Input Voltage -0.3	I _{IL}	Input LOW Current ¹⁰	V_{DD} = 2.6V V_{I} = GND/ V_{DDQ}			±5	μΑ		
Single-Ended Inputs V _{IH} DC Input HIGH 1.7 V V _{IL} DC Input LOW 0.7 V Differential Inputs V _{DIF} DC Differential Voltage 0.2 V V _{CM} DC Common Mode Input Voltage 1150 1250 1350 mV V _{IH} DC Input HIGH 0.6,9 V V _{IL} DC Input LOW 0.7 V V _{IL} DC Input LOW 0.7 V V _{REF} Single-Ended Reference Voltage 0.9 V V _{OH} Output HIGH Voltage I _{OH} = -12mA V _{DDQ} - 0.4 V V _{OH} Output LOW Voltage I _{OH} = -100μA V _{DDQ} - 0.1 V V _{OL} Output LOW Voltage I _{OL} = 12mA 0.4 V I _{OL} = 100μA V _{DDQ} - 0.1 V I _{OL} = 100μA I _{OL} = 100μA 0.1 V I _{OL}	Vıĸ	Clamp Diode Voltage	V_{DD} = 2.4V, I_{IN} = -18mA	A	- 0.7	- 1.2	V		
V _{IH} DC Input HIGH 1.7 V V _{IL} DC Input LOW 0.7 V Differential Inputs V _{DIF} DC Differential Voltage ^{3,9} 0.2 V V _{CM} DC Common Mode Input Voltage ^{4,9} 1150 1250 1350 mV V _{IH} DC Input HIGH ^{5,6,9} V _{REF} + 100 mV mV V _{IL} DC Input LOW ^{5,7,9} V _{REF} + 100 mV V _{REF} Single-Ended Reference Voltage ^{5,9} 1250 mV Output Characteristics I _{OH} = -12mA V _{DDQ} - 0.4 V V _{OH} Output HIGH Voltage I _{OH} = -12mA V _{DDQ} - 0.4 V V _{OL} Output LOW Voltage I _{OL} = 12mA 0.4 V V _{OL} Output LOW Voltage I _{OL} = 12mA 0.4 V	V _{IN}	DC Input Voltage		-0.3		+3.6	V		
ViL DC Input LOW 0.7 V Differential Inputs V _{DIF} DC Differential Voltage ^{3,9} 0.2 V V _{CM} DC Common Mode Input Voltage ^{4,9} 1150 1250 1350 mV V _{IH} DC Input HIGH ^{5,6,9} V _{REF} + 100 mV V _{IL} DC Input LOW ^{5,7,9} V _{REF} + 100 mV V _{REF} Single-Ended Reference Voltage ^{5,9} 1250 mV Output Characteristics V _{OH} Output HIGH Voltage I _{OH} = -12mA V _{DDQ} - 0.4 V V _{OL} Output LOW Voltage I _{OH} = -100μA V _{DDQ} - 0.1 V V _{OL} Output LOW Voltage I _{OL} = 12mA 0.4 V	Single-E	inded Inputs ²							
Differential Inputs D.2 V V V D.2 D.2 D.2 V V V D.2 D.2 D.3	V _{IH}	DC Input HIGH		1.7			V		
V _{DIF} DC Differential Voltage ^{3,9} 0.2 V V _{CM} DC Common Mode Input Voltage ^{4,9} 1150 1250 1350 mV V _{IH} DC Input HIGH ^{5,6,9} V _{REF} + 100 mV V _{IL} DC Input LOW ^{5,7,9} V _{REF} - 100 mV V _{REF} Single-Ended Reference Voltage ^{5,9} 1250 mV Output Characteristics V _{OH} Output HIGH Voltage I _{OH} = -12mA V _{DDQ} - 0.4 V I _{OH} = -100µA V _{DDQ} - 0.1 V V _{OL} Output LOW Voltage I _{OL} = 12mA 0.4 V I _{OL} = 100µA 0.1 V	V _{IL}	DC Input LOW				0.7	V		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Differenti	ial Inputs							
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	V_{DIF}	DC Differential Voltage ^{3,9}		0.2			V		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	V _{CM}	Voltage ^{4,9}		1150	1250	1350	mV		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	V_{IH}	DC Input HIGH ^{5,6,9}		V _{REF} + 100			mV		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	V_{IL}					V _{REF} - 100	mV		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	V_{REF}	Single-Ended Reference Voltage ^{5,9}			1250		mV		
V_{OH} Output HIGH Voltage	Output 0	Characteristics							
V_{OL} Output LOW Voltage I_{OH} = -100 μ A V_{DDQ} - 0.1 V I_{OL} = 12mA V V_{DD} 0.4 V V_{DD} 0.1 V	Vou	Output HIGH Voltage	I _{OH} = -12mA	V _{DDQ} - 0.4			V		
V_{OL} Output LOW Voltage I_{OL} = 100 μ A 0.1 V	V OH	Catpat Hori Voltage	I _{OH} = -100μA	V _{DDQ} - 0.1			V		
I _{OL} = IUUµA U.1 V	Voi	Output LOW Voltage				_			
			· · · · · · · · · · · · · · · · · · ·			0.1	V		

- 2. For 2.5V LVTTL single-ended operation, the RxS pin is tied HIGH and AV_{REF} is tied to GND.

 3. V_{DIF} specifies the minimum input differential voltage (V_{TR} V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- 4. V_{CM} specifies the maximum allowable range of $(V_{TR} + V_{CP})/2$. Differential mode only. 5. For single-ended operation, in differential mode, A/V_{REF} is tied to the DC voltage V_{REF} .
- 6. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- 7. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
- 8. Typical values are at V_{DD} = 2.5V, V_{DDQ} = V_{DD}, +25°C ambient.
 9. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.
- 10. For differential mode (RxS = LOW), A and A/V_{RFF} must be at the opposite rail.



Power Supply Characteristics for 2.5V LVTTL Outputs¹

Symbol	Parameter	Test Conditions ²	Тур	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	20	30	mA
I _{DDQQ}	Quiescent V _{DDQ} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	0.1	0.3	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	25	40	μΑ/MHz
I _{DDDQ}	Dynamic V _{DDQ} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	45	70	μΑ/MHz
	Total Power V _{DD} Supply	V _{DDQ} = 2.5V., F _{REFERENCE CLOCK} = 100MHz, C _L = 15pF	25	40	m Λ
I _{TOT}	Current	V _{DDQ} = 2.5V., F _{REFERENCE} CLOCK= 200MHz, C _L = 15pF	45	70	mA
	Total Power V _{DDQ} Supply	V _{DDQ} = 2.5V., F _{REFERENCE} CLOCK= 100MHz, C _L = 15pF	40	80 /	A
Ιτοτα	Current	V _{DDQ} = 2.5V., F _{REFERENCE CLOCK} = 200MHz, C _L = 15pF	100	200	mA

Notes: 1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.

Differential Input AC Test Conditions for 2.5V LVTTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ¹	V_{DD}	V
V _X	Differential Input Signal Crossing Point ²	V _{DD} /2	V
V_{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t _R , t _F	Input Signal Edge Rate ⁴	2.5	V/nS

Notes: 1. A nominal 2.5V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.

Single-ended Input AC Test Conditions for 2.5V LVTTL

Symbol	Parameter	Value	Units
V _{IH}	Input HIGH Voltage	V_{DD}	V
V _{IL}	Input LOW Voltage	0	V
V _{THI}	Input Timing Measurement Reference Level ¹	V _{DD} /2	V
t_R , t_F	Input Signal Edge Rate ²	2	V/nS

Notes: 1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.

^{2.} The termination resistors are excluded from these measurements.

^{3.} If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

 ^{2.} A nominal 1.25V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_x specification under actual use conditions.
 3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

^{4.} The input signal edge rate of 2.5V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.

^{2.} The input signal edge rate of 2V/nS or greater is to be maintained in the 10% to 90% range of the input waveform.



DC Electrical Characteristics Over Operating Range for 1.8V LVTTL¹

Symbol	Parameter	Test Conditions	Min	Typ ⁸	Max	Unit
Input Chara	cteristics					
I _{IH}	Input HIGH Current ¹²	V_{DD} = 2.6V V_{I} = V_{DDQ} /GND			±5	μA
I _{IL}	Input LOW Current ¹²	V_{DD} = 2.6V V_{I} = GND/ V_{DDQ}			±5	μΑ
V_{IK}	Clamp Diode Voltage	V _{DD} = 2.4V, I _{IN} = -18mA		-0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3		V _{DDQ} + 0.3	V
Single-End	ded Inputs ²					
V_{IH}	DC Input HIGH		1.073 ¹¹			V
V_{IL}	DC Input LOW				0.683 ¹¹	V
Differentia	I Inputs					
V_{DIF}	DC Differential Voltage ^{3,9}		0.2	M.		V
V _{CM}	DC Common Mode Input Voltage ^{4,9}		825	900	975	mV
V_{IH}	DC Input HIGH ^{5,6,9}	4	V _{REF} + 100			mV
V_{IL}	DC Input LOW ^{5,7,9}			Jan 1997	V _{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage ^{5,9}	A	1	900		mV
Output Ch	aracteristics					
V_{OH}	Output HIGH Voltage	I _{OH} = -6mA	V _{DDQ} - 0.4			V
V OH	Output HIGH Voltage	I _{OH} = -100μA	V _{DDQ} - 0.1			V
V _{OL}	Output LOW Voltage	I _{OL} = 6mA			0.4	V
V OL	Output LOW Voltage	I _{OL} = 100μA			0.1	V

- 2. For 1.8V LVTTL single-ended operation, the RxS pin is allowed to float or tied to VDD/2 and A/VREF is tied to GND.
- 3. V_{DIF} specifies the minimum input differential voltage (V_{TR} V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- 4. V_{CM} specifies the maximum allowable range of $(V_{TR} + V_{CP})/2$. Differential mode only.
- 5. For single-ended operation in differential mode, AVREF is tied to the DC voltage VREF. The input is guaranteed to toggle within ±200mV of VREF when V_{REF} is constrained within +600mV and V_{DDI}-600mV, where V_{DDI} is the nominal 1.8V power supply of the device driving the A input. To guarantee switching in voltage range specified in the JEDEC 1.8V LVTTL interface specification, V_{REF} must be maintained at 900mV with appropriate
- 6. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- 7. Voltage required to maintain a logic LOW, single-ended operation in differential mode. 8. Typical values are at $V_{DD} = 2.5V$, $V_{DDQ} = 1.8V$, $+25^{\circ}C$ ambient.
- 9. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.
- 10. This value is the worst case minimum V_{IH} over the specification range of the 1.8V power supply. The 1.8V LVTTL specification is $V_{IH} = 0.65 \cdot V_{DD}$ where V_{DD} is 1.8V \pm 0.15V. However, the LVTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value ($V_{IH} = 0.65 \cdot [1.8 \cdot 0.15V]$) rather than reference against a nominal 1.8V supply.
- 11. This value is the worst case maximum V_{IL} over the specification range of the 1.8V power supply. The 1.8V LVTTL specification is V_{IL} = 0.35 V_{DD} where V_{DD} is 1.8V ± 0.15V. However, the LVTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value (V_{IL} = 0.35 • [1.8 + 0.15V]) rather than reference against a nominal 1.8 \forall supply. 12. For differential mode (RxS = LOW), A and A/V_{REF} must be at the opposite rail.



Power Supply Characteristics for 1.8V LVTTL Outputs¹

Symbol	Parameter	Test Conditions ²	Тур	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	20	30	mA
I _{DDQQ}	Quiescent V _{DDQ} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	0.1	0.3	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	20	40	μΑ/MHz
I _{DDDQ}	Dynamic V _{DDQ} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	55	80	μΑ/MHz
	Total Power V _{DD} Supply	V _{DDQ} = 1.8V., F _{REFERENCE CLOCK} = 100MHz, C _L = 15pF	25	40	mA
I _{TOT}	Current	V _{DDQ} = 1.8V., F _{REFERENCE} CLOCK= 200MHz, C _L = 15pF	40	60 🎤	, IIIA
	Total Power V _{DDQ} Supply Current	V _{DDQ} = 1.8V., F _{REFERENCE CLOCK} = 100MHz, C _L = 15pF	50	100	A
Ιτοτα		V _{DDQ} = 1.8V., F _{REFERENCE CLOCK} = 200MHz, C _L = 15pF	120	240	mA

Notes: 1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.

Differential Input AC Test Conditions for 1.8V LVTTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ¹	V_{DDI}	V
Vx	Differential Input Signal Crossing Point ²	V _{DDI} /2	mV
V_{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t _R , t _F	Input Signal Edge Rate ⁴	1.8	V/nS

Notes:1. V_{DDI} is the nominal 1.8V supply (1.8V ± 0.15V) of the part or source driving the input. A nominal 1.8V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.

3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

Single-ended Input AC Test Conditions for 1.8V LVTTL

Symbol	Parameter	Value	Units
V _{IH}	Input HIGH Voltage ¹	V_{DDI}	V
VIL	Input LOW Voltage	0	V
V_{THI}	Input Timing Measurement Reference Level ²	V _{DDI} /2	mV
t _R , t _F	Input Signal Edge Rate ³	2	V/nS

The termination resistors are excluded from these measurements.

^{3.} If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

^{2.} A nominal 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.

^{4.} The input signal edge rate of 1.8V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.

Notes: 1. V_{DDI} is the nominal 1.8V supply (1.8V ± 0.15V) of the part or source driving the input.

2. A nominal 900mV timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE)

^{3.} The input signal edge rate of 2V/nS or greater is to be maintained in the 10% to 90% range of the input waveform.



AC Electrical Characteristics Over Operating Range⁵

Symbo I	Pa	rameter	Min	Тур	Max	Unit
Skew Par	ameters					
t _{SK(O)}	Same Device Output Pin-to-Pin Skew ¹	Single-Ended and Differential Modes Single-Ended in Differential			25	pS
	Thirte Thireston	Mode (DSE)		25		
t _{sk(INV)}	Inverting Skew ²	Single-Ended and Differential Modes			300	pS
SK(IINV)	involuing exew	Single-Ended in Differential Mode (DSE)		300		ρο
t _{SK(P)}	Pulse Skew ³	Single-Ended and Differential Modes			300	pS
SK(P)	ruise Skew	Single-Ended in Differential Mode (DSE)		300		ро
t _{SK(PP)}	Part-to-Part Skew ⁴	Single-Ended and Differential Modes	4		300	pS
ISK(PP)		Single-Ended in Differential Mode (DSE)		300		ρο
V_{OX}	HSTL and eHSTL Differer Output Crossing Voltage I	ntial True and Complementary Level	V _{DDQ} /2 - 200	V _{DDQ} /2	V _{DDQ} /2 + 200	mV
Propagati	on Delay					
t _{PLH}	Propagation Delay A to Qn/Qn	2.5V / 1.8V LVTTL Outputs			2.5	nS
t_PHL	Qn/Qn	HSTL / eHSTL Outputs			2	110
t _R	Output Rise Time	2.5V /1.8V LVTTL Outputs	350		1050	pS
чĸ	(20% to 80%)	HSTL / eHSTL Outputs	350		1350	ро
t⊧	Output Fall Time	2.5V /1.8V LVTTL Outputs	350		1050	pS
ч -	(20% to 80%)	HSTL / eHSTL Outputs	350		1350	ро
f_{Ω}	Frequency Range (HSTL/	eHSTL outputs)			250	MHz
10	Frequency Range (2.5V/1	.8V LVTTL outputs)			200	IVIIIZ
Output G	Sate Enable/Disable Del	ay				
t _{PGE}	Output Gate Enable to Qr	n/Qn			3.5	nS
t _{PGD}	Output Gate Enable to Qr Level	n/Qn Driven to GL Designated			3	nS

Notes: 1. Skew measured between all outputs or output pairs under identical input and output interfaces, transitions and load conditions on any one device. For single ended and differential LVTTL outputs, this measurement is made when each output voltage passes through V_{DDQ}/2. For differential LVTTL outputs, the true outputs are compared only with other true outputs and the complementary outputs are compared only with other complementary outputs. For differential HSTL outputs, the measurement takes place at the crossing point of the true and complementary signals.

^{2.} For operating with either 1.8V or 2.5V LVTTL output interfaces with both true and complementary outputs enabled. Inverting skew is the skew between true and complementary outputs switching in opposite directions under identical input and output interfaces, transitions and load conditions on any one device.

^{3.} Skew measured is the difference between propagation delay times t_{PHL} and t_{PLH} of any output or output pair under identical input and output interfaces, transitions and load conditions on any one device. For single ended and differential LVTTL outputs, this measurement is made when each output voltage passes through $V_{DDO}/2$. The measurement applies to both true and complementary signals. For differential HSTL outputs, the measurement takes place at the crossing point of the true and complementary signals.

^{4.} Skew measured is the magnitude of the difference in propagation times between any outputs or output pairs of two devices, given identical transitions and load conditions at identical V_{DD}/V_{DDQ} levels and temperature.

^{5.} Guaranteed by design.



AC Differential Input Specifications¹

Symbol	Parameter	Min	Тур	Max	Unit	
t w	Reference Clock Pulse Width HIGH or LOW (HSTL/eHSTL outputs) ²	1.73				
	Reference Clock Pulse Width HIGH or LOW (2.5V / 1.8V LVTTL outputs) ²	2.17		A	nS	
HSTL/eH	HSTL/eHSTL/1.8V LVTTL/2.5V LVTTL					
V_{DIF}	AC Differential Voltage ³	400	A		mV	
V _{IH}	AC Input HIGH ^{4,5}	V _x + 200			mV	
V _{IL}	AC Input LOW ^{4,6}			V _x - 200	mV	
LVEPECI	LVEPECL					
V_{DIF}	AC Differential Voltage ³	400			mV	
V _{IH}	AC Input HIGH⁴	1275			mV	
V _{IL}	AC Input LOW ⁴			875	mV	

- Notes: 1. For differential input mode, RxS is tied to GND.
 2. Both differential input signals should not be driven to the same level simultaneously. The input will not change state until the inputs have crossed and the voltage range defined by V_{DIF} has been met or exceeded.
 - 3. Differential mode only. V_{DIF} specifies the minimum input voltage (V_{TR} V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.

 4. For single-ended operation, AV_{REF} is tied to DC voltage (V_{REF}). Refer to each input interface's DC specification for the correct V_{REF} range.

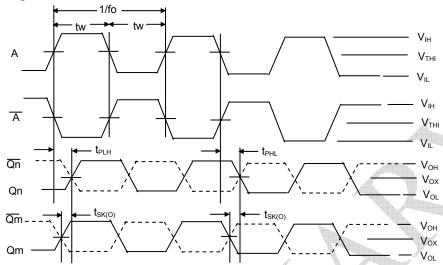
 5. Voltage required to switch to a logic HIGH, single-ended operation only.

 6. Voltage required to switch to a logic LOW, single-ended operation only.

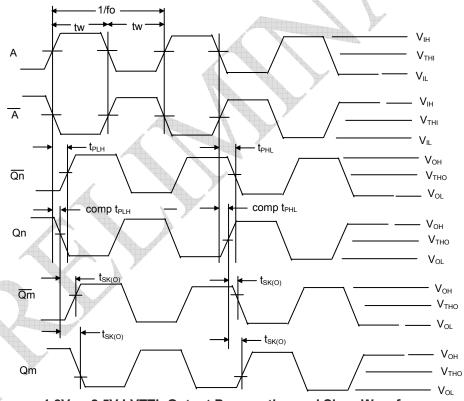




Differential AC Timing Waveforms



HSTL and eHSTL Output Propagation and Skew Waveforms



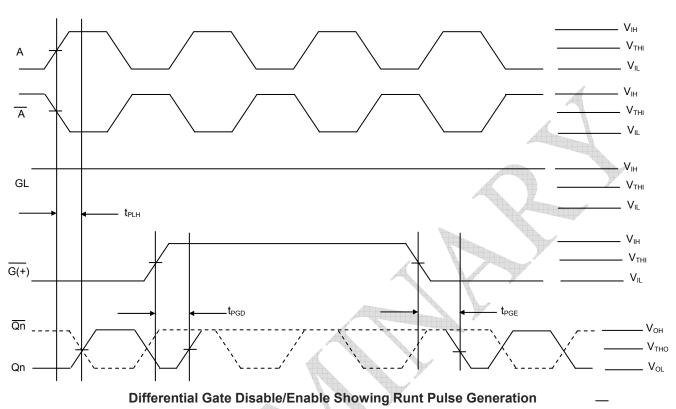
1.8V or 2.5V LVTTL Output Propagation and Skew Waveforms

Notes: 1. For the HSTL and eHSTL outputs, t_{PHL} and t_{PLH} are measured from the input passing through V_{THI} or input pair crossing to the crossing point of each

- 2. For 1.8V and 2.5V LVTTL outputs, t_{PHL} and t_{PLH} are measured from the input passing through V_{THI} or input pair crossing to the slower of Qn or Qn passing through V_{THO}.
- 3. Pulse skew is calculated using the following expression:

where t_{PHL} and t_{PLH} are measured on the controlled edges of any one output from the rising and falling edges of a single pulse. Note that the t_{PHL} and t_{PLH} shown above are not valid measurements for this calculation because they are not taken from the same pulse.

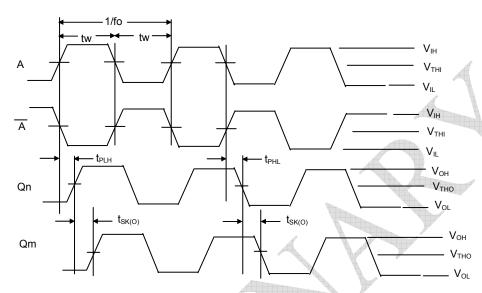




Notes: 1. The waveforms shown only gate "true" output, Qn.
2. As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their Gx signals to avoid this problem.



SDR AC TIMING WAVEFORMS



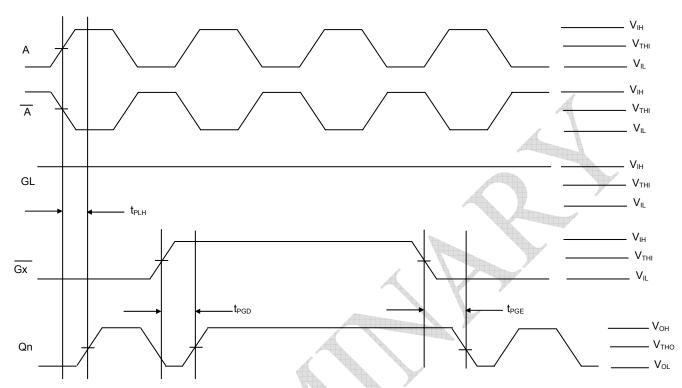
Propagation and Skew Waveforms

Notes: 1. t_{PHL} and t_{PLH} signals are measured from the input passing through V_{THI} or input pair crossing to Qn passing through V_{THO} .

2. Pulse Skew is calculated using the following expression:

 $t_{SK(P)} = |t_{PHL} - t_{PLH}|$ where t_{PHL} and t_{PLH} are measured on the controlled edges of any one output from rising and falling edges of a single pulse. Please note that the and t_{PLH} shown are not valid measurements for this calculation because they are not taken from the same pulse.



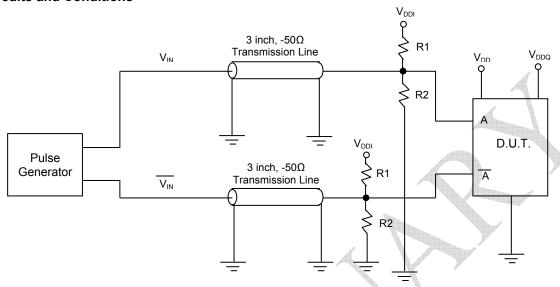


SDR Gate Disable/Enable Showing Runt Pulse Generation

Note: As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their Gx signals to avoid this problem.



Test Circuits and Conditions

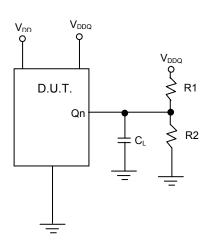


Test Circuit for Differential Input¹

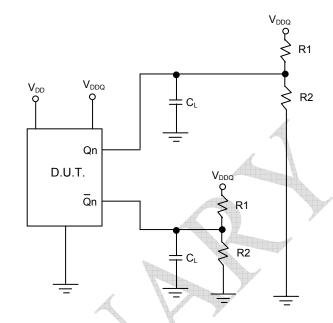
Differential Input Test Conditions

Symbol	$V_{DD} = 2.5V \pm 0.1V$	Unit	
R1	100	Ω	
R2	100	Ω	
V _{DDI}	V _{CM} *2	V	
V _{THI}	HSTL: Crossing of A and \overline{A} eHSTL: Crossing of A and \overline{A} LVEPECL: Crossing of A and \overline{A} 1.8V LVTTL: V _{DDI} /2	V	
	2.5V LVTTL: V _{DD} /2		

Note: 1. This input configuration is used for all input interfaces. For single-ended testing, the V_{IN} input is tied to GND. For testing single-ended in differential input mode, the V_{IN} is left floating.







Test Circuit for Differential Outputs

SDR Output Test Conditions

Symbol	V _{DD} = 2.5V ± 0.1V V _{DDQ} = Interface Specified	Unit	
C L	15	pF	
R1	100	Ω	
R2	100	Ω	
V_{THO}	V _{DDQ} / 2	V	

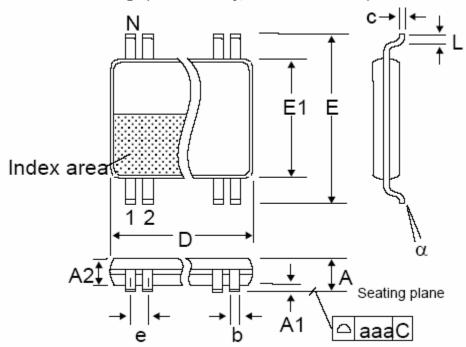
Differential Output Test Contions

Symbol	V_{DD} = 2.5V ± 0.1V V_{DDQ} = Interface Specified	Unit	
C L	15	pF	
R1	100	Ω	
R2	100	Ω	
Vox	HSTL: Cross <u>ing</u> of Qn and Qn	W	
VOX	eHSTL: Crossing of Qn and Qn	V	
V_{THO}	1.8V LVTTL: V _{DDQ} /2	V	
V THO	2.5V LVTTL: V _{DDQ} /2	V	



Package Information

Package (6.10 mm Body, JEDEC MO-153-ED)



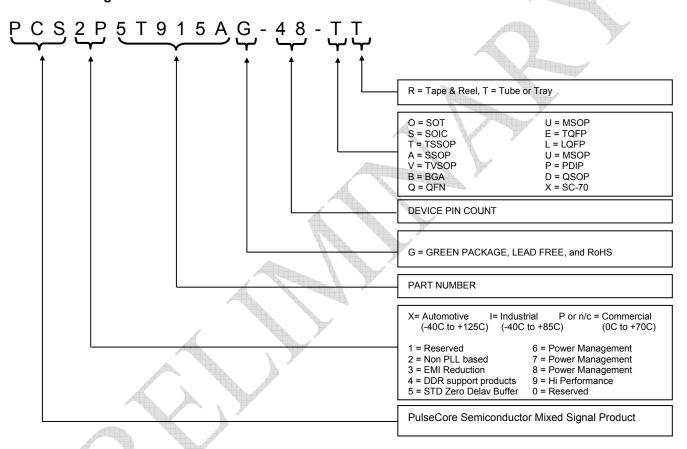
	Dimensions				
Symbol	Inches		Millimeters		
	Min	Max	Min	Max	
Α	/	0.047		1.20	
A1	0.002	0.006	0.05	0.15	
A2	0.031	0.041	0.8	1.05	
b	0.008 BSC		0.20 BSC		
С	0.004	0.008	0.09	0.20	
D	0.488	0.496	12.40	12.60	
E1	0.236	0.244	6.00	6.20	
E	0.319 BSC		8.10 BSC		
е	0.020 BSC		0.50 BSC		
L	0.018	0.030	0.45	0.75	
N	4		8		
α	0°	8°	0°	8°	



Ordering Information

Part Number	Marking	Package Type	Temperature
PCS2P5T915AG	2P5T915AG	48 pin TSSOP Package	Commercial
PCS2I5T915AG	2I5T915AG	48 pin TSSOP Package	Industrial

Device Ordering Information



Licensed under US patent Nos 5,488,627 and 5,631,920.





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Fax: 408-879-9018 www.pulsecoresemi.com Copyright © PulseCore Semiconductor All Rights Reserved Preliminary Information Part Number: PCS2P5T915A Document Version: v0.2

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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