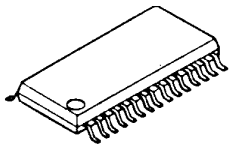
PWM 3-PHASE DC BRUSHLESS MOTOR CONTROLLER

■ GENERAL DESCRIPTION

The NJW4303 is a 3-Phase Brushless DC Motor Control pre-driver IC with PWM control. It generates the most optimal current flow patterns by receiving rotor magnetic pole detection signals from hall elements of 3-phase brushless motor.

Operational voltage range for the IC has margin as 9.0V to 35V(maximum voltage of 40V), and it fits for a 12V/24V power supply. It is possible to put practical use such as speed control by internal oscillation circuit, and torque limiter control by current sensory circuit. With NJW4303, high reliability of various motor drive controls can be realized by a variety of function and a substantial protection circuit.

■ PACKAGE OUTLINE

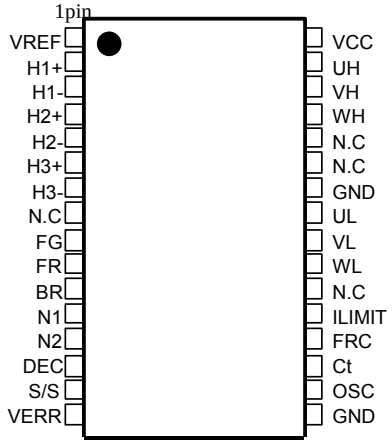


NJW4303V

■ FEATURES

- Maximum Supply Voltage : 40V
- Operating Voltage : 9.0 V to 35V
- 3-Phase Full-Wave PWM Predriver : Hi-side: Pch-FET/ Low-side: Nch-FET
- Low-side Gate Voltage Clamp : Gate Voltage=18V max.
- Internal PWM Oscillation Circuit : Frequency Setting by External Capacitor
- Current Protection Circuit : Current limit=0.25V±10%
- Low-Voltage Protection Circuit
- Forward/Reverse Direction : Changeable while Rotating
  : Controllable Dead-Time Settings
- Soft-Start Function : Using External Capacitor
- ON/OFF Function : Stop with S/S Pin
- Brake Function
- Lock Protection System
- Thermal Shutdown Circuit
- 120°/60° Phase Difference Change Function
- Multi-FG Output : 2bit Input Change Type
- Bi-CDMOS Technology
- Package Outline : SSOP32

■ PIN CONNECTION



1.VREF	17.GND
2.H1+	18.OSC
3.H1-	19.Ct
4.H2+	20.FRC
5.H2-	21.ILIMIT
6.H3+	22.N.C
7.H3-	23.WL
8.N.C	24.VL
9.FG	25.UL
10.FR	26.GND
11.BR	27.N.C
12.N1	28.N.C
13.N2	29.WH
14.DEC	30.VH
15.S/S	31.UH
16.VERR	32.VCC

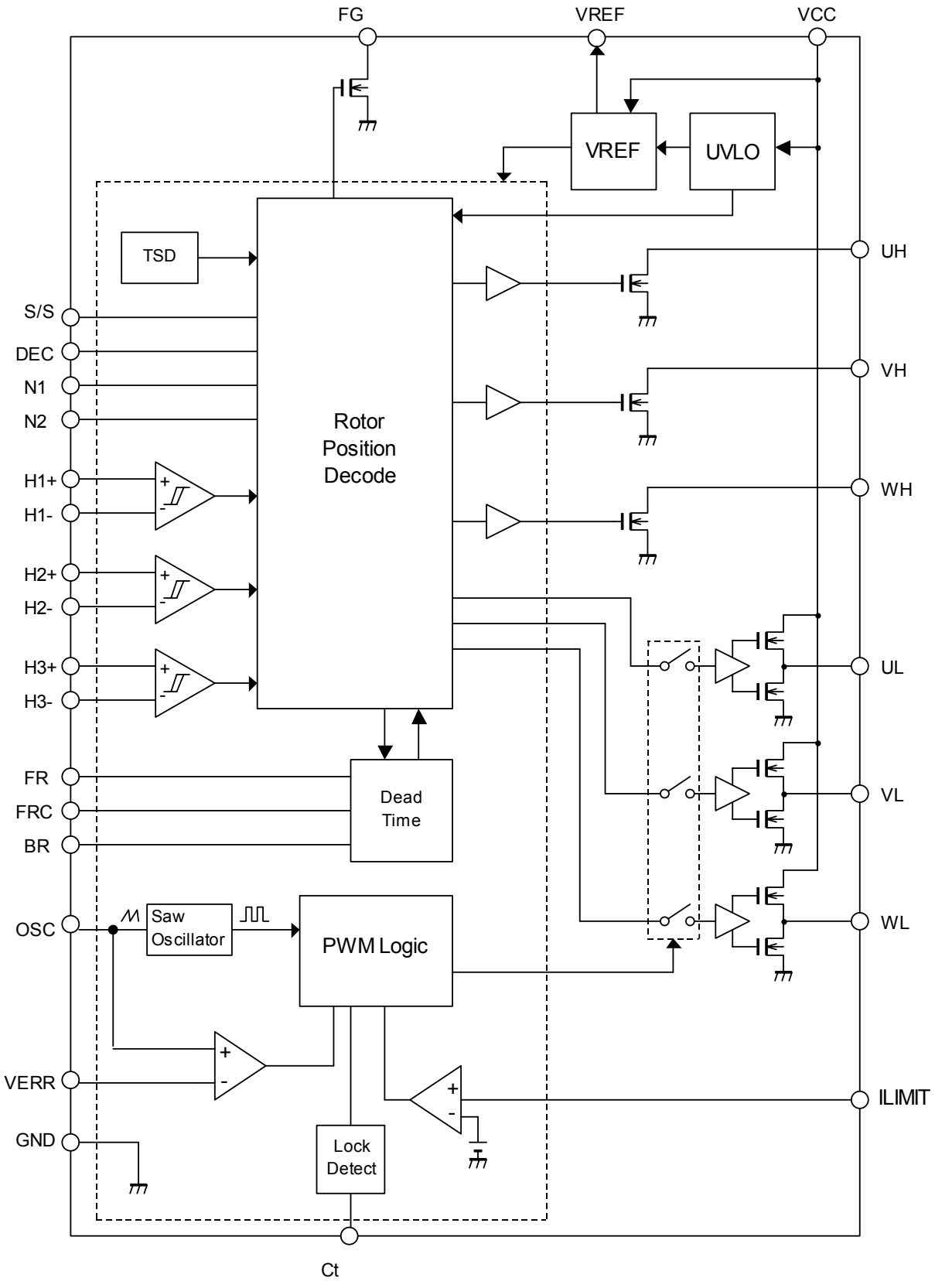
■ PIN FUNCTION LIST

Pin#	Terminal Name	Function	Remark
1	VREF	5V Output Voltage Terminal	Outputs Supply Voltage of 5V
2	H1+	Hall Element Input Terminal H1+	Use with H1-
3	H1-	Hall Element Input Terminal H1-	Use with H1+
4	H2+	Hall Element Input TerminalH2+	Use with H2-
5	H2-	Hall Element Input Terminal H2-	Use with H2+
6	H3+	Hall Element Input Terminal H3+	Use with H3-
7	H3-	Hall Element Input Terminal H3-	Use with H3+
8,22,27,28	N.C.	No Connection	No Connection
9	FG	FG pulse Output Terminal	Output Rotary Signal
10	FR	Forward/Reverse Direction Input Terminal	L, or Open=Forward Direction, H=Reverse Direction
11	BR	Short Brake Input Terminal	L, or Open=Rotation, H=Short Brake
12	N1	FG Pattern Switching Terminal1	Set FG Pattern by Combination with N2. Cf. the below table
13	N2	FG Pattern Switching Terminal2	Set FG Pattern by Combination with N1. Cf. the below table
14	DEC	Hall Input Phase Switching Terminal	L, or Open=120° Hall Input, H=60° Hall Input
15	S/S	Start and Stop input Terminal	L, or Open=Start, H=Stop
16	VERR	Error Amp Voltage Input Terminal	Set Output ON Duty H=Output ON Duty 100%, L=Output ON Duty 0% Pull-up to VREF PIN in nonuse
17,26	GND	Logic Ground Terminal	Connecting with Ground
18	OSC	PWM Control Capacitor Terminal	Insert a Capacitor between Grounds. Set PWM frequency depending on the value of the Capacitor
19	Ct	Lock Protection Capacitor Connection Terminal	Insert a Capacitor between Grounds. Depending on the value of the Capacitor, set On/Off timer for the Output at the time of activated Lock Protection.
20	FRC	Dead-Time Capacitor Connection Terminal	Insert a Capacitor between Grounds. Depending on the value of the Capacitor, set Output Dead Band at the time of FR switching
21	ILIMIT	Over Current Sensing Terminal	Connect to the ground side of the external driver
23	WL	Output Terminal WL	Connect to Nch Gate Driver
24	VL	Output Terminal VL	Connect to Nch Gate Driver
25	UL	Output Terminal UL	Connect to Nch Gate Driver
29	WH	Output Terminal WH	Connect to Pch Gate Driver
30	VH	Output Terminal VH	Connect to Pch Gate Driver
31	UH	Output Terminal UH	Connect to Pch Gate Driver
32	VCC	Motor Voltage Supply Terminal	Connect motor power source to the terminal

* All Ground Pins must be connected at the outside.
* Electrical potential of all unused output pins must be fixed at the outside.

FG Pattern by combination with N1 and N2			
No.	N1	N2	FG
1	H	H	1/2 Frequency Signal from H1
2	H	L/OPEN	Signal from H1
3	L/OPEN	H	1/2 Frequency Signal from 3 Hall Compound Signals
4	L/OPEN	L/OPEN	3 Hall Compound Signals

■ **BLOCK DIAGLAM**



■ **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	Remark
Supply Voltage	V_{CC}	40	V	VCC PIN
Hi-side Output Terminal Voltage	V_{OH}	40	V	UH, VH, WH PIN
FG Terminal Voltage	V_{FG}	7	V	FG PIN
LIMIT Terminal Voltage	V_{LIM}	3.5	V	ILIMIT PIN
VERR Terminal Voltage	V_{VERR}	6	V	VERR PIN
Hall Input Terminal Voltage	V_{IH}	4.5	V	H1+, H1-, H2+, H2-, H3+, H3- PIN
Logic Input Terminal Voltage	V_{IN}	7	V	BR, FR, DEC, N1/N2, S/S PIN
Reference Voltage Output Current	I_{REF}	30	mA	VREF PIN
Hi-side Output Current	I_{OH}	40	mA	UH, VH, WH PIN
Low-side Output Current	I_{OL}	±40	mA	UL, VL, WL PIN
FG Output Current	I_{FG}	15	mA	FG PIN
Power Dissipation	P_D	1190	mW	※ Board Mounted
Operating Ambient Temperature	Topr	-40 to +85	°C	
Storage Temperature	Tstg	-50 to +150	°C	

※ Mounted on designated board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers, FR-4)

■ **RECOMMENDED OPERATIONAL CONDITIONS** (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Logic Supply Voltage	V_{CC}		9.0	24.0	35.0	V

■ **ELECTRICAL CHARACTERISTICS**

V_{CC}=24V, V_{IH1+}= V_{IH3+}=3.0V, V_{IH1-}= V_{IH2-}= V_{IH3-}=2.0V, V_{IH2+}=1.0V, V_{IN}= V_{LIM}= V_{CT}=0V,
V_{VERR}=4.5V, V_{OSC}=4.5V→0.5V, C_{VREF}=1uF, Ta=25°C

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
■ GENERAL						
Supply current 1	I_{CC1}	V_{CC}=12V	-	5.3	8.3	mA
Supply current 2	I_{CC2}		-	6.4	9.4	mA
■ THERMAL SHUTDOWN BLOCK						
Thermal shutdown operating	T_{TSD1}		-	170	-	°C
Thermal shutdown recovery	T_{TSD2}			135		°C
Thermal shutdown hysteresis	ΔT_{TSD}		-	35	-	°C
■ UNDER VOLTAGE LOCK OUT BLOCK						
UVLO operating voltage	V_{UVLO1}	V_{CC} Decreasing	6.3	6.8	7.3	V
UVLO recovery voltage	V_{UVLO2}	V_{CC} Increasing	6.8	7.3	7.8	V
UVLO hysteresis voltage	ΔV_{UVLO}		-	0.5	-	V
■ LOCK PROTECTION BLOCK (Ct PIN)						
High level voltage	V_{HCt}		3.30	3.55	3.80	
Low level voltage	V_{LCt}		0.90	1.00	1.30	
Lock charge current	I_{CHGCt}		2.5	5.5	9.0	uA
Lock discharge current	I_{DCHGCt}		0.25	0.55	0.90	uA
Lock charge/discharge current	I_{CHGCt}/I_{DCHGCt}		-	10	-	-
■ REFERENCE VOLTAGE BLOCK (VREF PIN)						
Reference voltage supply	V_{REF}	I_{VREF}=1mA	4.5	5.0	5.5	V
Load regulation	ΔV_{LOVREF}	I_{VREF}=1 to 10 mA	-	15	60	mV
Line regulation	ΔV_{LIVREF}	V_{CC}=9 to 35V, I_{VREF}=1 mA	-	50	100	mV
■ HALL AMP BLOCK (H1+, H1-, H2+, H2-, H3+, H3- PIN)						
Hysteresis Voltage range	ΔV_{HYSIH}		10	30	50	mV
Input bias current	I_{BIH}	Per each input	-	-	1.5	uA
■ HI-SIDE BLOCK (UH, VH, WH PIN)						
Hi-side output voltage	V_{OLH}	I_{OH}=30 mA	-	0.5	1.0	V
Hi-side leak current	I_{OLEAKH}	V_{OH}=35V	-	-	1	uA
■ LOW-SIDE BLOCK (UL, VL, WL PIN)						
Low-side output H voltage1	V_{OHL1}	$I_{OLSOURCE}$=30 mA ,V_{CC}=12V	8.0	10.0	-	V
Low-side output H voltage2	V_{OHL2}	$I_{OLSOURCE}$=30 mA	8.0	10.0	-	V
Low-side output L voltage	V_{OLL}	I_{OLSINK}=30 mA	-	0.5	1.0	V
Low-side clamp voltage	V_{CLL}	$I_{OLSOURCE}$=0.1 mA ,V_{CC}=35V	-	-	18	V
■ FG OUTPUT (FG PIN)						
Output voltage	V_{FGL}	I_{FG}=10 mA	-	0.3	0.7	V
Leak current	I_{LEAKFG}	V_{FG}=5V	-	-	1	uA

■ ELECTRICAL CHARACTERISTICS

V_{CC}=24V, V_{IH1+}= V_{IH3+}=3.0V, V_{IH1-}= V_{IH2-}= V_{IH3-}=2.0V, V_{IH2+}=1.0V, V_{IN}= V_{LIM}= V_{CT}=0V,
V_{VERR}=4.5V, V_{OSC}=4.5V→0.5V, C_{VREF}=1uF, Ta=25°C

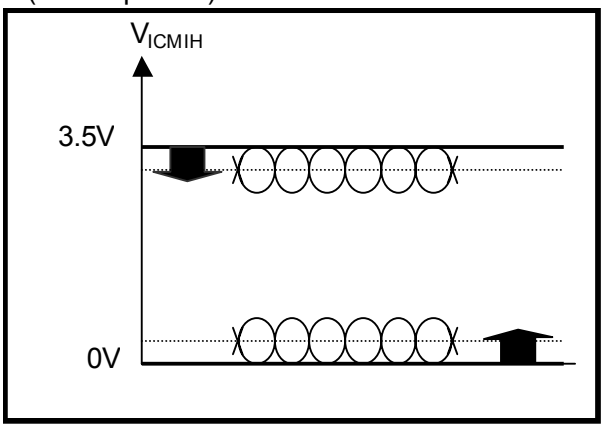
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
■ OVER CURRENT SENSOR BLOCK (ILIMIT PIN)						
Sense voltage	V_{DETLIM}		0.225	0.250	0.275	V
Input bias current	I_{BILM}		-	1.6	5.0	uA
■ ERROR AMP BLOCK (VERR PIN)						
PWM0% sense voltage	$V_{PWM1VERR}$	PWMDUTY=0%	-	-	0.5	V
PWM100% sense voltage	$V_{PWM2VERR}$	PWMDUTY=100%	3.6	-	-	V
Input bias current	I_{BVERR}		-	1.6	5.0	uA
■ OSCILLATOR BLOCK (OSC PIN)						
Saw wave peak voltage	V_{POSC}		2.7	3.0	3.3	V
Saw wave bottom voltage	V_{BOSC}		1.00	1.35	1.60	V
OSC charge current	I_{CHGOSC}		30	50	70	uA
OSC discharge current	$I_{DCHGOSC}$		1	2	3	mA
Oscillation frequency	f_{OSC}	C_{OSC}=1000pF	-	28	-	kHz
■ FR DEAD TIME BLOC (FRC PIN)						
High level voltage	V_{HFRC}		3.15	3.5	3.85	V
Low level voltage	V_{LFRC}		0.9	1.0	1.2	V
FRC charge current	I_{CHGFRC}		16	26	36	uA
FRC discharge current	$I_{DCHGFRC}$		8	18	28	uA
FRC dead band time1	t_{DFRC1}	C_{FRC}=1uF	-	140	-	ms
FRC dead band time2	t_{DFRC2}	C_{FRC}=1uF	-	100	-	ms
■ CONTOROL INPUT BLOCK (FR, BR, DEC, N1, N2, S/S PIN)						
Input High level current	I_{HIN}	V_{IN}=4.5V,per each input	25	40	60	uA
Input low level current	I_{LIN}	V_{IN}=0V,per each input	-	-	1	uA
Pull-down resistance	R_{IN}		-	110	-	kΩ

■ PIN OPERATIONAL CONDITIONS

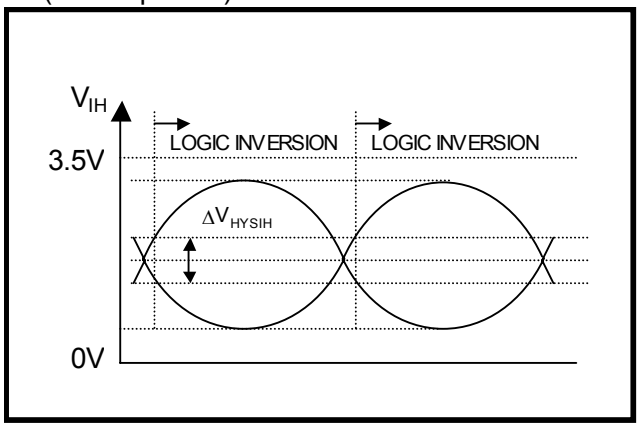
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
■ HALLAMP INPUT (H1+, H1-, H2+, H2-, H3+, H3- PIN)						
Hall Input Sensitivity	ΔV_{MIH}	Peak to peak	0.1	-	-	V
Hall Input voltage range	V_{ICMIH}		0	-	3.5	V
■ CONTOROL INPUT (FR, BR, DEC, N1, N2, S/S PIN)						
High level voltage	V_{HIN}		2	-	5	V
Low level voltage	V_{LIN}		0	-	0.8	V
■ VERR INPUT (VERR PIN)						
Input voltage range	$V_{ICMVERR}$		0	-	4.5	V

■ PIN / CIRCUIT OPERATIONAL DEFINITION

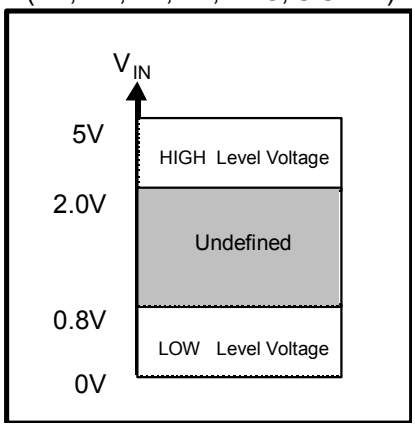
◆ Hall Input Pin Input Common-Mode Voltage Definition (Hall Amp Block)



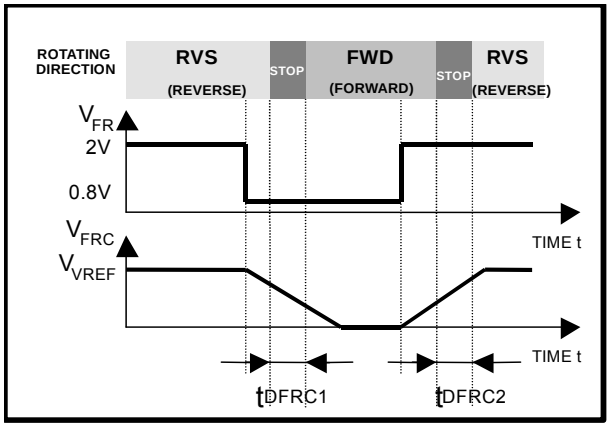
◆ Hall Input Hysteresis Voltage Definition (Hall Amp Block)



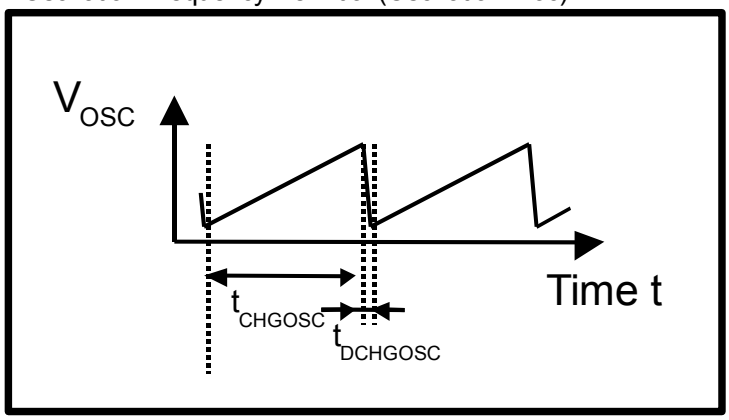
◆ Input pins thresh operational Definition (FR, BR, N1, N2, DEC, S/S PIN)



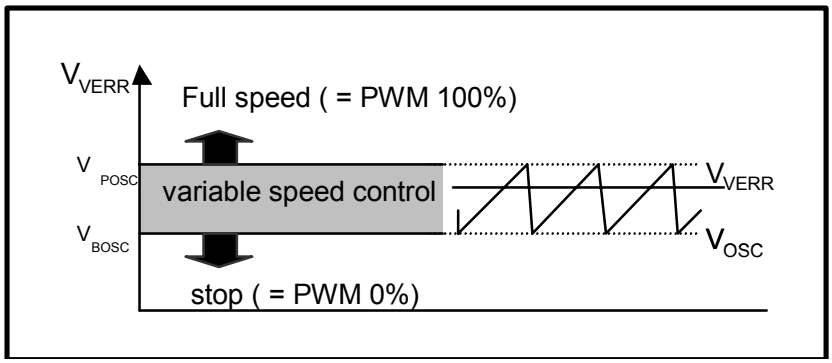
◆ FR Dead Time Definition (FR Dead Time Block)



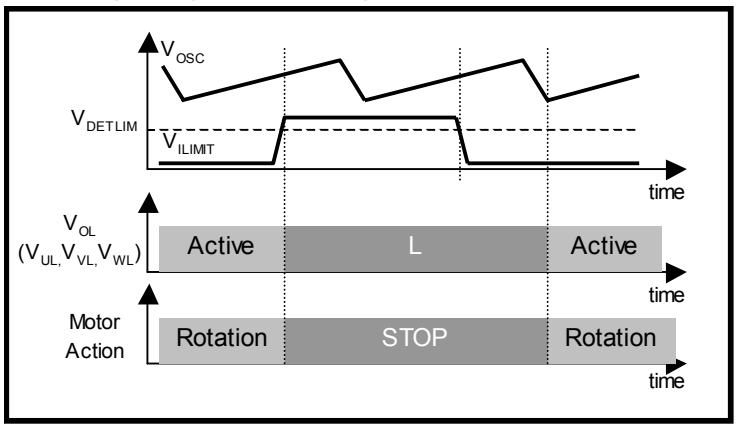
◆Oscillation Frequency Definition(Oscillation Bloc)



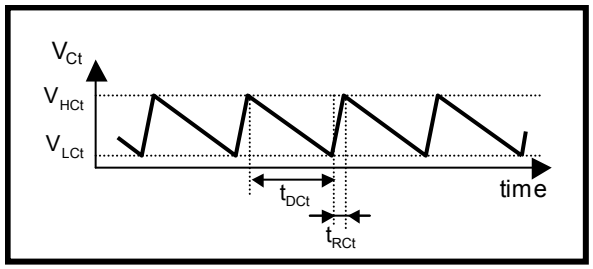
◆ PWM 100% Sensory Voltage / PWM 100% Sensory Voltage Definition (Error Amplifier Block)



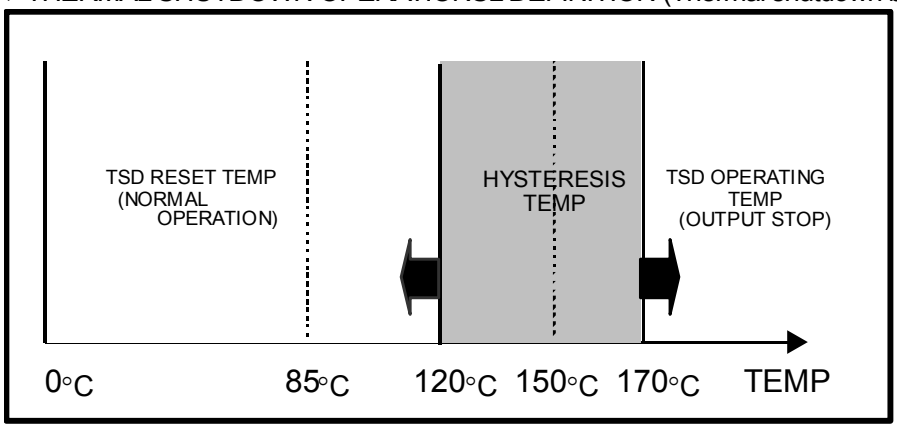
◆ Sensing Voltage/ Reset Voltage Definition (Over Current Sensing Block)



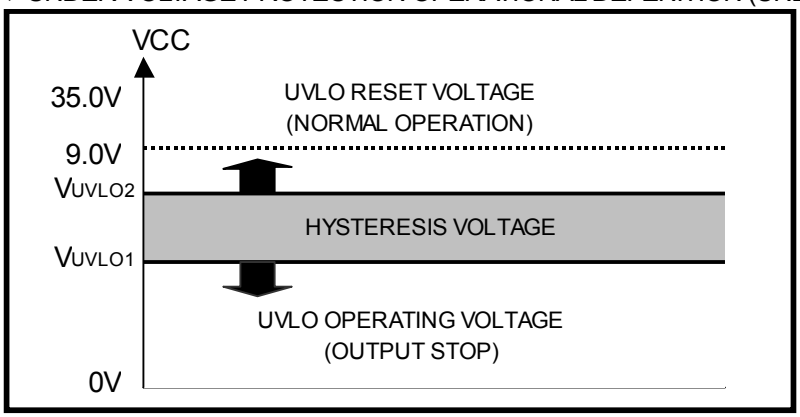
◆ Lock Protection Detection/ Reset Time Definition (Lock Protection Block)



◆ THERMAL SHUTDOWN OPERATIONSL DEFINITION (Thermal shutdown block)



◆ UNDER VOLTAGE PROTECTION OPERATIONAL DEFENITION (UNDER VOLTAGE PROTECTION BLOCK)



■ TRUTH TABLE

◆ INPUT VS OUTPUT TRUTH TABLE1 (DEC=L, H1+>H1-, H2+>H2-, H3+>H3-="H", Don't Care="X")

H1	H2	H3	BR	TSD	UVLO	S/S	VERR	FR	DEC	N1	N2	UH	VH	WH	UL	VL	WL	FG	VREF	COMMENT
H	L	L	L	OFF	OFF	L	H	L	L	L	L	Hi-Z	Hi-Z	L	H	L	L	L	ON	FR="L" FWD Rotation
H	H	L										Hi-Z	Hi-Z	L	L	H	L	Hi-Z		
L	H	L										L	Hi-Z	Hi-Z	L	H	L	L		
L	H	H										L	Hi-Z	Hi-Z	L	L	H	Hi-Z		
L	L	H										Hi-Z	L	Hi-Z	L	L	H	L		
H	L	H										Hi-Z	L	Hi-Z	H	L	L	Hi-Z		
H	L	L	L	OFF	OFF	L	H	H	L	L	L	L	Hi-Z	Hi-Z	L	L	H	L	ON	FR="H" REV Rotation
H	H	L										Hi-Z	L	Hi-Z	L	L	H	Hi-Z		
L	H	L										Hi-Z	L	Hi-Z	H	L	L	L		
L	H	H										Hi-Z	Hi-Z	L	H	L	L	Hi-Z		
L	L	H										Hi-Z	Hi-Z	L	L	H	L	L		
H	L	H										L	Hi-Z	Hi-Z	L	H	L	Hi-Z		
H	L	L	L	OFF	OFF	L	H	X	L	L	L	Hi-Z	Hi-Z	L	H	L	L	L	ON	FRC="L" FWD Rotation
H	H	L										Hi-Z	Hi-Z	L	L	H	L	Hi-Z		
L	H	L										L	Hi-Z	Hi-Z	L	H	L	L		
L	H	H										L	Hi-Z	Hi-Z	L	L	H	Hi-Z		
L	L	H										Hi-Z	L	Hi-Z	L	L	H	L		
H	L	H										Hi-Z	L	Hi-Z	H	L	L	Hi-Z		
H	L	L	L	OFF	OFF	L	X	X	L	L	L	Hi-Z	Hi-Z	L	L	L	L	L	ON	LOCK PROTECTION Operation
H	H	L										Hi-Z	Hi-Z	L				Hi-Z		
L	H	L										L	Hi-Z	Hi-Z				L		
L	H	H										L	Hi-Z	Hi-Z				Hi-Z		
L	L	H										Hi-Z	L	Hi-Z				L		
H	L	H										Hi-Z	L	Hi-Z				Hi-Z		
H	L	L	L	OFF	OFF	L	X	X	L	L	L	Hi-Z	Hi-Z	L	L	L	L	L	ON	OVER CURRENT Operation
H	H	L										Hi-Z	Hi-Z	L				Hi-Z		
L	H	L										L	Hi-Z	Hi-Z				L		
L	H	H										L	Hi-Z	Hi-Z				Hi-Z		
L	L	H										Hi-Z	L	Hi-Z				L		
H	L	H										Hi-Z	L	Hi-Z				Hi-Z		
H	L	L	L	OFF	OFF	L	**L**	X	L	L	L	Hi-Z	Hi-Z	L	L	L	L	L	ON	VERR="L" PWM Operation
H	H	L										Hi-Z	Hi-Z	L				Hi-Z		
L	H	L										L	Hi-Z	Hi-Z				L		
L	H	H										L	Hi-Z	Hi-Z				Hi-Z		
L	L	H										Hi-Z	L	Hi-Z				L		
H	L	H										Hi-Z	L	Hi-Z				Hi-Z		
H	L	L	L	X	X	**H**	X	X	L	L	L	Hi-Z	Hi-Z	Hi-Z	L	L	L	L	ON	S/S="H" STOP Operation
H	H	L																Hi-Z		
L	H	L																L		
L	H	H																Hi-Z		
L	L	H																L		
H	L	H																Hi-Z		
H	L	L	L	X	**ON**	X	X	X	L	L	L	Hi-Z	Hi-Z	Hi-Z	L	L	L	L	ON	UVLO=ON UVLO Operation
H	H	L																Hi-Z		
L	H	L																L		
L	H	H																Hi-Z		
L	L	H																L		
H	L	H																Hi-Z		
H	L	L	L	**ON**	X	X	X	X	L	L	L	Hi-Z	Hi-Z	Hi-Z	L	L	L	L	ON	TSD=ON TSD Operation
H	H	L																Hi-Z		
L	H	L																L		
L	H	H																Hi-Z		
L	L	H																L		
H	L	H																Hi-Z		
H	L	L	**H**	X	X	X	X	X	L	L	L	L	L	L	L	L	L	L	ON	BR="H" BRAKE Operation
H	H	L																Hi-Z		
L	H	L																L		
L	H	H																Hi-Z		
L	L	H																L		
H	L	H																Hi-Z		

◆ INPUT VS OUTPUT TRUTH TABLE2 (DEC=L, Invalid Code Pattern)
(H1+>H1-, H2+>H2-, H3+>H3-="H", Don't Care="X")

H1	H2	H3	BR	TSD	UVLO	S/S	VERR	FR	DEC	N1	N2	UH	VH	WH	UL	VL	WL	FG	VREF	COMMENT
H	**H**	**H**	L	X	X	X	X	X	L	L	L	Hi-Z	Hi-Z	Hi-Z	L	L	L	L	ON	Invalid Code Pattern
L	**L**	**L**																Hi-Z		
H	**H**	**H**	**H**	X	X	X	X	X	L	L	L	L	L	L	L	L	L	L	ON	Invalid Code Pattern BR="H" BARKE Operation
L	**L**	**L**																Hi-Z		

◆ INPUT VS OUTPUT TRUTH TABLE3 (DEC=H, H1+>H1-, H2+>H2-, H3+>H3-="H", Don't Care="X")

H1	H2	H3	BR	TSD	UVLO	S/S	VERR	FR	DEC	N1	N2	UH	VH	WH	UL	VL	WL	FG	VREF	COMMENT
H	L	L	L	OFF	OFF	L	H	L	H	L	L	Hi-Z	Hi-Z	L	H	L	L	Hi-Z	ON	FR="L" FWD Rotation
H	H	L										Hi-Z	Hi-Z	L	L	H	L	L		
H	H	H										L	Hi-Z	Hi-Z	L	H	L	Hi-Z		
L	H	H										L	Hi-Z	Hi-Z	L	L	H	L		
L	L	H										Hi-Z	L	Hi-Z	L	L	H	Hi-Z		
L	L	L										Hi-Z	L	Hi-Z	H	L	L	L		
H	L	L	L	OFF	OFF	L	H	H	H	L	L	L	Hi-Z	Hi-Z	L	L	H	Hi-Z	ON	FR="H" REV Rotation
H	H	L										Hi-Z	L	Hi-Z	L	L	H	L		
H	H	H										Hi-Z	L	Hi-Z	H	L	L	Hi-Z		
L	H	H										Hi-Z	Hi-Z	L	H	L	L	L		
L	L	H										Hi-Z	Hi-Z	L	L	H	L	Hi-Z		
L	L	L										L	Hi-Z	Hi-Z	L	H	L	L		
H	L	L	L	OFF	OFF	L	X	X	H	L	L	Hi-Z	Hi-Z	L	L	L	L	Hi-Z	ON	LOCK PROTECTION Operation
H	H	L										Hi-Z	Hi-Z	L				L		
H	H	H										L	Hi-Z	Hi-Z				Hi-Z		
L	H	H										L	Hi-Z	Hi-Z				L		
L	L	H										Hi-Z	L	Hi-Z				Hi-Z		
L	L	L										Hi-Z	L	Hi-Z				L		
H	L	L	L	OFF	OFF	L	X	X	H	L	L	Hi-Z	Hi-Z	L	L	L	L	Hi-Z	ON	OVER CURRENT Operation
H	H	L										Hi-Z	Hi-Z	L				L		
H	H	H										L	Hi-Z	Hi-Z				Hi-Z		
L	H	H										L	Hi-Z	Hi-Z				L		
L	L	H										Hi-Z	L	Hi-Z				Hi-Z		
L	L	L										Hi-Z	L	Hi-Z				L		
H	L	L	L	OFF	OFF	L	**L**	X	H	L	L	Hi-Z	Hi-Z	L	L	L	L	Hi-Z	ON	VERR="L" PWM Operation
H	H	L										Hi-Z	Hi-Z	L				L		
H	H	H										L	Hi-Z	Hi-Z				Hi-Z		
L	H	H										L	Hi-Z	Hi-Z				L		
L	L	H										Hi-Z	L	Hi-Z				Hi-Z		
L	L	L										Hi-Z	L	Hi-Z				L		
H	L	L	L	X	X	**H**	X	X	H	L	L	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	ON	S/S="H" STOP Operation
H	H	L																L		
H	H	H																Hi-Z		
L	H	H																L		
L	L	H																Hi-Z		
L	L	L																L		
H	L	L	L	X	**ON**	X	X	X	H	L	L	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	ON	UVLO=ON UVLO Operation
H	H	L																L		
H	H	H																Hi-Z		
L	H	H																L		
L	L	H																Hi-Z		
L	L	L																L		
H	L	L	L	**ON**	X	X	X	X	H	L	L	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	ON	TSD=ON TSD Operation
H	H	L																L		
H	H	H																Hi-Z		
L	H	H																L		
L	L	H																Hi-Z		
L	L	L																L		
H	L	L	**H**	X	X	X	X	X	H	L	L	L	L	L	L	L	L	Hi-Z	ON	BR="H" BRAKE Operation
H	H	L																L		
H	H	H																Hi-Z		
L	H	H																L		
L	L	H																Hi-Z		
L	L	L																L		

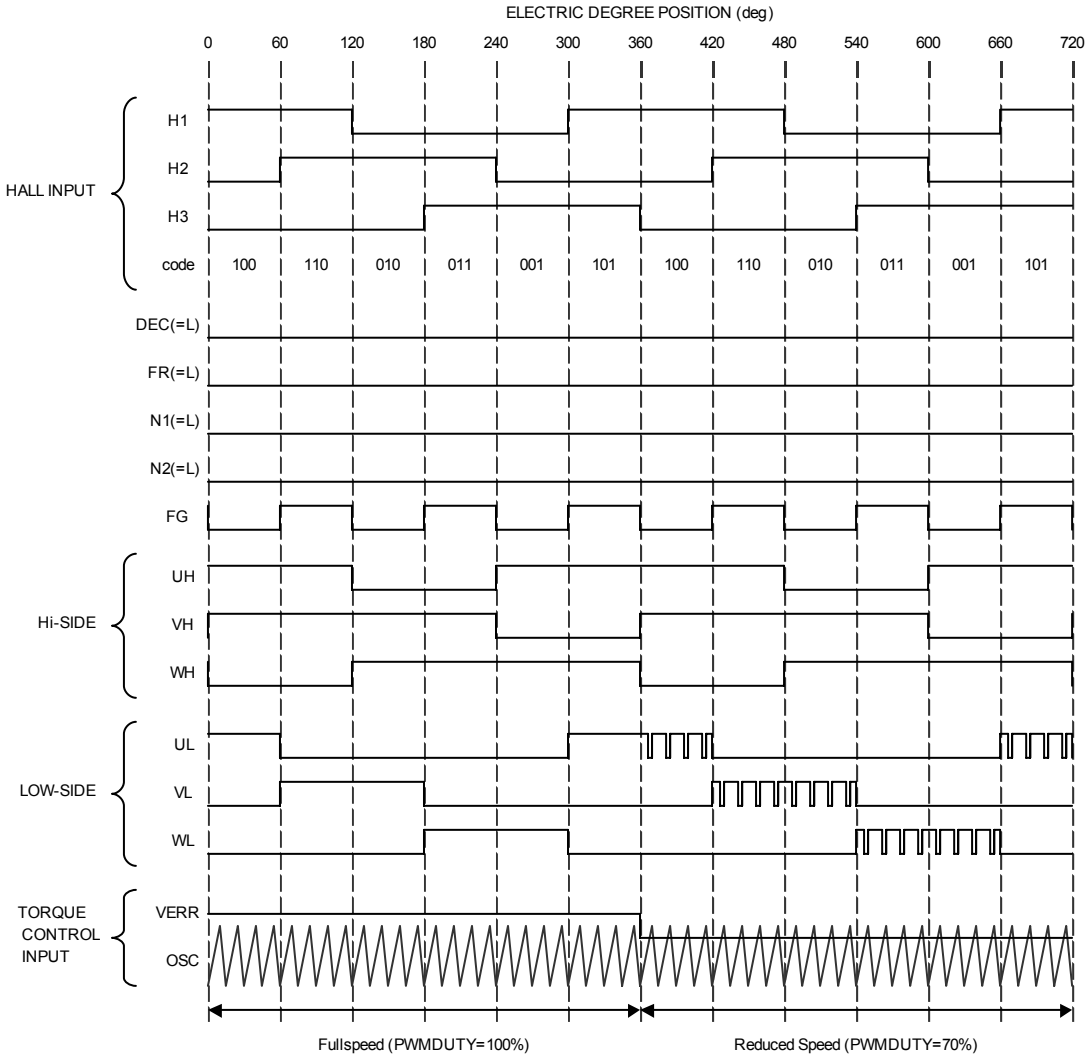
◆ INPUT VS OUTPUT TRUTH TABLE4 (DEC=H, Invalid Code Pattern)
(H1+>H1-, H2+>H2-,H3+>H3-="H", Don't Care="X")

H1	H2	H3	BR	TSD	UVLO	S/S	VERR	FR	DEC	N1	N2	UH	VH	WH	UL	VL	WL	FG	VREF	COMMENT
H	**L**	**H**	L	X	X	X	X	X	H	L	L	Hi-Z	Hi-Z	Hi-Z	L	L	L	L	ON	Invalid Code Pattern
L	**H**	**L**																Hi-Z		
H	**L**	**H**	**H**	X	X	X	X	X	H	L	L	L	L	L	L	L	L	L	ON	Invalid Code Pattern BR="H" BARKE Operation
L	**H**	**L**																Hi-Z		

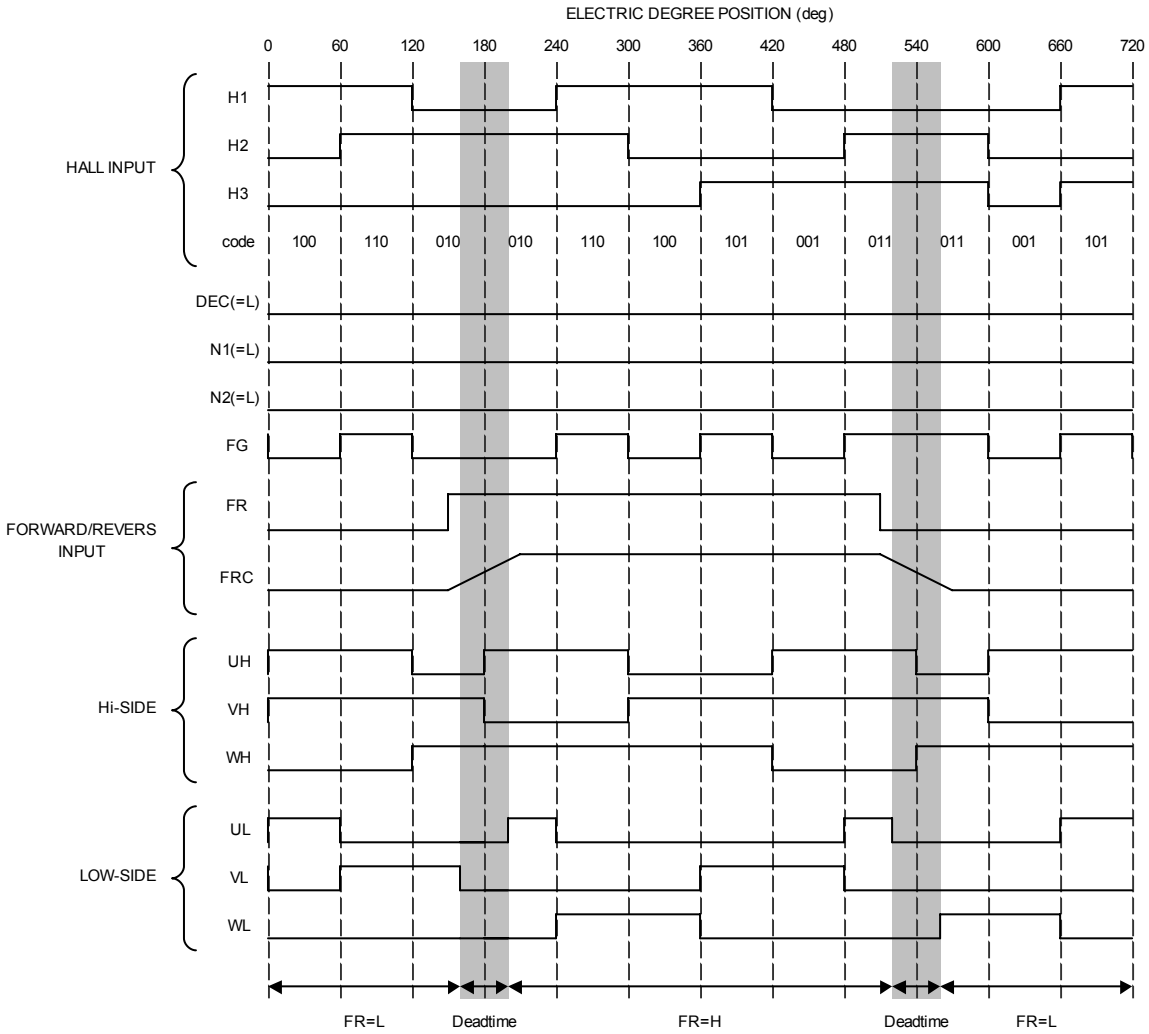
■ TIMING CHART

※ Codes used in Hall input:
Logics of H1, H2, H3 are expressed with each 3-colum starting from the top.
High Logic = 1, Low Logic = 0

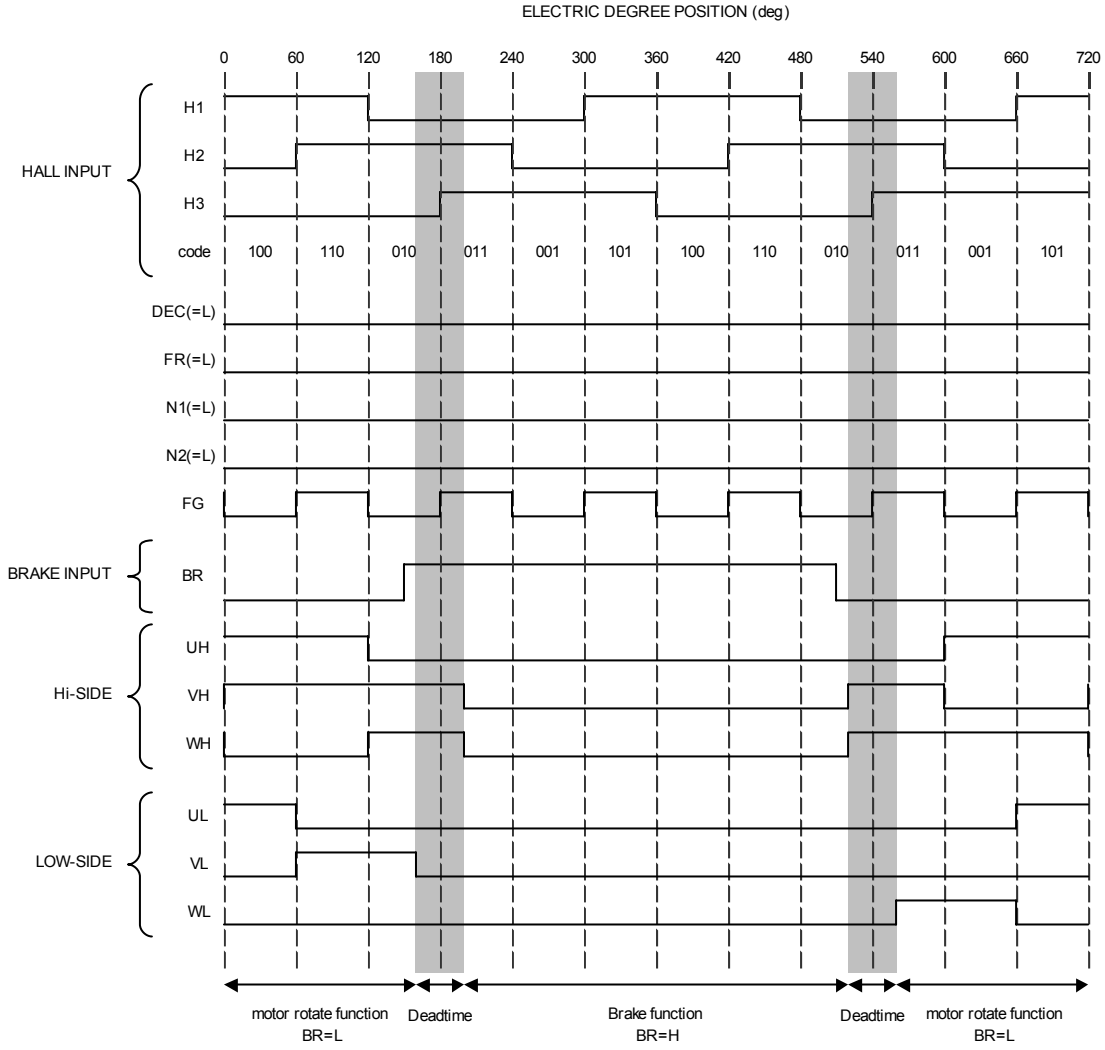
1. Normal Function→PWM Function



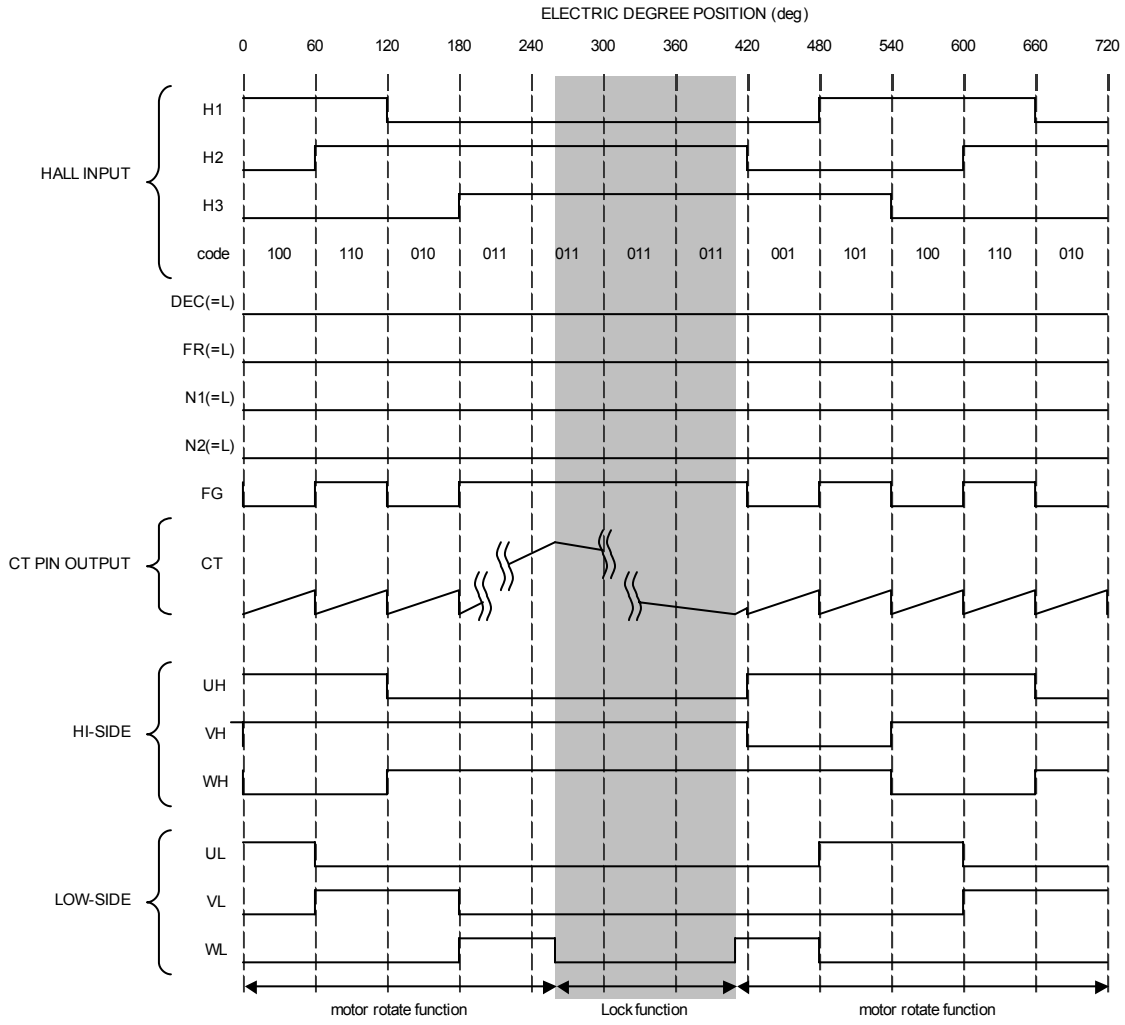
2. NORMAL FUNCTION→FORWARD/REVERSE SWITCHING while rotating



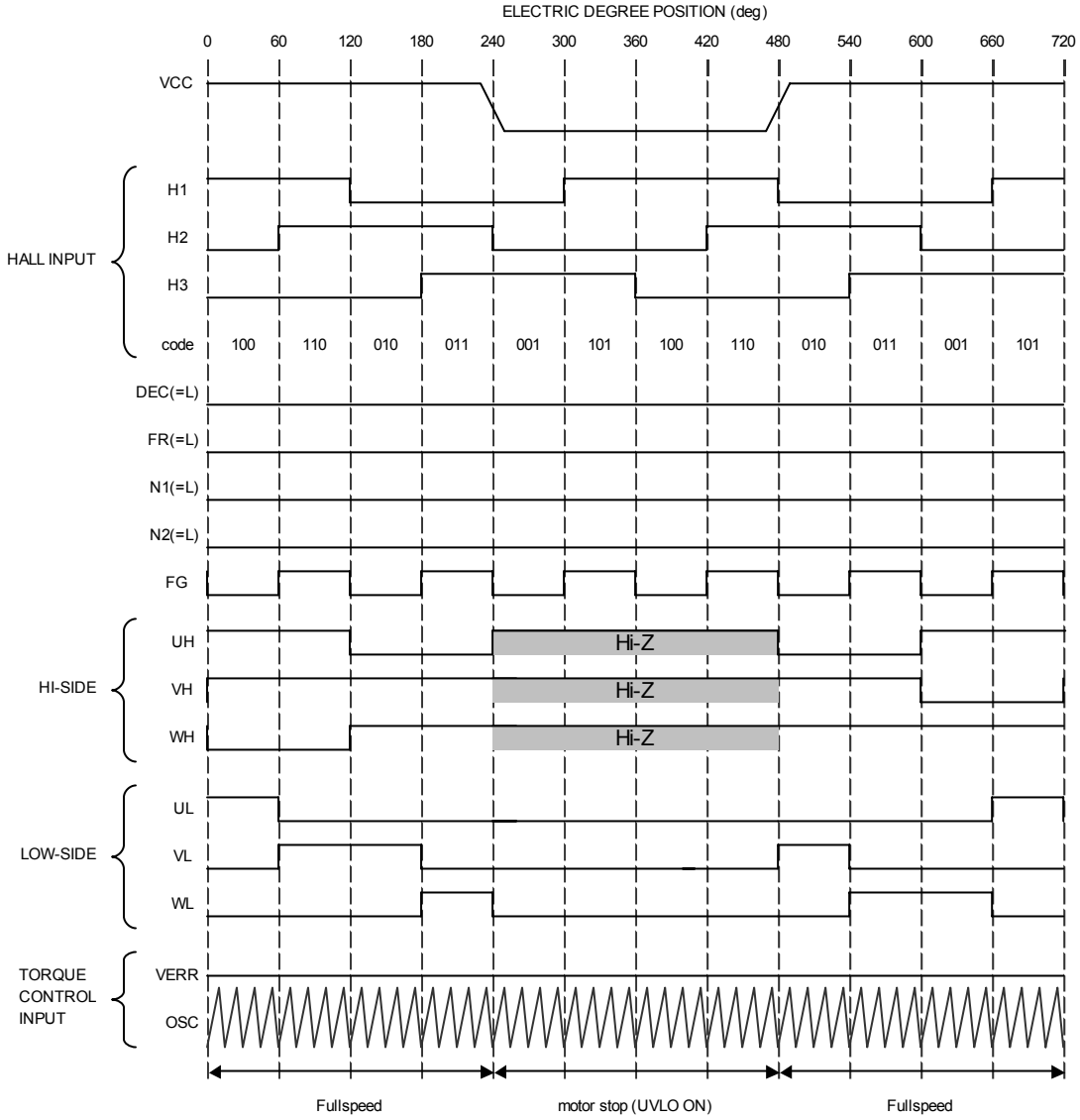
3. NORMAL FUNCTION→BRAKE CONTROL→BRAKE RESET



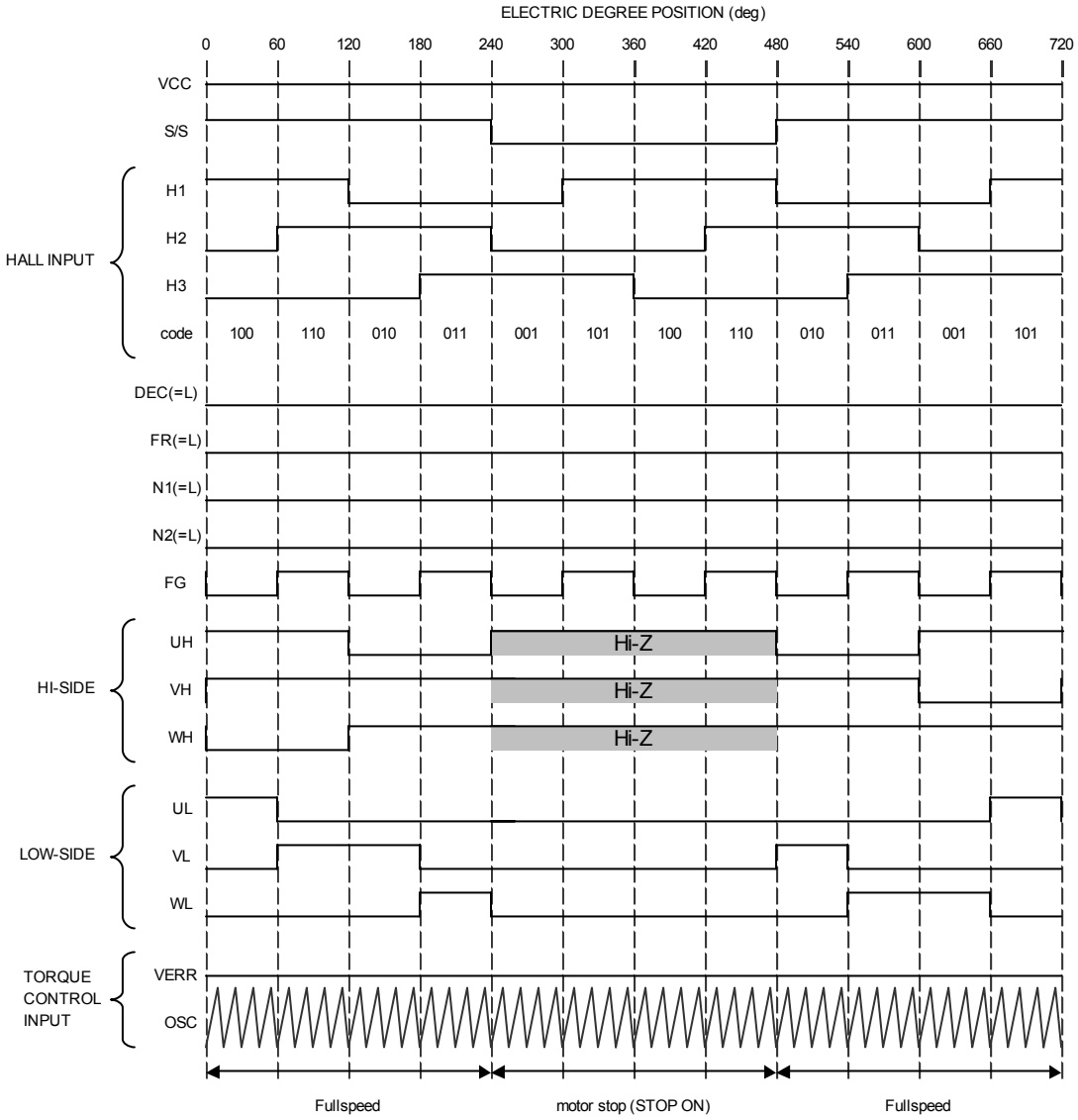
4. NORMAL FUNCTION→LOCK PROTECTION→LOCK RESET



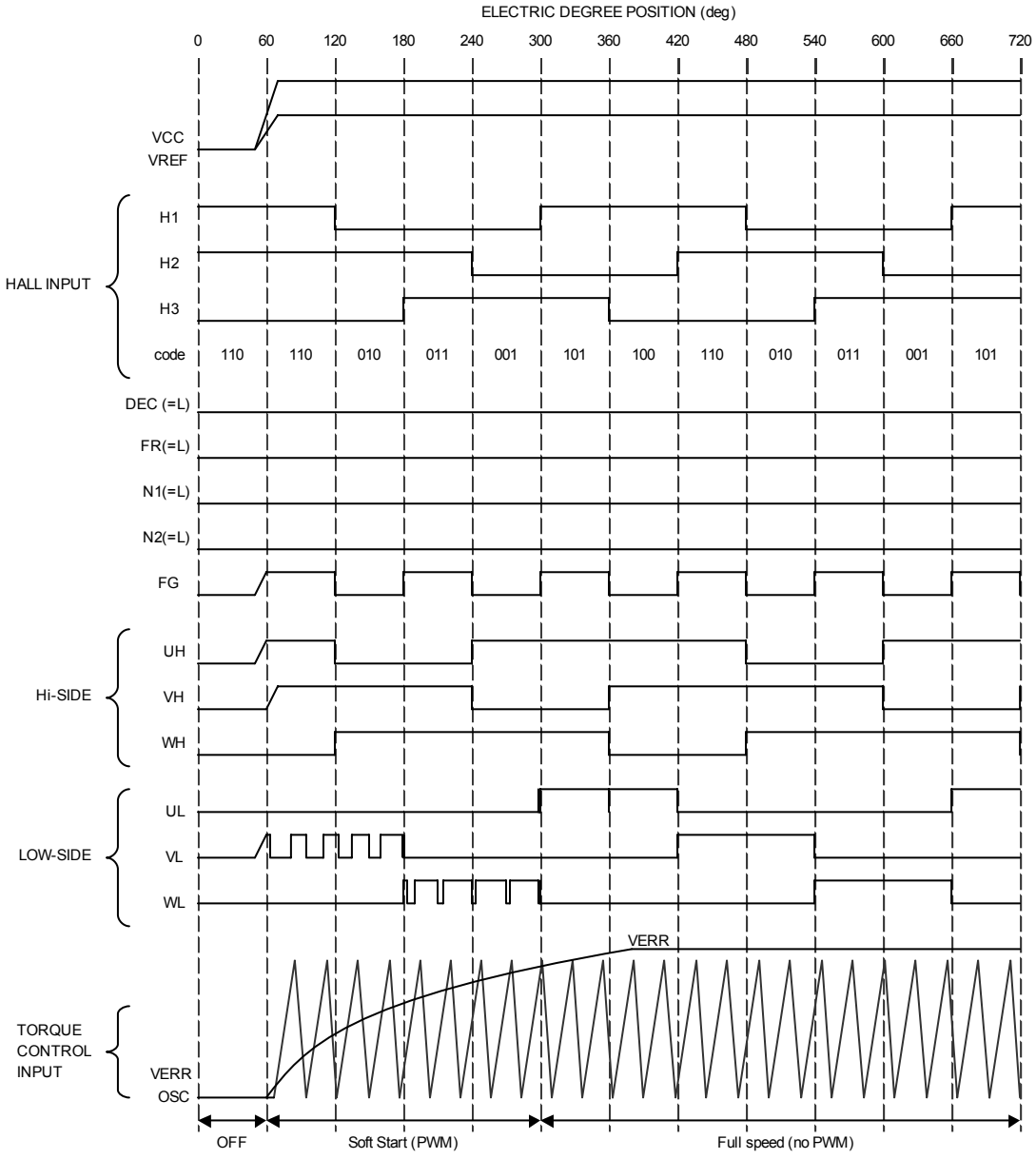
5. NORMAL FUNCTION→LOW VOLTAGE PROTECTION→NORMAL FUNCTION



6. NORMAL FUNCTION→STOP FUNCTION (S/S=H)→NORMAL FUNCTION

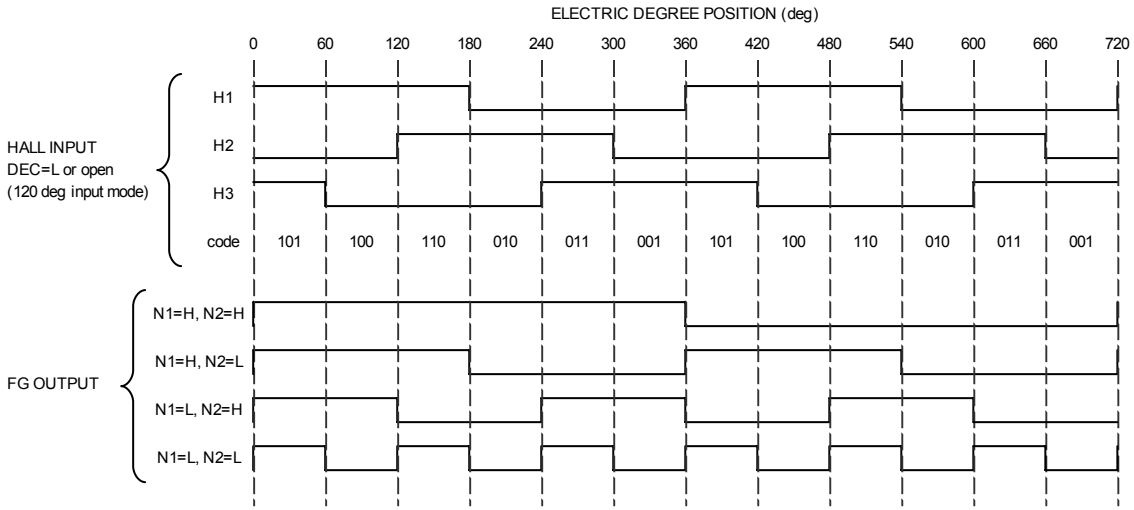


7. SOFT START FUNCTION

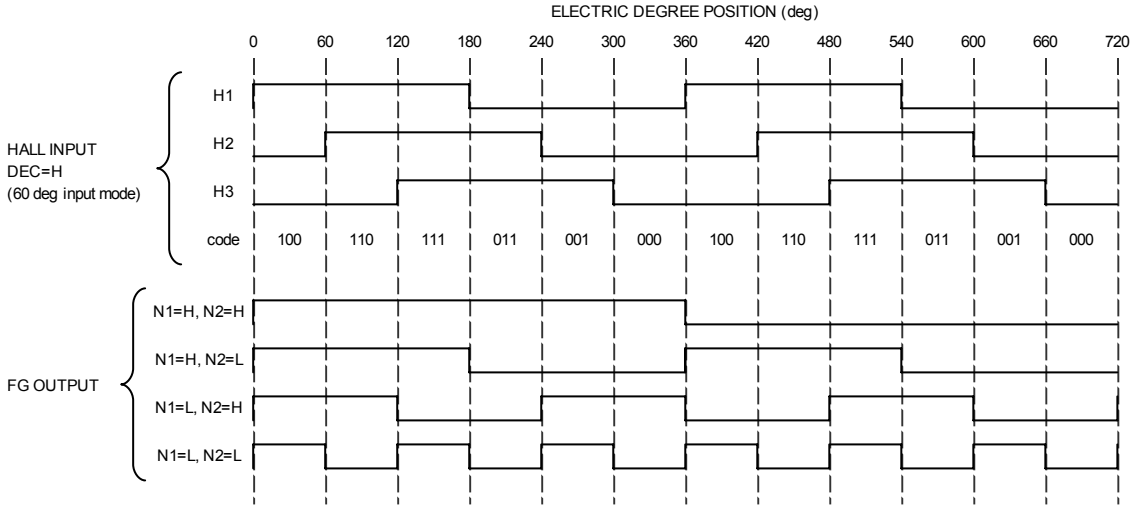


8. FG OUTPUT TIMING CHART

OUTPUT TIMING CHART 1 (120 deg Input Mode)



OUTPUT TIMING CHART 2 (60 deg Input Mode)



* When the status of N1/N2 is H/H or L/H, FG output is not synchronized with Hall input, because FG output is produced by using a frequency divider.

■ FUNCTION DESCRIPTION

◆ Lock Protection Block – Detect/Reset Time

Lock Protection can be done by charging/discharging to the capacitor C_{Ct}. Lock Protection Detect time (t_{DCt}) and Reset time (t_{RCt}) are determined by the value of either Ct charging current (I_{CHGCt}) or Ct discharging current (I_{DCHGCt}) and the value of the external capacitor C_{Ct}. To adjust Detect/Reset Time, change the value of C_{Ct}. The calculation formula for Detect/Reset Time can be described in equation below: adjustment range for C_{Ct} is 0.1μF to 10μF.

	Symbol	Formula	Comments
Detect Time	t_{DCt}	$t_{DCt} \cong 4.6 \cdot 10^6 \cdot C_{Ct}$	
Reset Time	t_{RCt}	$t_{RCt} \cong 0.46 \cdot 10^6 \cdot C_{Ct}$	

Figure1: Lock Protection Detect/ Reset Time Calculating Formula

When the motor is rotating, electric charge of C_{Ct} capacitor discharging is produced repeatedly by input from hall signal. However, when we set the motor to low speed using the speed control application, input time from hall signal is longer, with this, Ct voltage level will increase and malfunction can be expected. When this occurs, it is recommended to add Ct discharge circuit by using FG signal output. Please refer to typical application circuit 2.

◆ Reference Voltage Block – How to use VREF

When using VREF pin, make sure that it is not oscillating.
Use the recommended VCC operational condition.

◆ Hall Amp Block - Capacitor

Input from hall signal requires more than that of the Hall Input Sensitivity (ΔV_{MIH}=100mV).
Taking measures in keeping noise immunity, when using FG output, FG jitter can be expected. When this occurs, it is recommended to add capacitors more than 0.01μF between Hall input pins.

◆ Hall Amp Block – How to use Hall IC

Hall input pins H1-, H2- and H3- are biased to VREF/2.
To keep Hall IC Output voltage within the Hall Input voltage range (V_{ICMIH}), it needs to add 2 pieces of biased resistor for every H1+, H2+ and H3+ pins.

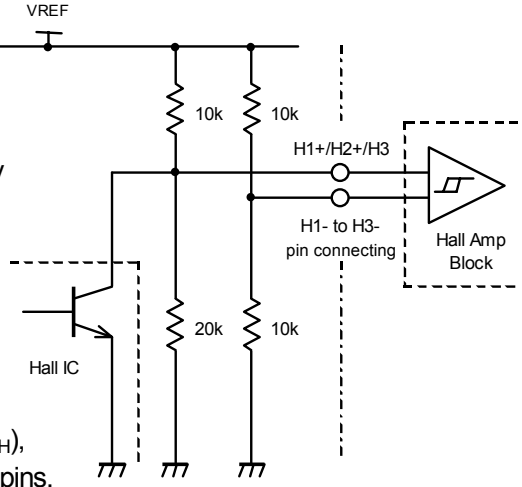


Figure2: Hall IC application

◆ Oscillation Block - Oscillation Frequency

OSC pin produce Oscillating wave by charging/discharging to the capacitor C_{OSC}. Oscillating frequency (f_{OSC}) is modulated by C_{OSC}, and determined by charging time (t_{CHGOSC}) and discharging time ($t_{DCHGOSC}$). The oscillation frequency depends on t_{CHGOSC} in great deal compare to $t_{DCHGOSC}$, so that the calculation formula for oscillation frequency can be described in equation below: adjustment range for C_{OSC} is 330pF to 2200pF.

	Symbol	Formula	Comments
Oscillation Frequency	f_{OSC}	$F_{OSC} \cong 28 \cdot 10^{-6} / C_{OSC}$	

Figure3: Oscillation Frequency Calculating Formula

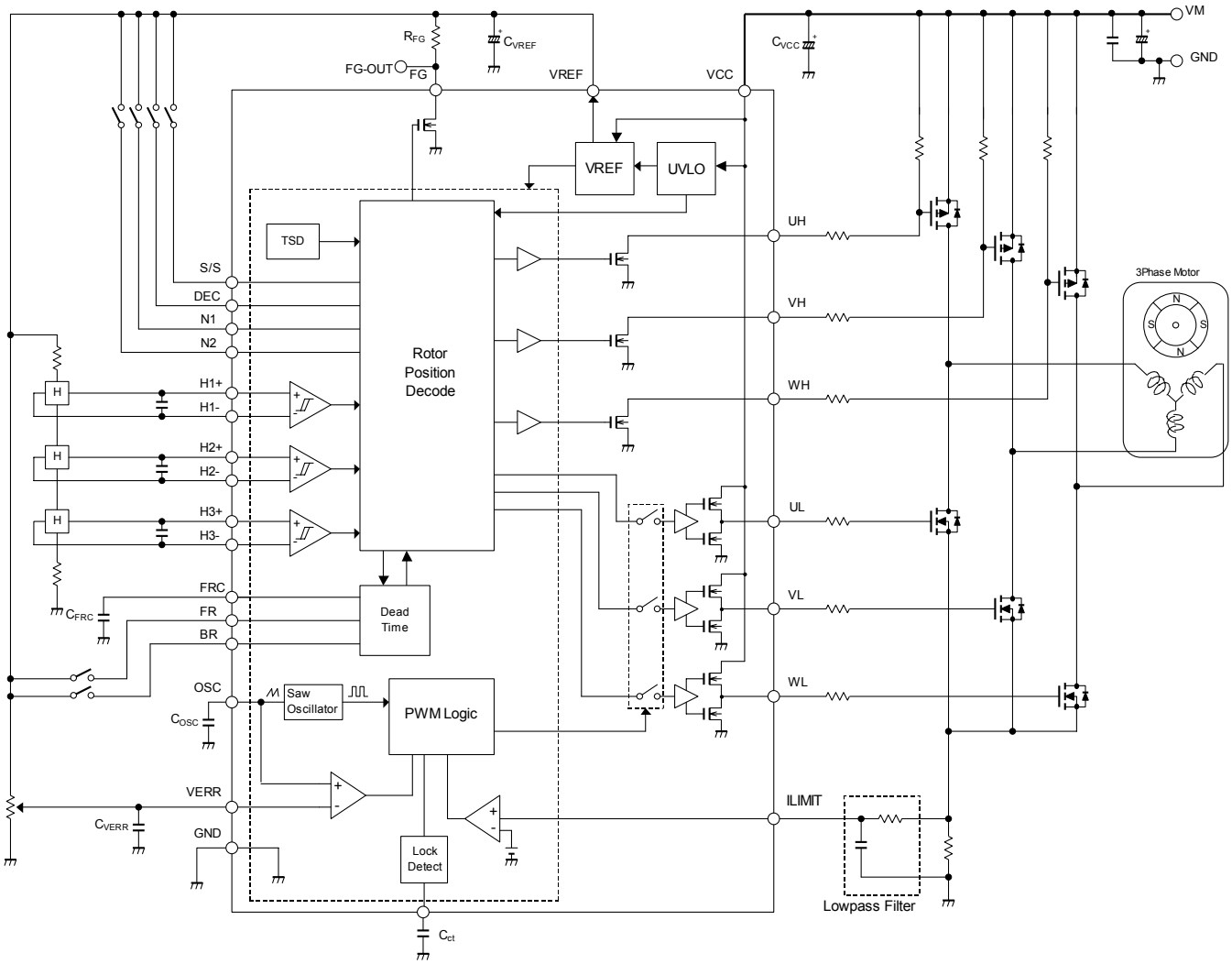
◆ FR Dead Time Block – Dead Band Time

FR Dead band time is divided in two types depending on giving conditions.
The two dead band time are determined by the value of either FRC charged current or FRC discharge current $I_{DCHGFRC}$, and the value of an external capacitor. To adjust the dead band time, change the value of C_{FRC}. FR dead band time can be expressed as following: adjustment range for C_{FRC} is more than 1pF.

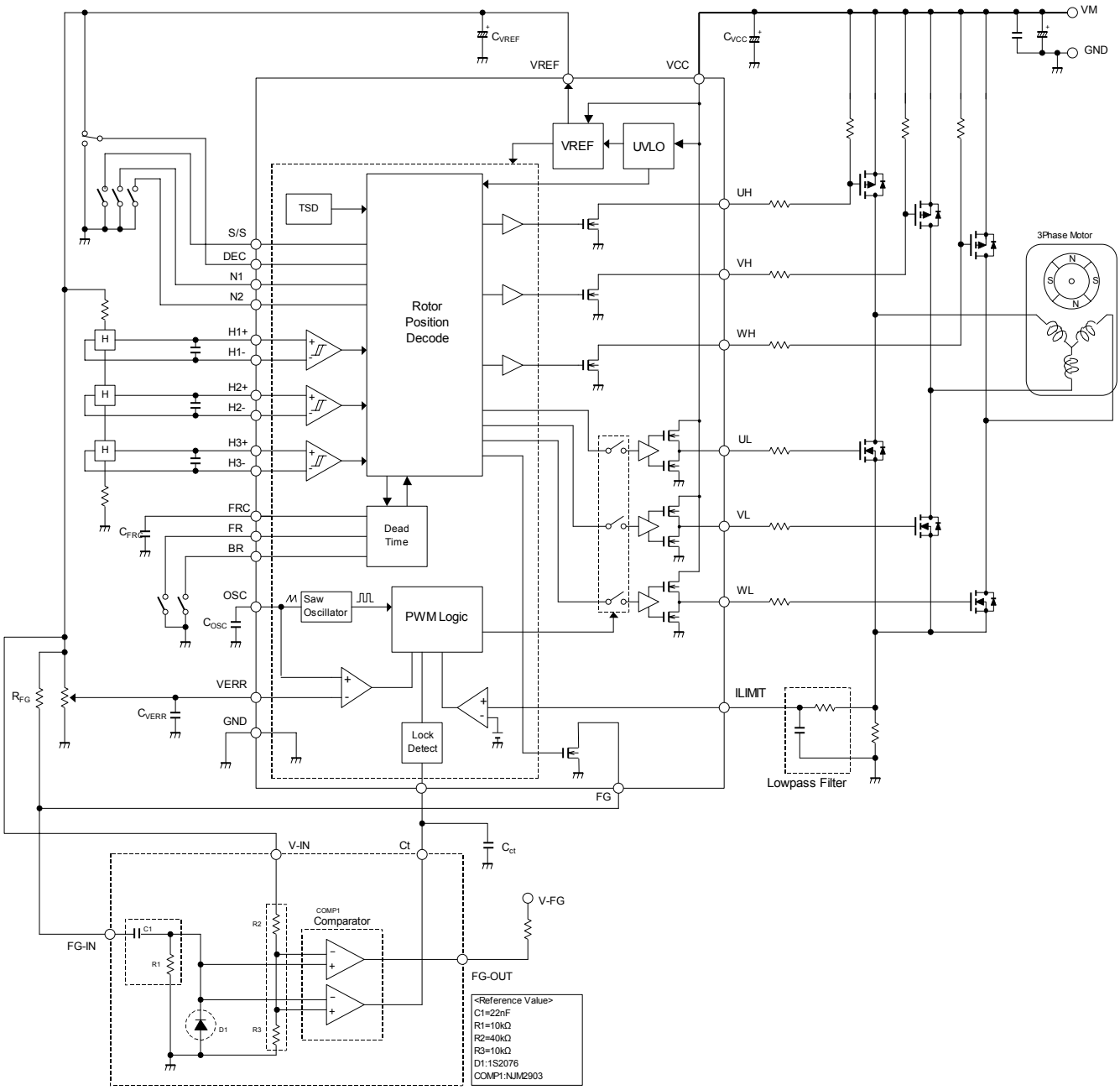
	Symbol	Formula	Comments
FR Dead Band Time1	t_{DFRC1}	$t_{DFRC1} \cong 140 \cdot 10^3 \cdot C_{FRC}$	FR : H → L (open)
FR Dead Band Time2	t_{DFRC2}	$t_{DFRC2} \cong 140 \cdot 10^3 \cdot C_{FRC}$	FR : L (open) → H

Figure4: Dead Band Time Calculating Formula

■ TYPICAL APPLICATION CIRCUIT 1

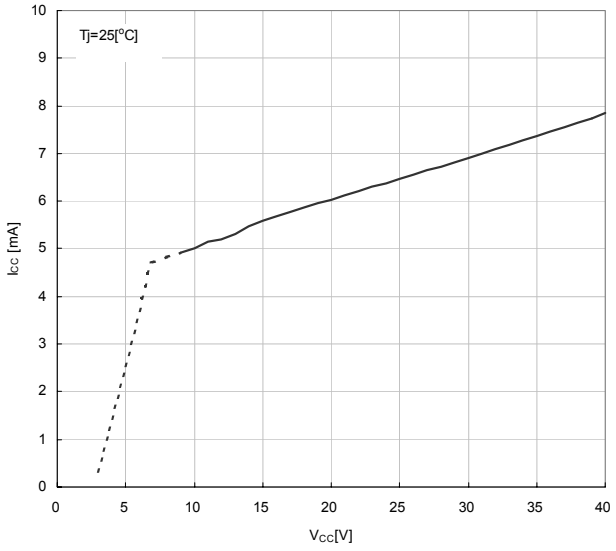


■ TYPICAL APPLICATION CIRCUIT 2

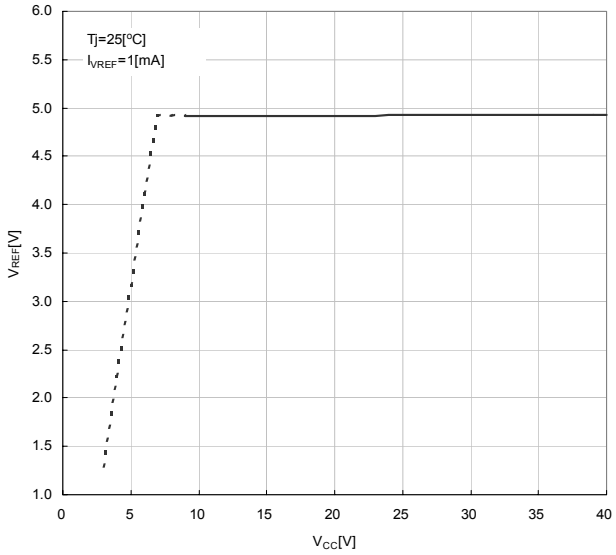


■ TYPICAL CHARACTERISTICS

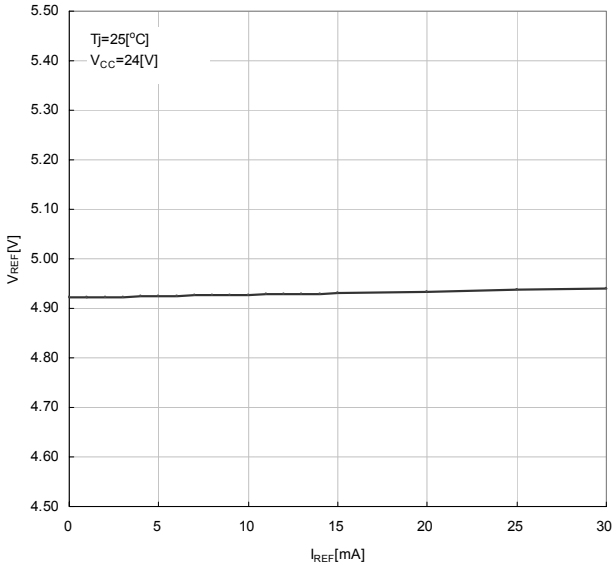
V_{CC} vs I_{CC}



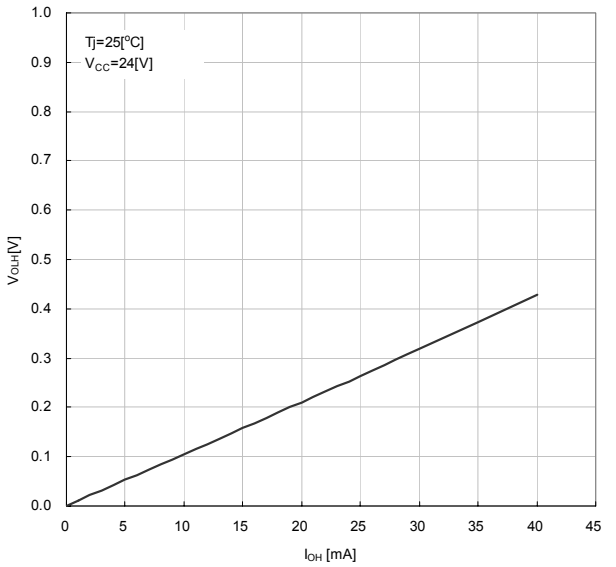
V_{CC} vs V_{REF}



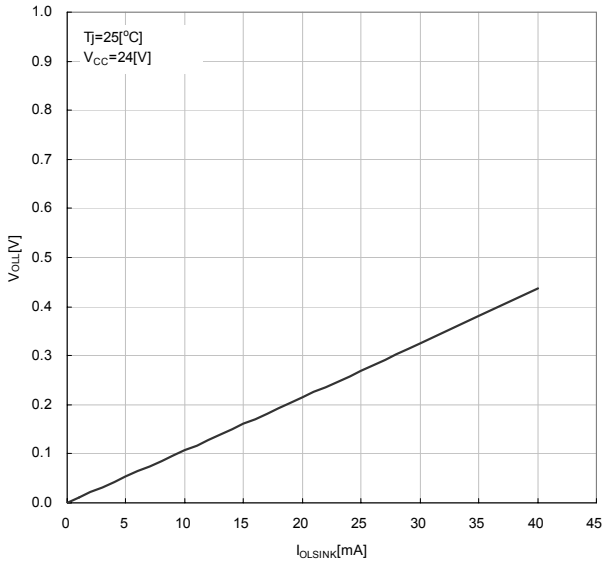
I_{REF} vs V_{REF}



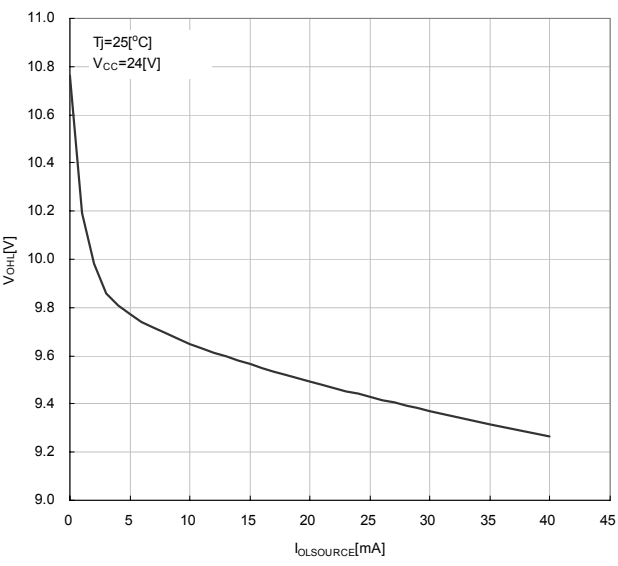
I_{OH} vs V_{OLH}



I_{OLSINK} vs V_{OLL}

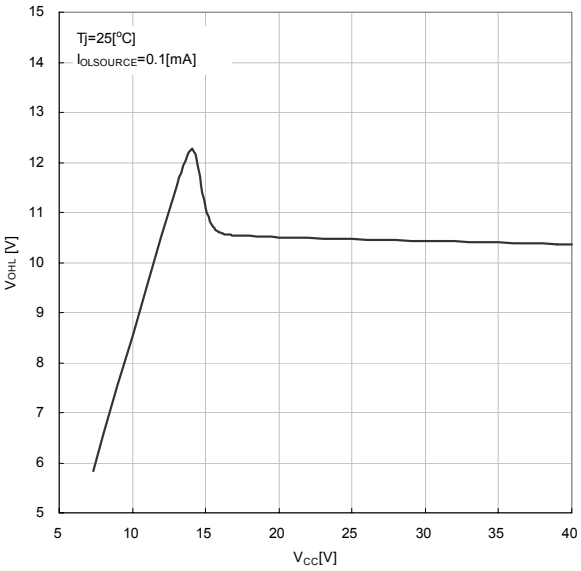


$I_{OLSOURCE}$ vs V_{OHL}

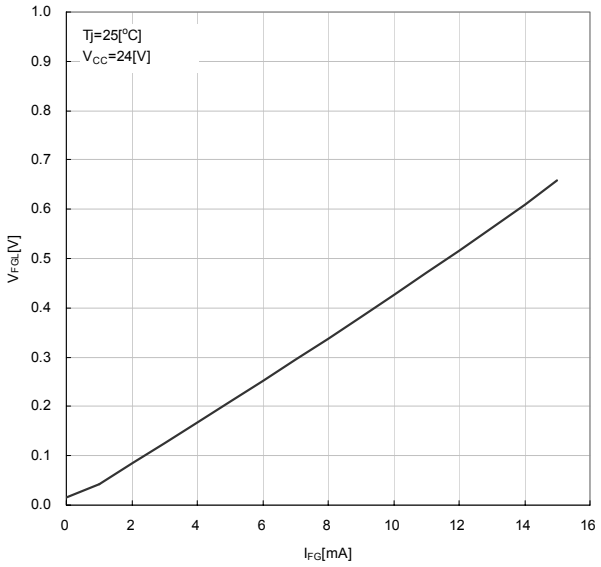


■ TYPICAL CHARACTERISTICS

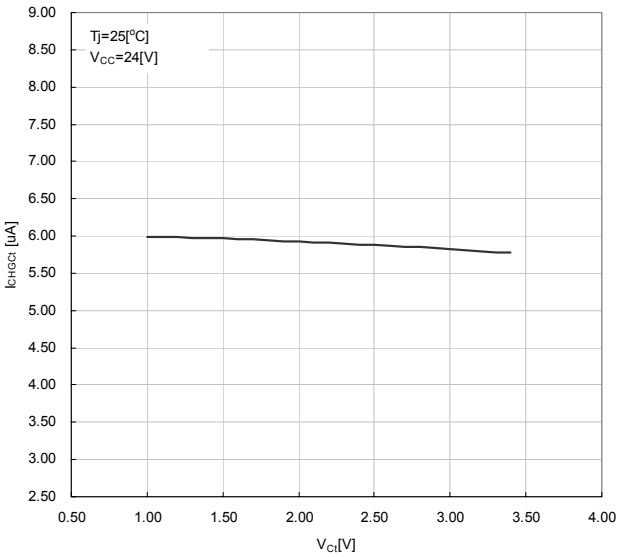
V_{CC} vs V_{OHL}



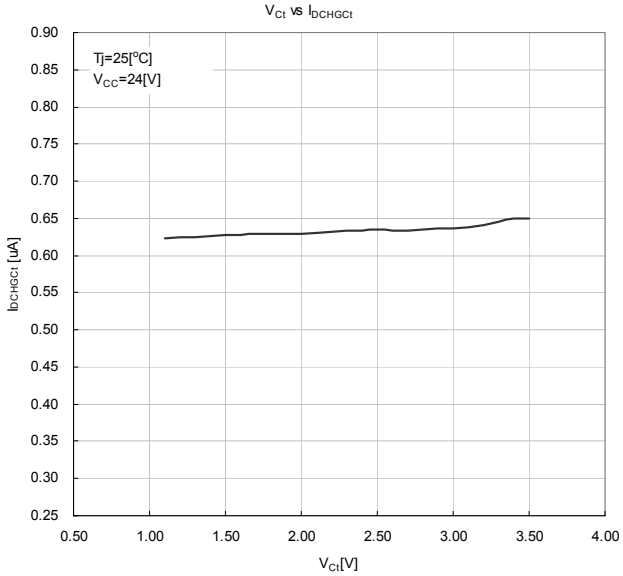
I_{FG} vs V_{FGL}



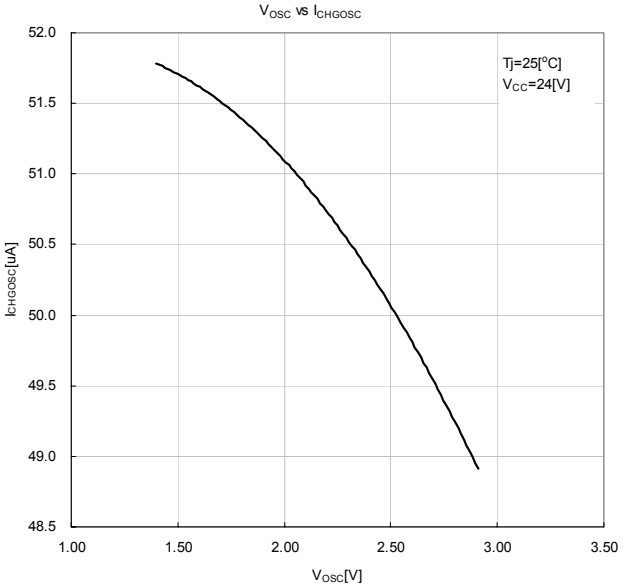
V_{Ct} vs I_{CHGCt}



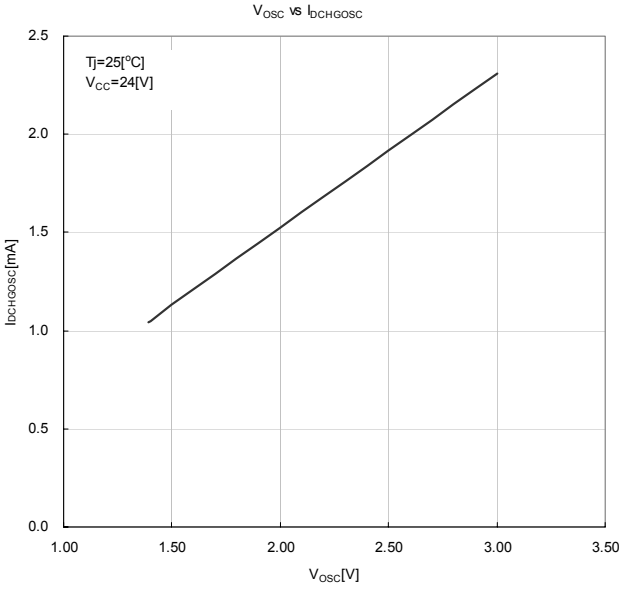
V_{Ct} vs I_{DCHGCt}



V_{OSC} vs I_{CHGOSC}

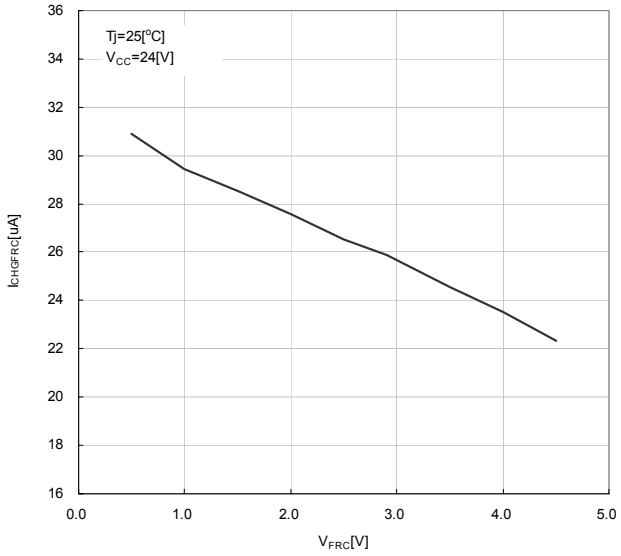


V_{OSC} vs $I_{DCHGOSC}$

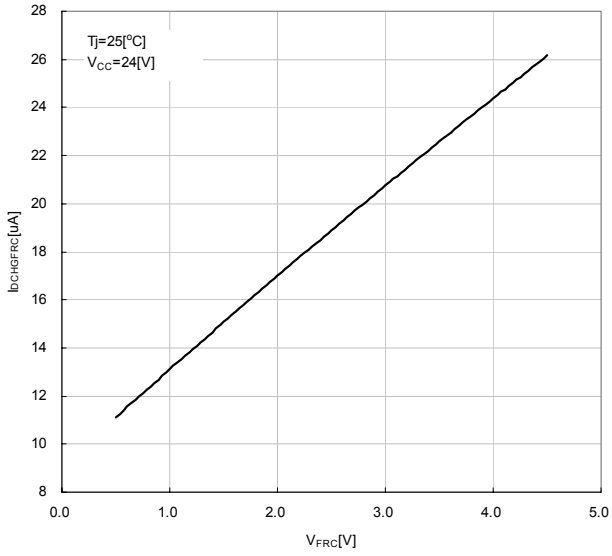


■ TYPICAL CHARACTERISTICS

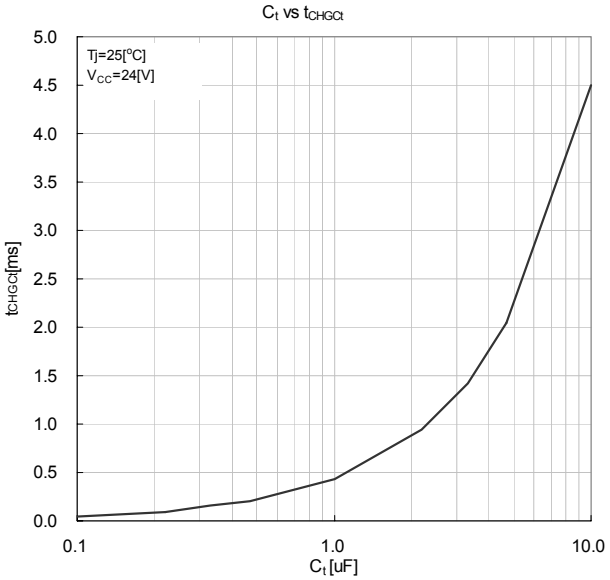
V_{FRC} vs I_{CHGFRC}



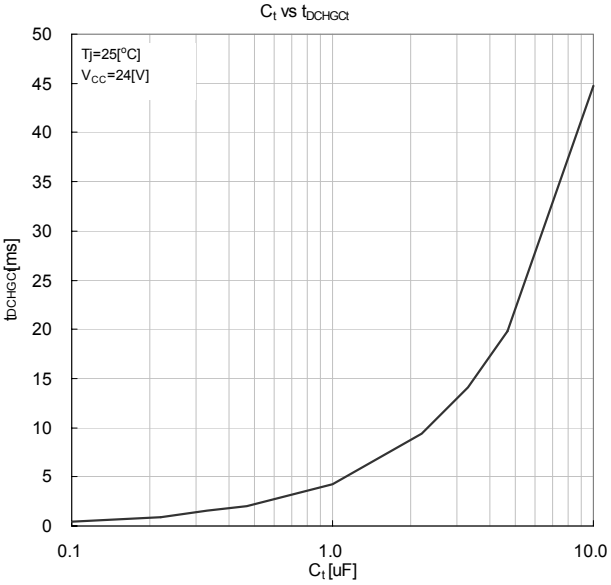
V_{FRC} vs $I_{DCHGFRC}$



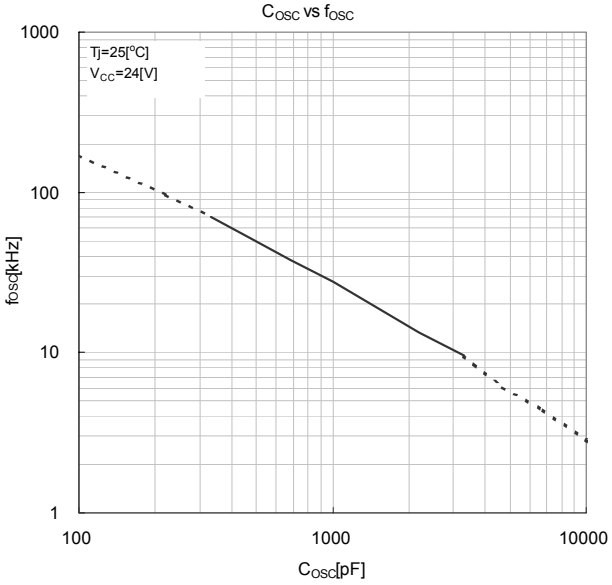
C_t vs t_{CHGCt}



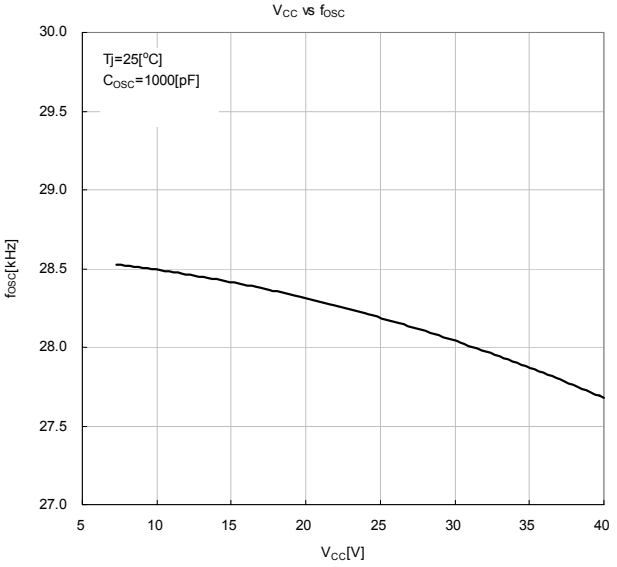
C_t vs t_{DCHGCt}



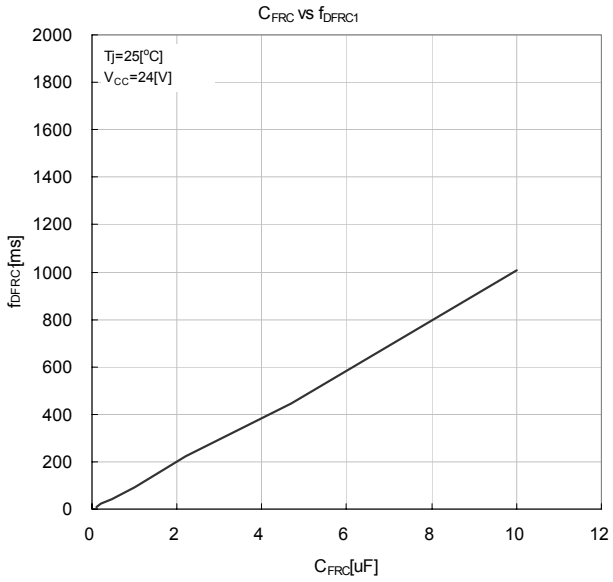
C_{OSC} vs f_{OSC}

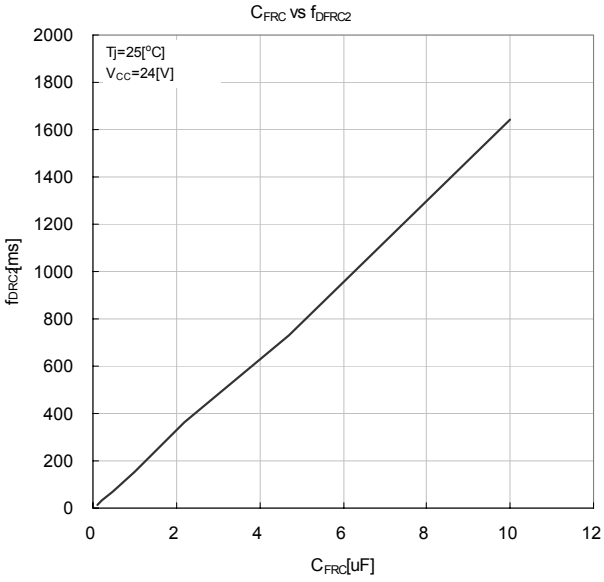


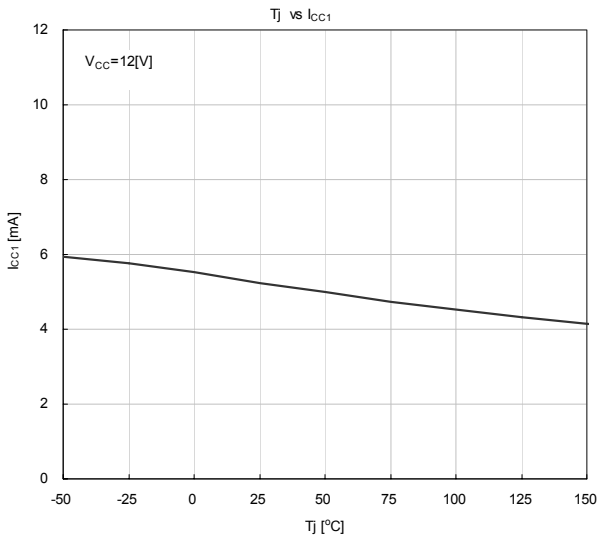
V_{CC} vs f_{OSC}

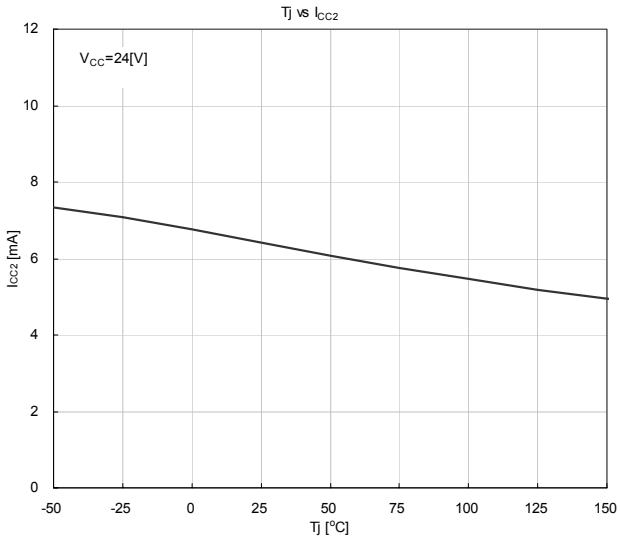


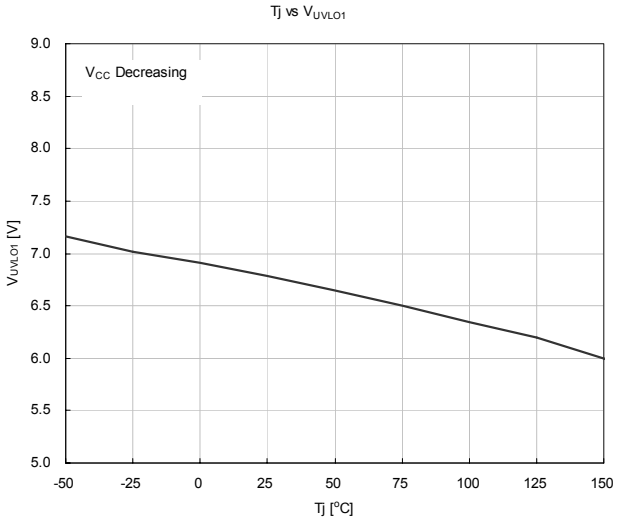
■ TYPICAL CHARACTERISTICS

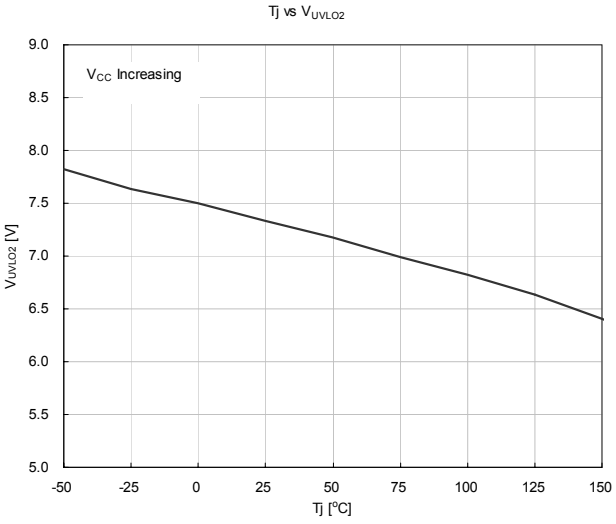






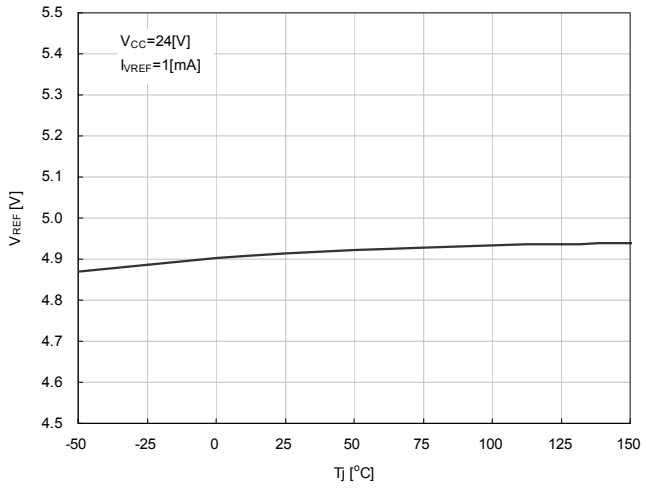




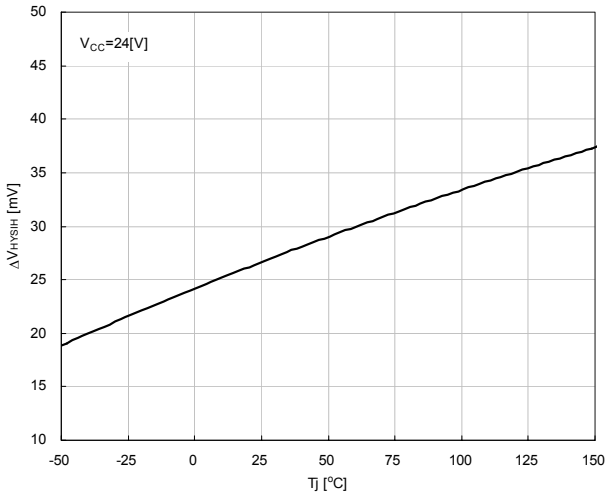


■ TYPICAL CHARACTERISTICS

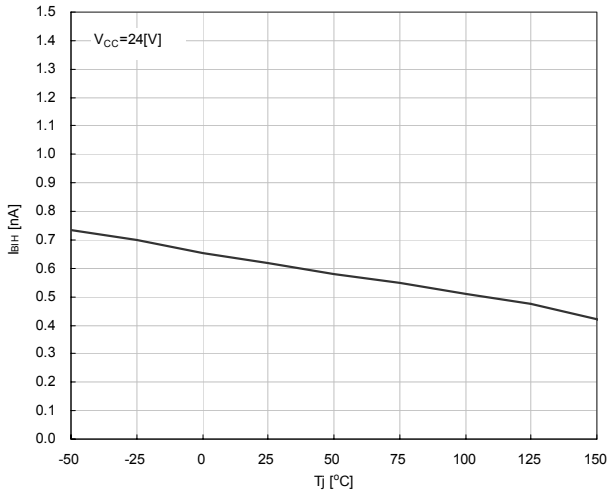
Tj vs V_{REF}



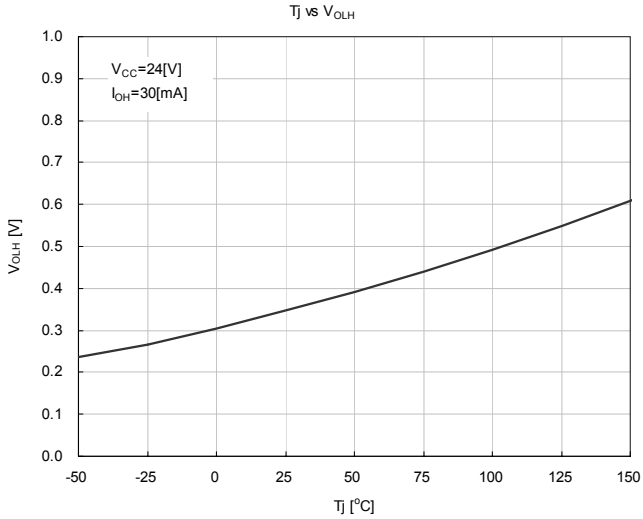
Tj vs ΔV_{HYSIH}



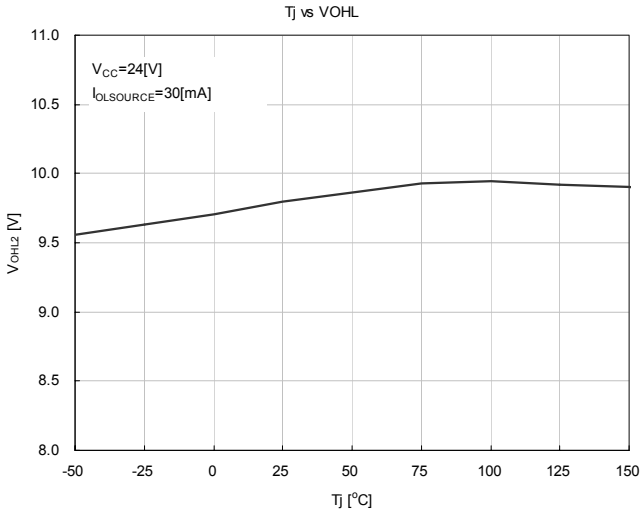
Tj vs I_{BIH}



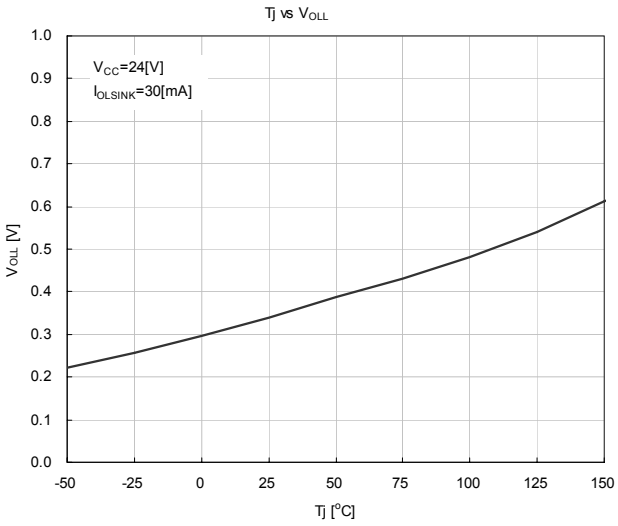
Tj vs V_{OLH}



Tj vs VOHL

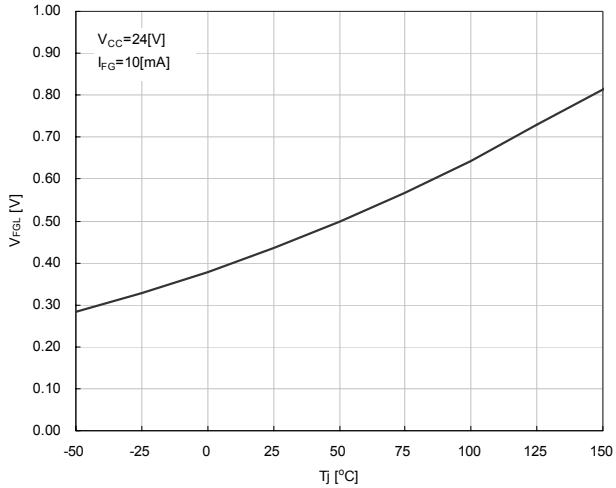


Tj vs V_{OLL}

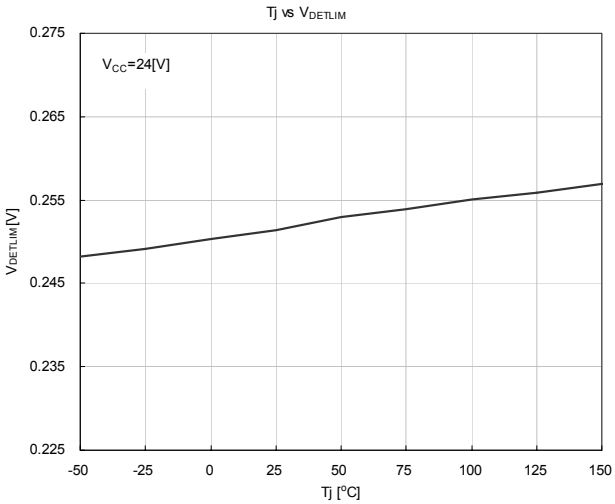


■ TYPICAL CHARACTERISTICS

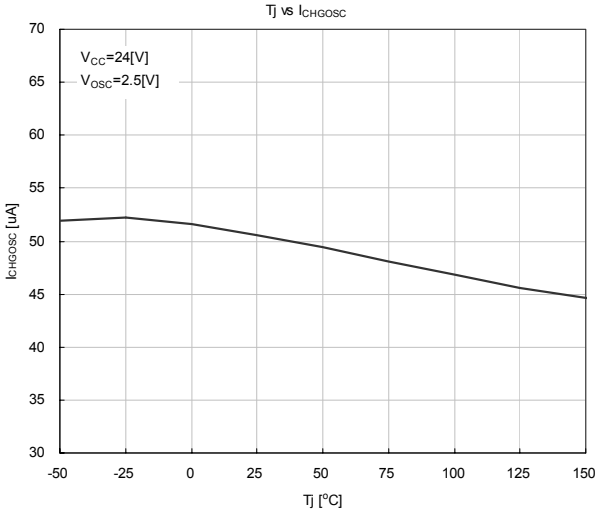
Tj vs V_{FGL}



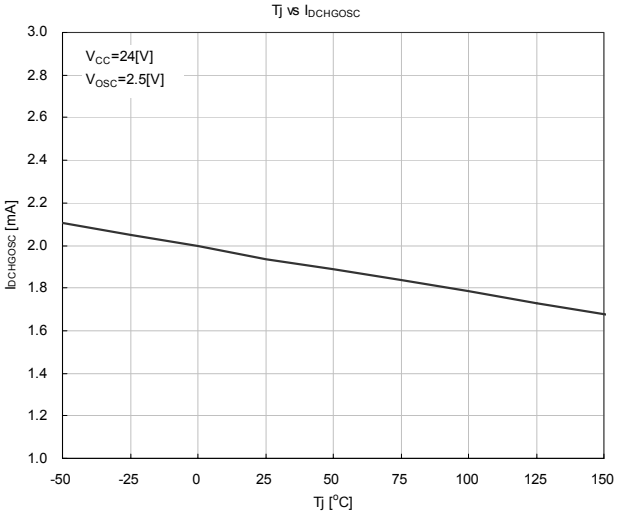
Tj vs V_{DETLIM}



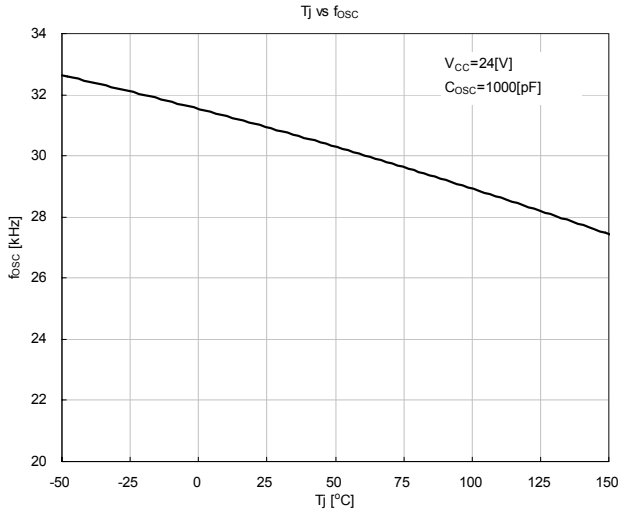
Tj vs I_{CHGOSC}



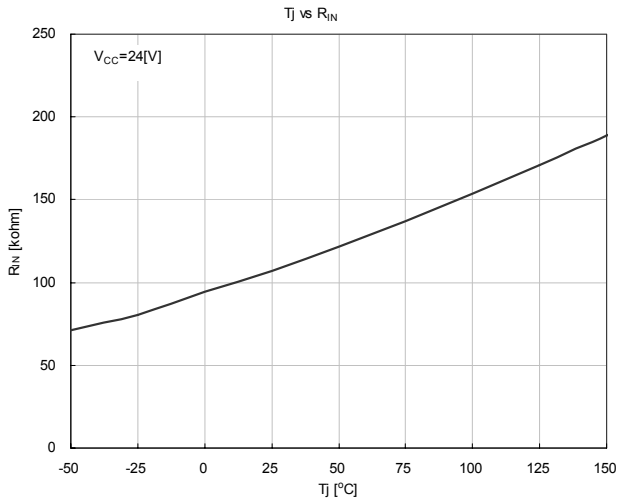
Tj vs $I_{DCHGOSC}$



Tj vs f_{OSC}



Tj vs R_{IN}



■ TYPICAL CHARACTERISTICS