

## ZXMHC3F381N8

### 30V SO8 Complementary enhancement mode MOSFET H-Bridge

#### Summary

Device	$V_{(BR)DSS}$	$Q_G$	$R_{DS(on)}$	$I_D$ $T_A = 25^\circ C$
N-CH	30V	9.0nC	33m $\Omega$ @ $V_{GS} = 10V$	5.0A
			60m $\Omega$ @ $V_{GS} = 4.5V$	3.9A
P-CH	-30V	12.7nC	55m $\Omega$ @ $V_{GS} = -10V$	-4.1A
			80m $\Omega$ @ $V_{GS} = -4.5V$	-3.3A



#### Description

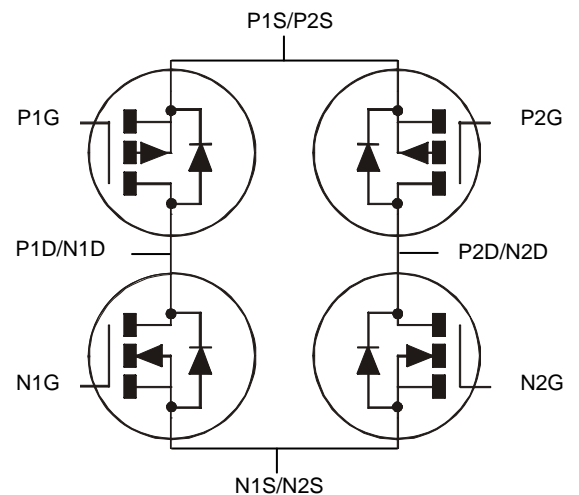
This new generation complementary MOSFET H-Bridge features low on-resistance achievable with low gate drive.

#### Features

- 2 x N + 2 x P channels in a SOIC package
- Low voltage ( $V_{GS} = 4.5 V$ ) gate drive

#### Applications

- DC Motor control
- DC-AC Inverters

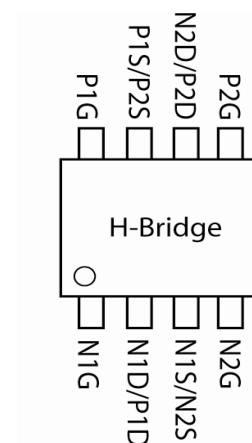


#### Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMHC3F381N8TC	13	12	2,500

#### Device marking

ZXMHC  
3F381



## Absolute maximum ratings

Parameter	Symbol	N-channel	P-channel	Unit
Drain-Source voltage	$V_{DSS}$	30	-30	V
Gate-Source voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain current @ $V_{GS}=10V$ ; $T_A=25^\circ C$ <sup>(b)</sup> @ $V_{GS}=10V$ ; $T_A=70^\circ C$ <sup>(b)</sup> @ $V_{GS}=10V$ ; $T_A=25^\circ C$ <sup>(a)</sup> @ $V_{GS}=10V$ ; $T_L=25^\circ C$ <sup>(f)</sup>	$I_D$	4.98 3.98 3.98 4.17	-4.13 -3.31 -3.36 -3.51	A
Pulsed Drain current @ $V_{GS}=10V$ ; $T_A=25^\circ C$ <sup>(c)</sup>	$I_{DM}$	22.9	-19.6	A
Continuous Source current (Body diode) at $T_A=25^\circ C$ <sup>(b)</sup>	$I_S$	2.0	-2.0	A
Pulsed Source current (Body diode) at $T_A=25^\circ C$ <sup>(c)</sup>	$I_{SM}$	22.9	-19.6	A
Power dissipation at $T_A=25^\circ C$ <sup>(a)</sup> Linear derating factor	$P_D$	0.87 6.94		W mW/ $^\circ C$
Power dissipation at $T_A=25^\circ C$ <sup>(b)</sup> Linear derating factor	$P_D$	1.35 10.9		W mW/ $^\circ C$
Power dissipation at $T_L=25^\circ C$ <sup>(f)</sup> Linear derating factor	$P_D$	0.95 7.63	0.98 7.81	W mW/ $^\circ C$
Operating and storage temperature range	$T_j, T_{stg}$	-55 to 150		$^\circ C$

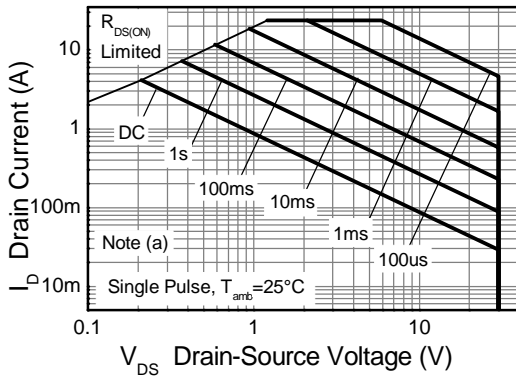
## Thermal resistance

Parameter	Symbol	Value	Unit
Junction to ambient <sup>(a)</sup>	$R_{\theta JA}$	144	$^\circ C/W$
Junction to ambient <sup>(b)</sup>	$R_{\theta JA}$	92	$^\circ C/W$
Junction to ambient <sup>(d)</sup>	$R_{\theta JA}$	106	$^\circ C/W$
Junction to ambient <sup>(e)</sup>	$R_{\theta JA}$	254	$^\circ C/W$
Junction to lead <sup>(f)</sup>	$R_{\theta JL}$	131	128 $^\circ C/W$

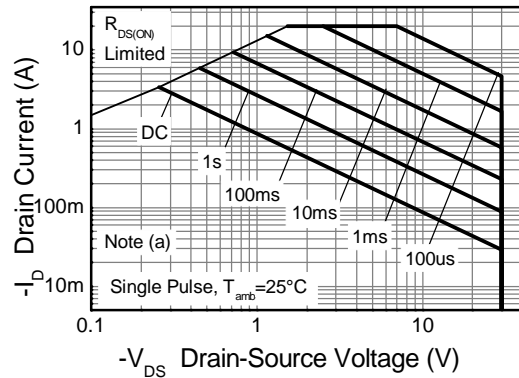
### NOTES:

- For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions with the heat-sink split into two equal areas (one for each drain connection); the device is measured when operating in a steady-state condition with one active die.
- Same as note (a), except the device is measured at  $t \leq 10$  sec.
- Same as note (a), except the device is pulsed with  $D=0.02$  and pulse width 300  $\mu s$ . The pulse current is limited by the maximum junction temperature.
- For a device surface mounted on 50mm x 50mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions with the heat-sink split into two equal areas (one for each drain connection); the device is measured when operating in a steady-state condition with one active die.
- For a device surface mounted on minimum copper 1.6mm FR4 PCB, in still air conditions; the device is measured when operating in a steady-state condition with one active die.
- Thermal resistance from junction to solder-point (at the end of the drain lead); the device is operating in a steady-state condition with one active die.

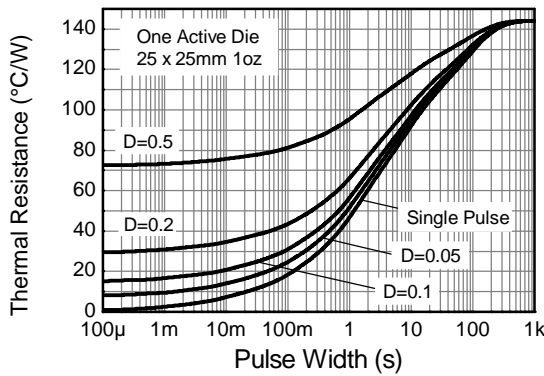
## Thermal characteristics



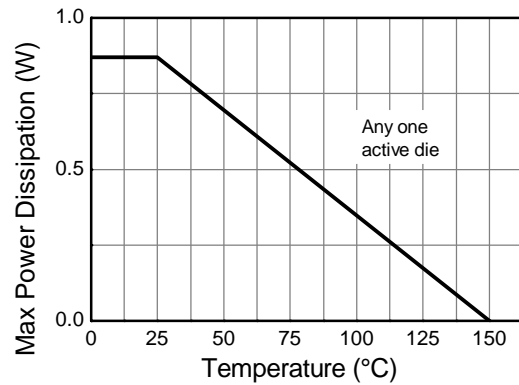
**N-channel Safe Operating Area**



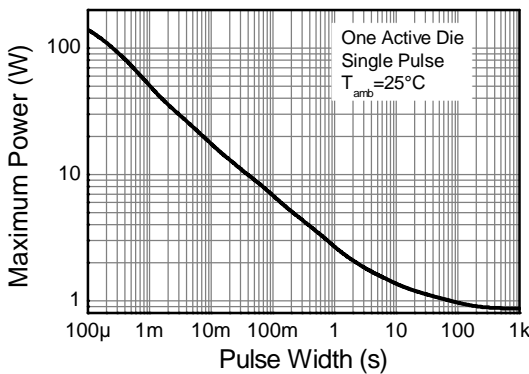
**P-channel Safe Operating Area**



**Transient Thermal Impedance**



**Derating Curve**



**Pulse Power Dissipation**

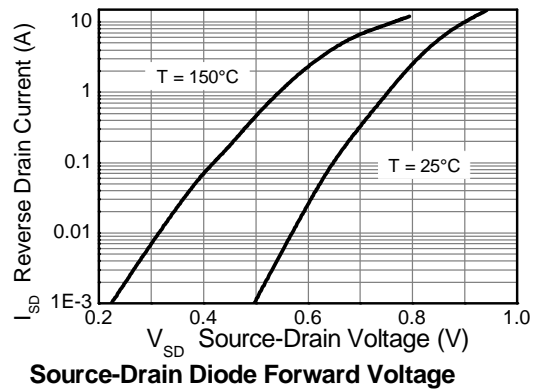
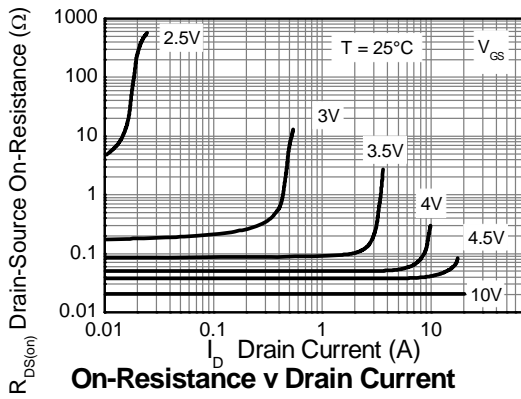
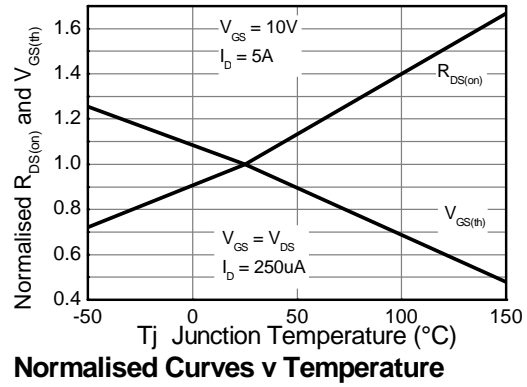
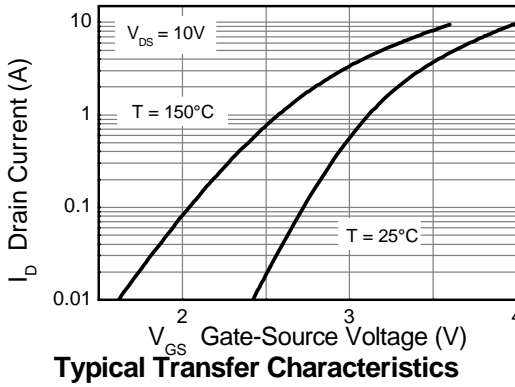
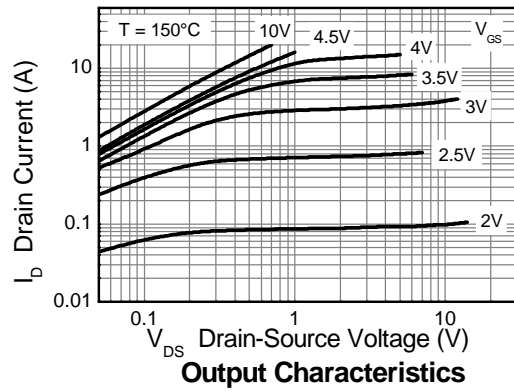
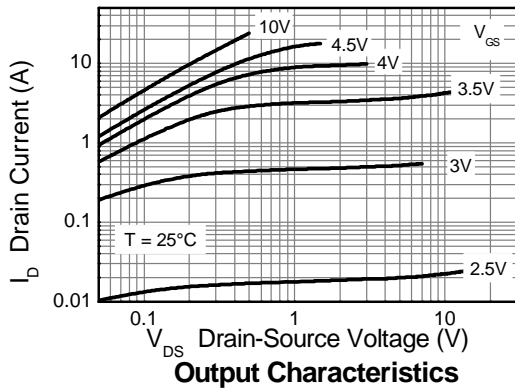
## N-channel electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>Static</b>						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	30			V	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$
Zero Gate voltage Drain current	$I_{DSS}$			0.5	$\mu\text{A}$	$V_{DS} = 30\text{V}$ , $V_{GS} = 0\text{V}$
Gate-Body leakage	$I_{GSS}$			$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
Gate-Source threshold voltage	$V_{GS(th)}$	1.0		3.0	V	$I_D = 250\mu\text{A}$ , $V_{DS} = V_{GS}$
Static Drain-Source on-state resistance <sup>(a)</sup>	$R_{DS(on)}$			0.033 0.060	$\Omega$	$V_{GS} = 10\text{V}$ , $I_D = 5\text{A}$ $V_{GS} = 4.5\text{V}$ , $I_D = 4\text{A}$
Forward Transconductance <sup>(a) (c)</sup>	$g_{fs}$		11.8		S	$V_{DS} = 15\text{V}$ , $I_D = 5\text{A}$
<b>Dynamic</b>						
<b>Capacitance</b> <sup>(c)</sup>						
Input capacitance	$C_{iss}$		430		pF	$V_{DS} = 15\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	$C_{oss}$		101		pF	
Reverse transfer capacitance	$C_{rss}$		56		pF	
<b>Switching</b> <sup>(b) (c)</sup>						
Turn-on-delay time	$t_{d(on)}$		2.5		ns	$V_{DD} = 15\text{V}$ , $V_{GS} = 10\text{V}$ $I_D = 1\text{A}$ $R_G \cong 6\Omega$ ,
Rise time	$t_r$		3.3		ns	
Turn-off delay time	$t_{d(off)}$		11.5		ns	
Fall time	$t_f$		6.3		ns	
<b>Gate charge</b> <sup>(c)</sup>						
Total Gate charge	$Q_g$		9.0		nC	$V_{DS} = 15\text{V}$ , $V_{GS} = 10\text{V}$ $I_D = 5\text{A}$
Gate-Source charge	$Q_{gs}$		1.7		nC	
Gate-Drain charge	$Q_{gd}$		2.0		nC	
<b>Source-Drain diode</b>						
Diode forward voltage <sup>(a)</sup>	$V_{SD}$		0.82	1.2	V	$I_S = 1.7\text{A}$ , $V_{GS} = 0\text{V}$
Reverse recovery time <sup>(c)</sup>	$t_{rr}$		12		ns	$I_S = 2.1\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge <sup>(c)</sup>	$Q_{rr}$		4.9		nC	

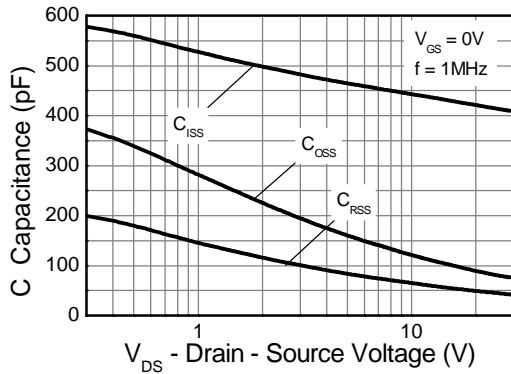
### NOTES:

- (a) Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .  
 (b) Switching characteristics are independent of operating junction temperature.  
 (c) For design aid only, not subject to production testing

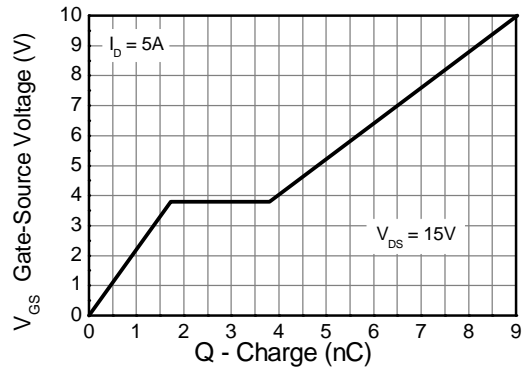
## N-channel typical characteristics



## N-channel typical characteristics –continued

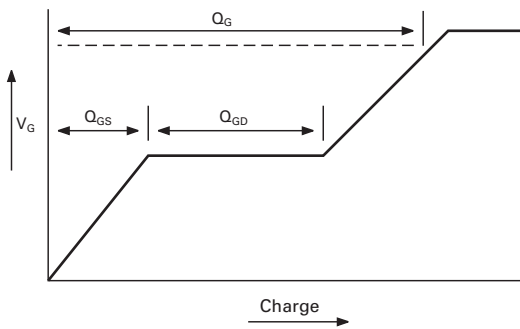


Capacitance v Drain-Source Voltage

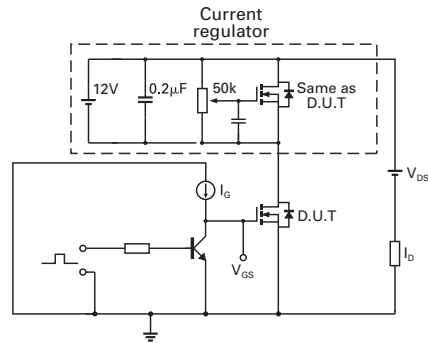


Gate-Source Voltage v Gate Charge

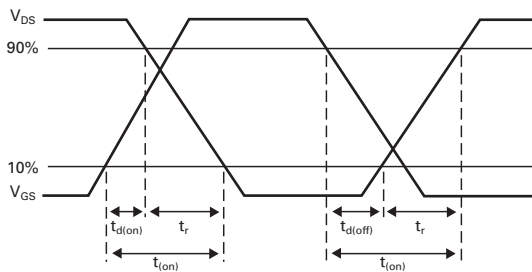
## Test circuits



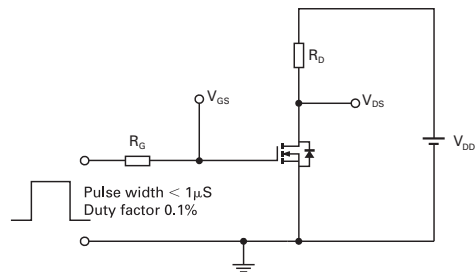
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



Switching time test circuit

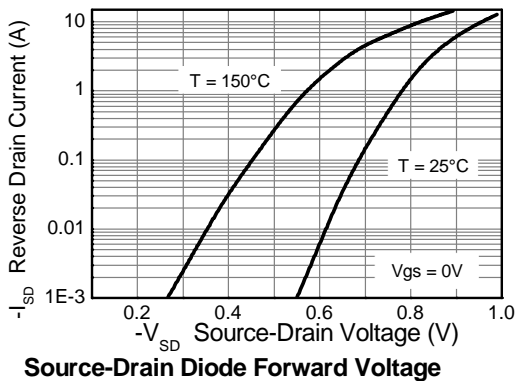
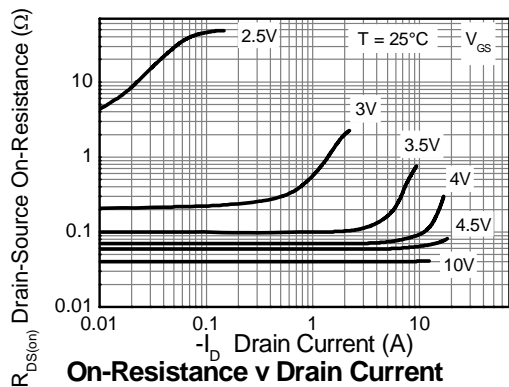
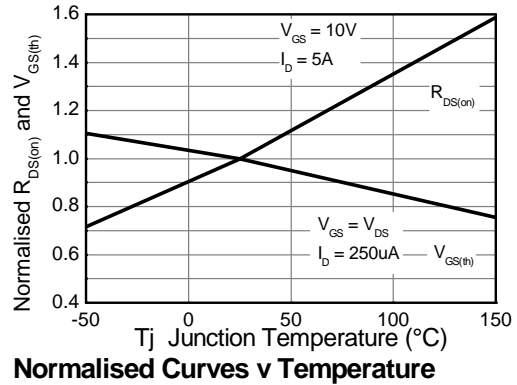
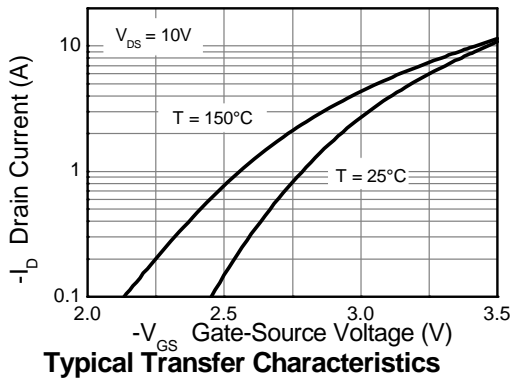
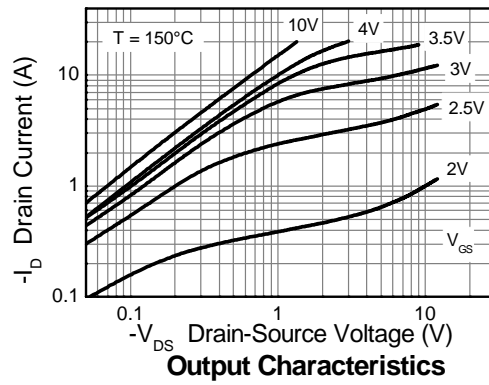
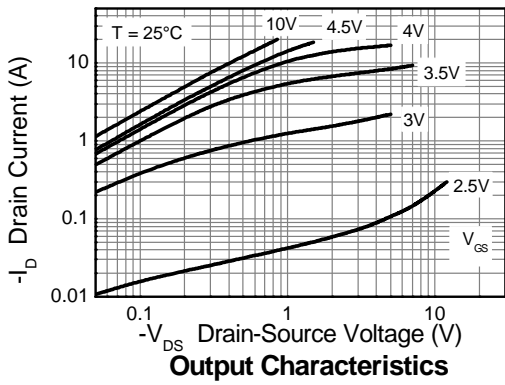
## P-channel electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>Static</b>						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	-30			V	$I_D = -250\mu\text{A}$ , $V_{GS} = 0\text{V}$
Zero Gate voltage Drain current	$I_{DSS}$			-0.5	$\mu\text{A}$	$V_{DS} = -30\text{V}$ , $V_{GS} = 0\text{V}$
Gate-Body leakage	$I_{GSS}$			$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
Gate-Source threshold voltage	$V_{GS(th)}$	-1.0		-3.0	V	$I_D = -250\mu\text{A}$ , $V_{DS} = V_{GS}$
Static Drain-Source on-state resistance <sup>(a)</sup>	$R_{DS(on)}$			0.055 0.080	$\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -5\text{A}$ $V_{GS} = -4.5\text{V}$ , $I_D = -4\text{A}$
Forward Transconductance <sup>(a) (c)</sup>	$g_{fs}$		14		S	$V_{DS} = -15\text{V}$ , $I_D = -5\text{A}$
<b>Dynamic</b>						
<b>Capacitance</b> <sup>(c)</sup>						
Input capacitance	$C_{iss}$		670		pF	$V_{DS} = -15\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	$C_{oss}$		126		pF	
Reverse transfer capacitance	$C_{rss}$		70		pF	
<b>Switching</b> <sup>(b) (c)</sup>						
Turn-on-delay time	$t_{d(on)}$		1.9		ns	$V_{DD} = -15\text{V}$ , $V_{GS} = -10\text{V}$ $I_D = -1\text{A}$ $R_G \cong 6\Omega$
Rise time	$t_r$		3.0		ns	
Turn-off delay time	$t_{d(off)}$		30		ns	
Fall time	$t_f$		21		ns	
<b>Gate charge</b> <sup>(c)</sup>						
Total Gate charge	$Q_g$		12.7		nC	$V_{DS} = -15\text{V}$ , $V_{GS} = -10\text{V}$ $I_D = -5\text{A}$
Gate-Source charge	$Q_{gs}$		2.0		nC	
Gate-Drain charge	$Q_{gd}$		2.4		nC	
<b>Source-Drain diode</b>						
Diode forward voltage <sup>(a)</sup>	$V_{SD}$		-0.82	-1.2	V	$I_S = -1.7\text{A}$ , $V_{GS} = 0\text{V}$
Reverse recovery time <sup>(c)</sup>	$t_{rr}$		16.5		ns	$I_S = -2.1\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge <sup>(c)</sup>	$Q_{rr}$		11.5		nC	

### NOTES:

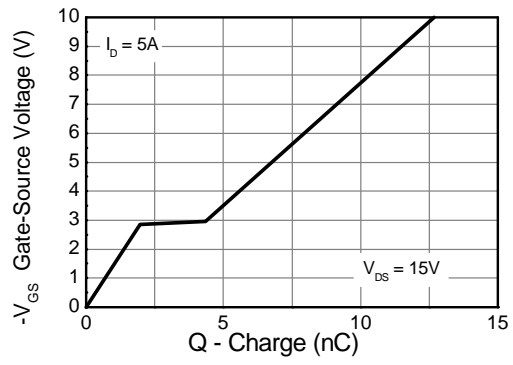
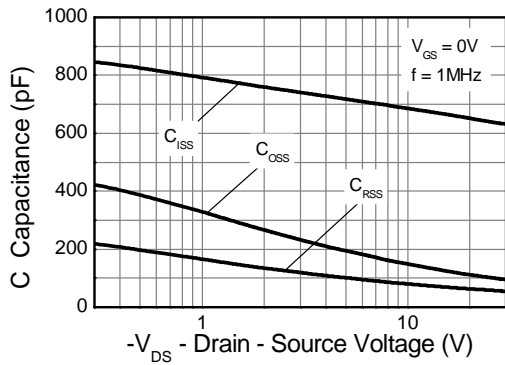
- (a) Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .  
 (b) Switching characteristics are independent of operating junction temperature.  
 (c) For design aid only, not subject to production testing

## P-channel typical characteristics

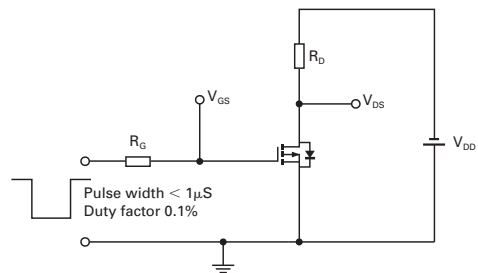
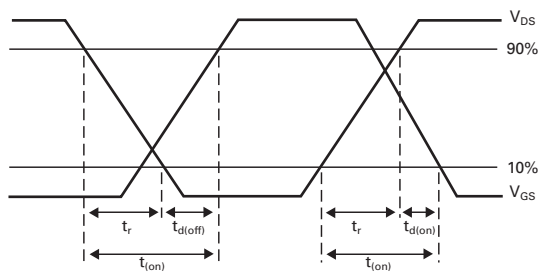
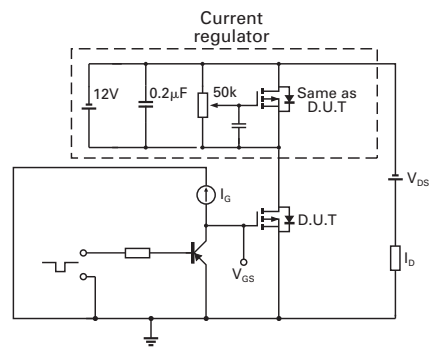
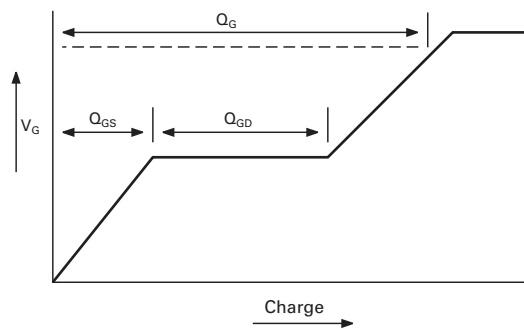




## P-channel typical characteristics –continued

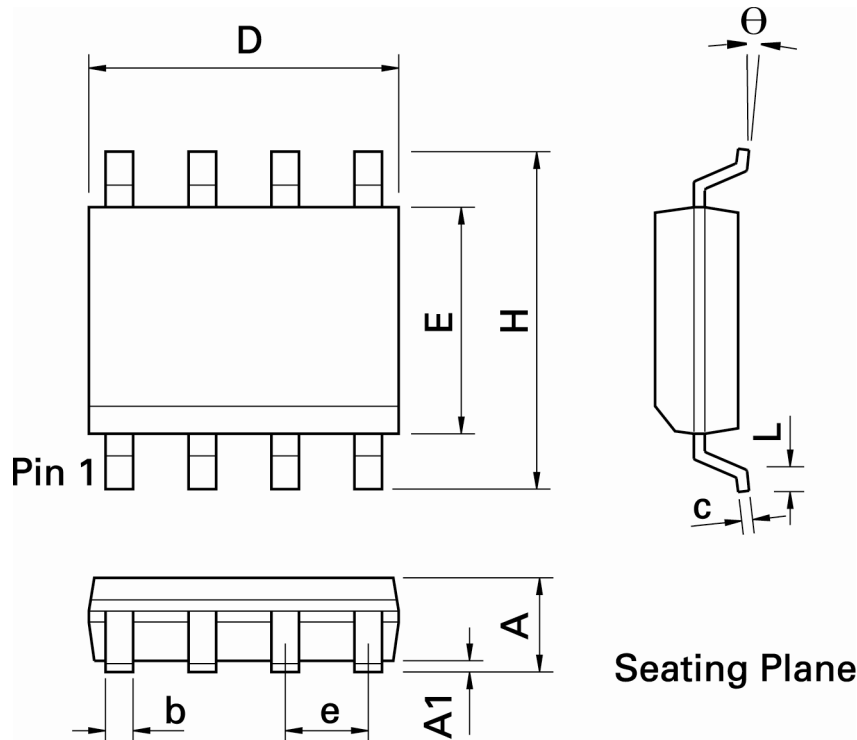


## Test circuits



# ZXMHC3F381N8

## Packaging details - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	-	-	-	-	-
L	0.016	0.050	0.40	1.27	-	-	-	-	-

**Note:** Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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