

# PHD38N02LT

N-channel TrenchMOS logic level FET

Rev. 02 — 2 February 2007

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Low on-state resistance
- 2.5 V gate drive

### 1.3 Applications

- Linear regulator for Double-Data Rate (DDR) memory

### 1.4 Quick reference data

- $V_{DS} \leq 20$  V
- $I_D \leq 44.7$  A
- $R_{DSon} \leq 16$  m $\Omega$
- $P_{tot} \leq 57.6$  W

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	<p>SOT428 (DPAK)</p>	
2	drain (D) <a href="#">[1]</a>		
3	source (S)		
mb	mounting base; connected to drain (D)		

[1] It is not possible to make a connection to pin 2.

### 3. Ordering information

**Table 2. Ordering information**

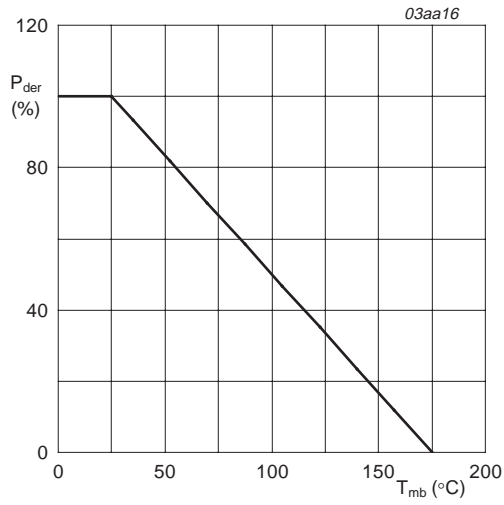
Type number	Package		Version
	Name	Description	
PHD38N02LT	DPAK	plastic single-ended surface-mounted package; 3 leads (one lead cropped)	SOT428

### 4. Limiting values

**Table 3. Limiting values**

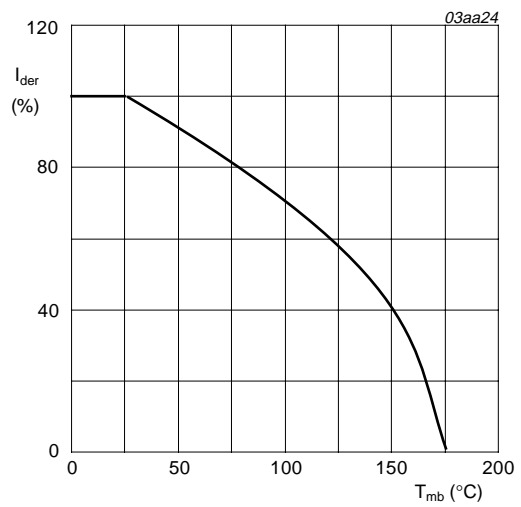
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	20	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	20	V
$V_{GS}$	gate-source voltage		-	$\pm 12$	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	44.7	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 2</a>	-	31.6	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	179	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	57.6	W
$T_{stg}$	storage temperature		-55	+175	°C
$T_j$	junction temperature		-55	+175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	44.7	A
$I_{SM}$	peak source current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	179	A



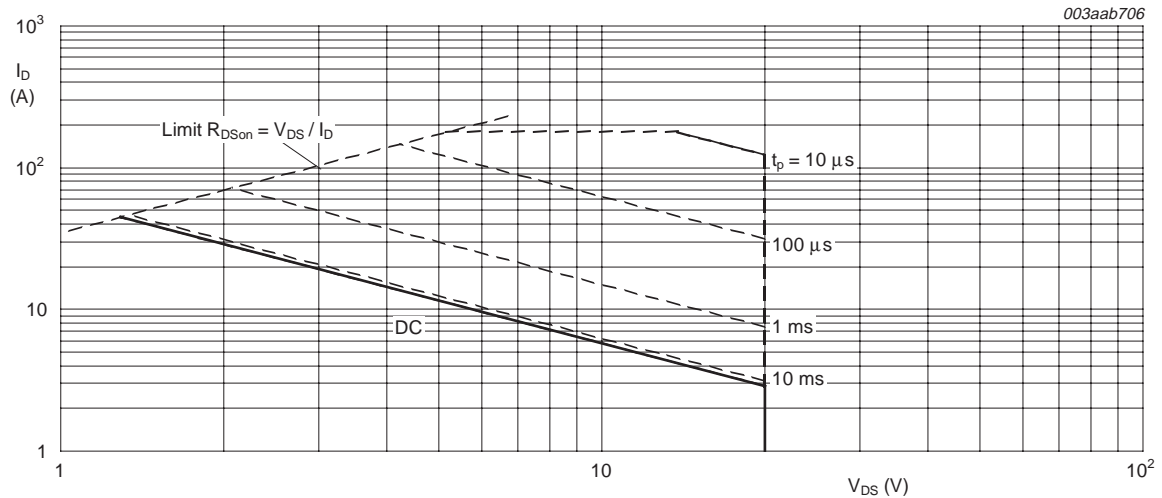
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse; V<sub>GS</sub> = 5 V

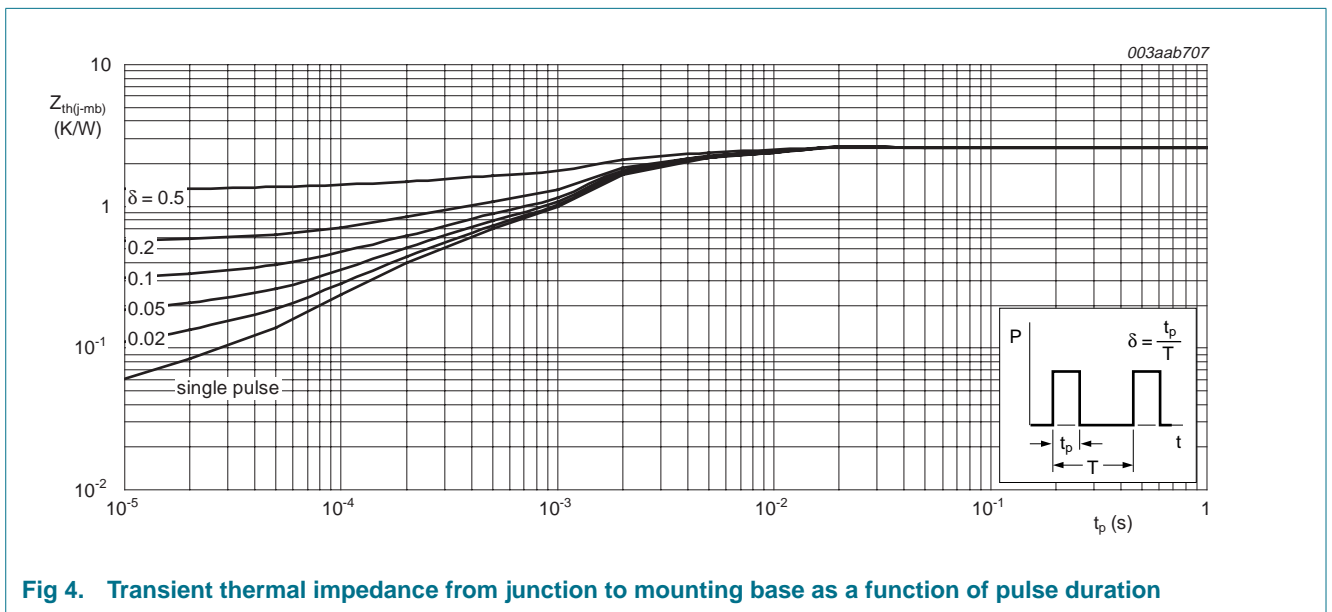
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

**Table 4. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOT428				
		minimum footprint	-	75	-	K/W
		SOT404 minimum footprint	[1]	50	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

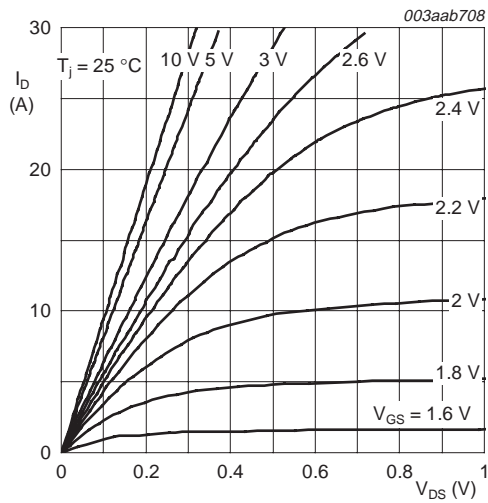


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

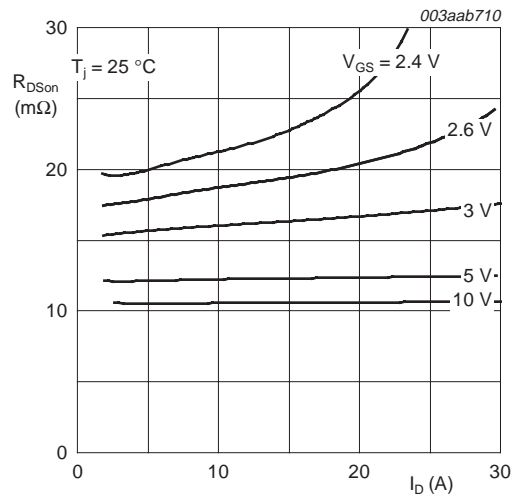
**Table 5. Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	20	-	-	V
		T <sub>j</sub> = -55 °C	18	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; see <a href="#">Figure 9</a> and <a href="#">10</a> T <sub>j</sub> = 25 °C	0.5	1.0	1.5	V
		T <sub>j</sub> = 175 °C	0.3	-	-	V
		T <sub>j</sub> = -55 °C	-	-	1.8	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	-	0.05	1.0	μA
		T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = ±12 V; V <sub>DS</sub> = 0 V	-	10	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; see <a href="#">Figure 6</a> and <a href="#">8</a> T <sub>j</sub> = 25 °C	-	13.5	16	mΩ
		T <sub>j</sub> = 175 °C	-	24.3	28.8	mΩ
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 10 V; V <sub>GS</sub> = 5 V; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	15.1	-	nC
Q <sub>GS</sub>	gate-source charge		-	4.5	-	nC
Q <sub>GD</sub>	gate-drain charge		-	4.2	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; f = 1 MHz; see <a href="#">Figure 14</a>	-	800	-	pF
C <sub>oss</sub>	output capacitance		-	260	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	190	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 25 A; V <sub>GS</sub> = 10 V; R <sub>G</sub> = 5.6 Ω	-	4	-	ns
t <sub>r</sub>	rise time		-	12.5	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	30	-	ns
t <sub>f</sub>	fall time		-	23	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; see <a href="#">Figure 13</a>	-	0.98	1.2	V



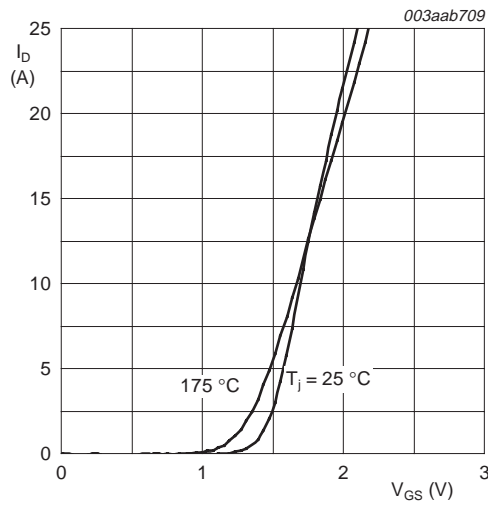
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



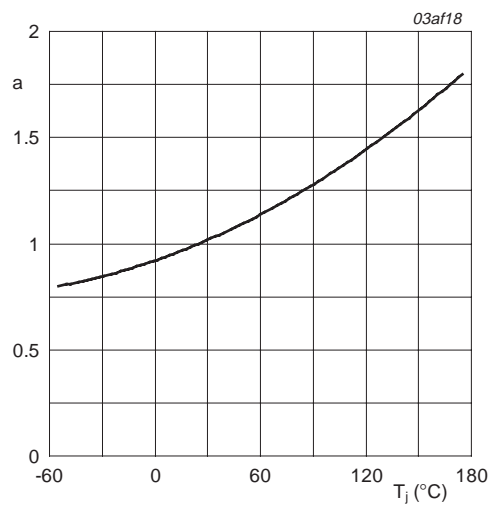
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



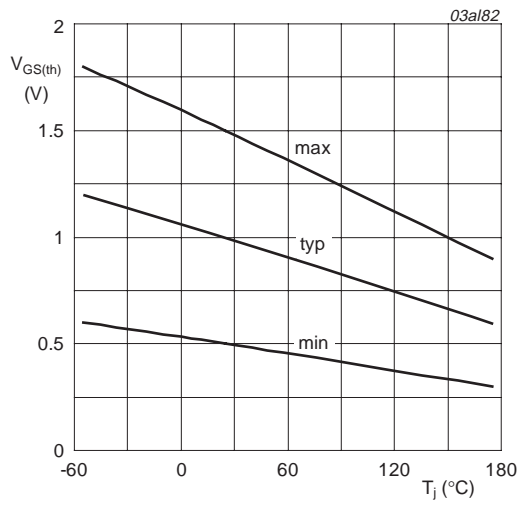
$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



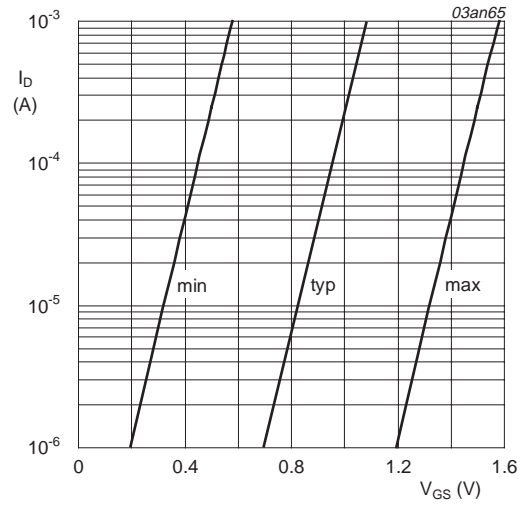
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



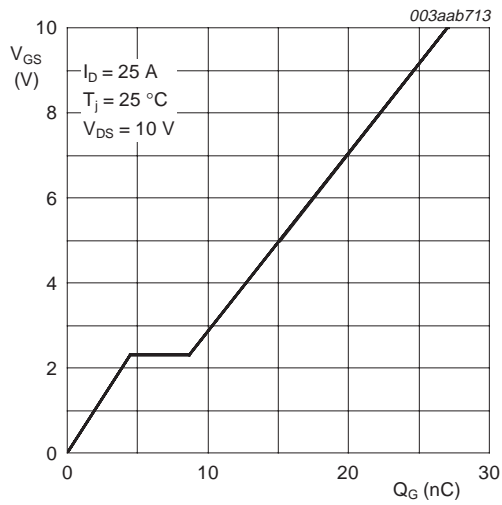
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



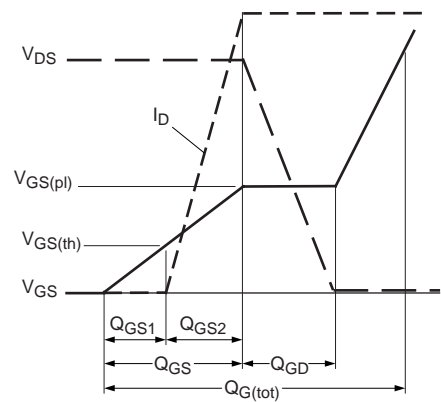
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**

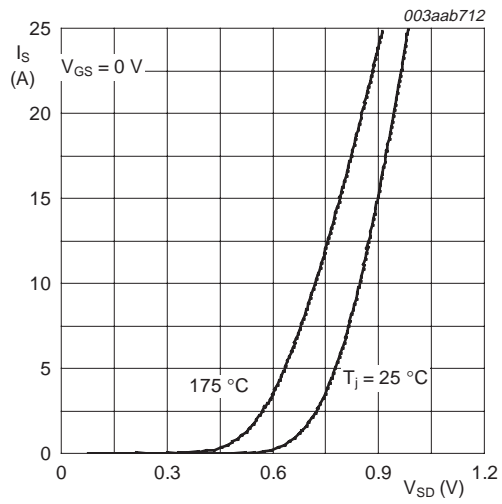


$I_D = 25 \text{ A}; V_{DS} = 10 \text{ V}$

**Fig 11. Gate-source voltage as a function of gate charge; typical values**

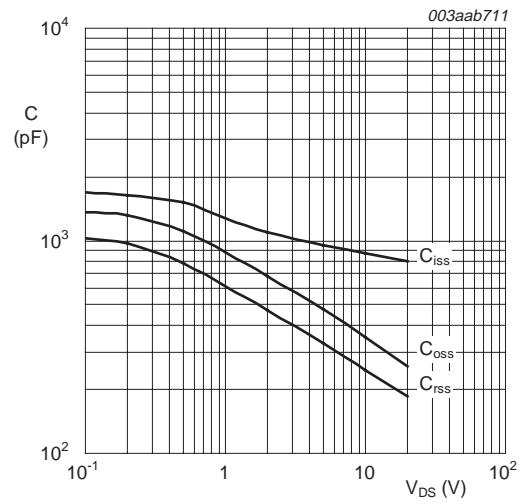


**Fig 12. Gate charge waveform definitions**



$T_j = 25\text{ °C}$  and  $175\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

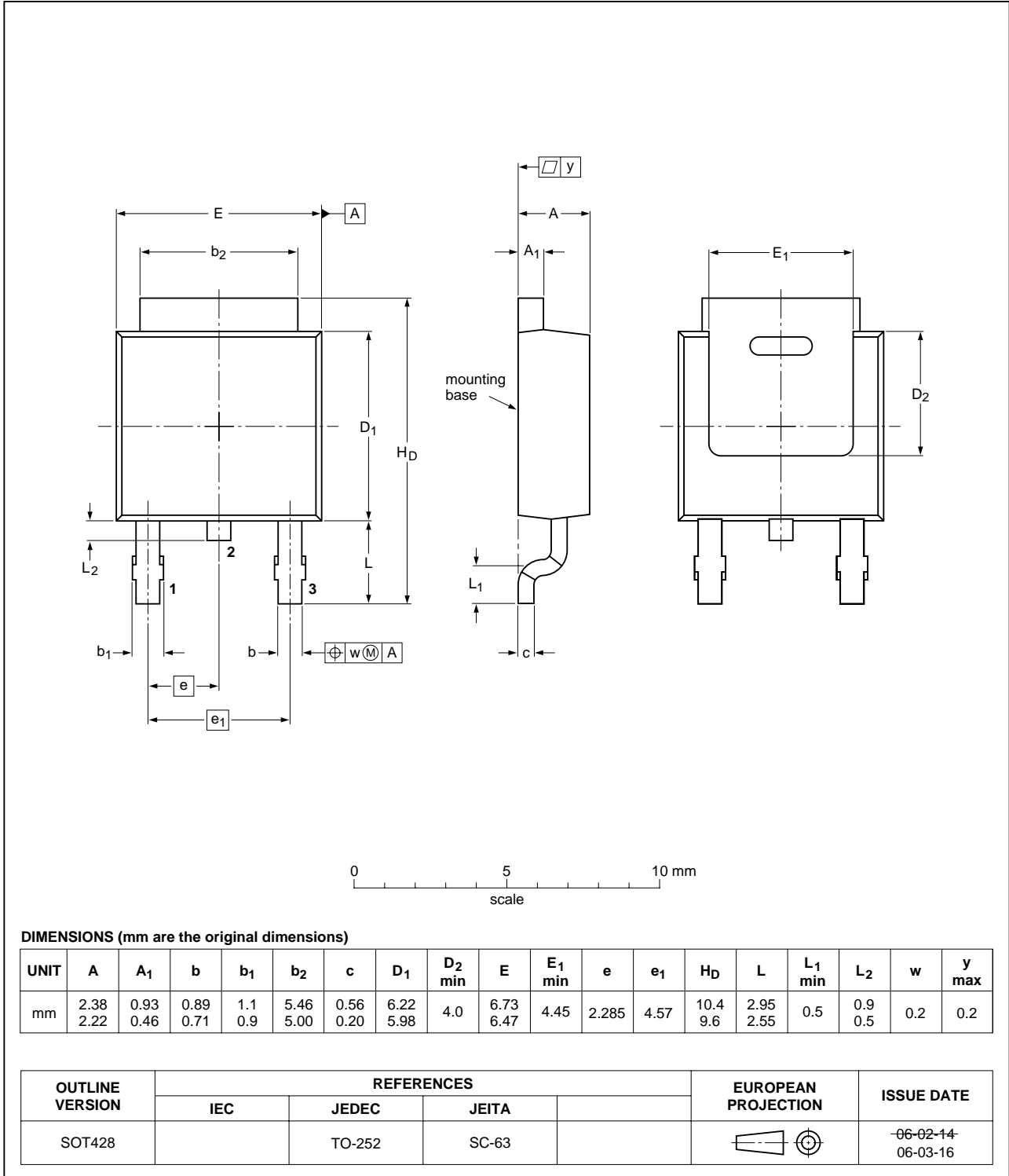


Fig 15. Package outline SOT428 (DPAK)

## 8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD38N02LT_2	20070202	Product data sheet	-	PHB_PHD38N02LT-01
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• PHB38N02LT has been discontinued.</li></ul>			
PHB_PHD38N02LT-01 (9397 750 11614)	20030630	Product data	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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