



HIGH PERFORMANCE CMOS BUS INTERFACE REGISTER

IDT54/74FCT821A/B

FEATURES:

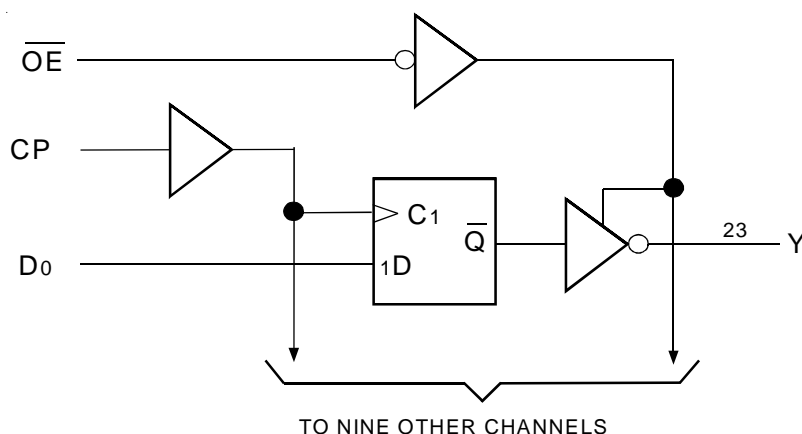
- Equivalent to AMD's Am29821-25 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT821A equivalent to FAST™ speed
- IDT54/74FCT821B 25% faster than FAST
- $I_{OL} = 48\text{mA}$ (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output compatibility
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series ($5\mu\text{A}$ max.)
- Military product compliant to MIL-STD-883, Class B
- Available in the following packages:
 - Commercial: SOIC
 - Military: CERDIP, LCC

DESCRIPTION:

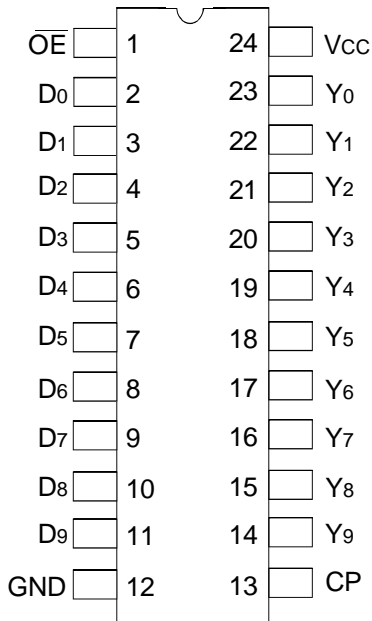
The FCT821 series is built using an advanced dual metal CMOS technology. The FCT821 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The 74FCT821 is a buffered, 10-bit wide version of the popular FCT374 function.

The FCT821 high-performance interface family is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

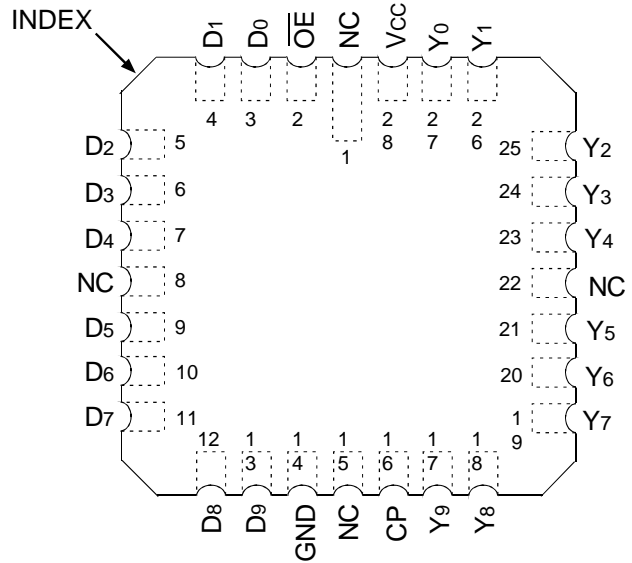
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



CERDIP/ SOIC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Outputs and I/O terminals only.

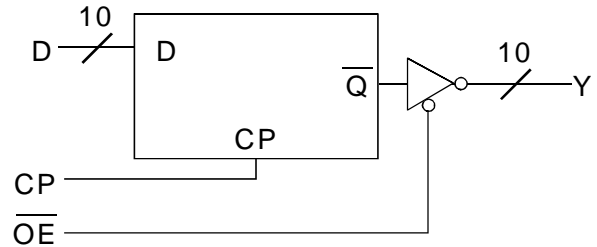
CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

LOGIC SYMBOL



PIN DESCRIPTION

Pin Name	I/O	Description
D _x	I	D Flip-Flop Data Inputs
CP	I	Clock Pulse for the Register. Enters data into the register on the LOW-to-HIGH transition
Y _x	O	Register 3-State Outputs
\overline{OE}	I	Output Control. When the \overline{OE} input is HIGH, the Y _x outputs are in the high impedance state. When the \overline{OE} input is LOW, the TRUE register data is present at the Y _x outputs.

FUNCTION TABLE⁽¹⁾

Inputs			Outputs	Function
\overline{OE}	Dx	CP	Yx	
H	L	↑	Z	High Z
H	H	↑	Z	
H	X	X	Z	Clear
L	X	X	L	
H	X	X	Z	Hold
L	X	X	NC	
H	L	↑	Z	Load
H	H	↑	Z	
L	L	↑	L	
L	H	↑	H	

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change
↑ = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, VCC = 5.0V ±5%; Military: TA = -55°C to +125°C, VCC = 5.0V ±10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V	
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I _{IH}	Input HIGH Current	V _{CC} = Max. V _I = V _{CC}	—	—	5	μA	
		V _I = 2.7V	—	—	5 ⁽⁴⁾		
I _{IL}	Input LOW Current	V _{CC} = Max. V _I = 0.5V	—	—	-5 ⁽⁴⁾	μA	
		V _I = GND	—	—	-5		
I _{OZH}	Off State (High Impedance) Output Current	V _{CC} = Max. V _O = V _{CC}	—	—	10	μA	
			V _O = 2.7V	—	—		10 ⁽⁴⁾
			V _O = 0.5V	—	—		-10 ⁽⁴⁾
			V _O = GND	—	—		-10
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V	
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾	-75	-120	—	mA	
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{Hc} , I _{OH} = -32μA	V _{Hc}	V _{CC}	—	V	
		V _{CC} = Min V _{IN} = V _{IH} or V _{IL}	I _{OH} = -300μA	V _{Hc}	V _{CC}		—
			I _{OH} = -15mA MIL	2.4	4.3		—
		I _{OH} = -24mA COM	2.4	4.3	—		
V _{OL}	Output LOW Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{Hc} , I _{OL} = 300μA	—	GND	V _{LC}	V	
		V _{CC} = Min V _{IN} = V _{IH} or V _{IL}	I _{OL} = 300μA	—	GND		V _{LC} ⁽⁴⁾
			I _{OL} = 32mA MIL	—	0.3		0.5
		I _{OL} = 48mA COM	—	0.3	0.5		

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed, but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open OE = GND One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle OE = GND One Bit Toggling at f _i = 5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	1.7	4	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2.2	6	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle OE = GND Eight Bits Toggling at f _i = 2.5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	4	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	6.2	16.8 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at V_{CC} = 5.0V, +25°C ambient.

3. Per TTL driven input; (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} \frac{D_H N_T}{N_T} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Output Frequency

N_i = Number of Outputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

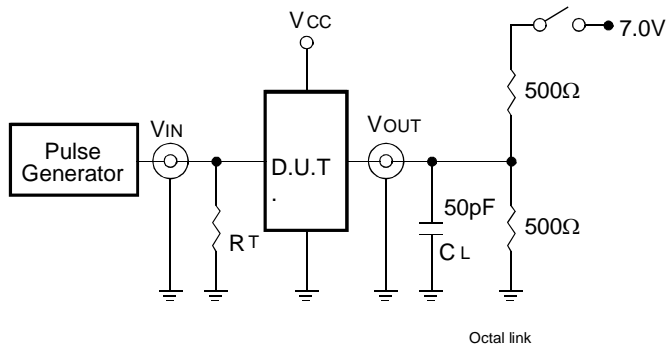
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Conditions ⁽¹⁾	IDT54/74FCT821A				IDT54/74FCT821B				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to Yx (\overline{OE} = LOW)	CL = 50pF RL = 500Ω	—	10	—	11.5	—	7.5	—	8.5	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	—	20	—	20	—	15	—	16	
t _{SU}	Set-up Time HIGH or LOW, Dx to CP	CL = 50pF	4	—	4	—	3	—	3	—	ns
t _H	Hold Time HIGH or LOW, Dx to CP	RL = 500Ω	2	—	2	—	1.5	—	1.5	—	
t _w	CP Pulse Width, HIGH or LOW		7	—	7	—	6	—	6	—	
t _{PZH} t _{PZL}	Output Enable Time \overline{OE} to Yx	CL = 50pF RL = 500Ω	—	12	—	13	—	8	—	9	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	—	23	—	25	—	15	—	16	
t _{PHZ} t _{PLZ}	Output Disable Time \overline{OE} to Yx	CL = 5pF ⁽³⁾ RL = 500Ω	—	7	—	8	—	6.5	—	7	ns
		CL = 50pF RL = 500Ω	—	8	—	9	—	7.5	—	8	

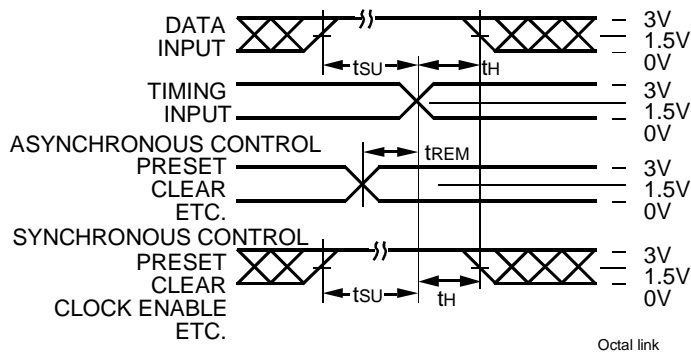
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

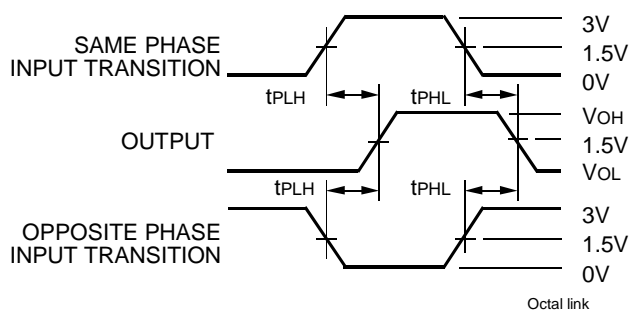
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



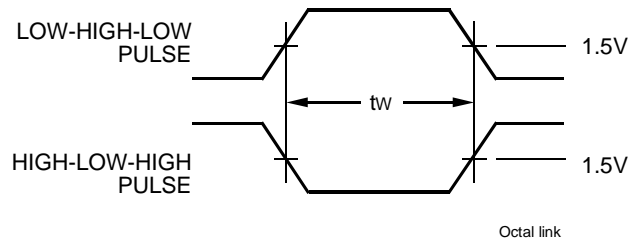
Propagation Delay

SWITCH POSITION

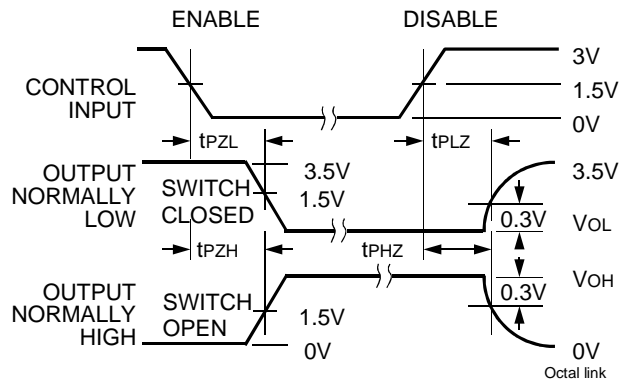
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

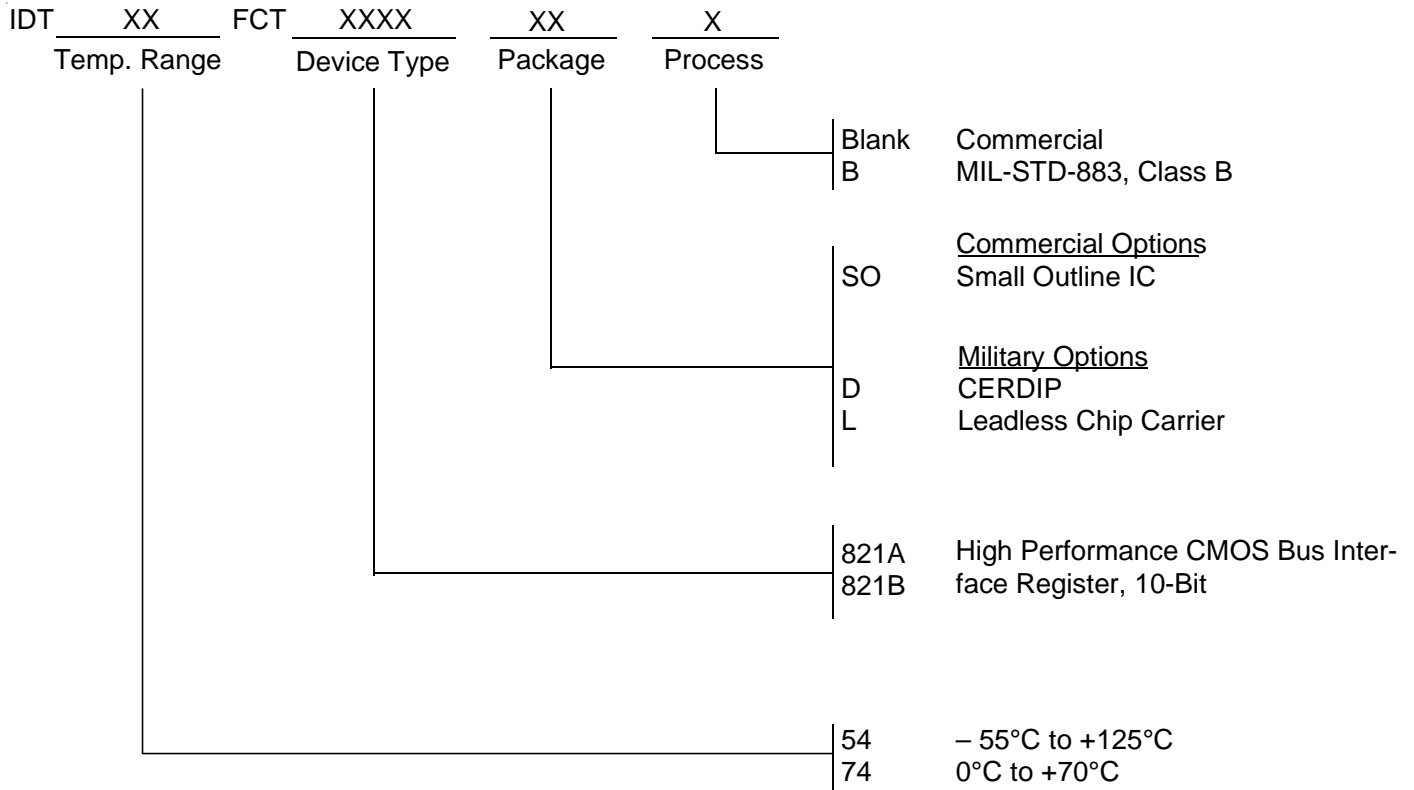


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_0 \leq 50\Omega$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

6/25/2002 Updated as per PDNs Logic-00-07 and Logic-01-04



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