

STRUCTURE Silicon Monolithic Integrated Circuit
PRODUCT SERIES 4-Channel Switching Regulator Controller for Digital Camera
TYPE **BD9352GUL**
BLOCK DIAGRAM Fig. 1
PACKAGE Fig. 2
PIN ASSIGNMENT Fig. 3
Functions

- Contains cross converter(1ch), step-down converter(2ch), step-up converter(1ch), configurable for inverting/step-down converter(1ch).
- 2channels contain transistor for synchronous rectifying action mode.
- 1channels contain FETs for the step-up converter.
- All channels contain internal compensation.
- It is possible separately control all channel
- Operating frequency 1.5MHz(CH2), 750kHz(CH1,3,4).
- Contains output interception circuit when over load.
- 1 channels have high side switches with soft start function.
- 3.3mm × 3.3mm t = 0.55mm WLCSP package (VCSP50L3)

○Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	VCC	−0.3~7	V
Power Input Voltage	VHx1~2	−0.3~7	V
	HS4H	−0.3~7	V
	VLx4	−0.3~22	V
	VDCM3	VCC−15~0.3	V
Output Current	IomaxHx1	+2.0	A
	IomaxHx2	+1.0	A
	IomaxHS4	+1.2	A
	IomaxLx4	±1.0	A
Power Dissipation	Pd	1325(*1)	mW
Operating Temperature	Topr	−25~+85	°C
Storage Temperature	Tstg	−55~+150	°C
Junction Temperature	Tjmax	+150	°C

(*1) When mounted on a glass epoxy PCB (50 mm x 58 mm x 1.75 mm). Reduced by 10.6 m W/°C when using at Ta = 25 °C or higher.

○Recommended operating conditions

Parameter	Symbol	Limit			Unit
		MIN	TYP	MAX	
Power Supply Voltage	VCC	2.5	—	5.5	V
VREF Pin Connecting Capacitor	CVREF	0.47	1.0	4.7	μ F
VREGA Pin Connecting Capacitor	CVREGA	0.47	1.0	4.7	μ F

Status of this document

The Japanese version of this document is the official specification. Please use the translation version of this document as a reference to expedite understanding of the official version.
If these are any uncertainty in translation version of this document, official version takes priority.

○Electrical characteristics (Ta=25°C, VCC=3.0V, STB1~4=3V)

Parameter	Symbol	Limit			Unit	Conditions
		MIN	TYP	MAX		
【Internal Regulator VREGA】						
Output Voltage	VREGA	2.4	2.5	2.6	V	Io=5mA
【Prevention Circuit of Miss Operation by Low voltage Input】						
Threshold Voltage	Vstd2	2.25	2.3	2.35	V	VCC Monitor
Hysteresis Width	Δ Vstd1	50	100	150	mV	
【Short Circuit Protection】						
SCP detect time	Tscp	20	25	30	ms	
Timer start threshold voltage	Vtcinv	0.38	0.48	0.58	V	INV Monitor CH2
【Oscillator】						
Frequency CH2	fosc1	1.2	1.5	1.8	MHz	
Frequency CH1,3,4	fosc2	0.6	0.75	0.9	MHz	
Max duty CH1 LX11	Dmax11	—	—	100	%	
Max duty CH1 LX12	Dmax12	86	92	96	%	
Max duty 2 (step-down)	Dmax2	—	—	100	%	
Max duty 3,4	Dmax3,4	86	92	96	%	
【Error Amp】						
Input Bias current	IINV	—	0	50	nA	INV1~4, NON3=3.0V
INV threshold 1	VINV1	0.79	0.80	0.81	V	CH1, 2, 4
【For Inverting Base Bias Voltage Vref】						
CH3 Output Voltage	VOUT3	-7.105	-7.00	-6.895	V	
Line Regulation	DVLI	—	4.0	12.5	mV	VCC=2.8~5.5V
Output Current When Shorted	Ios	0.2	1.0	—	mA	Vref=0V
【Soft start】						
CH1 Soft Start Time	Tss1	2.6	3.5	4.4	msec	
CH2 Soft Start Time	Tss2	0.6	0.9	1.2	msec	
CH3 Soft Start Time	Tss3	2.6	3.5	4.4	msec	
CH4 Soft Start Time	Tss4	2.6	3.5	4.4	msec	

Parameter	Symbol	Limit			Unit	Conditions	
		MIN	TYP	MAX			
【Output Driver】							
CH1 LX11 terminal Highside SW ON Resistance	RON11P	—	120	200	mΩ	Hx1=3.0V	
CH1 LX11 terminal Lowside SW ON Resistance	RON11N	—	130	210	mΩ	VCC=3.0V	
CH1 LX12 terminal Highside SW ON Resistance	RON12P	—	120	200	mΩ	VOUT1=3.0V	
CH1 LX12 terminal Lowside SW ON Resistance	RON12N	—	100	160	mΩ	VCC=3.0V	
CH2 Highside SW ON Resistance	RON2P	—	250	400	mΩ	Hx2=3.0V	
CH2 Lowside SW ON Resistance	RON2N	—	250	400	mΩ	VCC=3.0V	
CH3 Driver Output voltage H	Vout3H	VCC -1.5	VCC -1.0	—	V	IOUT3=-50mA ,NON3=0.2V	
CH3 Driver Output voltage L	Vout3L	—	0.5	1.0	V	IOUT3=50mA NON3=-0.2V	
CH4 NMOS SW ON Resistance	RON4N	—	500	800	mΩ	VCC=3.0V	
CH4 Load SW ON Resistance	RON4P	—	250	350	mΩ	HS4H=3V , VCC=3.0V	
【Discharge switch】							
CH3discharge SW ON Resistance	RDCM	82	165	330	Ω		
【Switch to configure Inverting/Step-down】							
IDSEL Control voltage	Step down	VIDDO	VCC × 0.7	—	VCC	V	(※1)
	Inverting	VIDIN	0	—	VCC × 0.3	V	(※1)
【STB1~4】							
STB Control voltage	Active	VSTBH1	1.5	—	5.5	V	
	Not Active	VSTBL1	-0.3	—	0.3	V	
Pull down Resistance		RSTB1	250	400	700	kΩ	
【Circuit Current】							
Stand-by Current	VBAT terminal	ISTB1	—	—	5	μA	
	Hx terminal	ISTB2	—	—	5	μA	Step down
	Lx terminal	ISTB3	—	—	5	μA	Step up
	HS4H terminal	ISTB4	—	—	5	μA	
Circuit Current (VCC current when voltage supplied for the terminal)		Icc	—	2.0	4.0	mA	INV1~ 4=1.2V , NON3=-0.2V

(※1)The input of IDSEL terminal is CMOS inverter input that makes VCC a power supply.

Please connect to either of GND or VCC for irregular prevention.

◎This product is not designed for normal operation with in a radioactive environment

○Block Diagram

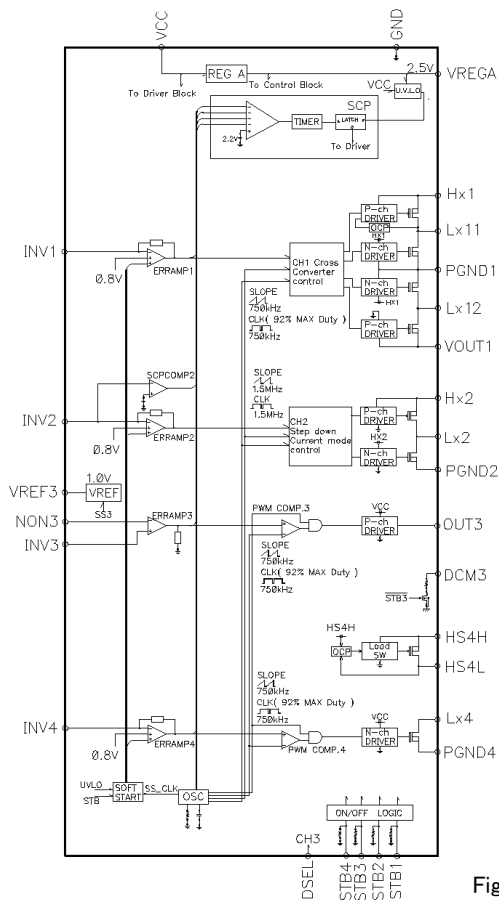


Fig. 1

○Pin Assignment

	1	2	3	4	5	6
A	GND	HX2	LX2	PGND2	HX1	HX1
B	GND	INV2	STB2	STB1	STB3	LX11
C	VCC	VREGA			STB4	PGND1
D	HS4H	INV4			IDSEL	LX12
E	HS4L	VREF3	NON3	INV3	INV1	VOUT1
F	TEST1	LX4	PGND34	OUT3	DCM3	TEST2

Fig. 3

○Package

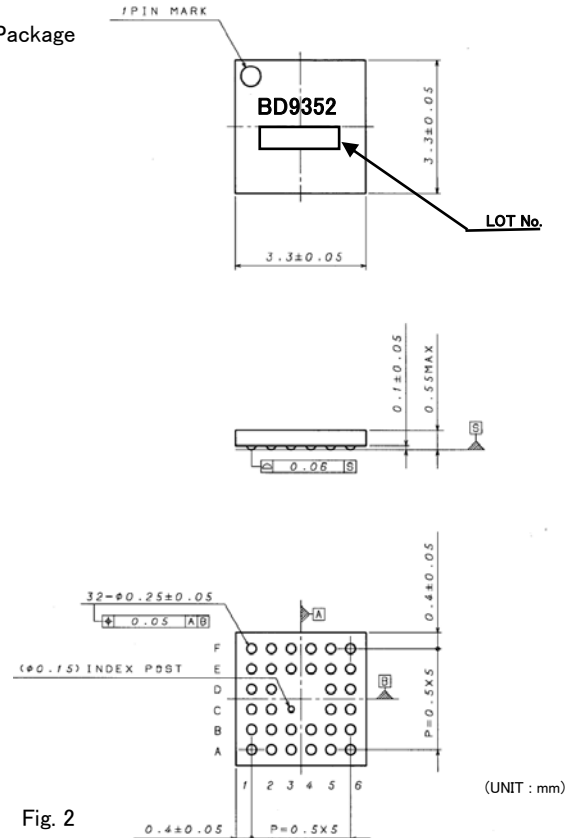


Fig. 2

Exposing the package to strong light like the strobe will cause incorrect operation of the device. Please confirm the operation after measure of shading so that light should not enter.

Pin No.	Pin Name	Functions
A1,B1	GND	Ground terminal
A2	HX2	CH2 Input terminal for synchronous High side switch, Power supply for Pch Driver
A3	LX2	CH2 Terminal for connecting inductors
A4	PGND2	CH2 Ground terminal for internal FET
A5, A6	HX1	CH1 Input terminal for synchronous High side switch, Power supply for Pch Driver
B2	INV2	CH2 Error AMP inverted input
B3	STB2	CH2 ON/OFF switch
B4	STB1	CH1 ON/OFF switch
B5	STB3	CH3 ON/OFF switch
B6	LX11	Terminal for connecting inductor for CH1 input
C1	VCC	Input for battery voltage
C2	VREGA	VREGA Output
C5	STB4	CH4 ON/OFF switch
C6	PGND1	CH1 Ground terminal for internal FET
D1	HS4H	CH4 Power supply for internal load switch
D2	INV4	CH3 Error AMP inverted input
D5	IDSEL	CH3 Inverting /Step down mode selector L : Inverting, H : Step down
D6	LX12	Terminal for connecting inductor for CH2 output
E1	HS4L	CH4 Power supply for internal load switch
E2	VREF3	CH3 base bias voltage
E3	NON3	CH3 Error AMP non-inverted input
E4	INV3	CH3 Error AMP inverted input
E5	INV1	CH1 Error AMP inverted input
E6	VOUT1	CH1 voltage output terminal
F1	TEST1	TEST terminal. Please short GND or OPEN
F2	LX4	CH4 Terminal for connecting inductors
F3	PGND34	Ground terminal for CH3 driver and CH4 internal FET
F4	OUT3	Terminal for connecting gate of CH3 PMOS
F5	DCM3	CH3 output voltage discharge terminal. When you don't use discharge function, please short GND terminal.
F6	TEST2	TEST terminal. Please short GND or OPEN

○Operation Notes

1.) Absolute maximum ratings

This product is produced with strict quality control. However, the IC may be destroyed if operated beyond its absolute maximum ratings. If the device is destroyed by exceeding the recommended maximum ratings, the failure mode will be difficult to determine. (E.g. short mode, open mode) Therefore, physical protection counter-measures (like fuse) should be implemented when operating conditions beyond the absolute maximum ratings anticipated.

2.) GND potential

Make sure GND is connected at lowest potential. All pins except NON3, must not have voltage below GND. Also, NON3 pin must not have voltage below - 0.3V on start up.

3.) Setting of heat

Make sure that power dissipation does not exceed maximum ratings.

4.) Pin short and mistake fitting

Avoid placing the IC near hot part of the PCB. This may cause damage to IC. Also make sure that the output-to-output and output to GND condition will not happen because this may damage the IC.

5.) Actions in strong magnetic field

Exposing the IC within a strong magnetic field area may cause malfunction.

6.) Mutual impedance

Use short and wide wiring tracks for the main supply and ground to keep the mutual impedance as small as possible. Use inductor and capacitor network to keep the ripple voltage minimum.

7.) Voltage of STB pin

The threshold voltages of STB pin are 0.3V and 1.5V. STB state is set below 0.3V while action state is set beyond 1.5V.

The region between 0.3V and 1.5V is not recommended and may cause improper operation.

The rise and fall time must be under 10msec. In case to put capacitor to STB pin, it is recommended to use under $0.01 \mu F$.

8.) Thermal shutdown circuit (TSD circuit)

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

9.) Light sensitivity

Exposing the package to strong light like the strobe will cause incorrect operation of the device.

Please confirm the operation after measure of shading so that light should not enter.

10.) IC Terminal Input

This IC is a monolithic IC that has a P- board and P+ isolation for the purpose of keeping distance between elements. A P-N junction is formed between the P-layer and the N-layer of each element, and various types of parasitic elements are then formed.

For example, an application where a resistor and a transistor are connected to a terminal (shown in Fig.4):

○When GND > (terminal A) at the resistor and GND > (terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.

○When GND > (terminal B) at the transistor (NPN), a parasitic NPN transistor operates as a result of the NHayers of other elements in the proximity of the aforementioned parasitic diode.

Parasitic elements are structurally inevitable in the IC due to electric potential relationships. The operation of parasitic elements induces the interference of circuit operations, causing malfunctions and possibly the destruction of the IC. Please be careful not to use the IC in a way that would cause parasitic elements to operate. For example, by applying a voltage that is lower than the GND (P-board) to the input terminal.

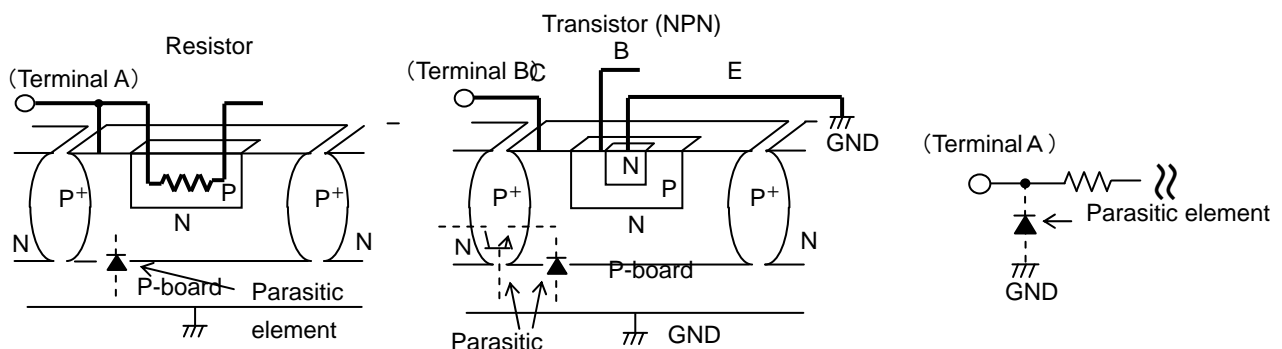


Fig – 4 Simplified structure of a Bipolar IC

Notes

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