

- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-leg IGBT) or a UV fault (Lower-side supply).
- Input interface : 3, 5V line CMOS/TTL compatible. (High Active)
- UL Approved : Yellow Card No. E80276

AC100V~200V inverter drive for small power motor control.

All outer lead terminals are with Pb-free solder plating.

- 1: In order to get enough creepage distance between the terminals, please take some countermeasure such as a slit on P-OB.
- 2: To the terminal VNO of PS21564-P as NC. (just the same as DIP-IPM ver.2) However, external connection of VNO with N terminals is necessary for PS21562-P or PS21563-P.

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TRANSFER-MOLD TYPE

INSULATED TYPE

MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CC}	Supply voltage	Applied between P-N	450	V
V _{CC(surge)}	Supply voltage (surge)	Applied between P-N	500	V
V _{CES}	Collector-emitter voltage		600	V
±I _C	Each IGBT collector current	$T_f = 25^\circ\text{C}$	15	A
±I _{CP}	Each IGBT collector current (peak)	$T_f = 25^\circ\text{C}$, less than 1ms	30	A
P _C	Collector dissipation	$T_f = 25^\circ\text{C}$, per 1 chip	22.2	W
T _j	Junction temperature	(Note 1)	-20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_f \leq 100^\circ\text{C}$) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(\text{ave})} \leq 125^\circ\text{C}$ (@ $T_f \leq 100^\circ\text{C}$).

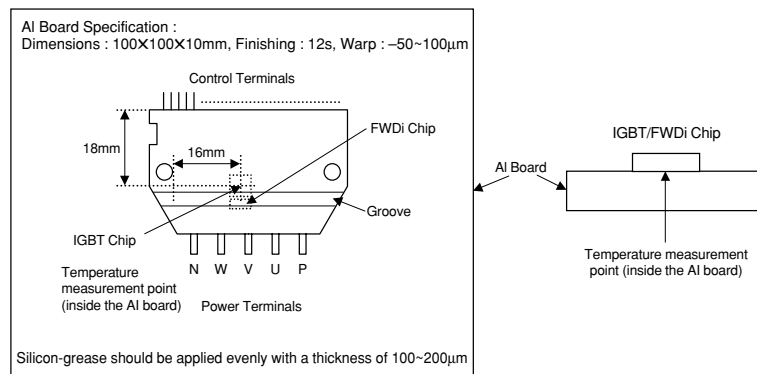
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VNC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{IN}	Input voltage	Applied between UP, VP, WP, UN, VN, WN-VNC	-0.5~V _D +0.5	V
V _{FO}	Fault output supply voltage	Applied between FO-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at FO terminal	1	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(prot)}	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part $T_j = 125^\circ\text{C}$, non-repetitive, less than 2 μs	400	V
T _f	Module case operation temperature	(Note 2)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, 1 minute, All connected pins to heat-sink plate	2500	V _{rms}

Note 2 : T_f measurement point



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THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-f)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	4.5	°C/W
$R_{th(j-f)F}$		Inverter FWD part (per 1/6 module)	—	—	6.5	°C/W

Note 3: Grease with good thermal conductivity should be applied evenly with about +100 μ m~+200 μ m on the contacting surface of DIP-IPM and heat-sink.

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 5\text{V}$	—	1.45	1.95	V
		$I_C = 15\text{A}, T_j = 25^\circ\text{C}$ $I_C = 15\text{A}, T_j = 125^\circ\text{C}$	—	1.55	2.05	
V_{EC}	FWD forward voltage	$T_j = 25^\circ\text{C}, -I_C = 15\text{A}, V_{IN} = 0\text{V}$	—	1.50	2.00	V
t_{on}	Switching times	$V_{CC} = 300\text{V}, V_D = V_{DB} = 15\text{V}$ $I_C = 15\text{A}, T_j = 125^\circ\text{C}, V_{IN} = 0 \leftrightarrow 5\text{V}$ Inductive load (upper-lower arm)	0.60	1.20	1.80	μs
t_{rr}			—	0.30	—	μs
$t_{c(on)}$			—	0.40	0.60	μs
t_{off}			—	1.50	2.10	μs
$t_{c(off)}$			—	0.50	0.80	μs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$ $T_j = 25^\circ\text{C}$	—	—	1	mA
		$T_j = 125^\circ\text{C}$	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
Id	Circuit current	VD = VDB = 15V VIN = 5V	Total of VP1-VNC, VN1-VNC	—	—	5.00	mA
			VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	—	—	0.40	
		VD = VDB = 15V VIN = 0V	Total of VP1-VNC, VN1-VNC	—	—	7.00	
			VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	—	—	0.55	
VFOH	Fault output voltage	VSC = 0V, FO circuit pull-up to 5V with 10kΩ		4.9	—	—	V
VFOL		VSC = 1V, IFO = 1mA		—	—	0.95	V
VSC(ref)	Short circuit trip level	Tf = -20~100°C, Vd = 15V (Note 4)		0.45	—	0.52	V
IIN	Input current	VIN = 5V		1.0	1.5	2.0	mA
UVDBt	Control supply under-voltage protection	Tj ≤ 125°C	Trip level	10.0	—	12.0	V
UVDBr			Reset level	10.5	—	12.5	V
UVDt			Trip level	10.3	—	12.5	V
UVDr			Reset level	10.8	—	13.0	V
tFO	Fault output pulse width	CFO = 22nF (Note 5)		1.0	1.8	—	ms
Vth(on)	ON threshold voltage	Applied between UP, VP, WP-VNC, UN, VN, WN-VNC		2.1	2.3	2.6	V
Vth(off)	OFF threshold voltage			0.8	1.4	2.1	V

Note 4: Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the current rating.

5: Fault signal is asserted corresponding to a short circuit or lower side control supply under-voltage failure. The fault output pulse width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : $C_{FO} = 12.2 \times 10^{-6} \times t_{FO} [\text{F}]$.

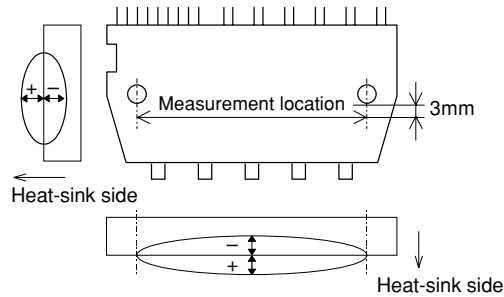
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MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	Recommended : 0.78 N·m	0.59	—	0.98	N·m
Weight			—	20	—	g
Heat-sink flatness	(Note 6)		-50	—	100	μm

Note 6: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Recommended value			Unit
				Min.	Typ.	Max.	
VCC	Supply voltage	Applied between P-N		0	300	400	V
VD	Control supply voltage	Applied between VP1-VNC, VN1-VNC		13.5	15.0	16.5	V
VDB	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS		13.0	15.0	18.5	V
ΔVD, ΔVDB	Control supply variation			−1	—	1	V/μs
tdead	Arm shoot-through blocking time	For each input signal, Tf ≤ 100°C		2.0	—	—	μs
fPWM	PWM input frequency	Tf ≤ 100°C, Tj ≤ 125°C		—	—	20	kHz
Io	Allowable r.m.s. current	VCC = 300V, VD = VDB = 15V, P.F = 0.8, sinusoidal output Tf ≤ 100°C, Tj ≤ 125°C (Note 7)	fPWM = 5kHz	—	—	7.5	Arms
			fPWM = 15kHz	—	—	4.8	
PWIN(on)	Allowable minimum input pulse width	(Note 8)		0.3	—	—	μs
PWIN(off)		200 ≤ VCC ≤ 350V, 13.5 ≤ VD ≤ 16.5V, 13.0 ≤ VDB ≤ 18.5V, −20°C ≤ Tf ≤ 100°C, N-line wiring inductance less than 10nH (Note 9)	Below rated current	0.5	—	—	
			Between rated current and 1.7 times of rated current	2.0	—	—	
			Between 1.7 times and 2.0 times of rated current	2.6	—	—	
VNC	VNC variation	Between VNC-N (including surge)		−5.0	—	5.0	V

Note 7: The allowable r.m.s. current value depends on the actual application conditions.

8: The input pulse width less than PWIN(on) might make no response.

9: IPM might not work properly or make response for the input signal with OFF pulse width less than PWIN(off).

Please refer to Fig.7.

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Fig. 4 THE DIP-IPM INTERNAL CIRCUIT

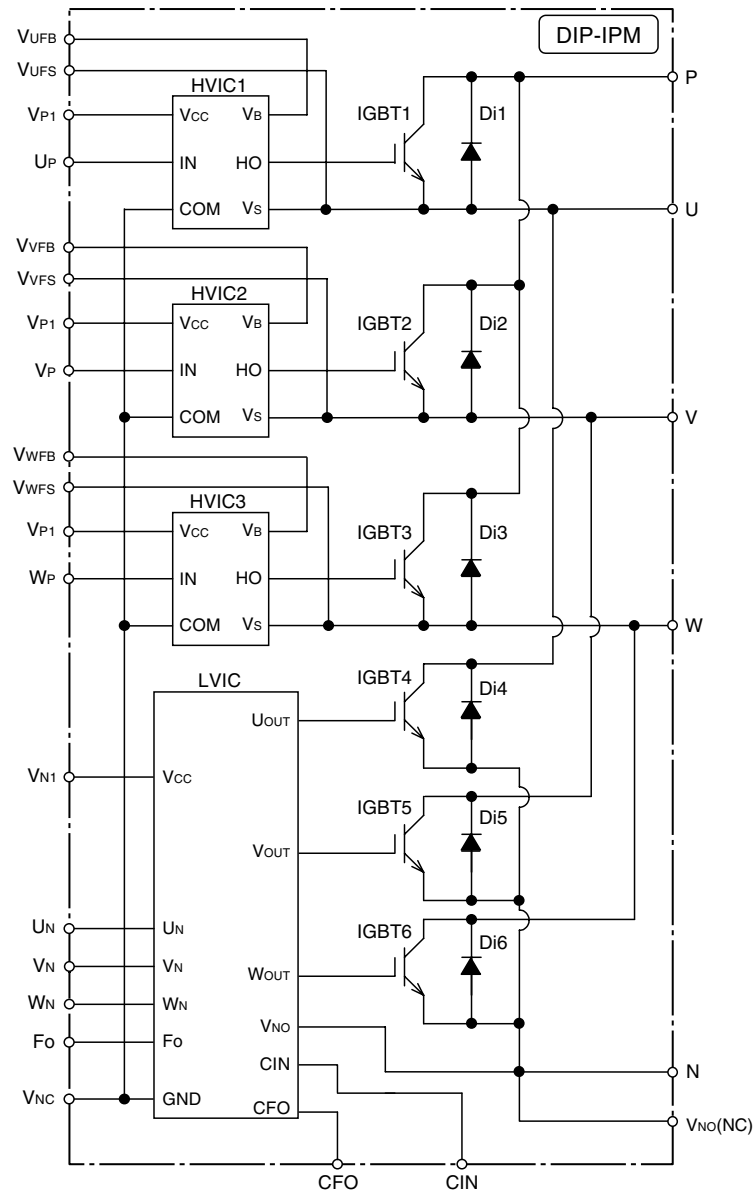
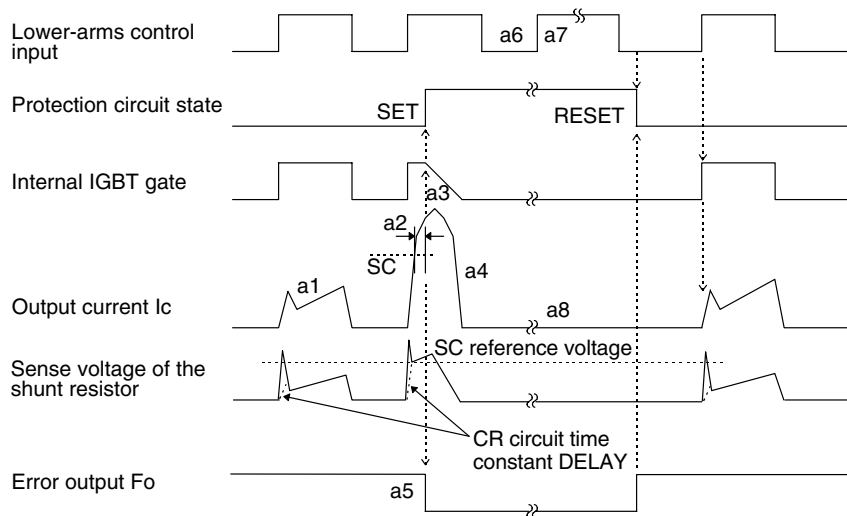


Fig. 5 TIMING CHART OF THE DIP-IPM PROTECTIVE FUNCTIONS

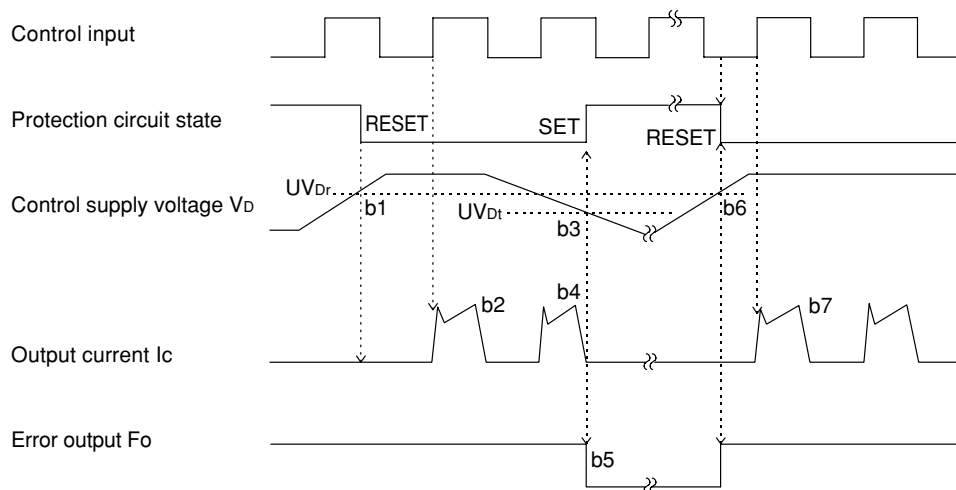
[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. FO timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{FO}.
- a6. Input "L" : IGBT OFF.
- a7. Input "H" : IGBT ON.
- a8. IGBT OFF in spite of input "H".



[B] Under-Voltage Protection (Lower-arm, UVd)

- b1. Control supply voltage rises : After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV_{Dt}).
- b4. IGBT OFF in spite of control input condition.
- b5. FO operation starts.
- b6. Under voltage reset (UV_{Dr}).
- b7. Normal operation : IGBT ON and carrying current.



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[C] Under-Voltage Protection (Upper-arm, UV_{DB})

- c1. Control supply voltage rises : After the voltage reaches UVDBr, the circuits start to operate when next input is applied.
- c2. Normal operation : IGBT ON and carrying current.
- c3. Under voltage trip (UVDBt).
- c4. IGBT OFF in spite of control input condition, but there is no FO signal output.
- c5. Under voltage reset (UVDBr).
- c6. Normal operation : IGBT ON and carrying current.

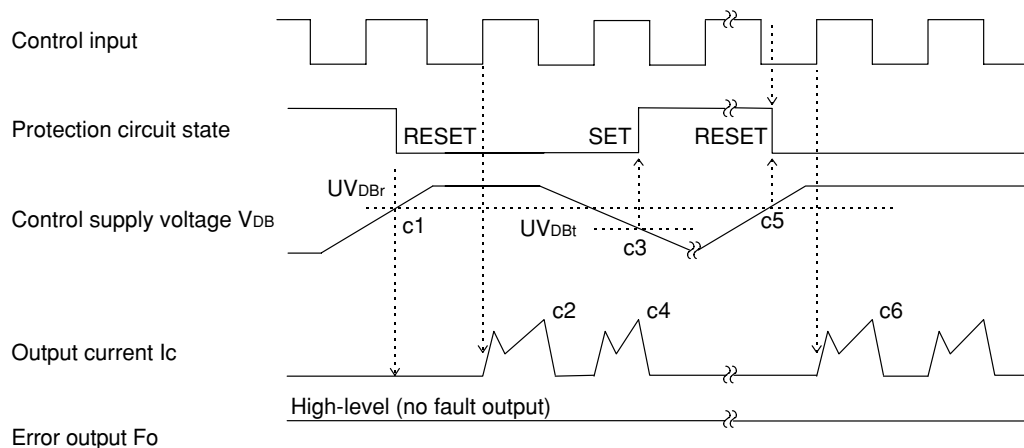
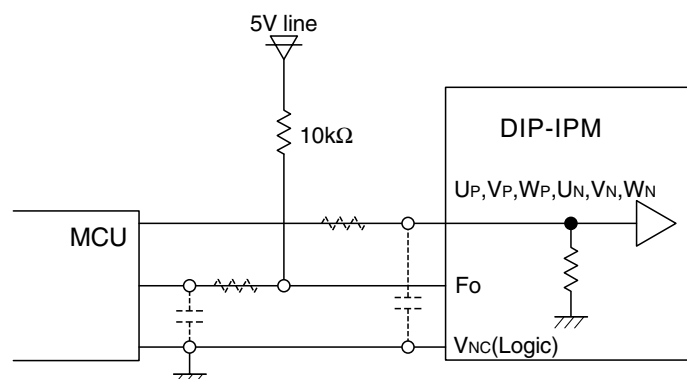


Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT



Note : The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.

The DIP-IPM input section integrates a 2.5k Ω (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

Fig. 7 WIRING CONNECTION OF SHUNT RESISTOR

