Z-Communications, Inc.

9939 Via Pasar • San Diego, CA 92126
TEL (858) 621-2700   FAX (858) 621-2722

PCA0090A
PHASE LOCKED LOOP
Rev A1

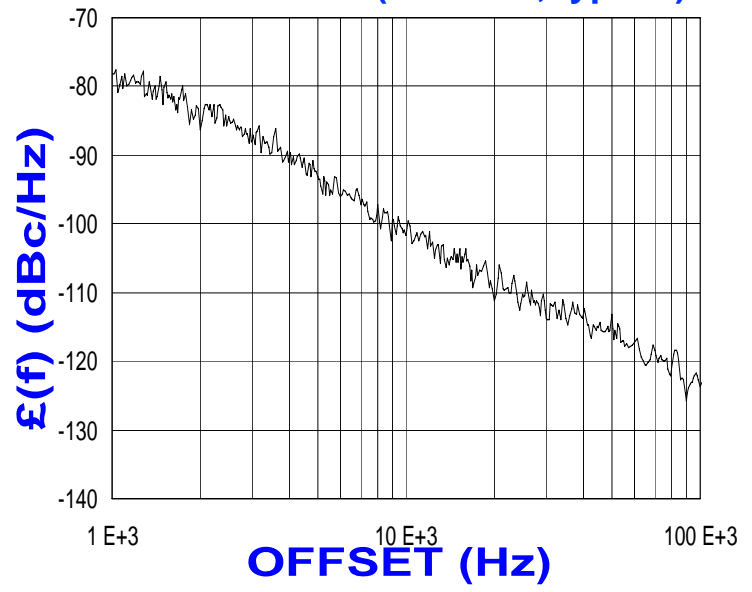## PHASE NOISE (1 Hz BW, typical)

FEATURES

- Frequency Range: 85 - 95 MHz
- Step Size: 50 KHz
- cPLL - Style Package

APPLICATIONS

- Telecommunications
- Satellite
- Telemetry

PERFORMANCE SPECIFICATIONS	VALUE	UNITS
Frequency Range	85 - 95	MHz
Phase Noise @ 10 kHz offset (1 Hz BW, typ.)	-101	dBc/Hz
Harmonic Suppression (2nd, typ.)	-10	dBc
Sideband Spurs (typ.)	-65	dBc
Power Output	0.5±2.5	dBm
Load Impedance	50	Ω
Step Size	50	KHz
Charge Pump Output Current	1250	μA
Switching Speed (typ., adjacent channel)	<4	mSec
Startup Lock Time (typ.)	4	mSec
Operating Temperature Range	-40 to 85	°C
Package Style	cPLL	
POWER SUPPLY REQUIREMENTS		
Supply Voltage (Vcc, nom.)	3.3	Vdc
Supply Current (Icc, typ.)	25	mA

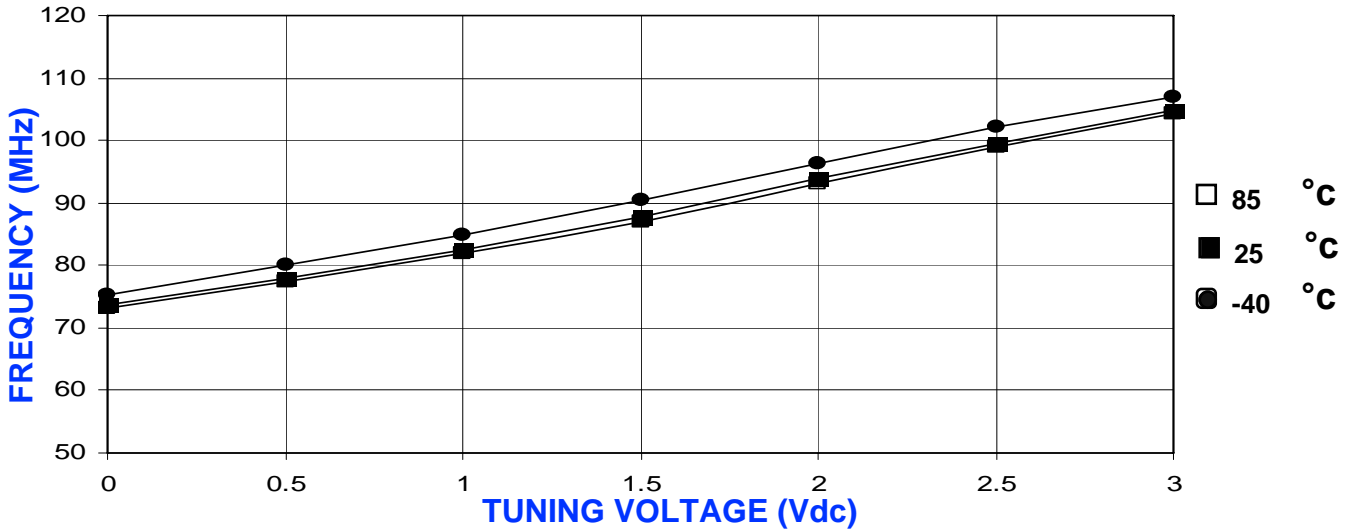All specifications are typical unless otherwise noted and subject to change without notice.

APPLICATION NOTES

- AN-107 : How to Solder Z-COMM VCOs / PLLs
- AN-200 : Mounting and Grounding of Z-COMM PLLs
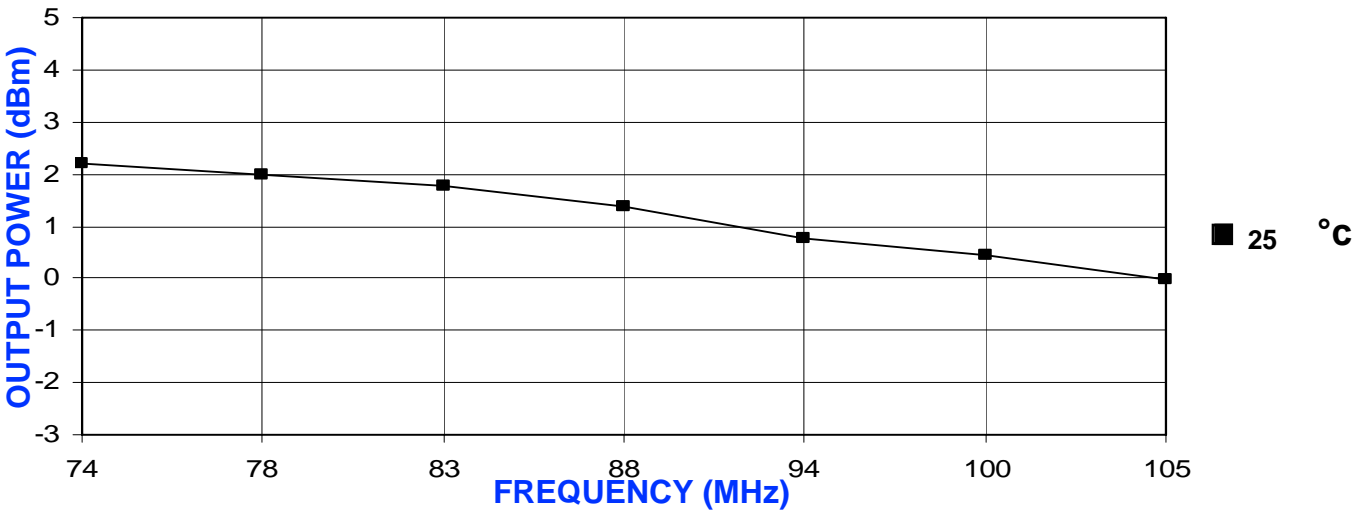- AN-201 : PLL Fundamentals   AN-202 : PLL Functional Description

NOTES:

Reference Oscillator Signal: 5 MHz<f_{osc}<100 MHz
Frequency Synthesizer: Analog Devices - ADF4001

VCO TUNING CURVE, typ.

Y-axis: **FREQUENCY (MHz)** — 50 to 120
X-axis: **TUNING VOLTAGE (Vdc)** — 0 to 3

Legend:
- □ 85 °C
- ■ 25 °C
- ⬤ -40 °C

VCO POWER CURVE, typ.

Y-axis: **OUTPUT POWER (dBm)** — -3 to 5
X-axis: **FREQUENCY (MHz)** — 74, 78, 83, 88, 94, 100, 105

Legend:
- ■ 25 °C

PHYSICAL DIMENSIONS

CPLL
415-0108 REV. A
(DRAWING NOT TO SCALE)

BOTTOM

-0.120
0.000
0.130
0.260
SEE DETAIL 'A'
0.380

0.500
0.380
0.250
0.120
0.000

SEE DETAIL 'B'

.065
.015
.030

DETAIL B (TYP)
(8 PLACES)

0.032
0.140

DETAIL A

TABS RANGE:
SEE NOTE 5
(4 PLACES)

TOP

12 11 10
1   9
2   8
3   7
4 5 6

P1   RF OUTPUT
P2   REFERENCE OSCILLATOR INPUT
P3   CLOCK
P4   DATA
P5   LOAD ENABLE
P6   LOCK DETECT
P7   VCC
P8   OPTIONAL
P9   NO CONNECTION
P10-12   GROUND

NOTES:
1. THE INSIDE RADIUS OF ALL 12 HALF HOLES AT THE PERIMETER OF THE BOARD ARE PLATED TO PROVIDE A SURFACE FOR THE ATTACHMENT OF THE PLL MODULE TO A PCB IN 11 LOCATIONS, WITH 8 PADS BEING USED FOR ELECTROMECHANICAL INTERFACE AND 3 PADS FOR GROUNDING.
2. THE SURFACE OF THE SHIELD IS TIN PLATED AND MAY BE SOLDERED TO. THE SHIELD'S BASE METAL IS COLD ROLLED STEEL.
3. THE GROUND PLANE IS GROUND AND ATTACHES TO A GROUND TRACK ON THE UPPER SIDE OF THE BOARD AS WELL AS THE SHIELD BY PTH.
4. UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES.
5. UNLESS OTHERWISE NOTED ALL TOLERANCES ARE AS FOLLOWS:
   .XXX= ± .010