

3W Mono Fully Differential

Audio Power Amplifier

DESCRIPTION

The EUA6204A is a mono fully-differential audio amplifier, capable of delivering 3W of continuous average power to an 3Ω BTL load with less than 10% distortion (THD+N) from a 5V power supply, and 720mW to a 8Ω load from a 3.6V power supply.

The EUA6204A is ideal for PDA/notebook and portable devices application due to features such as -80-dB supply voltage rejection from 20Hz to 2kHz, improved RF rectification immunity, and a fast startup with minimal pop.

The EUA6204A is available in a SOP-8(FD).

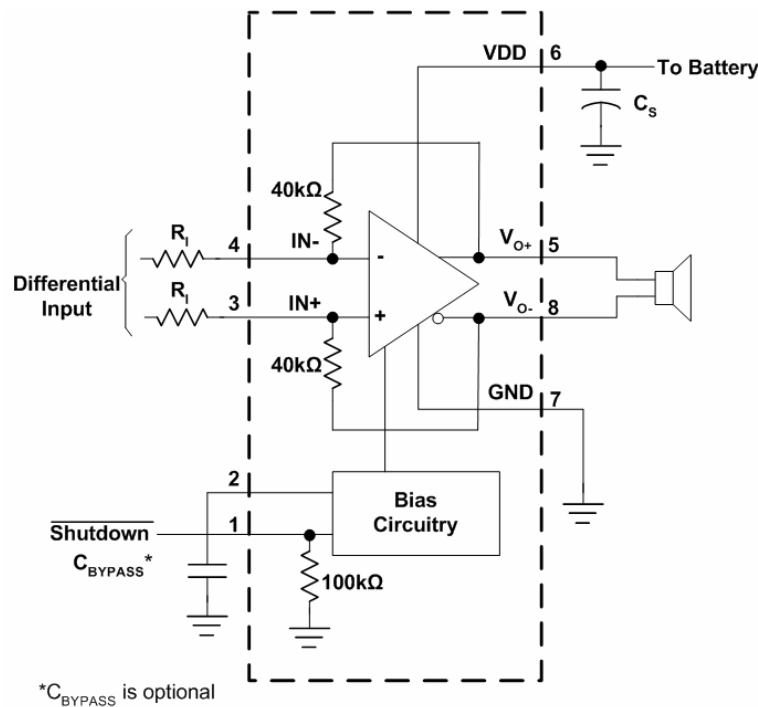
FEATURES

- Supply Voltage 2.5V to 5.5V
- 2.3W into 3Ω from a 5-V Supply at THD=1% (typ)
3W into 3Ω at THD=10%
- Low Supply Current: 4mA typ at 5V
- Shutdown Current: 0.01μA typ
- Fast Startup with Minimal Pop
- Only Three External Components
 - Improved PSRR (-80dB) for Direct Battery Operation
 - Full Differential Design Reduces RF Rectification
 - -63dB CMRR Eliminates Two Input Coupling Capacitors
- RoHS Compliant and 100% Lead (Pb)-Free

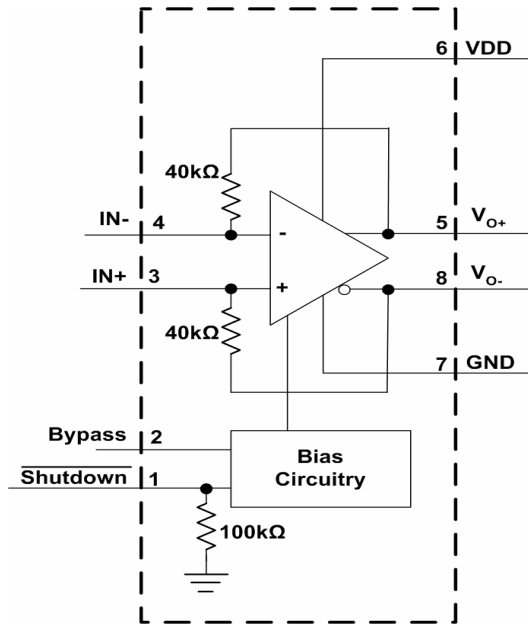
APPLICATIONS

- PDAs
- Portable Devices
- Notebook

Typical Application Circuit



Block Diagram




Pin Configurations

Package	Pin Configurations
Plastic SOP-8(FD)* * Thermal Pad	<p>The diagram shows the physical pin configuration for the Plastic SOP-8(FD) package. Pin 1 (Shutdown) is at the top left, pin 2 (Bypass) is below it, pin 3 (IN+) is below that, and pin 4 (IN-) is at the bottom left. On the right side, pin 8 (VO-) is at the top, pin 7 (GND) is below it, pin 6 (VDD) is below that, and pin 5 (VO+) is at the bottom right. A central Thermal Pad is located between the two sides of the package.</p>

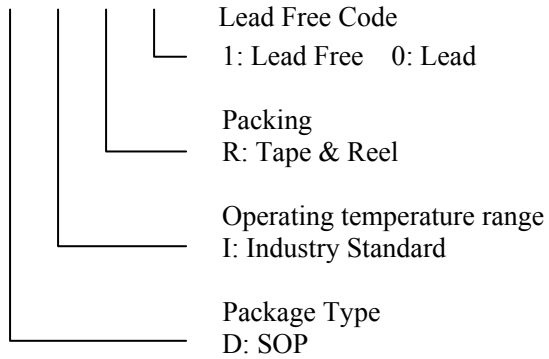
Pin Description

SYMBOL	PIN	DESCRIPTION
Shutdown	1	Shutdown terminal
Bypass	2	Mid-supply voltage, adding a bypass capacitor improves PSRR
IN+	3	Positive differential input
IN-	4	Negative differential input
VO+	5	Positive BTL output
VDD	6	Power supply
GND	7	High-current ground
VO-	8	Negative BTL output

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUA6204ADIR1	SOP-8	 xxxx EUA6204 A	-40°C to 85°C

EUA6204A



Absolute Maximum Ratings

Supply voltage, V_{DD}	6V
Input voltage, V_I	-0.3 V to $V_{DD} + 0.3V$
Storage temperature rang, T_{stg}	-65°C to 150°C
ESD Susceptibility	2kV
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (SOP-8)	42.3°C/W

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	2.5		5.5	V
High-level input voltage, V_{IH}	1.55			V
Low-level input voltage, V_{IL}			0.5	
Operating free-air temperature, T_A	-40		85	°C

Electrical Characteristics, $T_A=25^\circ\text{C}$

Symbol	Parameter	Conditions	EUA6204A			Unit
			Min	Typ	Max.	
V_{OS}	Output offset voltage (measured differentially)	$V_I=0V$ differential, Gain=1V/V, $V_{DD}=5.5V$	-9	2	9	mV
PSRR	Power supply rejection ratio	$V_{DD}=2.5V$ to 5.5V		-85	-60	dB
V_{IC}	Common mode input range	$V_{DD}=2.5V$ to 5.5V	0.5		$V_{DD}-0.8$	V
CMRR	Common mode rejection range	$V_{DD}=2.5V$, $V_{IC}=0.5V$ to 1.7V		-63	-40	dB
		$V_{DD}=5.5V$, $V_{IC}=0.5V$ to 4.7V		-63	-40	
	Low-output swing	$R_L=8\Omega$, Gain=1V/V $V_{IN+}=V_{DD}$, $V_{IN-}=0V$ or $V_{IN+}=0V$, $V_{IN-}=V_{DD}$	$V_{DD}=5.5V$	0.45		V
$V_{DD}=3.6V$			0.37			
$V_{DD}=2.5V$			0.26	0.4		
	High-output swing	$R_L=8\Omega$, Gain=1V/V $V_{IN+}=V_{DD}$, $V_{IN-}=0V$ or $V_{IN-}=V_{DD}$, $V_{IN+}=0V$	$V_{DD}=5.5V$	4.95		V
$V_{DD}=3.6V$			3.18			
$V_{DD}=2.5V$			2	2.13		
$ I_{IH} $	High-level input current, Shutdown	$V_{DD}=5.5V$, $V_I=5.8V$		58	100	μA
$ I_{IL} $	Low-level input current, Shutdown	$V_{DD}=5.5V$, $V_I=-0.3V$		3	100	μA
I_Q	Quiescent current	$V_{DD}=2.5V$ to 5.5V, no load		4	8	mA
$I_{(SD)}$	Supply current	$V(\text{Shutdown}) \leq 0.5V$, $V_{DD}=2.5V$ to 5.5V, $R_L=8\Omega$		0.01	1	μA
	Gain	$R_L=8\Omega$	$\frac{38k\Omega}{RI}$	$\frac{40k\Omega}{RI}$	$\frac{42k\Omega}{RI}$	V/V
	Resistance from shutdown to GND			100		k Ω

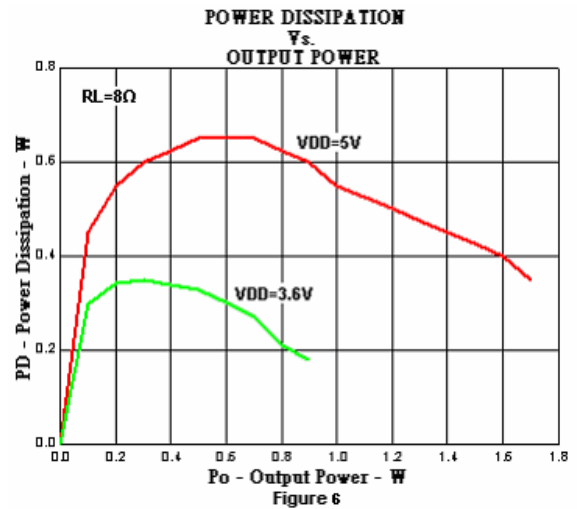
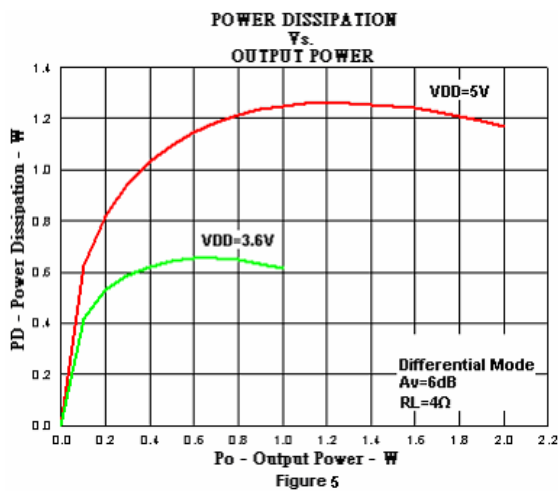
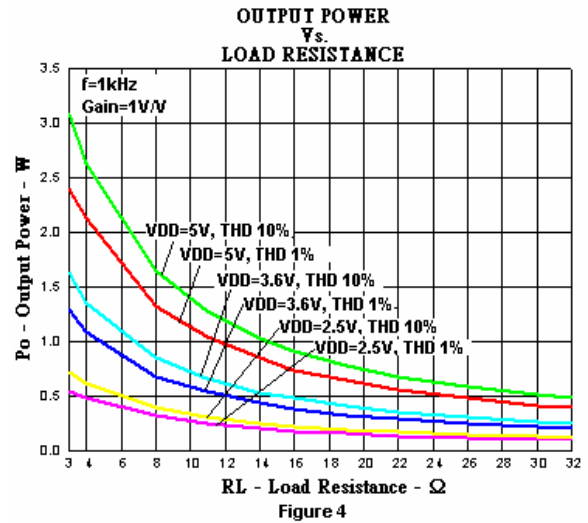
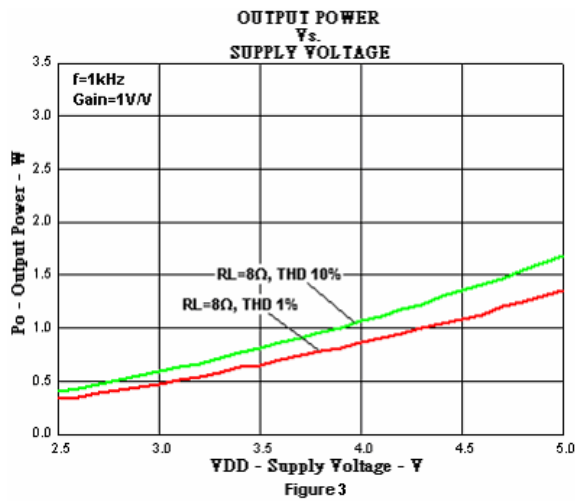
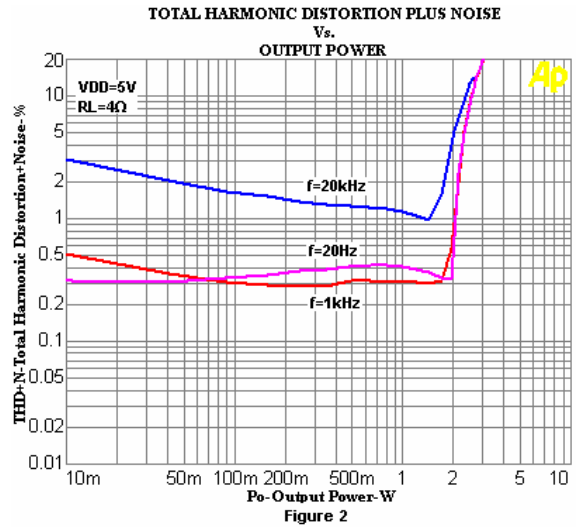
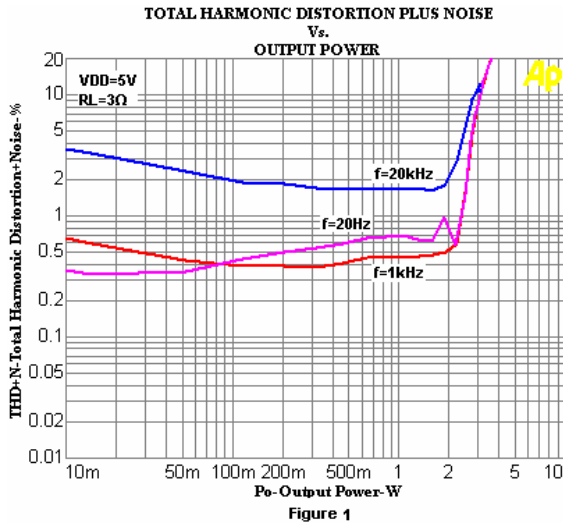
Operating Characteristics, $T_A=25^\circ\text{C}$, Gain=1V/V

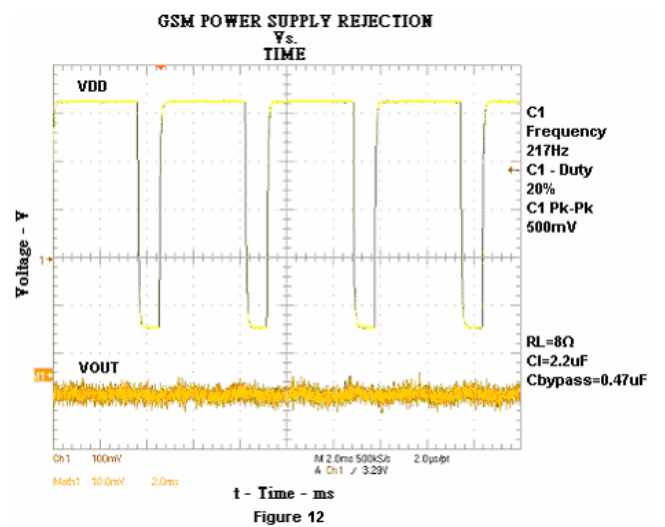
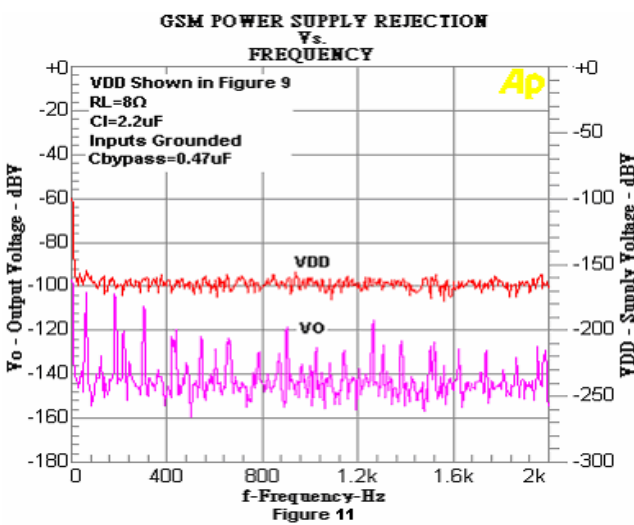
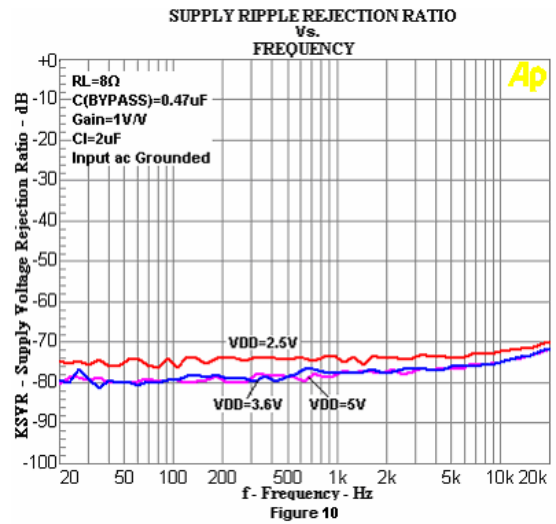
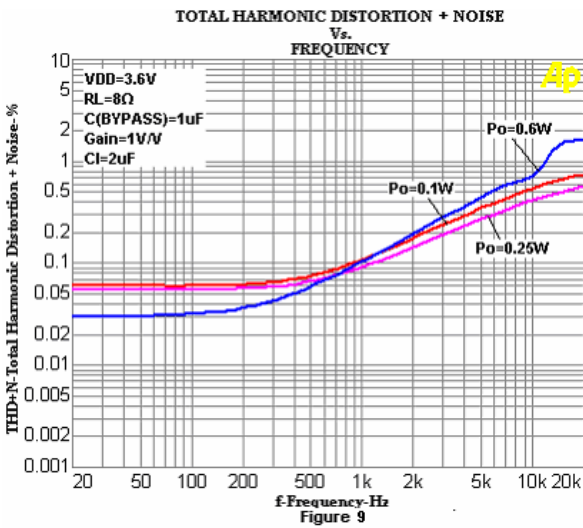
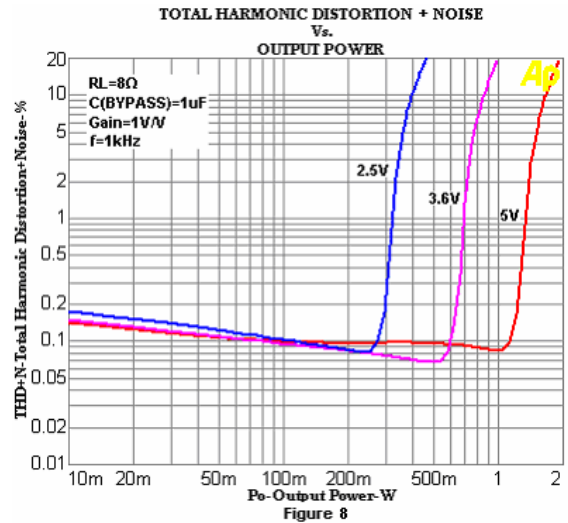
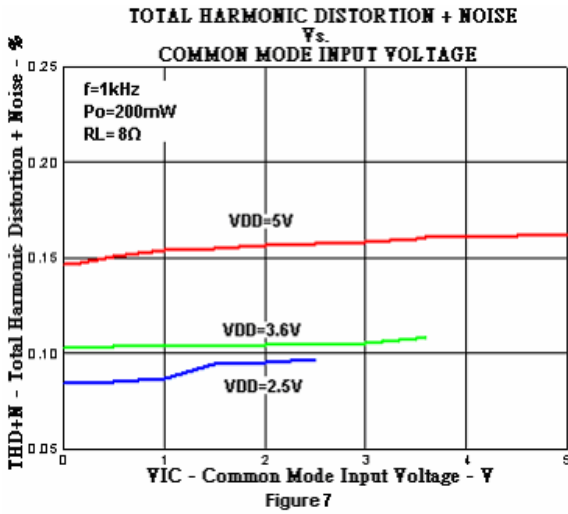
Symbol	Parameter	Conditions		EUA6204A			Unit
				Min	Typ	Max.	
P_O	Output power	THD+N=1%, f=1kHz, $V_{DD}=5\text{V}$	$R_L=3\Omega$		2.3		W
			$R_L=4\Omega$		2.1		
			$R_L=8\Omega$		1.36		
		THD+N=10%, f=1kHz, $V_{DD}=5\text{V}$	$R_L=3\Omega$		3		W
			$R_L=4\Omega$		2.6		
			$R_L=8\Omega$		1.7		
THD+N	Total harmonic distortion plus noise	$V_{DD}=5\text{V}$, $P_O=1\text{W}$, $R_L=8\Omega$, f=1kHz			0.15		%
		$V_{DD}=3.6\text{V}$, $P_O=0.5\text{W}$, $R_L=8\Omega$, f=1kHz			0.1		
		$V_{DD}=2.5\text{V}$, $P_O=200\text{mW}$, $R_L=8\Omega$, f=1kHz			0.1		
K_{SVR}	Supply ripple rejection ratio	$V_{DD}=3.6\text{V}$, Inputs ac-grounded with $C_i=2\mu\text{F}$, $V_{(\text{Ripple})}=200\text{mVpp}$	f = 217Hz		-77		dB
			f=20Hz to 20kHz		-60		
SNR	Signal-to-noise ratio	$V_{DD}=5\text{V}$, $P_O=1\text{W}$, $R_L=8\Omega$			100		dB
V_n	Output voltage noise	$V_{DD}=3.6\text{V}$, f=20Hz to 20kHz, Inputs ac-grounded with $C_i=2\mu\text{F}$	No weighting		25		μV_{RMS}
			A weighting		19		
CMRR	Common mode rejection ratio	$V_{DD}=3.6\text{V}$ $V_{IC}=1\text{Vpp}$	f=217Hz		-64		dB
R_F	Feedback resistance			38	40	44	k Ω
	Start-up time from shutdown	$V_{DD}=3.6\text{V}$, $C_{\text{BYPASS}}=0.1\mu\text{F}$			27		ms

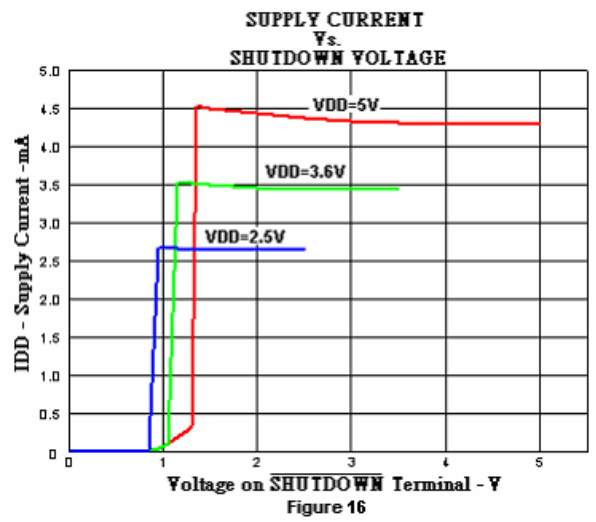
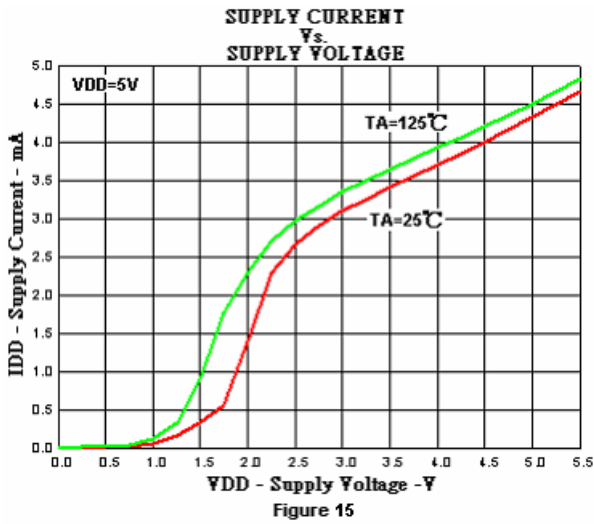
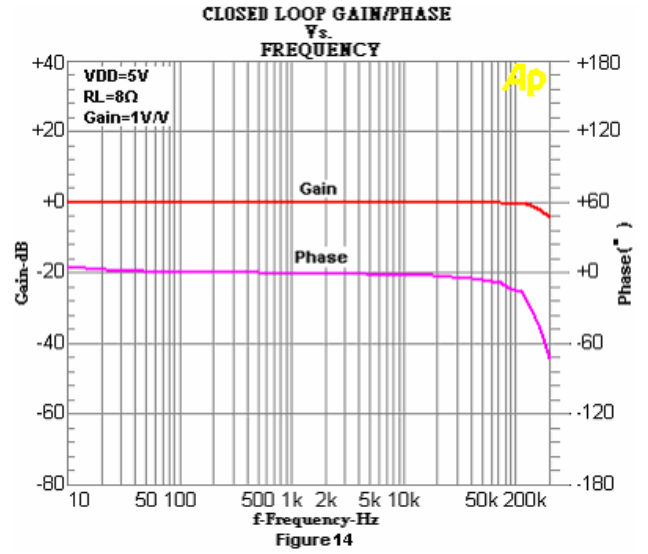
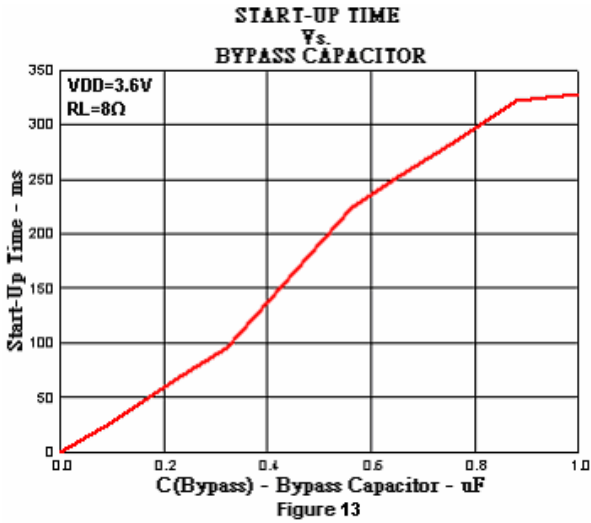
Note:

1. When driving 3 Ω or 4 Ω load from a 5V supply, the EUA6204A must be mounted to a circuit board with thermal pad.

Typical Operating Characteristics







Application Information

Application Schematics

Figure17 through Figure18 show application schematics for differential and single-ended inputs. Typical values are shown in Table1.

Table1. Typical Component Value

Component	Value
R _I	40kΩ
C _(BYPASS)	0.22μF
C _S	1μF
C _I	0.22μF

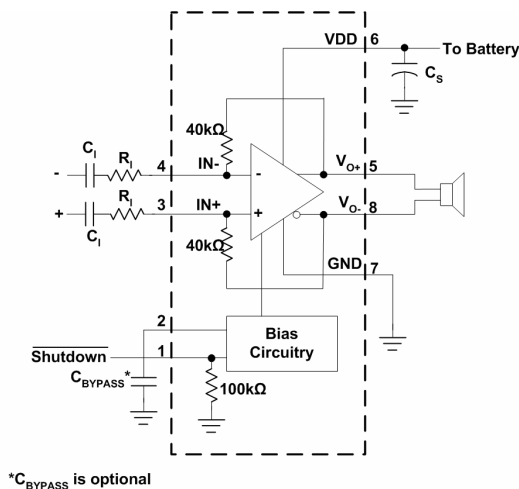
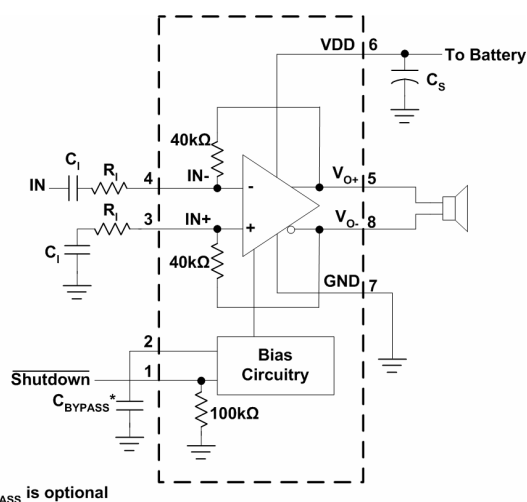


Figure17. Differential Input Application Schematic Optimized with Input Capacitors



** Due to the fully differential design of this amplifier, the performance is severely degraded if you connect the unused input to BYPASS when using single-ended inputs

Figure18. Single-Ended Input Application Schematic

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the EUA6204A has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs of from equation 1.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \text{ -----(1)}$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determine from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the EUA6204A. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power.

Proper Selection of External Components

Gain-Setting Resistor Selection

The input resistor (R_I) can be selected to set the gain of the amplifier according to equation 2.

$$\text{Gain} = R_F / R_I \text{ (2)}$$

The internal feedback resistors (R_F) are trimmed to 40kΩ. Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

Bypass Capacitor (C_{BYPASS}) and Start-up Time

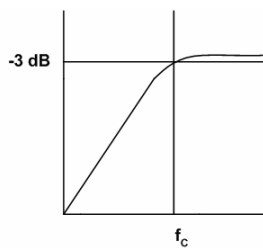
The internal voltage divider at the Bypass pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to V_{DD}/2. Adding a capacitor to this pin filters any noise into this pin and increases k_{SVR}. C_(BYPASS) also determines the rise time of V_{O+} and V_{O-} when the device is taken out of shutdown. The larger the capacitor, the slower the rise time. Show the relationship of C_(BYPASS) to start-up time as Figure13.

Input Capacitor (C_I)

The EUA6204A does not require input coupling capacitors if using a differential input source that is biased from 0.5V to $V_{DD} - 0.8V$. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application an input capacitor, C_I , is required to allow the amplifier to bias the input signal to the proper dc level. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 3.

$$f_C = \frac{1}{2\pi R_I C_I} \quad (3)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit.

Consider the example where R_I is 10k Ω and the specification calls for a flat bass response down to 100Hz. Equation 3 is reconfigured as equation 4.

$$C_I = \frac{1}{2\pi R_I f_C} \quad (4)$$

In this example, C_I is 0.16 μ F, so one would likely choose a value in the range of 0.22 μ F to 0.47 μ F.

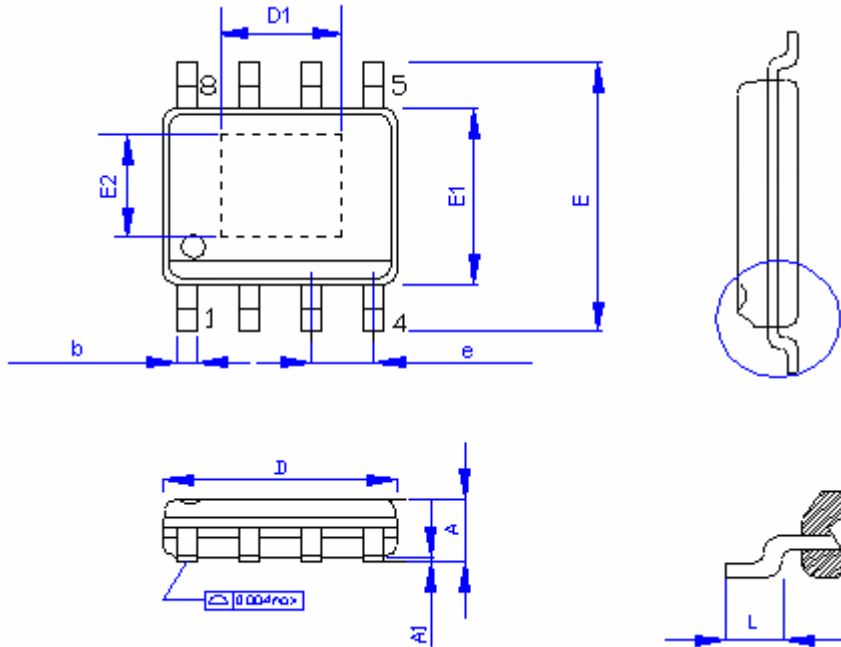
Ceramic capacitors should be used when possible, as they are the best choice in preventing leakage current. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (C_S)

The EUA6204A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μ F to 1 μ F, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a 10- μ F or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

Package Information

SOP-8 (FD)



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.05	0.25	0.002	0.010
D	4.90		0.193	
E1	3.90		0.153	
E	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
b	0.33	0.51	0.013	0.020
e	1.27		0.500	
D1	2.06		0.081	
E2	2.06		0.081	