# 4-BIT MCU FOR REMOTE CONTROLLER(MASK TYPE)

DESCRIPTION

SC73C1402 is one of Silan's 4-bit CMOS single-chip micro-controllers for infrared remote control transmitters (IRCTs). It can be implemented in various IRCT circuits by mask option.

FEATURES

* Operating voltage range: (2.0 ~ 4.0V)
  Low static power consumption (<1uA)
* Program memory: 2Kx 9 bits
  The last 1K areas can also be used as data table
* Data memory (RAM): 16 x 4 bits
* Timer/counter: 10~15 bits
* 20 I/O ports, where there is a 4-bit input, two 4-bit outputs and two 4-bit programmable input/output ports(P53 is output but not used as keypress).
* Oscillator frequency (fosc):
  300KHz~2MHz or 2MHz~6MHz selectable by mask option
* Operating frequency (fmain):
  fmain=fosc   (when fosc in the range of 300KHz~2MHz)
  fmain=fosc/8 (when fosc in the range of 2MHz~6MHz)
* Carrier frequency: fmain/12
* Carrier duty: 1/2 or 1/3 duty selectable by program
* Instruction cycle: 5/fmain
* Handles various user's codes, repeat key, persist-key press and many other functions
* Power on reset
* Supports voltage-drop detection
* Supports 56 keys in 20-pin package, and 80 keys in 24-pin package.

SOP-20-300-1.27

SOP-20-375-1.27
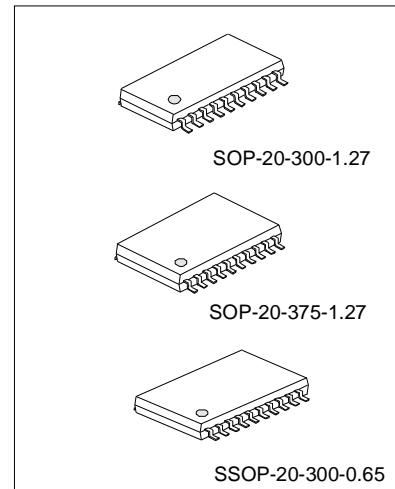
SSOP-20-300-0.65

ORDERING INFORMATION

Device	Package
SC73C1402	SOP-24-375-1.27
SC73C1402A	SOP-20-300-1.27
SC73C1402B	SSOP-20-300-0.65
SC73C1402C	SOP-20-375-1.27
SC73C1402D	DIE
SC73C1402E	SSOP-24-300-0.65

APPLICATIONS

* Infrared remote control devices, such as TV, Video Cassette Recorder, VTR, laser phonograph and acoustics remote controllers.

BLOCK DIAGRAM
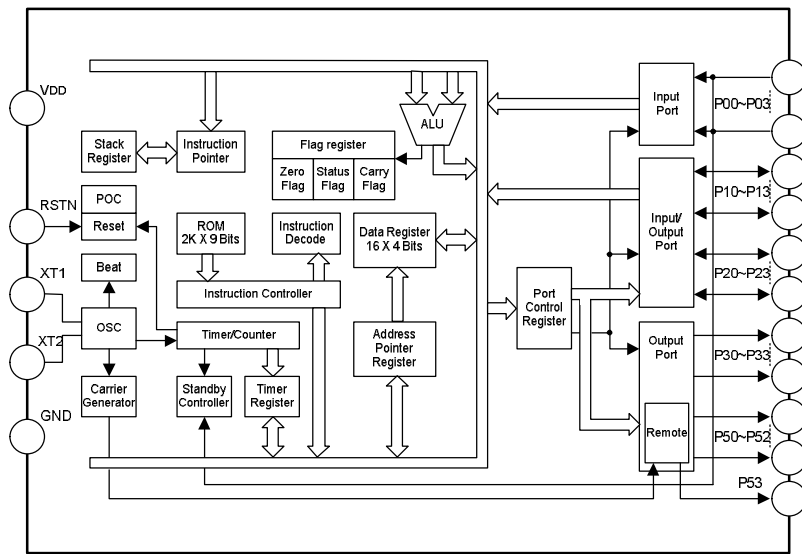
ABSOLUTE MAXIMUM RATINGS (Tamb=25°C)

Characteristics	Symbol	Value	Units
Supply Voltage	V_{DD}	-0.3 ~ +5.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Output Current	I_{OUT} (P53)	-6	mA
Power Consumption	P_D	500	mW
Storage Temperature	T_{stg}	-40~+125	°C
Operating Temperature	T_{opr}	-10~+70	°C

ELECTRICAL CHARACTERISTICS (Tamb=25°C, VDD=3.0V)

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units.
Power Supply Voltage	V_{DD}	All function		2	--	4	V
Operating Current	I_{DD}	In operating		--	--	0.5	mA
Oscillation Frequency	F_{OSC}	MASK1		300K	455k	2M	Hz
		MASK2		2M	4M	6M	Hz
Static Current	I_{DS}	Oscillator stops		--	--	1	μA
Input Pull-Down Resistor	R	V_{DD}=3V	P51, P52	50	65	80	KΩ
			P00-P03 P10-P13	80	95	110	KΩ
High Input Voltage	V_{IH}	--		0.7V_{DD}	--	V_{DD}	V
Low Input Voltage	V_{IL}	--		0	--	0.3V_{DD}	V

(To be continued)

(Continued)

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units.
High Output Current	IOH	V$_{DD}$=3V V$_{OH}$=2.7V	P53	--	-5.5	--	mA
			P52	--	-3.6	--	
			P10-P13 P20-P23 P30-P33 P50-P51	--	-0.8	--	
Low Output Current	IOL	V$_{DD}$=3V V$_{OL}$=0.3V	P53	--	1.3	--	mA
			P52	--	0.17	--	
			P10-P13 P20-P23 P30-P33 P50-P51	--	0.17	--	

PIN CONFIGURATIONS

SOP-24
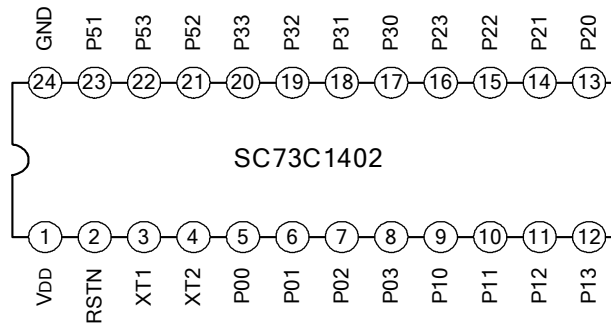
SOP-20/SSOP-20 project 1   **SOP-20/SSOP-20 project 2**
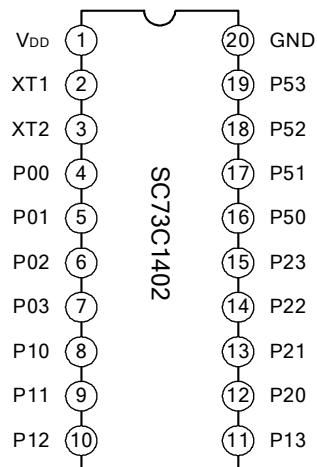
SOP-20/SSOP-20 project 3

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         ┌───────∪───────┐
P22  (1) │               │ (20)  P21
P23  (2) │               │ (19)  P20
P51  (3) │               │ (18)  P13
P52  (4) │               │ (17)  P12
P53  (5) │   SC73C1402   │ (16)  P11
VDD  (6) │               │ (15)  P10
XT1  (7) │               │ (14)  P03
XT2  (8) │               │ (13)  P02
GND  (9) │               │ (12)  P01
RSTN (10)│               │ (11)  P00
         └───────────────┘
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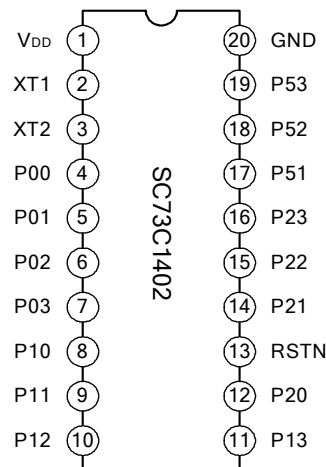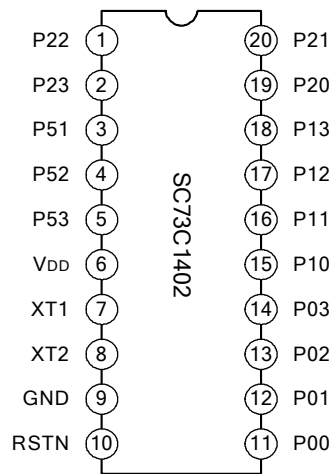
PIN DESCRIPTION

Symbol	Description
VDD	Power supply (2.0V~4.0V)
GND	
RSTN	Reset （active low）
P50	P-channel open-drain output
XT1	Crystal oscillator output
XT2	Crystal oscillator input
P00~P03	4-bit input pin (with internal pull-down resistor). This pin is used for keyboard scan and to control internal circuit.
P10~P13	4-bit I/O port (It can be set to input or output by program, with internal pull-down resistor). In input mode, it can be used for keyboard scan. In output mode, used for keyboard scan output.
P20~P23	4-bit I/O port (It can be set to input or output by program, with internal pull-down resistor). In input mode, it can be used for keyboard scan. In output mode, can be used for keyboard scan output.
P30~P33	4-bit output pin can be used for keyboard scan output.
P52	It can be set input/output mode by mask option. In output mode, have large current when output high level(can be used to drive LED). In input mode, it can be used for keyboard scan input.
P53	Outputs remote signal with carrier.
P51	It can be set input/output mode by mask option. In output mode, it can be used for keyboard scan output. In input mode, it can be used for keyboard scan input.

FUNCTION DESCRIPTION

1. PC: 11 bits

PC refers to program counter. The maximum addressing area is 2K bytes in ROM. The program counter contains the address of the instruction that will be executed next. When reset, the value of the PC is cleared to 0. The PC is set to predefined value when one of the 3 following occasions occurs: 1) when the JUMP instruction is executed; 2) when a subroutine call is back; 3) when a program call is back. In the SC73C1402, all instructions are 1-byte OP Code instructions, PC increments by 1 each time an instruction is executed.

2. MBR

Memory buffer register (MBR) is the write-only, higher 4-bit of the program pointer. The ROM of the SC73C1402 can be divided into 16 blocks. Each block has 128 bytes. These blocks can be addressed by the MBR. When the program starts executing a branch instruction, it will load the corresponding value to the MBR register, and then executes the command BSS label.

3. STACK

STACK refers to stack register (11 bits). It stores the previous value of program pointer during execution of subroutine calls. Because there is only one-level hardware stack register, only one-level programs can be called. When the user tries to make a nested two-level program call, an error will occur.

4. B, H, D

BHD refers to the pointers to data table. They are all 4-bit. The last 1K-byte area of ROM (400H~7FFH) can also be used for data table. When addressing the data of the program in ROM, the registers act as the pointers to the data table. In other cases, the H, D registers can be used as general purpose registers. Data stored in the data table can be addressed by the 2 transmit instructions (see the following 2 instructions: LDL A, @HD, and LDH A, @HD. When executing the above 2 transmit-instructions, the program searches the data in the data table automatically. The lower 10-bit of the ROM is decided by the lower 2-bit of the B register, and all bits of the H & D register.

When the BR [3] of B register is set to "1", the carrier duty is 1/2; when BR [3] is set to "0", then the carrier duty is 1/3.

The BR [2] of B register is "1", the carrier output port is opened, if BR [2]=0, the carrier output port is closed.

5. ROM

Address	2k x 9bits
000H 001H	Reset address
002H ⋮ 01FH	Subroutine address
020H ⋮ 3FFH	Program address
400H ⋮ 7FFH	Data table and program multiplex areas

6. LR

LR refers to the L register (4 bits). It is often used to store the pointer of RAM addresses, and can also be used as a general-purpose register.

7. RAM

RAM refers to data memory. It consists of 16 x 4bits and is used to store temporary data and results after a program is executed. There are two RAM addressing modes: one for indirect addressing by the LR register, it can address the entire RAM areas. The other is instruction direct addressing, the lower 3-bit of the instruction specifying the address of the RAM. It can be used to address the lower 8-bit of the RAM, but SC73C1402 does not support this mode. When reset, the contents of RAM are not defined. We recommend users to initialize it at the beginning of the program.

8. ALU

The arithmetic and logic unit plays a leading role in performing various operations of 4-bit binaries. The operation of the ALU will change the carry flag and the zero flag.

9. Acc

4-bit accumulator, it is mostly used to store data and results.

10. CF

CF refers to carry flag.

11. SF

SF refers to the status flag. When reset, the status flag is initialized to 1.

12. PR

PR refers to the port register, which specifies the input mode or output mode of the I/O ports, is 4-bit write-only. When one bit of PR is 1, the corresponding port is set to output mode; if the bit of PR is 0; then set to input mode. The execution of the HOLD instruction won't affect the status of PORT1 and PORT2. When reset, the value of the PR is 0000B.

– – – –	P2S	P1HS	P1LS

P11, P10 mode select

P13, P12 mode select

PORT2 mode select
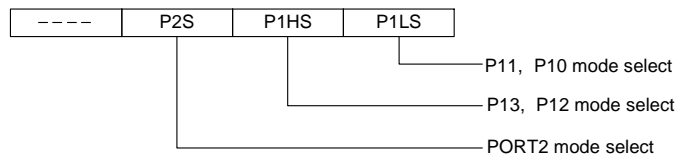
13. PORT

SC73C1402 has five groups of I/O ports, altogether 20 pins.

P0 port: P03~P00, 4-bit input port, with internal pull-down resistor; it can release the HOLD mode at high level.

P1 port (P13~P10) and P2 port (P23~P20) can be set to input/output mode by program. In input mode, it can release HOLD mode at high level.

P3 port (P30~P33) output port.

P5 port (P53, P52, P51, P50)

P50: output pin, P-channel open-drain output, this pin is always used to select system code.

P51: output pin, this pin is always used to select system code.

P52: output pin. It can output large current when output high level; this pin can be used to drive LED display.

P53: Large current output port, this pin can be used to output infrared remote signal. If P53 is set to 1.this pin outputs modulated signal with carrier whose frequency is OSC/12 (1/3 duty). If it is set to 0, this pin output s low level signal.

When the MCU reads the P5 port, it reads the contents of the timer instead of port status.

P53	P52	P51	P50
IT3	IT2	IT1	IT0

14. Timer/counter

SC73C1402 has an on-chip 17-bit timer. The clock source of the timer is the main frequency (fmain) of the circuit. There are timing steps from 10 steps (which generates pulses with frequency $fmain/2^{10}$) to 15 ($fmain/2^{15}$). The timer outputs pulse frequency ranging from $fmain/2^{10}$ to $fmain/2^{15}$, it can be used for timer after releasing the HOLD mode, and it can also be used as a WDT. After release the HOLD mode released and the timer reset instruction TMRST executed, the timer value is cleared.

15. TR

TR refers to the timer register. It selects the status of the timer mode, 4-bit write-only. The SC73C1402 has no special instructions to read the register, so please use the following instructions: LD A, %5 or LD @LR, %5.The corresponding relationships are: P53—IT3; P52—IT2; P51—IT1; P50—IT0.

3	2	1	0
IBNS	TIBS		

TR timer register
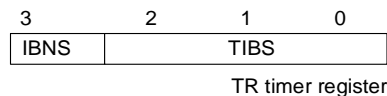
16. IBNS

The control bit of the read timer. When the value is 0, read P53 (IT3), IT2~IT0 become 0; when the value is 1, read 4-bit data P53~P50 (IT3~IT0).

P53: $2^{15}/fmain$

P52: $2^{14}/fmain$

P51: $2^{13}/fmain$

P50: $2^{12}/fmain$

TIBS: only valid when IBNS=0

000: $2^{10}/fmain$	50% duty	100: $2^{12}/fmain$	75% duty
001: $2^{11}/fmain$	50% duty	101: $2^{13}/fmain$	50% duty
010: $2^{11}/fmain$	75% duty	110: $2^{13}/fmain$	75% duty
011: $2^{12}/fmain$	50% duty	111: $2^{14}/fmain$	50% duty

The value of timer increments by 1 each time a clock is coming. When executing the instruction IN %5, A=LD A, %5 and IN %5, @LR=LD @LR, %5, the timer sends the complement value of the counter to the A and RAM. Therefore, after reset, every bit of the read timer is set to 1.

The maximum adjustable time of the timer is $2^{16}/FMAIN$. When the timer acts as a WDT and the timer is activated, it must execute the TMRST instruction and clear the timer in $2^{16}/FMAIN$'s time, otherwise, it will lead the WDT to overflow, and cause the MCU to reset.
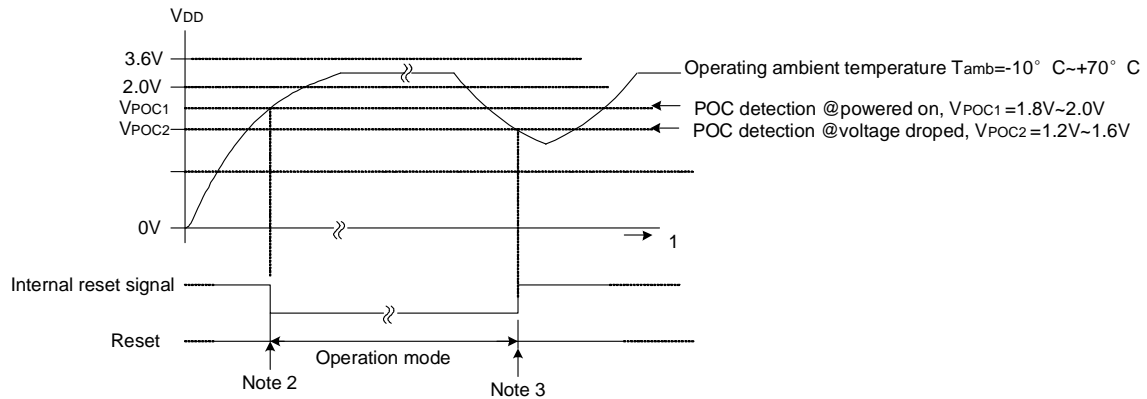
17. POC circuit

The POC circuit monitors the power supply voltage and applies an internal reset to the micro-controller.

The POC circuit has the following functions:

• Generates an internal reset signal when $V_{DD} \leq V_{POC}$ [note1].

• Cancels an internal reset signal when $V_{DD} > V_{POC}$.

Here, V_{DD}: power supply voltage, V_{POC}: POC detection voltage (including V_{POC1} & V_{POC2}).

Notes1. V_{POC} is different in different conditions. When powered on, the V_{POC} value is V_{POC1}(V_{POC1}=1.8V~2.0V);

when working, V_{POC} is approximately V_{POC2} in normal conditions(V_{POC2}=1.2V~1.6V).

2. Actually, there is a short oscillation stabilization wait time before the circuit is in operation mode.

The oscillation stabilization wait time is about 2^{16}/fmain.

3. The POC circuit generates an internal reset signal when the power supply voltage has fallen.

18. Instruction cycle

Instructions and internal operations are executed in sync with the main clock. The minimum unit of instruction is called the instruction cycle. SC73C1402 has 1 and 2-cycle OP code instructions.

An instruction cycle consists of 5 states (STCLK1 – STCLK5). Each state consists of 1 main clock. Therefore, the instruction cycle time is 5/fmain [s].

INSTRUCTION SETS

1.Transmit instruction：

Instruction	Operation	CF	SF	Cycle
LD A, L	A ← LR	---	1	1
LD A, D	A ← DC	---	1	1
LD A, H	A ←HR	---	1	1
LD A, @LR	A ← RAM (LR)	---	1	1
LD A, #K	A ← K	---	1	1
LDL A, @HD	A ← ROM (HD) L	---	1	2
LDH A, @HD	A ← ROM (HD) H	---	1	2
LD L, A	LR ← A	---	1	1
LD L, #K	LR ← K	---	1	1
LD @LR, A	RAM (LR) ← A	---	1	1
LD @LR, #K	RAM (LR) ← K	---	1	1
LD DC, A	DC ← A	---	1	1
LD P, A	PR ← A	---	1	1
LD T, A	TR ← A	---	1	1
LD B, A	BR ← A	---	1	1
LD H, A	HR ← A	---	1	1

a. LD A, L   Load values in the LR register to the accumulator.

b. LD A, D   Load values in the DC register to the accumulator.

c. LD A, H   Load the values in the HR register to the accumulator.

d. LD A, @LR   Load the contents of RAM pointed at by the LR register to the accumulator.

e. LD A, #K   Load the 4-bit immediate K to accumulator.

f. LDL A, @HD   Load the lower 4-bit of ROM data pointed at by the HD to the accumulator.

g. LDH A, @HD   Load the higher 4-bit of ROM data pointed at by the HD to the accumulator.

h. LD L, A   Load the contents of the accumulator to the LR register.

i. LD L, #K   Load immediate K to the LR register.

j. LD @LR, A   Load the content of the accumulator to RAM pointed at by the LR register.

k. LD @LR, #K   Load the immediate K to RAM pointed at by the LR register.

l. LD DC, A   Load the content of the accumulator to the DC register.

m. LD P, A   Load the content of the accumulator to the port register (PR).

n. LD T, A   Load the content of the accumulator to the timer register.

o   LD B, A   Load the content of the accumulator to the BR register.

p   LD H, A   Load the content of the accumulator to the HR register.

Executing the above 15 transmit-instructions will not affect the carry flag and the status flag remains 1.

2. Input/output instruction

Instruction	Operation	CF	SF	Cycle
IN A, %P	A ← PORT (P)	---	/Z	2
IN @LR, %P	@LR ← PORT (P)	---	/Z	2
OUT %P, A	PORT (P) ← A	---	1	2
OUT %P, @LR	PORT (P) ← @LR	---	1	2

a.   IN A, %P   Move the value of port (P) to the accumulator

b.   IN @LR, %P   Move the value of port (P) to ROM pointed at by the LR register.

c.   OUT %P, A   Move the contents of the accumulator to port (P).

d.   OUT %P, @LR   Load the contents of RAM pointed at by the LR register to port (P).

   The above four input/output instructions are used mostly for port operation; the two read instructions would affect the status flag SF.

3. Arithmetic and logical instructions

Instruction	Operation	CF	SF	Cycle
ADD A, @LR	A ← A+RAM (LR)	---	/C	1
ADDC A, @LR	A ← A+RAM (LR)+CF	C	/C	1
ADD A, #K	A ← A+K	---	/C	1
ADD L, #K	LR ← LR+K	---	/C	2
SUBRC A, @LR	A ← RAM (LR)-A-/CF	C	C	1
INC @LR	RAM (LR) ← RAM (LR)+1	---	/C	1
DEC @LR	RAM (LR) ← RAM (LR)-1	---	C	1
INC D	DC ← DC+1	---	/C	1
DEC D	DC ← DC-1	---	C	1
AND A, @LR	A ← A&RAM (LR)	---	/Z	1
OR A, @LR	A ← A	RAM (LR)	---	/Z	1
XOR A, @LR	A ← A^RAM (LR)	---	/Z	1

a.   ADD A, @LR   Add the contents of RAM pointed at by the LR to accumulator. Store the sum in the ACC. This operation will affect SF, SF=/CF.

b.   ADDC A, @LR   Add the contents of RAM pointed at by the LR register to accumulator with carry. Store the carry bit in the CF. This operation will affect SF, SF=/CF.

c.   ADD A, #K   Add immediate K to accumulator. Store the sum in the ACC. This operation will affect SF, SF=/CF.

d.   ADD L, #K   Add immediate K to the LR register. Store the sum in the LR. This operation will affect SF, SF=/CF.

e.   SUBRC A, @LR   Subtract instruction with borrow (the complement of carry). Subtract the contents of the accumulator from the contents of RAM pointed at by the LR register, subtract the complement of the carry bit, then store the results in the accumulator, transfer the carry bit to the CF. This will affect SF and CF, SF=CF.

f.   INC @LR   Increment instruction, it increments the contents of RAM pointed at by the LR register by 1. This will affect SF, SF=/CF.

g.   DEC @LR   Decrement instruction. The contents of RAM pointed at by the LR register decrement by 1. This will affect SF, SF=CF.

h.   INC D   Increment instruction, it increments the contents of the D register by 1. This will affect SF, SF=/CF.

i.   DEC D   Decrement instruction, it decrements the contents of the D register by 1. This will affect SF, SF=/CF.

j.   AND A, @LR   The contents of the accumulator and RAM pointed at by the L register are ANDed

and the results are stored in the accumulator. SF changed, SF=/Z.

k. OR A, @LR   The accumulator content and the contents of RAM pointed at by the L register are ORed and the results are entered in the accumulator. SF changed, SF=/Z.

l. XOR A, @LR   The contents of the accumulator and RAM pointed at by the L register are XORed and the results are stored in the accumulator. SF changed, SF=/Z.

4. Bit operation instructions

Instruction	Operation	CF	SF	Cycle
CLR @LR, b	RAM (LR) b←0	---	1	2
SET @LR, b	RAM (LR) b←1	---	1	2
TEST @LR, b	SF←/RAM (LR) b	---	*	2

a. CLR @LR, b   Clear the B bit of the RAM pointed at by the LR register.
b. SET @ LR, b   Set the B bit of the RAM pointed at by the LR register to be 1.
c. TEST @LR, b   Test the B bit of the RAM pointed at by the LR register. If this bit is1, the SF is set to 0; otherwise, the SF is set to 1.

5. Carry operation instructions

Instruction	Operation	CF	SF	Cycle
CLR CF	CF←0	0	1	2
SET CF	CF←1	1	1	2
TESTP CF	SF←CF	---	*	1

a. CLR CF   Clear the carry flag to logic zero.
b. SET CF   Set the carry flag to logic 1.
c. TESTP CF   Test the carry flag, sent the carry flag to SF.

6. Branch instructions

Instruction	Operation	CF	SF	Cycle
BSS label		---	1	2
LD MBR, #K		---	---	1

Only when SF is 1, the JUMP instruction is executed; otherwise it will execute the next instruction.

Notes:
a. Label   Jump destination address
b. #K   Immediate (0~15)
c. b   Bit addressing (0~3)
d. %P   Port address

7. Subroutine instructions

Instruction	Operation	CF	SF	Cycle
CALLS label		---	---	2
RET		---	---	2

When executing subroutine call and return instructions, the subroutine starting address is limited from 000H to 01FH。

8. Others

Instruction	Operation	CF	SF	Cycle
HOLD		---	1	1
NOP		---	---	1
TMRST	Reset timer counter	---	---	1

|		
a.	HOLD instruction	After executing this instruction, the MCU is in the power-save mode, the clock stops oscillation, and power consumption reduces.
b.	NOP instruction	Null operation. It doesn't affect anything.
c.	TMRST	Timer clear command, it will clear all values of the timer to 0. This instruction is often used to reset the WDT in program.

Note: C: CF, the carry flag is 1 if there is a carry when executing the addition instructions, or if there is no borrow when executing the subtract instructions.

Z: Zero, when the data sent to ACC and RAM is 0, the zero flag is 1.

*: The asterisk symbol means the value of the corresponding flag is directly set by the instruction.

--: This symbol means the instruction won't affect the corresponding flag.
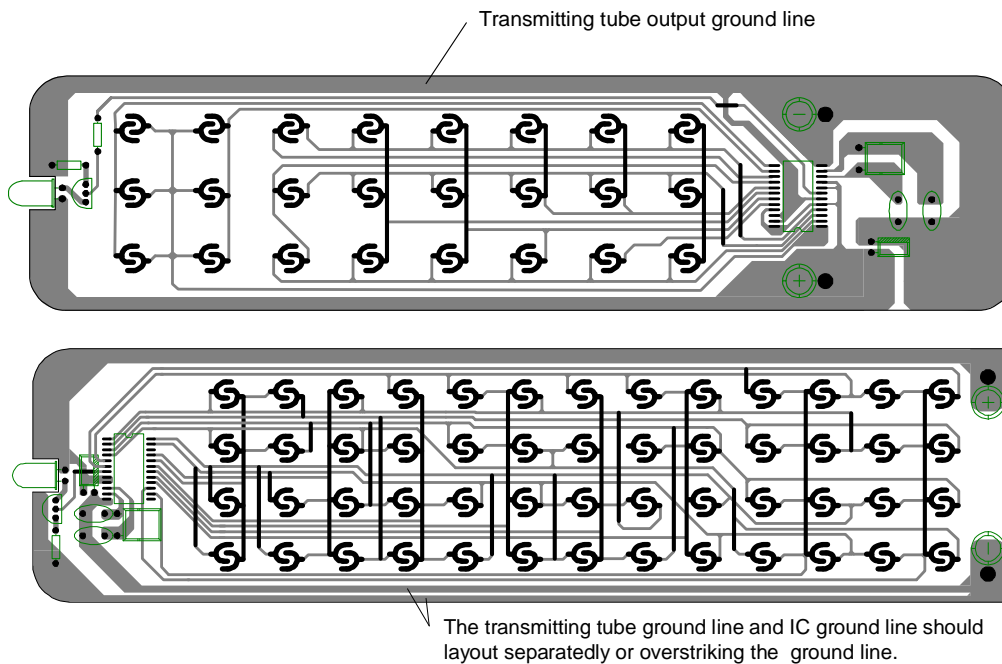
TYPICAL APPLICATION CIRCUIT
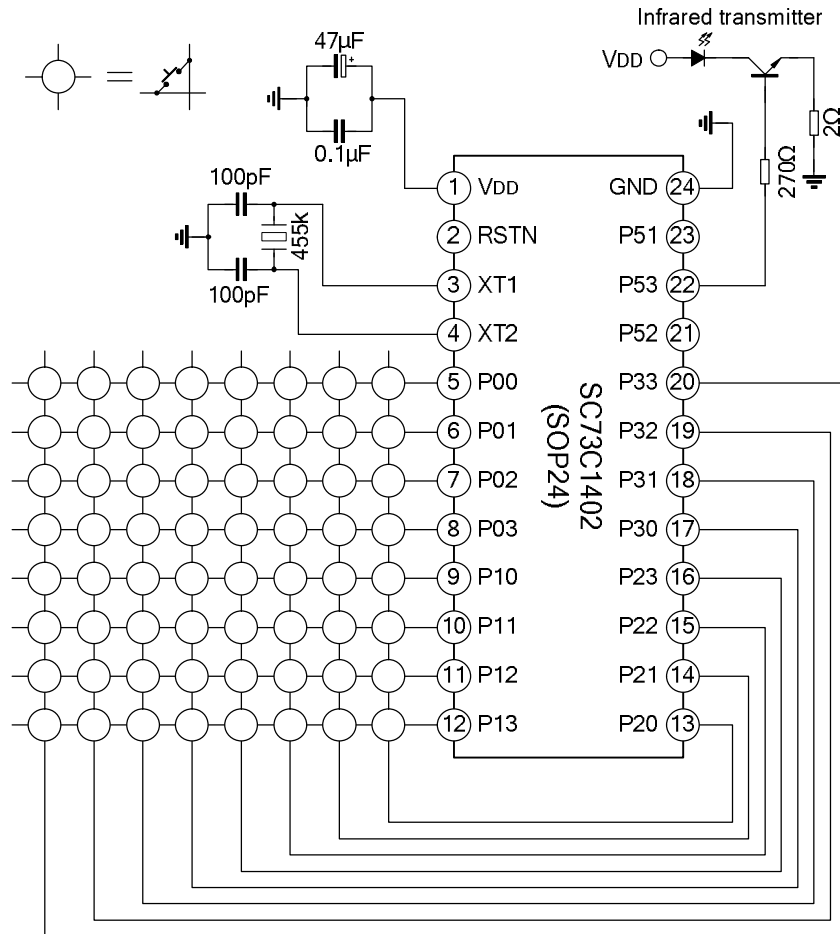
Note: 1. The connections of the two capacitors with VDD should be as close as possible to the application circuits.

2. The connections between the two capacitors and the VDD, the two capacitors and the ground should be as short as possible.

TYPICAL APPLICATION CIRCUIT (CONTINUED)
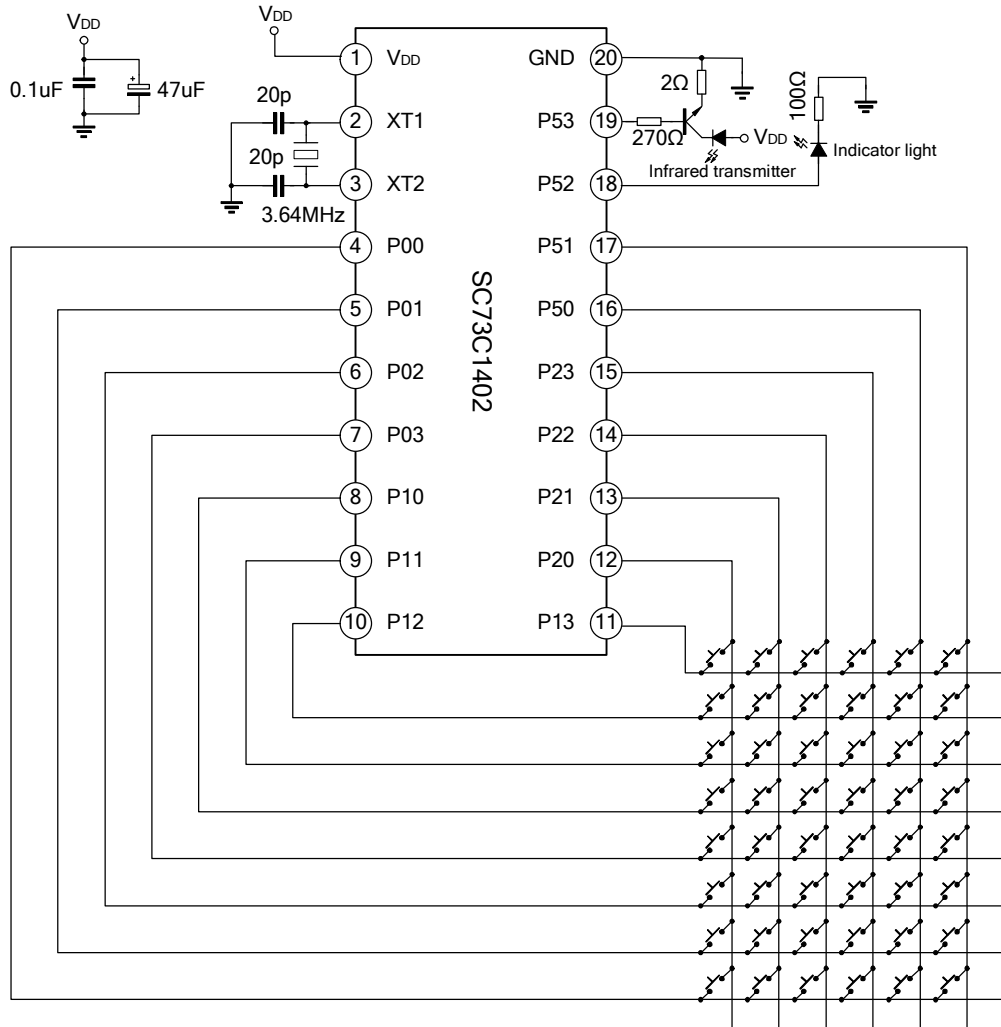
Note: 1. The connections of the two capacitors with VDD should be as close as possible to the application circuits.

2. The connections between the two capacitors and the VDD, the two capacitors and the ground should be as short as possible.

TYPICAL PCB WIRE LAYOUT SCHEMATIC:

Transmitting tube output ground line

The transmitting tube ground line and IC ground line should
layout separatedly or overstriking the ground line.

The above IC is only used to indicate the existence of it, not to specify.

Note:

* In wire layout, the power-filter-capacitor should be placed near to the IC.

* In wire layout, the user should avoid long power line and ground line.

* It is recommended infrared transmission unit and the IC ground line be laid out separately, or widening the
  connection lines.

* The emitter of the triode should connect a 1Ω resistor at least.

* It is recommended to use the 9014 triode.

CHIP TOPOGRAPHY
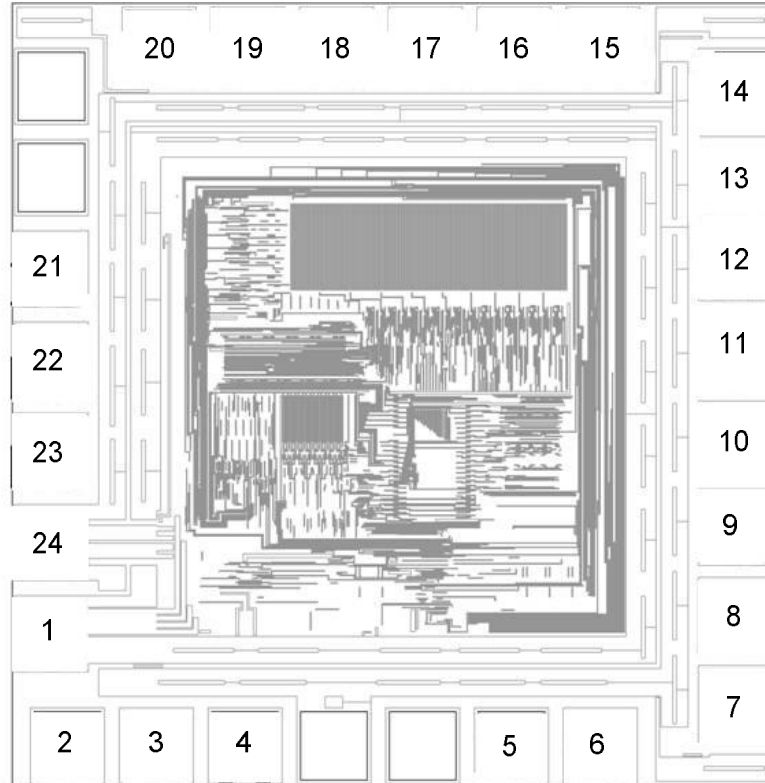
Chip size: 1.15X1.15(mm^2)

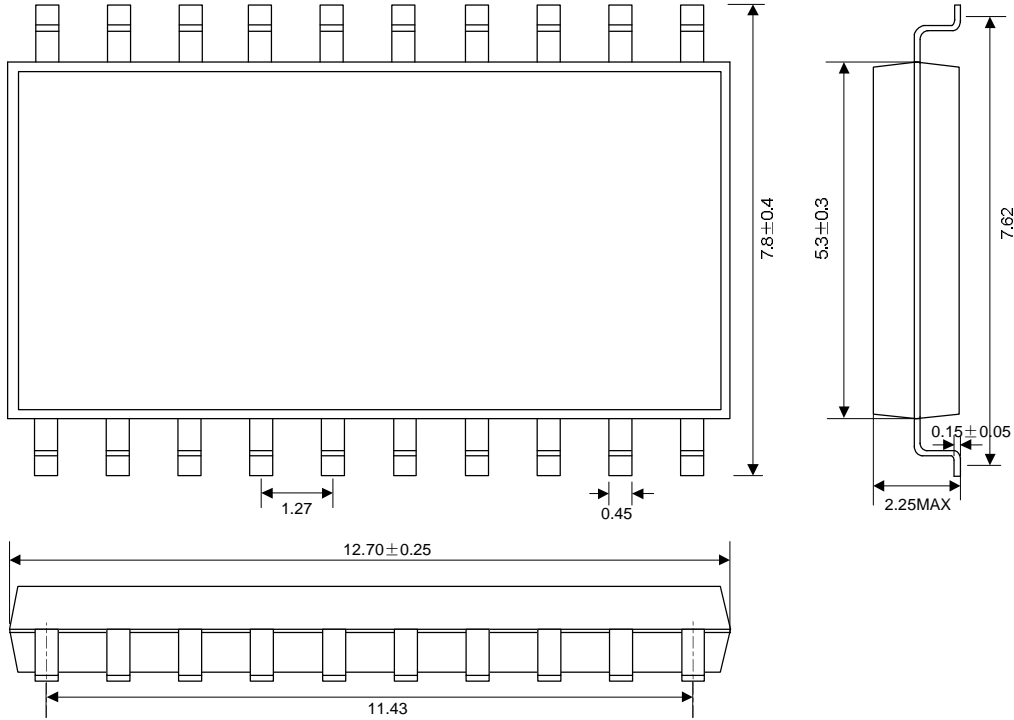Note: The substrate is connected with GND.

PAD COORDINATES

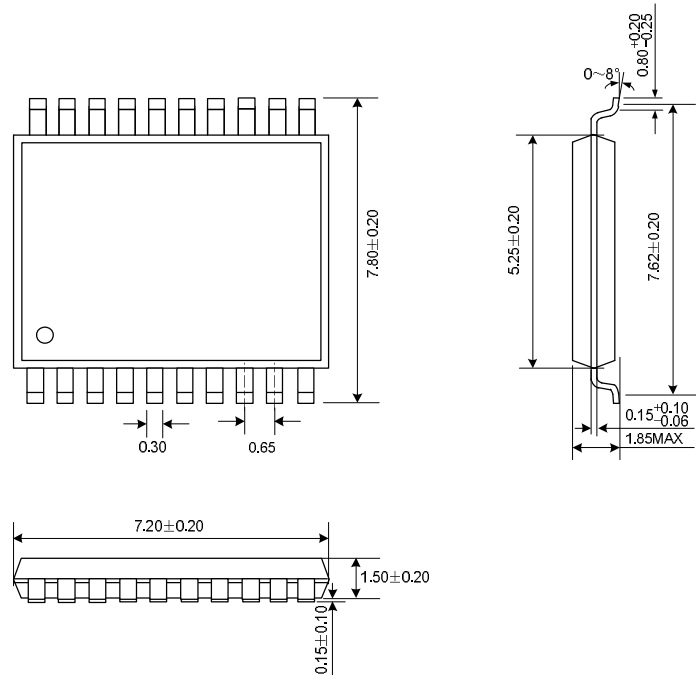| Pad No.	Symbol	X	Y	Pad No.	Symbol	X	Y
1	VDD	-462.00	-314.35	13	P20	462.00	289.65
2	RSTN	-440.40	-462.00	14	P21	462.00	405.65
3	XT1	-320.40	-462.00	15	P22	283.30	460.15
4	XT2	-200.40	-462.00	16	P23	163.30	460.15
5	P00	159.60	-462.00	17	P30	43.30	460.15
6	P01	279.60	-462.00	18	P31	-76.70	460.15
7	P02	462.00	-406.35	19	P32	-196.70	460.15
8	P03	462.00	-290.35	20	P33	-316.70	460.15
9	P10	462.00	-174.35	21	P52	-462.00	165.65
10	P11	462.00	-58.35	22	P53	-462.00	45.65
11	P12	462.00	57.65	23	P51	-462.00	-74.35
12	P13	462.00	173.65	24	GND	-462.00	-194.35

PACKAGE OUTLINE

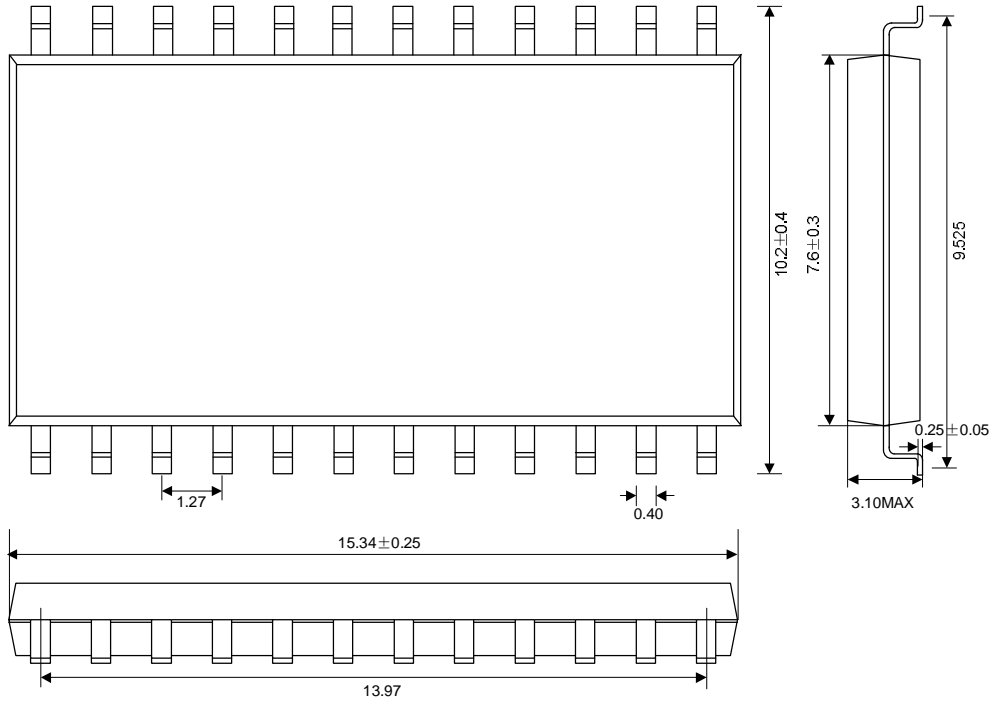**SOP-20-300-1.27**   **Unit: mm**

7.8±0.4
5.3±0.3
7.62
1.27
0.45
0.15±0.05
2.25MAX
12.70±0.25
11.43

SSOP-20-300-0.65   **Unit: mm**

7.80±0.20
0.80 +0.20/-0.25
0~8°
5.25±0.20
7.62±0.20
0.30
0.65
0.15 +0.10/-0.06
1.85MAX
7.20±0.20
1.50±0.20
0.15±0.10

PACKAGE OUTLINE

SOP-24-375-1.27   Unit: mm

10.2±0.4

7.6±0.3

9.525

1.27

0.40

0.25±0.05

3.10MAX

15.34±0.25

13.97

SOP-20-375-1.27   Unit: mm

10.2±0.4

7.6±0.3

9.525

1.27

0.4

0.25±0.05

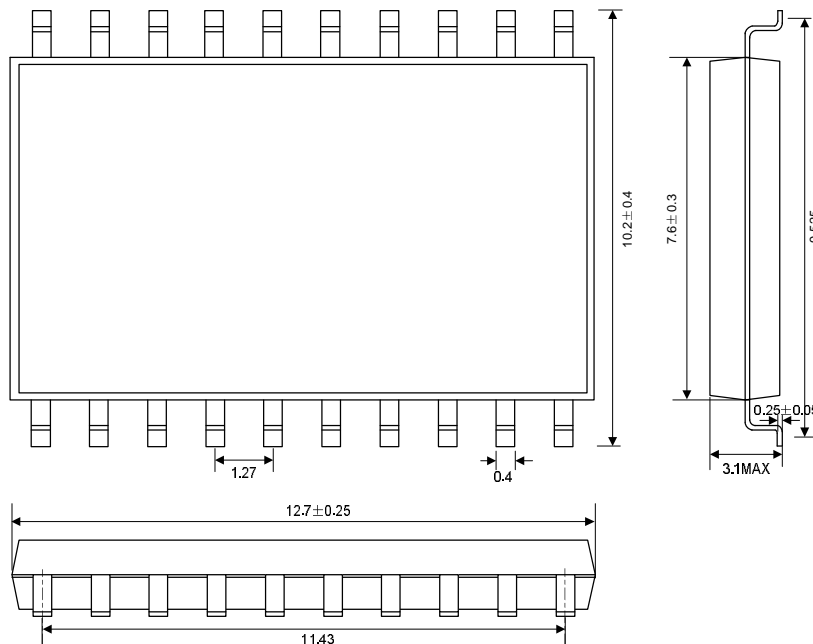3.1MAX

12.7±0.25

11.43

PACKAGE OUTLINE

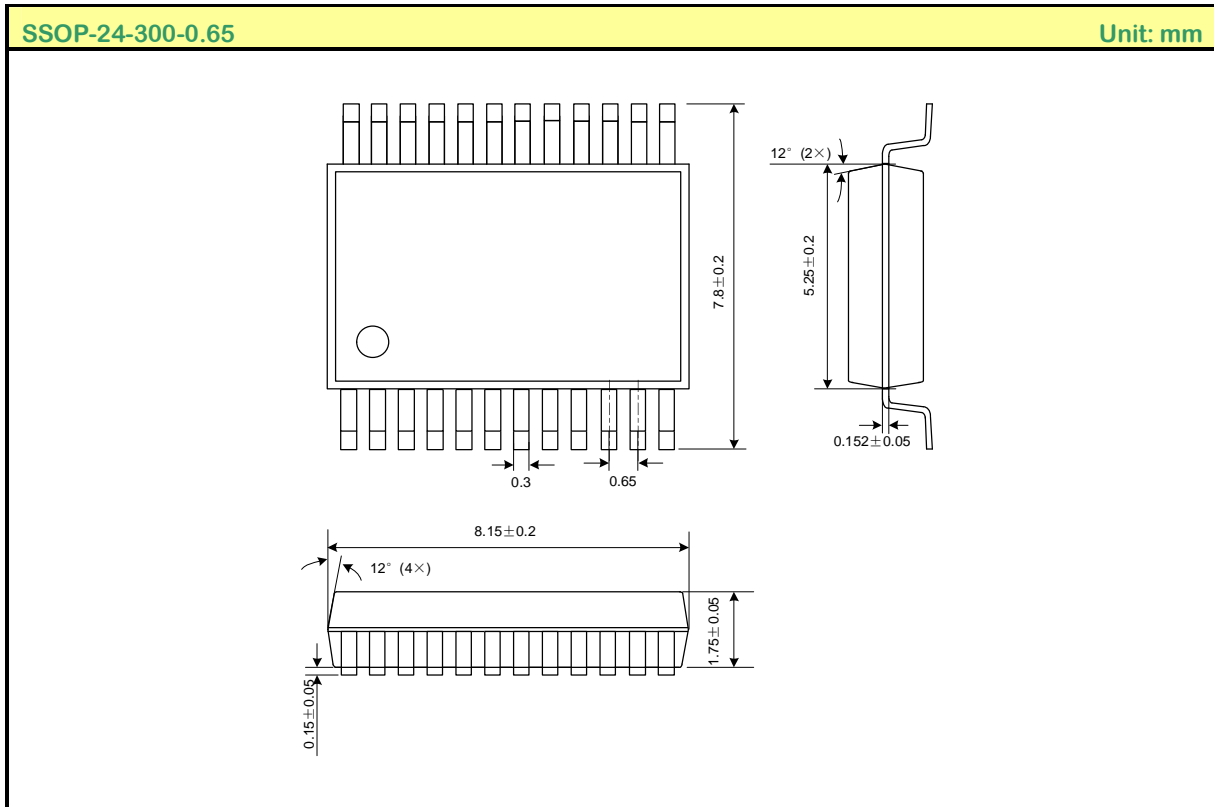SSOP-24-300-0.65   Unit: mm

HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

Note: IC oscillator input mustn't be on the outside layer, thus to avoid the abnormal working when human body touches the remote controller without crust in testing.