DESCRIPTION

The PT9250 is an advanced single chip GPS receiver to integrate baseband, RF and flash memory into the 7mm x 10mm package making for an extremely compact design. This advanced solution offers best-in-class acquisition & tracking sensitivity, TTFF and accuracy. The PT9250 architecture uses an FFT and Matched Filter that delivers performance equivalent to more than 75,000 correlators. This represents a quantum leap forward in GPS performance. The PT9250's architecture enables unmatched TTFF at low signal levels. The PT9250 includes a powerful GPS DSP integrated with a 32-bit RISC microprocessor, 1Mb of SRAM and 4Mb flash memory. The PT9250 also integrates a built-in low power RTC circuit for low power operation and battery backup RAM for satellite information. PTC supports full reference design, demonstration system, software evaluation tools and other supporting documentation.

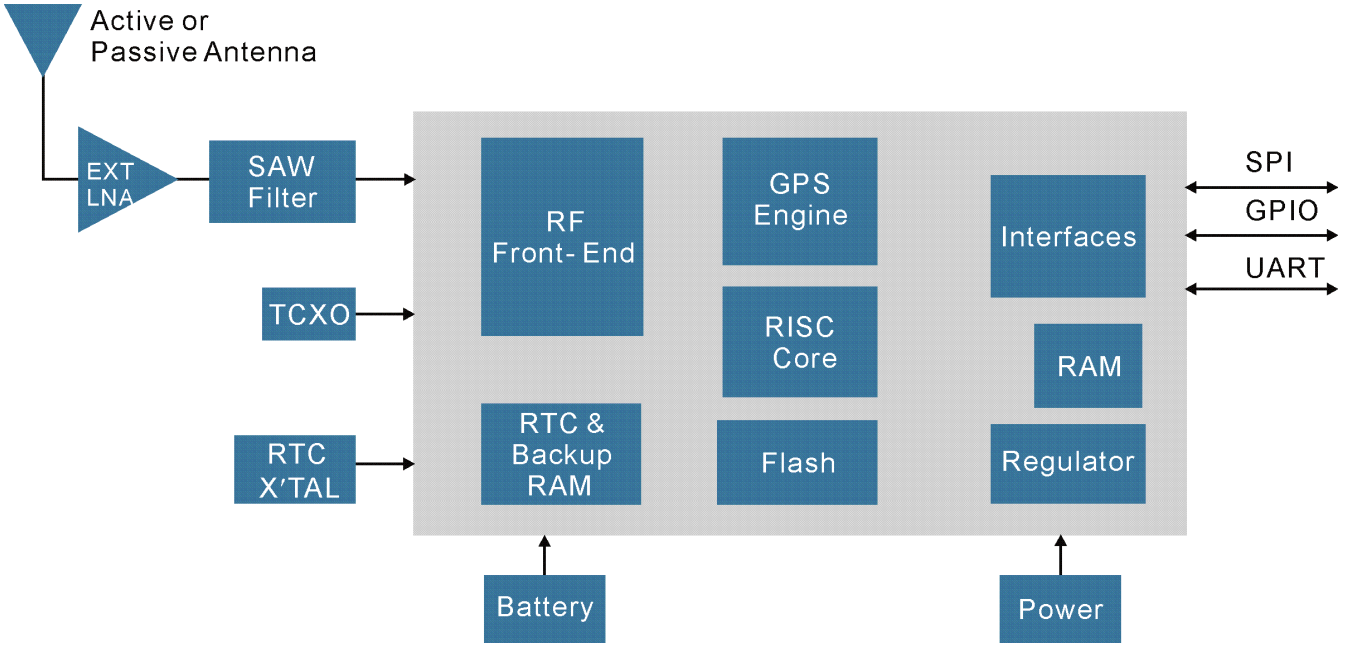
APPLICATIONS

- GPS receivers
- Vehicle navigator
- Cellular phone
- PDA
- PMP

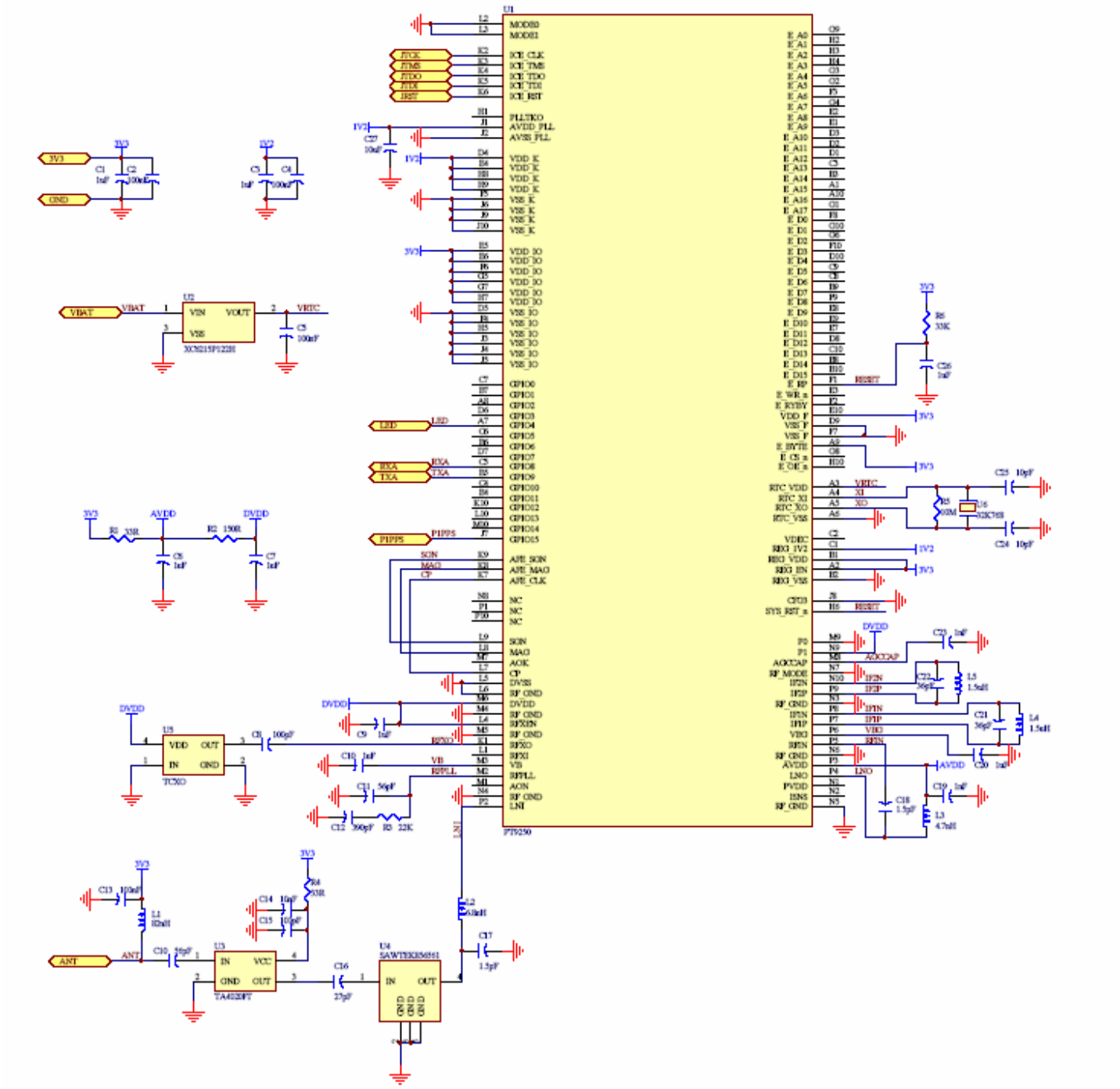
FEATURES

- Reception frequency: 1575.42MHz (L1 band, CA code)
- Reception frequency: 1575.42MHz (L1 band, CA code)
- Reference clock (TCXO) frequency: 16.368MHz or 16.369MHz
- Best-in-class acquisition and tracking sensitivity, TTFF and accuracy.
  - Tracking sensitivity -159dBm
  - Acquisition sensitivity -143dBm
- SoC to integrate major RF receiver, digital baseband and flash memory
- 48 channel acquisition and tracking engine
- 32 bits RISC CPU (MIPS)
- Internal low power real time clock
- Battery back-up SRAM
- 2-channel UART communication port
- SPI host interface
- 2 external interrupts
- Watch dog timer support
- 16 GPIOs
- 1 PPS output
- Support NMEA-0183(V3.01)
- 140 balls LFBGA
- Temperature range: -40℃/+85℃

BLOCK DIAGRAM



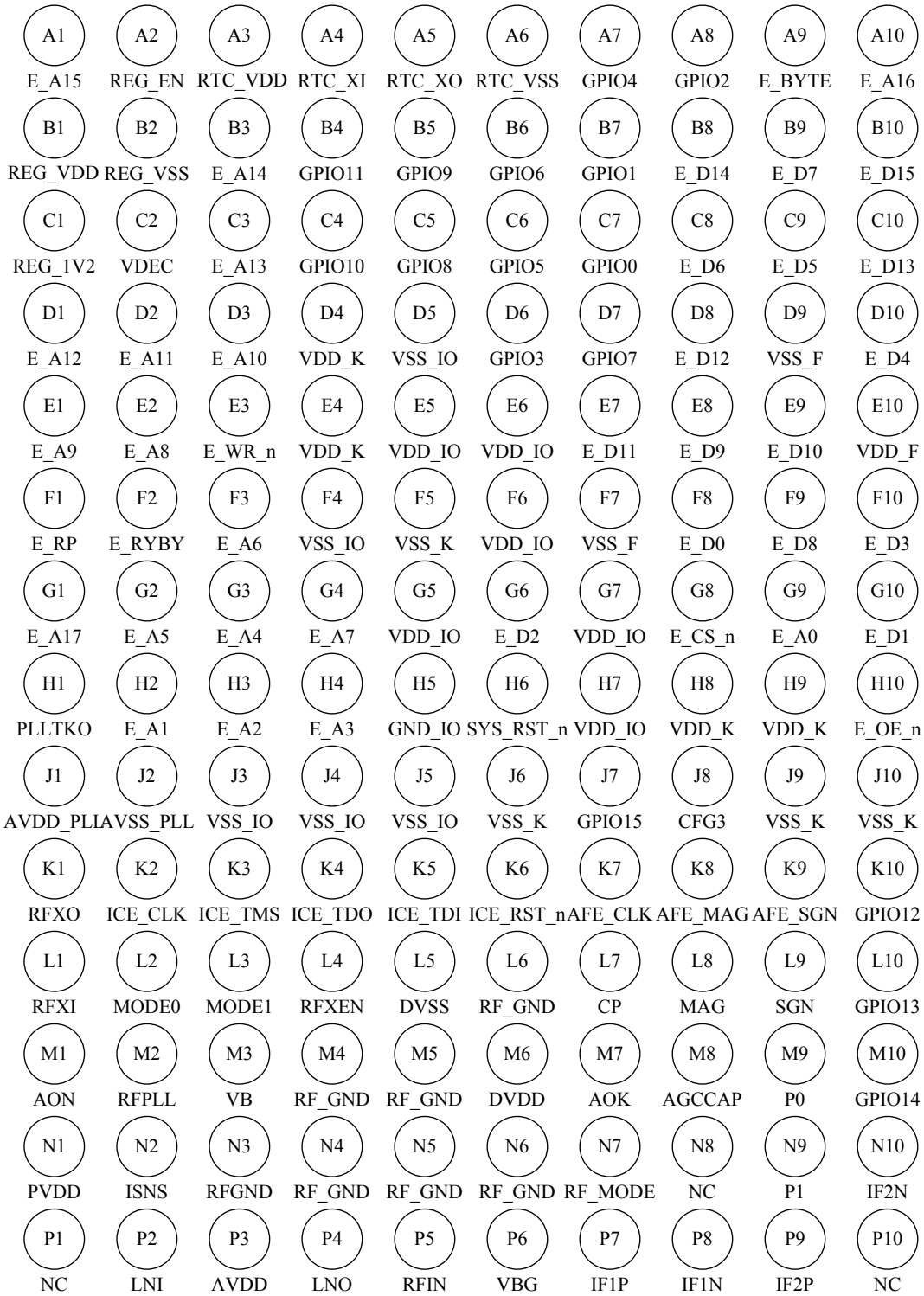
APPLICATION CIRCUITS



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT9250	10mmx7mm LFBGA	PT9250

BALL CONFIGURATION



BALL DESCRIPTION

Ball Name	I/O Type	Description
RF Interface		
SGN	O	Quantized 2nd IF “sign” bit
MAG	O	Quantized 2nd IF “magnitude” bit
AOK	O	Active antenna status output (AOK = HIGH = active antenna OK; AOK=LOW=active antenna either open or shorted)
CP	I/O	Reference clock input/output
RFXEN	I	Crystal oscillator enable pin (XEN=HIGH=enabled; XEN=LOW=disabled)
RFXI	I	Crystal oscillator input
RFXO	O	Crystal oscillator output
VB	O	Regulator (1.9V) output
RFPLL	O	Charge pump output
AON	O	Antenna switch-controlled supply voltage to active antenna
LNI	I	LNA input
ISNS	I	Antenna detector current sense input
PVDD	O	Supply voltage (active antenna)
LNO	O	LNA output
RFIN	I	Mixer input
VBG	O	Band gap reference (1.23V) output
IF1P	O	Differential first-stage IF amplifier output/differential IF AGC input
IF1N	O	
RFMODE	I	Reference frequency mode select input
AGCCAP	I/O	AGC capacitor connection. Sets the AGC time constant.
P1	I	Power-down control pins
P0	I	
RF Power Pins		
DVSS	G	Ground (digital circuitry)
DVDD	P	Supply voltage (digital circuitry)
AVDD	P	Supply voltage (analog circuitry)
RF_GND	G	Ground (analog circuitry)
Flash Interface		
E_D0 ~ E_D15	I/O	External Data bus bit 0 ~ 15
E_A0 ~ E_A17	O	External Address bus bit 0 ~ 17
E_CS_n	O	External memory chip select, active low
E_WR_n	O	External memory write signal, active low
E_OE_n	O	External memory output enable, active low
E_BYTE	I	Byte mode
E_RP	I	Reset of external memory
E_RYBY	O	Ready / Busy output
RF Chip Interface		
AFE_CLK	I	RF chip clock input
AFE_SGN	I	RF chip sign data bit
AFE_MAG	I	RF chip magnitude data bit
CPU Peripheral		
GPIO15(OPPS)	I/O	GPIO15 / One pulse per-second
GPIO14	I/O	GPIO14
GPIO13	I/O	GPIO13
GPIO12	I/O	GPIO12
GPIO11 (UATX1)	I/O	GPIO11 / UART 1 transmission data
GPIO10 (UARX1)	I/O	GPIO10 / UART 1 receive data
GPIO9 (UATX0)	I/O	GPIO9 / UART 0 transmission data
GPIO8 (UARX0)	I/O	GPIO8 / UART 0 receive data

Ball Name	I/O Type	Description
GPIO7(EXT_INT1)	I/O	GPIO7 / External interrupt input
GPIO6(EXT_INT0)	I/O	GPIO6 / External interrupt input
GPIO5	I/O	GPIO5
GPIO4	I/O	GPIO4
GPIO3 (CSIO_RDY)	I/O	GPIO3 / CSIO ready
GPIO2 (CSIO_CLK)	I/O	GPIO2 / CSIO clock
GPIO1 (CSIO_DO)	I/O	GPIO1 / CSIO data output
GPIO0 (CSIO_DI)	I/O	GPIO0 / CSIO data input
ICE Interface		
ICE_CLK	I	ICE clock
ICE_TMS	I	ICE mode select
ICE_RST_n	I	ICE reset, active low.
ICE_TDI	I	ICE data input
ICE_TDO	O	ICE data output
System Interface		
SYS_RST_n	I	System reset, active low
MODE0, MODE1	I	Test mode selection, pull low
CFG0,CFG1,CFG3	I	Configuration, pull low.
RTC_XO	O	RTC crystal clock output
RTC_XI	I	RTC crystal clock input
PLLTKO	O	PLL test clock output
Regulator		
REG_EN	I	Regulator enable
REG_1V2	O	Regulator 1.2V output
VDEC	I	Voltage detect
Baseband Power Pins		
VDD_REG	P	3.3V power supply for regulator
VSS_REG	G	Ground for regulator
AVDD_PLL	P	Analog 1.2V power supply for PLL circuit
AVSS_PLL	G	Analog Ground for PLL
VDD_RTC	P	1.2V power supply for RTC
VSS_RTC	G	Ground for RTC
VDD_IO	P	3.3V power supply for IO
VSS_IO	G	Ground for IO
VDD_K	P	1.2V power for internal logic core
VSS_K	G	Ground for internal logic
VDD_F	P	3.3V power supply for flash
VSS_F	G	Ground for flash
NC		Open
IO Types		
I	Input(3.3V CMOS level)	
O	Output (3.3V CMOS level)	
IO	Bi-direction IO(3.3V CMOS level)	
P	Power	
G	Ground	

IMPORTANT NOTICE

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