# DESCRIPTION

PT6324 is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/8 to 1/16 duty factor housed in 52-pin plastic QFP/LQFP. 24 segment output lines, 16 grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6324 via a three-line serial interface.

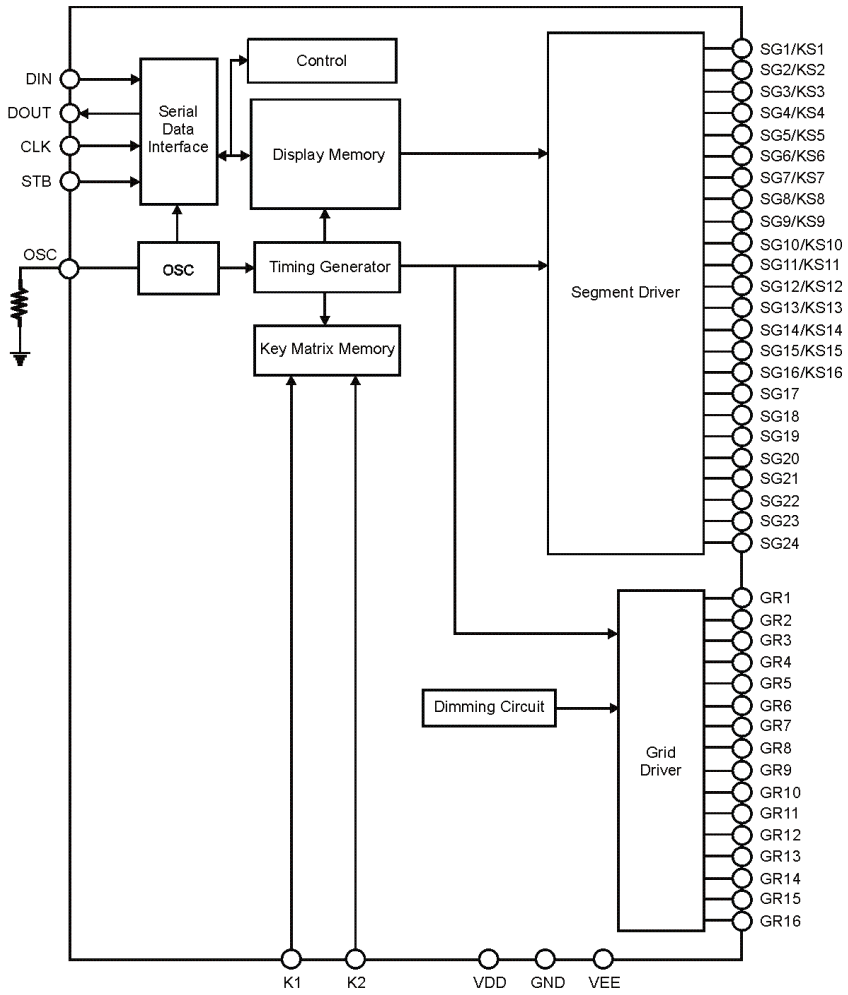
# APPLICATIONS

- Microcomputer peripheral devices
- Digital Audio/Video system: CD/MD/VCD/DVD players
- Car audio
- VCR
- Electric scale meter
- P.O.S.
- Electronic equipment with instructional display

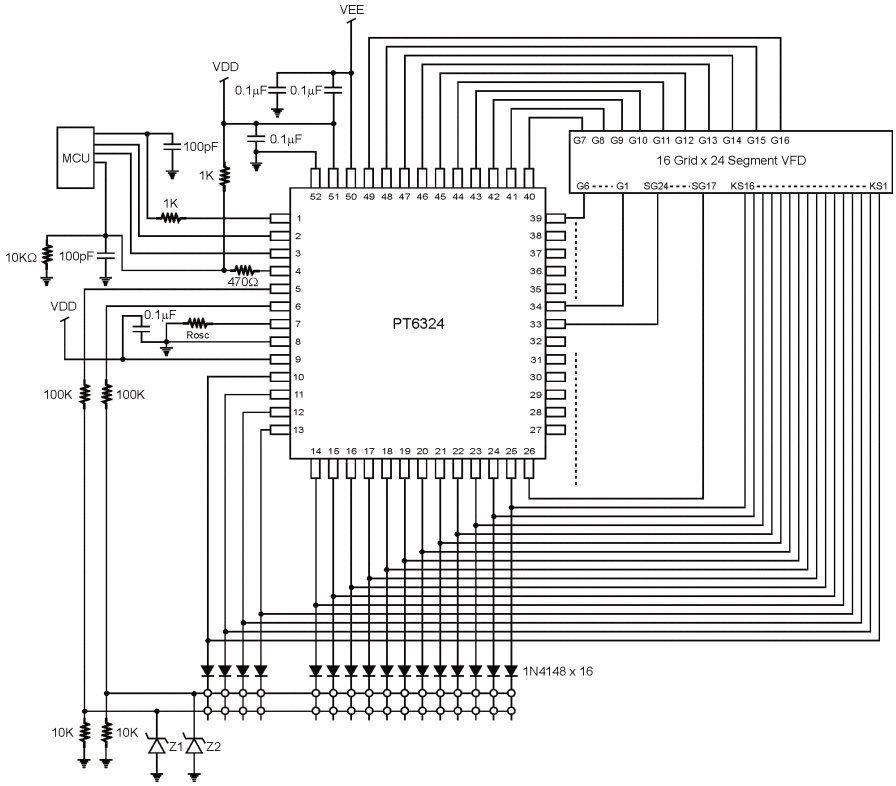
# FEATURES

- CMOS technology
- Low power consumption
- Wide operating voltage VDD=2.7V~5.5V
- Key scanning (16 x 2 matrix)
- Display modes: (24 segments, 8 digits to 24 segments, 16 digits)
- 8-Step dimming circuitry
- Serial interface for Clock, Data Input, Data Output, Strobe pins
- No external resistors needed for driver outputs

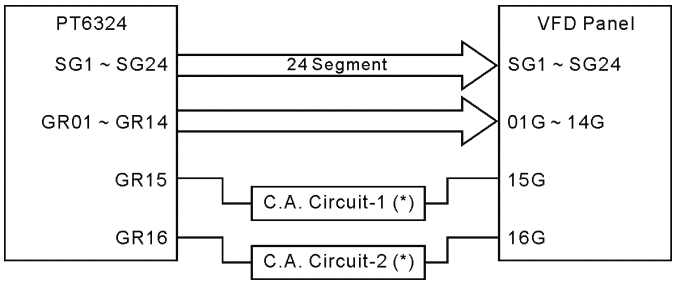
# BLOCK DIAGRAM



# 16-GRID X 24-SEGMENT VFD APPLICATION CIRCUIT

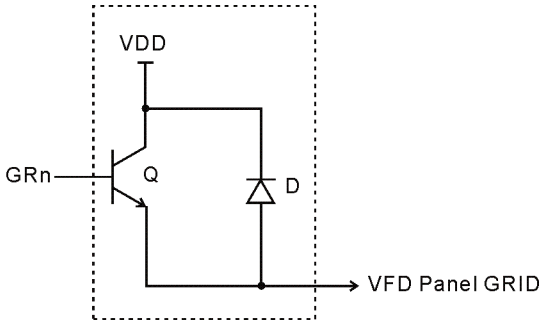



Notes:
1. The value of Rosc is depend on PT6324 IC chip supply voltage of $V_{DD}$ (Rosc=82KΩ, when $V_{DD}$=5V; Rosc=100KΩ, when $V_{DD}$=3.3V).
2. Z1, Z2=Zener diode 5.1V
3. Please adding the current amplifying circuit as following figure when $I_{OHGR}$>15mA on VFD panel for high brightness issue.




*=C.A. Circuit=Current amplifying circuit

C.A. Circuit-1 & C.A. Circuit-2 Ex.:



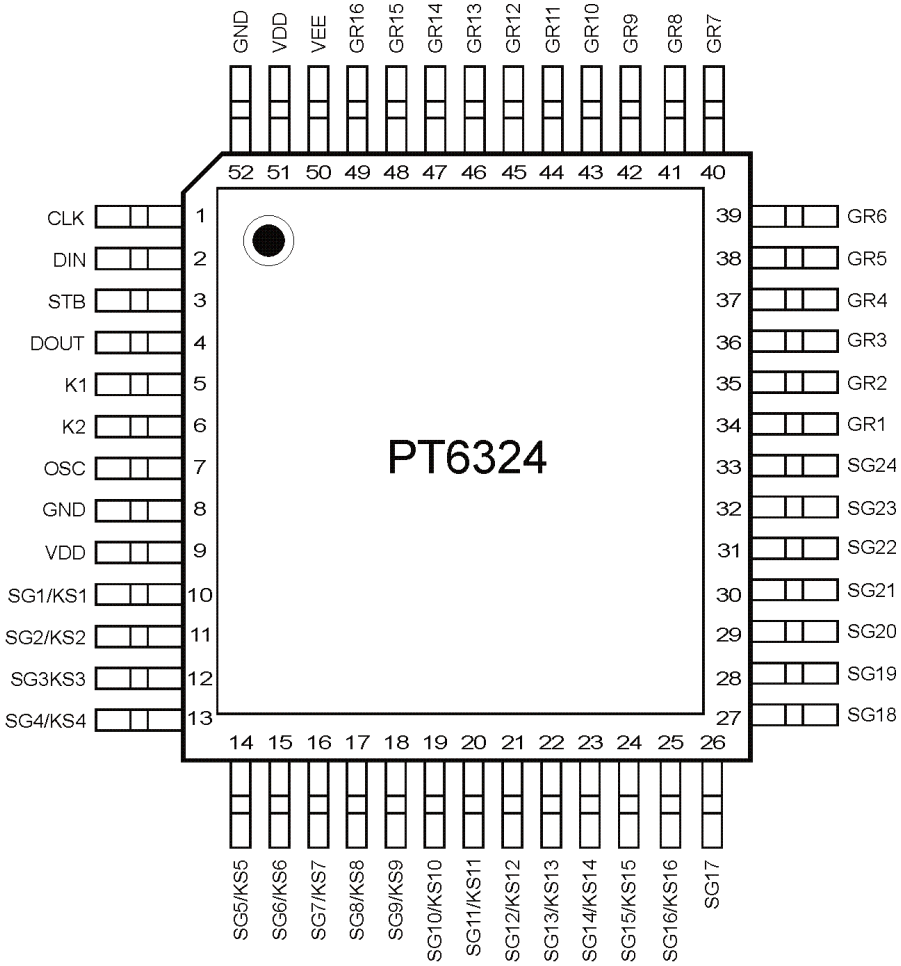

Parts recommended:

- Q=SAMSUNG-KSR1105 (General fast switching transistor)
- D=HITACHI-HSM221C (General fast recovery diode)

# ORDER INFORMATION

| Valid Part Number | Package Type | Top Code |
|---|---|---|
| PT6324-Q | 52-Pin, QFP | PT6324-Q |
| PT6324-LQ | 52-Pin, LQFP | PT6324-LQ |

# PIN CONFIGURATION



# PIN DESCRIPTION

| Pin Name | I/O | Description | Pin No. |
|---|---|---|---|
| CLK | I | Clock input pin<br>This pin reads serial data at the rising edge and outputs data at the falling edge. | 1 |
| DIN | I | Data input pin<br>When this pin acts as input pin, serial data is inputted at the rising edge of the shift clock (starting from the lower bit) | 2 |
| STB | I | Serial interface strobe pin<br>The data input after the STB has fallen is processed as a command. When this in is “HIGH”, CLK is ignored. | 3 |
| DOUT | O | Data output pin (N-channel, Open-drain)<br>When this pin acts as output pin, serial data is outputted at the falling edge of the shift clock (starting from the lower bit) | 4 |
| K1 to K2 | I | Key data input pins<br>The data inputted to these pins is latched at the end of the display cycle. | 5, 6 |
| OSC | I | Oscillator input pin<br>A resistor is connected to this pin to determine the oscillation frequency. | 7 |
| GND | - | Ground pin | 8, 52 |
| VDD | - | Logic power supply | 9, 51 |
| SG1/KS1 to SG16/KS16 | O | High-voltage segment output pins<br>Also acts as the key source | 10 to 25 |
| SG17 to SG24 | O | High-voltage segment output pins | 26 to 33 |
| GR1 to GR16 | O | High-voltage grid output pins | 34 to 49 |
| VEE | - | Pull-down level | 50 |