MX844

12 BIT, MULTI-CHANNEL POWER & TEMP SENSOR FOR MONITOR & CONTROL SYSTEMS

Features:

- Wide Input Supply Range: 4.5V to 40V
- Programmable gain differential amplifier (±10mV, ±25mV, ±50mV, ±250mV ranges)
- 4 channel differential input multiplexer (3 input channels plus ground)
- Integrated 12-bit ADC
- Serial data output (SDO) with data ready pin
- Fine calibration of Full Scale Range (FSR) using VTRIM pin
- Bi-directional Current Sense
- Internal temperature sensor with 0.2°C resolution
- Compatible with 3.3V and 5V Microcontrollers
- Operating Temperature Range: -40°C to 85°C
- 5mm x 5mm, QFN-28 RoHS Package

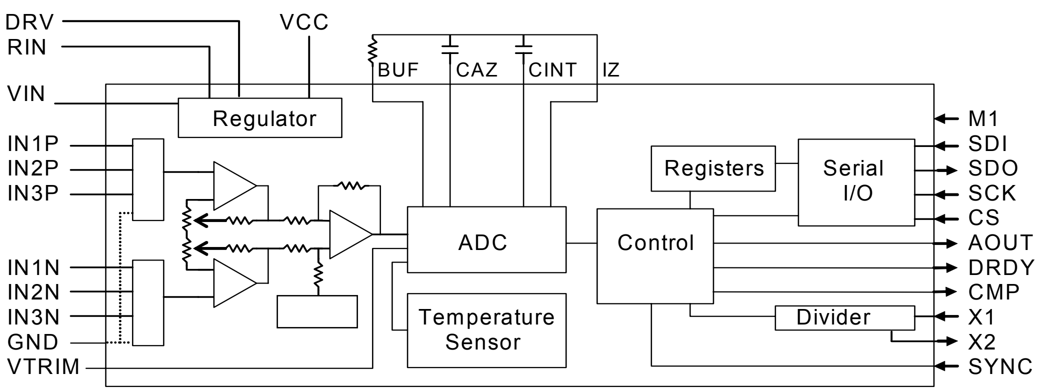
Ordering Information

Part No.	Description	Qty
MX844R	QFN-28 Tube	73
MX844RTR	QFN-28 Tape & Reel	2500

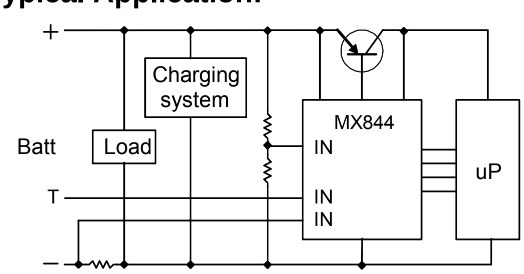
Description:

The MX844 is a fully integrated subsystem that measures temperature plus differential current and voltage. An internal temperature sensor measures ambient temperature with 2.5°C accuracy. Current and voltage measurements are made differentially through a four input multiplexer connected to a programmable gain fully differential sense amplifier. The differential sense amplifier is optimized to measure very small positive or negative voltages near ground for low side bi-directional sensing. A dual slope ADC converts the temperature sensor or sense amplifier outputs to a 12-bit digital word that includes 3 ½ digits plus sign. The input multiplexer channel and programmable gain amplifier range may be changed between ADC conversions. An on-chip voltage regulator enables the MX844 to operate over a wide input voltage range of 4.5 to 40 volts.

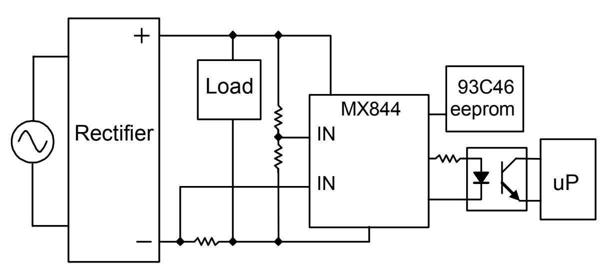
Controller interrupt or over-voltage/over-current signals may be generated by a pair of 12-bit digital comparators configured as a window comparator or simple threshold detection function. The serial port supports standard 4-wire synchronous serial data, or asynchronous serial "talk-only" data, and is compatible with most 3.3V and 5V microcontrollers.



Typical Application:



Battery charge/discharge current, voltage, temperature



Isolated voltage, current, and temperature sensing

Absolute Maximum Ratings (Voltages with respect to GND=0V)

Parameter	Symbol	Min	Max	Unit
VIN, RIN, DRV			45	V
All Other Pins			6	V
Storage Temperature	T_{STG}	-55	150	C°
Operating Ambient Temp	T_A	-40	85	C°
Operating Junction Temp	T_J		100	C°
Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	110 Typical		C°/W

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

ESD Warning

ESD (electrostatic discharge) sensitive device. Although the MX844 features proprietary ESD protection circuitry, permanent damage may be sustained if subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DC Electrical Characteristics

XTAL = 8MHz, T=25C, Cint = Caz = 10nF, Rint = 68K, T_A = +25°C

Parameter	Condition	Min	Typ	Max	Unit
VCC line regulation	VIN = 6 to 45V, no external load	4.8		5.3	V
VCC load regulation	VIN = 6V, 15 mA external load	4.7			V
VIN supply current	VIN = 6V		3.2	4.5	mA
Input bias current	selected input channel	10	20	40	nA
Input bias current offset		-4		4	nA
Input offset voltage	differential, input=0, +/-10mV scale	-0.4		0.4	mV
input common mode	all input channels	-300		300	mV
ADC gain error	+/-250mV range, at 90% input	-0.5		0.5	%
	+/-50mV range	-1.25		0.25	%
	+/-25mV range	-1.5		0.25	%
	+/-10mV range	-1		0.25	%
ADC linearity	at half full scale	-3	+/-0.5	3	lsb
ADC noise			1.5		rms lsb
Temperature error		-2.5		2.5	°C
Temperature slope			0.2		°C/lsb
Temperature offset	Zero °C		3310		lsb
Power on reset duration			100		uS
Digital output low	I = 20mA			0.5	V
Digital output high	I = 6mA	VCC-0.5			V
Digital input low		GND		0.5	V
Digital input high		2		VCC	V
Digital input current				±1	uA
Clock frequency	terminal X1	0.1		20	MHz
Clock input low	terminal X1	GND		0.4	V
Clock input high	terminal X1	2		VCC	V
Clock input current	terminal X1			50	uA

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	GND	Ground
2	VTRIM	Optional Full Scale Trim Input
3	BUF	Integrating Resistor Output
4	IZ	Integrator Zero Output
5	CAZ	Auto Zero Capacitor Input
6	CINT	Integrator Capacitor Input
7	IN1P	Input Channel 1 Positive
8	IN1N	Input Channel 1 Negative
9	IN2P	Input Channel 2 Positive
10	IN2N	Input Channel 2 Negative
11	IN3P	Input Channel 3 Positive
12	IN3N	Input Channel 3 Negative
13	M1	Divisor Mode Input
14	SYNC	A/D Converter Reset Input
15	DRDY	A/D Converter Data Ready Output (Active Low)
16	SCK	Serial Clock Input
17	SDO	Serial Data Output
18	SDI	Serial Data Input
19	CS	Serial Chip Select (Active Low)
20	X1	Xtal 1 Input
21	X2	Xtal 2 Output
22	AOUT	Asynchronous Data Output
23	CMP	Comparator Output
24	VCC2	Must Be Connected to Vcc
25	VCC	Regulator Output / Logic Supply Input
26	VIN	Regulator Voltage Input
27	RIN	Regulator Internal MOSFET Gate
28	DRV	Regulator External PNP Base Drive

APPLICATION OPERATING MODE

At the end of the power-on reset period, pin CS is sensed to determine the operating mode. Placing an external resistor to VCC on pin CS will cause the MX844 to enter the slave mode. In this mode the synchronous serial I/O port can be connected to a companion microcontroller for full control of the MX844 from the microcontroller.

If a resistor to GND is connected to CS, then the MX844 enters the master mode at power-up and fetches commands from a 93C46 serial EEPROM operating in the 64 by 16 mode. In this mode, the MX844 operates as the master and sends clock, data, and select to the EEPROM and reads back the EEPROM data. This mode is useful when the MX844 operates as a stand-alone data acquisition system with a fixed pattern of measurement scanning. To facilitate electrically isolated measurements the data can be sent to a computer's serial port using only one wire connected through a single opto-isolator.

If, neither an EEPROM or microcontroller are connected to the MX844, and CS is connected to VCC, operation defaults to that of all zeroes in the control register (ADC clock = input clock / 8, input channel IN1, +/- 50mV range). The asynchronous data output has a valid stream of measurement information.

FUNCTIONAL DESCRIPTION

Voltage Regulator

There are three methods of powering the MX844.

1) An external 4.5 to 5.5V supply is connected to VCC, VCC2, and VIN. Pins DRV and RIN are no-connect or connected together.

2) VIN is connected to a 6 to 40V supply. DRV is connected to RIN, thus utilizing the internal pass element.

3) VIN is connected to a 6 to 40V supply. An external PNP transistor such as the MMBTA56 or BCX53 is used for the pass element. The PNP transistor's emitter, base, and collector are connected to pins VIN, DRV, VCC respectively. RIN must be connected to VIN.

Power-On Reset

The MX844 contains a power-on reset circuit that resets all the internal flip-flops and initializes the internal registers to zero. The reset circuit will also generate a reset condition if the voltage at pin VCC drops to approximately 3.8V.

Oscillator

The oscillator configuration consists of a crystal/resonator connected between pins X1 and X2 and a capacitor to GND on both pins. The capacitor value depends on the crystal/resonator but is usually between 15 and 27pF. Alternatively, an external clock may be input to pin X1, with X2 floating. Nominal DC self-bias at pin X1 is 800mV. In either case the clock is internally AC coupled, therefore clock rates below 100KHz are not recommended.

Temperature Sensor

The internal temperature sensor is selected for measurement by setting the control register bits for a full scale of +/-250mV and setting the unipolar bit. The temperature value read from the ADC consists of an offset value plus the slope. To convert to a standard temperature scale it is necessary to subtract the constant offset and then multiply by a constant that matches the standard scale desired.

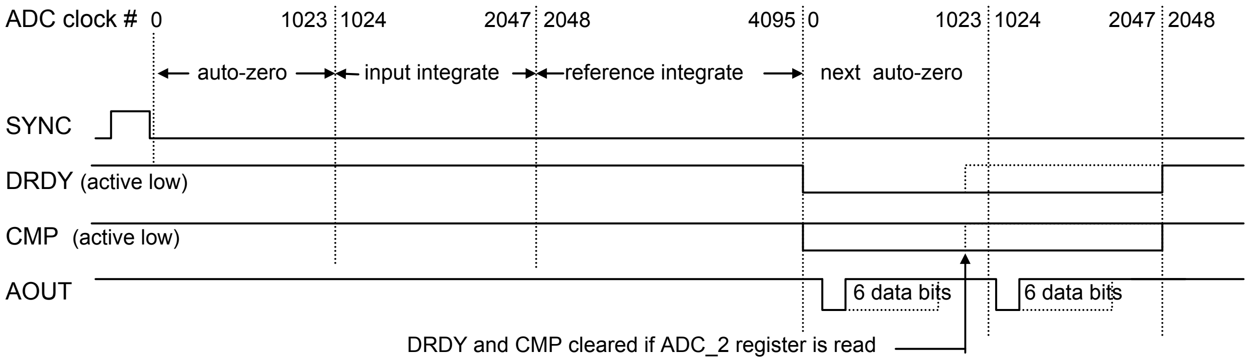
Self-heating of the internal temperature sensor will occur due to the device power dissipation. The maximum heating will occur when the internal pass element is used in conjunction with a high supply voltage.

Analog/Digital Converter

Selection of the input channel and the full scale range is accomplished by writing 5 bits in the control register. An additional 3 bits in the control register in combination with the M1 pin setup the internal clock dividers. The ADC is a bipolar-input dual slope type with clock period tAD equal to a multiple of the clock period at pin X1 (tClock). The ADC conversion time consists of 1024 * tAD of auto-zero, 1024 * tAD of input integration, and 2048 * tAD of reference integration. The result of the analog to digital conversion can be read using the serial I/O port and is also transmitted on pin AOUT in an asynchronous serial format. The DRDY pin transitions low at the end of the reference integration period to indicate that data is stable and may be read through the synchronous serial I/O. The data becomes not valid when DRDY returns high. The status of DRDY is also available in bit 7 of the ADC_1 register.

The SYNC pin is connected to GND to enable free-running ADC conversions. Alternatively, if SYNC transitions high, the ADC is immediately driven to the start of the auto-zero time. When SYNC is returned to a logic low, the next rising edge at pin X2 will start the ADC timing.

The input channel and full scale range may be changed in between ADC conversions, however it is recommended that such commands be written into the MX844 as soon as possible after pin DRDY transitions low. This allows the maximum settling time prior to the next ADC conversion.



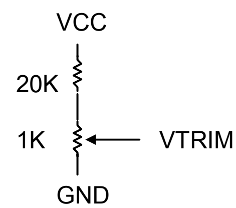
CMP is the digital compare output that is described later. AOUT is the asynchronous serial output of the ADC.

The ADC output code is offset-binary. An example of the coding is shown here for the +/-50mV range and the corresponding unipolar range of 0 to 100mV:

Bipolar input	Unipolar input	Binary Output (D11:D0)	Hexadecimal
50mV	100mV	111111111111	FFF
0 + 1/2 LSB	50mV + 1/2 LSB	100000000000	800
0 - 1/2 LSB	50mV - 1/2 LSB	011111111111	7FF
-50mV	0	000000000000	000

Two external components, Rin and Cint, should be chosen such that the value of Cint in pF is 4 to 7 * tAD and the time constant of Rint * Cint is 300 to 450 * tAD. The value of Rint should be between 47K and 220K ohm. For example, for t(AD) = 1.6 uS, a set of suitable values would be 56K ohm and 10nF (RC = 560uS, ratio = 350). The value of the auto-zero capacitor Caz is typically equal to Cint.

VTRIM is either a no-connect pin or can be used to fine trim the ADC full scale by +/- 1%. The following circuit is recommended if fine trimming is desired:



Digital Comparator

Two 12-bit registers form a window comparator of the ADC output data. The value of comparator1 must always be set to a value greater than comparator2. There are three cases to consider, depending on whether the comparator values are above or below 800h:

1) If the value of comparator1 is greater than 800h and the value of comparator2 is less than 800h, then CMP pulses when the ADC value is greater than or equal to comparator1, or less than or equal to comparator2.

2) If the value of comparator1 is greater than 800h and the value of comparator2 is greater than 800h, then CMP pulses when the ADC value is greater than or equal to comparator1, or less than comparator2.

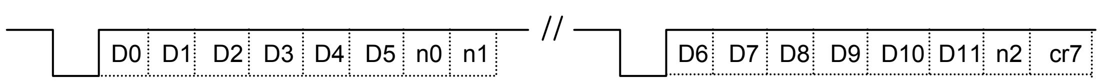
3) If the value of comparator1 is less than 800h and the value of comparator2 is less than 800h, then CMP pulses when the ADC value is greater than comparator1, or less than or equal to comparator2.

In all cases, CMP will go logic low at the same time as DRDY transitions low and CMP will return high when the ADC_2 register is read or after 2048 *tAD (see the ADC timing diagram). The status of CMP is also available in bit 6 of the ADC_1 register.

In a typical application CMP would cause a controller interrupt, at which time the controller reads the actual ADC output that caused the interrupt (which clears the DRDY and CMP status bits) and takes appropriate action. Another application would be to connect CMP to over-current or over-voltage shutdown circuitry.

ASYNCHRONOUS OUTPUT

The ADC result is transmitted on pin AOUT in 8-bit, no parity asynchronous NRZ serial format. Two characters of 8 bits each are transmitted for each ADC conversion, with a start bit just prior to the data (see the figure below).



D[11:0] is the 12-bit result of the ADC conversion. Bit cr7 is the value of the control register bit 7. Bits n2, n1, n0 are automatically inserted which indicate the address of the serial EEPROM. These bits can be used by the receiver to identify which channel and range are being transmitted. The EEPROM address is reset to zero by the SYNC pin pulse. The "ANALOG/DIGITAL CONVERTER" section of this document shows the timing of the asynchronous output bytes relative to the conversion cycle.

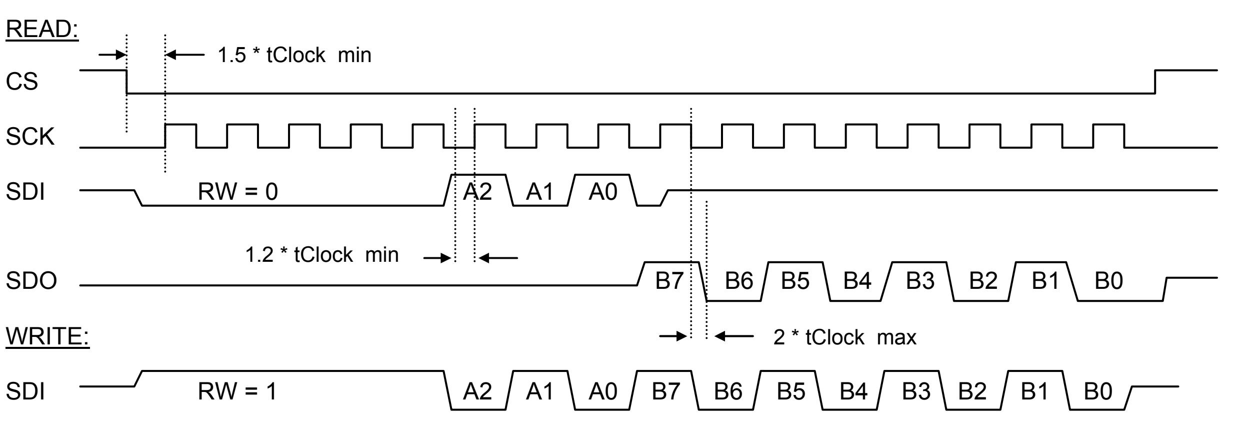
Example internal divider settings and clock frequencies for standard baud rates:

CR7:5	M1	Baud divider	ADC divider	Clock (MHz)	baud rate	ADC conv/s	Clock (MHz)	baud rate	ADC conv/s
000	1	8*52	8	12.0	28.8K	366	16.0	38.4K	488
001	1	4*52	4	6.0	28.8K	366	8.0	38.4K	488
010	1	12*64	12	11.059	14.4K	225	14.746	19.2K	300
011	1	13*64	13	12.0	14.4K	225	16.0	19.2K	300
000	0	8*64	8	14.746	28.8K	450	9.83	19.2K	300
001	0	4*64	4	14.746	57.6K	900	9.83	38.4K	600
010	0	6*64	6	11.059	28.8K	450	14.746	38.4K	600
011	0	3*64	3	11.059	57.6K	900	7.37	38.4K	600
100	1	8*128	8*4*5	9.83	9600	15			
101	1	9*128	9*4*5	11.059	9600	15			
110	1	12*128	12*4*5 14.746	9600	15				
111	1	13*128	13*4*5 16.0	9600	15				
100	0	8*128	8*4*6	9.83	9600	12.5			
101	0	9*128	9*4*6	11.059	9600	12.5			
110	0	12*128	12*4*6 14.746	9600	12.5				
111	0	13*128	13*4*6 16.0	9600	12.5				

SYNCHRONOUS SERIAL I/O

The MX844 (slave) can communicate with a microcomputer (master) via a three wire plus chip select serial interface. The control register, the two digital comparator values, and the ADC result are accessed by specifying a 3-bit address A[2:0]. Chip select CS, serial clock SCK, and serial data input SDI are output from the master controller to the MX844. Serial data output SDO is driven by the MX844 when selected by CS = 0. SDO is high impedance when CS = 1. SCK and SDI are don't care when CS = 1.

SERIAL INTERFACE TIMING tClock = the period of the X1 input clock



SCK minimum high or low time is 3 * tClock.

SDO is high impedance until data read out, and then returns to high impedance due to the rising edge of CS.

REGISTER ADDRESS AND BIT ASSIGNMENT

All registers are read/write except for the two ADC result registers which are read only. The left hand column refers to the data bits shown as B7 through B0 on the synchronous serial I/O timing diagram.

CONTROL REGISTER, address A[2:0] = 000 binary

		ADC Clock divisor		Baud rate divisor	
CR[7:5] Clock divisor	bits	M1 low	M1 high	M1 low	M1 high
	000	8	8	512	416
	001	4	4	256	208
	010	6	12	384	768
	011	3	13	192	832
	100	192	160	1024	1024
	101	216	180	1152	1152
	110	288	240	1536	1536
	111	312	260	1664	1664
CR[4:3] Input channel select	00	IN1			
	01	IN3			
	10	GND			
	11	IN2			
CR[2:0] Full scale select V(INxP) – V(INxN)	000	+/- 50 mV			
	001	+/- 25 mV			
	010	+/- 250 mV			
	011	+/- 10 mV			
	100	0 to 100 mV			
	101	0 to 50 mV			
	110	selects the internal temperature sensor			
	111	0 to 20 mV			

COMP_1 REGISTER, A[2:0] = 001 binary

7:0	Eight least significant bits of comparator 1

COMP_2 REGISTER, A[2:0] = 010 binary

7:0	Eight least significant bits of comparator 2

COMP_MSN REGISTER, A[2:0] = 011 binary

7:4	Four most significant bits of comparator 1
3:0	Four most significant bits of comparator 2

ADC_1 REGISTER, A[2:0] = 100 binary

7	DRDY status	0 = data ready 1 = data not ready
6	CMP status	0 = ADC data outside the comparator window 1 = ADC data inside the comparator window
5 4	reserved reserved	
3 2 1 0	ADC data D11 ADC data D10 ADC data D9 ADC data D8	

ADC_2 REGISTER, A[2:0] = 101 binary

7:0	ADC data D[7:0]

Note: Reading this address sets the DRDY and CMP status bits to logic 1 and pins DRDY and CMP = high.

EXTERNAL SERIAL EEPROM PROGRAMMING

In this mode the MX844 auto-increments the EEPROM address from 0 up to 7 and then the address rolls back to 0. A single EEPROM word is read at the beginning of every ADC auto-zero period and is interpreted by the MX844 as a synchronous serial I/O write command. These commands control the scanning sequence of the ADC channels, the full scale ranges, and the internal dividers. The MX844 accesses the EEPROM as if it were a ROM and will not write or erase the EEPROM. In the master mode the first data bit serially read out of the EEPROM must always be a logic 1 which indicates a write (of the MX844 register). The second through fourth bits are the address field, followed by eight data bits. The last four bits of the EEPROM word are don't cares.

One 16-bit word of the 93C46 serial EEPROM is used to hold one MX844 synchronous serial I/O instruction. Each pulse of SCK corresponds to one bit in the EEPROM. However, the data is aligned such that the MX844 R/W bit that occurs at the 5th SCK pulse of the serial interface timing is the MSB in the EEPROM word. The last 4 bits of the EEPROM word are always zero. For example, the instruction to write the byte 1Ah into the MX844 control register (IN2 +/-250mV scale) would be programmed into the EEPROM as the 16-bit quantity 81A0h. Entered into a typical programmer file editor in the least-significant-byte first format it would be the byte A0h followed by the byte 81h. Eight pairs of bytes can be specified in the programming file (EEPROM address 0 to 7). The MX844 will ignore the remaining contents of the EEPROM (address > 7).

MX844 command:

R/W	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	1	1	0	1	0
8				1				A			

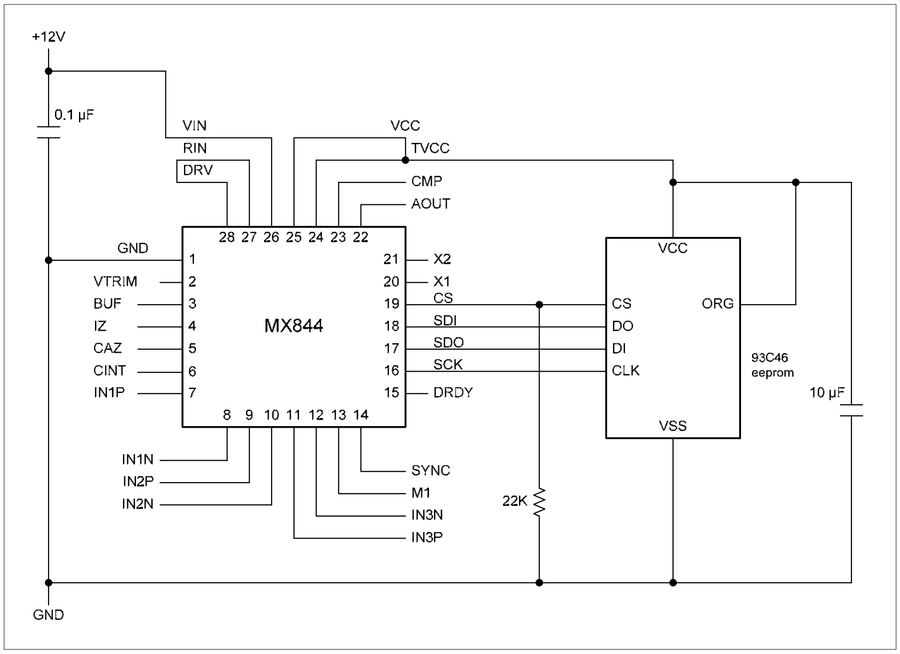
EEPROM programmer editor:

B3	B2	B1	B0					R/W	A2	A1	A0	B7	B6	B5	B4
				0	0	0	0								
A				0				8				1			

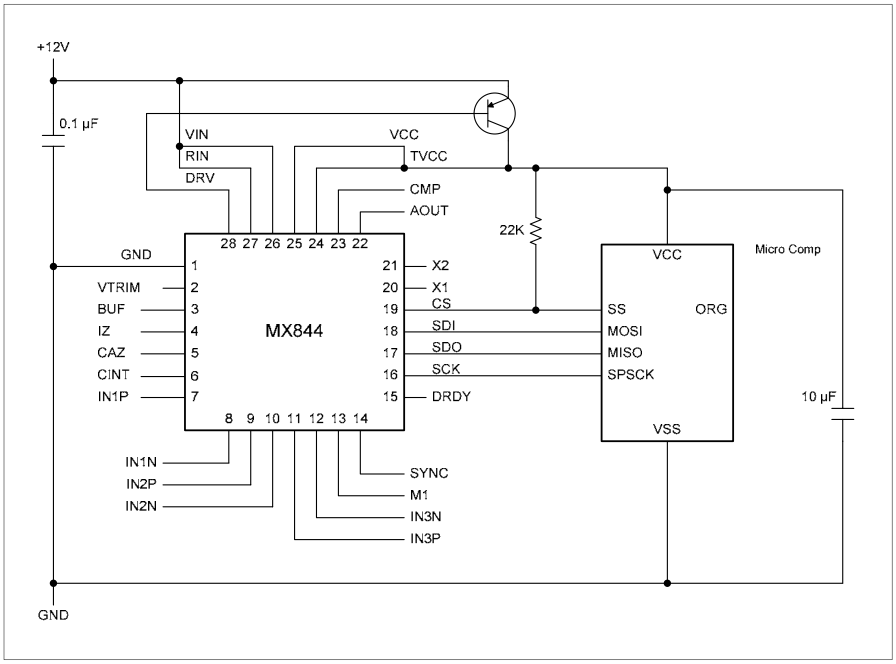
Circuit Examples

The two examples shown below are for illustration only, and are not complete schematics. The power dissipation will determine if the external pass element is required regardless of whether an eeprom or a microcontroller are connected.

MX844 INTERNAL PASS ELEMENT, SERIAL EEPROM CONNECTION



MX844 EXTERNAL PASS ELEMENT, MICROCONTROLLER CONNECTION



APPLICATION EXAMPLE - POWER MONITOR

This design example illustrates the application of the MX844 as an AC line power monitor.

In this design the MX844 operates as a serial bus master, reading instructions from an external serial EEPROM.

Following application of power, the first 16-bit word read from the EEPROM is 0x8200 (using "C" notation to indicate a hexadecimal number) which in conjunction with the connection of terminal M1 to VCC, causes the MX844 to set it's internal dividers for 488 A/D samples per second and an asynchronous baud rate of 38.4 Kbaud when using an 8 MHz clock. The first measurement is made from input channel IN1 on the +/- 50 mV scale. For the power meter this is a measurement of the AC line current flowing through sense resistor R1. A value of 0.002 Ohm for R1 results in a +/- 25A current scale.

The second instruction is 0x83A0, which results in a measurement from input channel IN2 on the +/- 250 mV scale. For the power meter this is a measurement of the AC line voltage through the voltage attenuator consisting of resistors R2, R3, and R4 which provide a full scale of +/- 407 V.

The MX844 cycles through the first eight addresses of the EEPROM. Therefore the first two instruction codes are repeated three more times in order to continuously alternate between AC line voltage and current measurements.

This is how the EEPROM contents would appear in a typical programmer buffer editor:

```
00  82  A0  83  00  82  A0  83  00  82  A0  83  00  82  A0  83
00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
```

Note that the 16-bit word is broken up into two bytes with the least significant byte first.

The power monitor is powered directly off the line using resistors R14 - R20, diodes D1 and D2, and capacitor C1 to produce an unregulated DC voltage for the MX844.

Opto-isolator U3 provides isolation between the AC power line and the computer serial port. Dual transistors Q1 and Q2 and related circuitry amplify the photodiode signal into the required RS-232 signal for the computer serial port. Power for the photodiode amplifier is very small and is supplied by the serial port DTR and RTS terminals.

By analyzing the data stream from the MX844 the computer software program can determine the RMS line voltage, the RMS line current, the RMS power consumed, and the power factor of the load.

Each digitized sample is transmitted to the computer as two 8-bit "characters" in asynchronous RS-232 format. Embedded in the two characters are the 12 bits of data and a 3-bit EEPROM address.

The software performs the following tasks:

1) Synchronize to the EEPROM address.
2) Acquire 256 samples.
3) Separate into 128 voltage readings and 128 current readings.
4) Calculate the RMS value of the voltage and the current (standard deviation of the 128 data set).
   Apparent power is Vrms * Irms.
5) Perform "flat top" windowing and then FFT on the voltage to determine the whether the frequency is 60Hz or 50Hz.
   The FFT also gives an RMS amplitude value for the voltage.
6) Determine the voltage at the time of the current measurements by sine wave interpolation between each pair of voltage readings.
7) Calculate the real power using the 128 measured current values and the 128 interpolated voltage values. Also calculate the power factor.

Program listing:

```
/* This program reads alternating samples of voltage and current from      */
/* the MX844 AOUT terminal which is connected to a PC com1 port with       */
/* the demo board circuitry.                                               */
/* This demo program directly accesses the PC's 16550 UART using inp()     */
/* and outp() functions and therefore must be compiled and run in          */
/* real mode (DOS box) under win98.                                        */

#include <stdio.h>
#include <conio.h>
#include <math.h>

void frier(double *, double *, int);
int round(double);

#define NMAX 256
double xd[NMAX+2];
double yd[NMAX+2];
double pd[NMAX+2];

FILE *inf;
int lost, m, onez, twoz, rdata, i, j, w, d[4*NMAX];
int ad[NMAX], ad2[NMAX], n[NMAX], n2[NMAX];
long t;
int np,imax;
double rt2,ln10,min,max,fmax,k,pi,nbw,resHz,samHz;
double wt, b, a, vrms, irms, pf, rp, cv;
double ivsum, sum, ss, sumi, ssi, aw, av;
float vscale, iscale;

main(argc,argv)
int argc;
char *argv[];
{
  rt2 = sqrt(2);
  ln10 = log(10);
  pi = 4 * atan(1);

  np = 128;       /* number of points in FFT time series */
  /* use the following line for 12MHz clock with a divider of 8
   or 6MHz clock with a divider of 4 */
  /* samHz = 12e6/8/4096/2;*/
  /* use the following line for 8MHz clock with a divider of 4 */
  samHz = 8e6/4/4096/2;

  vscale = (0.250 / 2048) * 1629 ; /* 440K & 270 resistor divider */
  iscale = (0.050 / 2048) / 0.002; /* 0.002 ohm shunt */
```

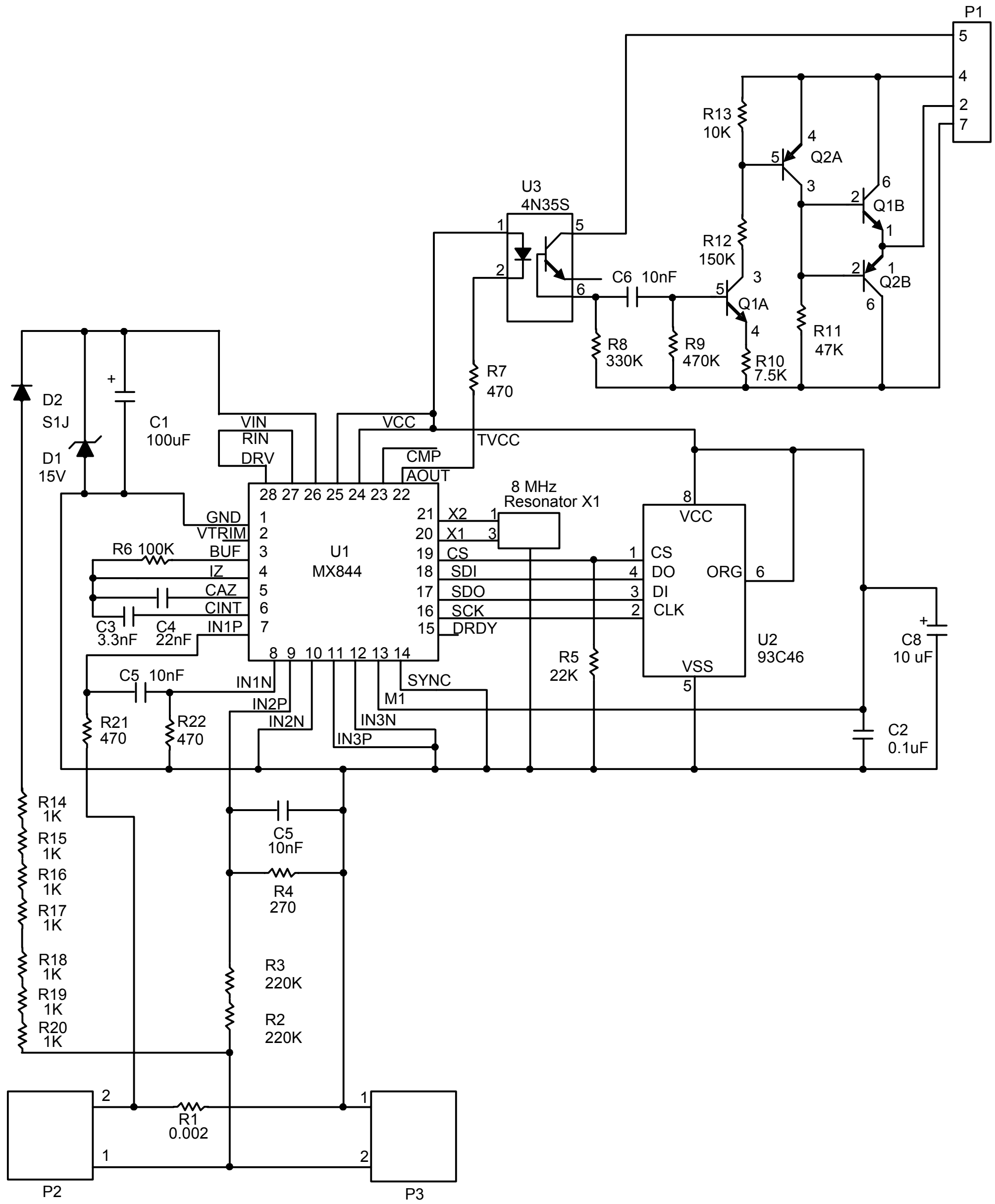
```
/* setup the com1 port */
outp(0x3fb,0x83);  /* 8 bits no parity, DLAB=1 */
outp(0x3f9,0);     /* upper divisor = 0 */
/*outp(0x3f8,4);*/   /* lower divisor = 4 (28800 baud) */
outp(0x3f8,3);     /* lower divisor = 3 (38400 baud) */
outp(0x3fc,1);     /* DTR +V, RTS -V */
outp(0x3fb,3);     /* DLAB = 0 */

/* open the output log file */
inf = fopen("meter.log","w");

/* initialize arrays */
for(i=0;i<np;i++)
  {
     ad[i] = 0;
     ad2[i] = 0;
     n[i] = 0;
     n2[i] = 0;
  }
for(i=0;i<4*np;i++) d[i] = 0;

/* start data acquisition from MX844 */
lost = 1;
while(lost == 1)
  {
    /* synchronize to MX844 async data stream */
    /* find n0,n1 = 00 and n2,n3 = 00 */
    twoz = 0;
    while (twoz == 0)
    {
             onez = 0;
             /* read bytes until n0,n1 = 00 */
             while (onez == 0)
             {
                    w = 0;
                    while ((inp(0x3fd) & 1) == 0) {w=1;} /*wait for data ready*/
                    d[0] = inp(0x3f8);
                    if((d[0] & 0x00c0) == 0) onez = 1;
             }
             /* read the next byte */
             w = 0;
             while ((inp(0x3fd) & 1) == 0) {w=1;}  /* wait for data ready */
             d[1] = inp(0x3f8);
             if((d[1] & 0x00c0) == 0) twoz = 1;
             else /* change "phase" */
             {
                    w = 0;
                    while ((inp(0x3fd) & 1) == 0) {w=1;} /*wait for data ready*/
                    d[0] = inp(0x3f8);
             }
    } /* end twoz */

  m=0;

  /* read the actual data */
  for(i=2;i<4*np;i++)
      {
        w = 0;
        while ((inp(0x3fd) & 1) == 0) {w=1;} /*wait for data ready */
        d[i] = inp(0x3f8);
        if(w==0) m++;
        /* printf("\n%02X  %1d",d[i],w); */
      }

  /* check for loss of sync in the data */
  lost = 0;
  for(i=0;i<np;i++)
      {
             m = ((0xc0 & d[2*i])>>6)+((0xc0 & d[2*i+1])>>4);
             if(m != i % 8) lost = 1;
      }
      if (lost == 1)
        {
          printf("lost sync\n");
          for(t=0;t<200000;t++); /* wait to try again */
        }
  } /* done with acquisition */
```

```
/* separate voltage and current, report data */
for(i=0;i<np;i++)
      {
             ad[i] = (0x3f & d[4*i])+(64*(0x3f & d[4*i+1]));
             ad2[i] = (0x3f & d[4*i+2])+(64*(0x3f & d[4*i+3]));

             n[i] = ((0xc0 & d[4*i])>>6)+((0xc0 & d[4*i+1])>>4);
             n2[i] = ((0xc0 & d[4*i+2])>>6)+((0xc0 & d[4*i+3])>>4);
      }

/* report voltage readings */
fprintf(inf,"Raw data: (n2,n1,n0) <ADC counts>\n");
fprintf(inf,"Voltage:\n");
for(i=0;i<np;i++)
        {
             fprintf(inf,"(%1d)%4d ",n[i],ad[i]);
             if(i%8 == 7) fprintf(inf,"\n");
        }
fprintf(inf,"\n");

/* report current readings */
fprintf(inf,"Current:\n");
for(i=0;i<np;i++)
        {
             fprintf(inf,"(%1d)%4d ",n2[i],ad2[i]);
             if(i%8 == 7) fprintf(inf,"\n");
        }

/* calculate Vrms */
sum = 0;
ss = 0;
for(i=0;i<np;i++)
        {
          sum += ad[i];
          ss += (double)ad[i] * (double)ad[i];
        }
vrms = sqrt(ss/np - (sum/np)*(sum/np));
fprintf(inf,"\n%8.1f Volts rms\n",vrms * vscale);
printf("\n%8.1f Volts rms\n",vrms * vscale);

/* calculate Irms */
sumi = 0;
ssi = 0;
for(i=0;i<np;i++)
      {
        sumi += ad2[i];
        ssi += (double)ad2[i] * (double)ad2[i];
      }
irms = sqrt(ssi/np - (sumi/np)*(sumi/np));
fprintf(inf,"%8.2f Amps rms\n",irms * iscale);
printf("%8.2f Amps rms\n",irms * iscale);

/* calculate apparent power (VA) */
aw = vrms * vscale * irms * iscale;
printf("%8.1f VA\n",aw);

fprintf(inf,"%8.1f VA\n",aw);
fprintf(inf,"%5.1f calculated average V counts\n",sum/np);
fprintf(inf,"%5.1f calculated average I counts\n",sumi/np);
av = sum/np;

/* fill the FFT data arrays */
for(i=1;i<=np;i++) /* fft data [1..np] instead of [0..np-1] */
  {
    xd[i] = ad[i-1];
    yd[i] = 0;
  }
xd[0] = 0; yd[0] = 0;
xd[np+1] = 0; yd[np+1] = 0;

/* perform the windowing */
k = 2 * pi / (np - 1); /* i*k==0 if i=0, ==2*pi if i=127 */
for(i=0;i<np;i++)
  { /* remember [1..np] */
      xd[i+1] *= 1-1.8533*cos(i*k)+0.7046*cos(2*i*k);
  }
```

```
  resHz = samHz / np;   /* frequency resolution */
  nbw = 3.44 * resHz;   /* calculate noise bandwidth */

  frier(xd,yd, round(log(np)/log(2)));

  /* report the FFT result */
  max = 0;
  for(i=1;i<=1+np/2;i++)
   {
     pd[i] = rt2 * sqrt(pow(xd[i],2) + pow(yd[i],2));
     fprintf(inf,"%8.2f %12.4f",resHz*(i-1),pd[i]);
     fprintf(inf,"   %12.4f  %12.4f\n",xd[i],yd[i]);

     if((pd[i] > max) && i>9)
         {
           max = pd[i];
           imax = i;
           fmax = resHz*(i-1);
         }
   }
  if(pd[imax+1]/pd[imax] > 0.8) fmax += resHz/2;
  if(pd[imax-1]/pd[imax] > 0.8) fmax -= resHz/2;
  fmax = (double)round(fmax);
  fprintf(inf,"%5.1f Vrms from FFT at %2.0f Hz\n",max*vscale,fmax);

  /* interpolate V at time of I and calculate real power */
  fprintf(inf,"Instantaneous VA:\n");
  ivsum = 0;
  for(i=0;i<np-1;i++)
    {
             b = (double)ad[i] - av;
             wt = 2*pi*fmax/samHz;
             a = ((double)ad[i+1]-av-b*cos(wt))/sin(wt);

             wt = 2*pi*fmax*0.5/samHz;
             cv = a*sin(wt) + b*cos(wt);
             rp = -(iscale*(ad2[i] - av)*vscale*cv);
             fprintf(inf,"%7.2f ",rp);
             if(i%8 == 7) fprintf(inf,"\n");
             ivsum += rp;
    }
  /* the last data point is special */
  wt = 2*pi*fmax*1.5/samHz;
  cv = a*sin(wt) + b*cos(wt);
  rp = -(iscale*(ad2[np-1] - av)*vscale*cv);
  fprintf(inf,"%7.2f ",rp);
  if(i%8 == 7) fprintf(inf,"\n");
  ivsum += rp;

  /* report the results */
  fprintf(inf,"\n");
  if(ivsum < 0) ivsum = -ivsum;
  printf("%8.1f real watts\n",ivsum/np);
  fprintf(inf,"%8.1f real watts\n",ivsum/np);
  pf = (ivsum/np) / aw;
  if(pf>1) pf=1;
  printf("%8.2f power factor\n",pf);
  fprintf(inf,"%8.2f power factor\n",pf);

  fclose(inf);

} /* end main */

/* rounding function */
int round(double x)
{
  if(x>0)
     return((int) (x + 0.5));
    else
     return((int) (x - 0.5));
}
```

```
/* FFT routine */
void frier(double *x, double *y, int ig)
/* ig = number of points as a power of 2 */
/* for example, ig = 8 for 256 point FFT */
{
  double p,y1,y2,y3,y4;
  int n,m,m1,m2,k,k1,k2,k3,k4,k5,i,j,l,ig1;

  n = 1 << ig;
  p = 8 * atan(1) / n;
  for(i=1;i<=n;i++)
   {
    *(x+i) /= n;
    *(y+i) /= n;
   }
  for(l=1;l<=ig;l++)
   {
    ig1 = 1 << (ig-l);
    m = 0;
    k4 = 1 << (l-1);
    for(i=1;i<=k4;i++)
     {
      k1 = m / ig1;
      k2 = 0;
      k3 = 1 << (ig-1);
      for(k=1;k<=ig;k++)
       {
        if((1 & k1) == 1) k2 += k3;
        k3 >>= 1;
        k1 >>= 1;
       }
      y1 = cos(p*k2);
      y2 = -sin(p*k2);
      for(k=1;k<=ig1;k++)
       {
        m1 = m + ig1 + 1;
        m2 = m + 1;
        y3 = *(x+m1) * y1 - *(y+m1) * y2;
        y4 = *(x+m1) * y2 + *(y+m1) * y1;
        *(x+m1) = *(x+m2) - y3;
        *(y+m1) = *(y+m2) - y4;
        *(x+m2) += y3;
        *(y+m2) += y4;
        m++;
       }
      m += ig1;
     }
   }
  for(i=1;i<=n;i++)
   {
    k1 = i - 1;
    k2 = 0;
    k3 = 1 << (ig-1);
    for(k=1;k<=ig;k++)
     {
      if((1 & k1) == 1) k2 += k3;
      k3 >>= 1;
      k1 >>= 1;
     }
    k5 = k2 + 1;
    if((k5-i) < 0)
     {
      y3 = *(x+i);
      *(x+i) = *(x+k5);
      *(x+k5) = y3;
      y3 = *(y+i);
      *(y+i) = *(y+k5);
      *(y+k5) = y3;
     }
   }
}
```

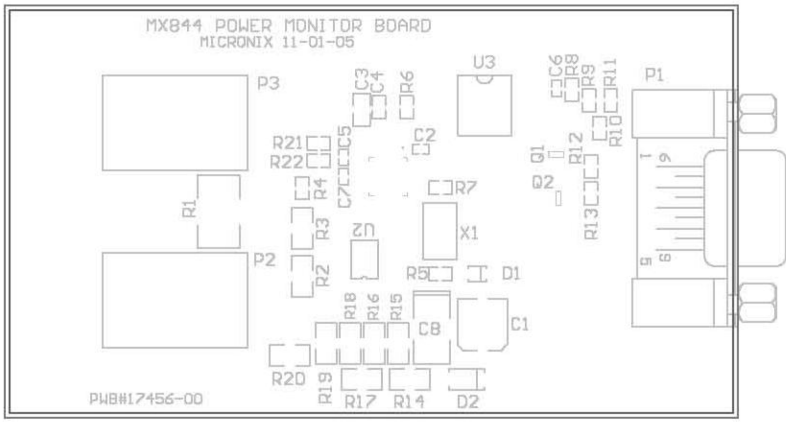
POWER MONITOR DEMO BOARD CIRCUIT SCHEMATIC



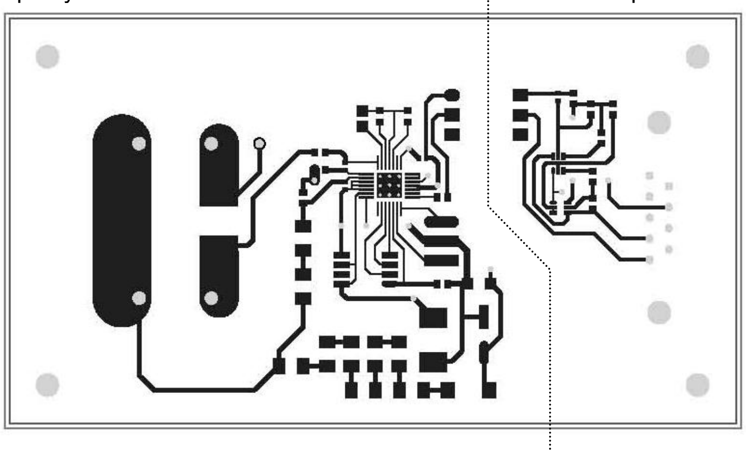
POWER MONITOR PRINTED CIRCUIT DEMO BOARD LAYOUT

Artwork scale approximately actual size.
P1 is a DB-9 connector for RS-232 connection.
P2 and P3 are screw-type terminals for AC power line connection.
All other components are surface mount.

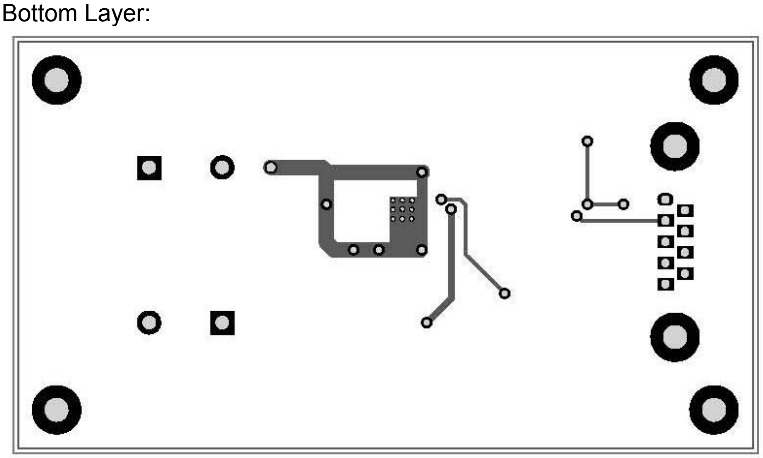
Silkscreen:



Top Layer: ← Isolation path



Bottom Layer:

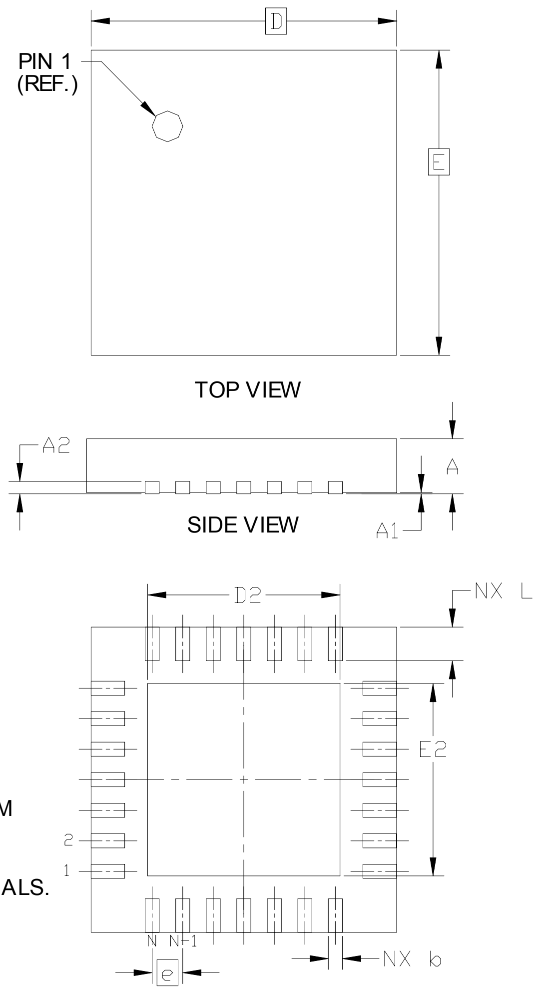


POWER MONITOR PRINTED CIRCUIT BOARD PARTS LIST

U1	MICRONIX MX844			28-QFN 5x5mm
U2	MICROCHIP 93LC46B	Serial EEPROM		8-SOIC
U3	LiteOn 4N35S	Opto-isolator		6-SMT
Q1	ON Semi MBT3904	Dual 2N3904		SOT-363
Q2	ON Semi MBT3906	Dual 2N3906		SOT-363
D1	ON Semi MMSZ5245B	15V 0.5W Zener		SOD-123
D2	Fairchild S1J	600V Rectifier		SMA
X1	Abracon AWSCR-8.00MGD-T	8MHz Resonator		7434-SMT
C1	Nichicon UWX1C101MCL1GB	100uF 16V		6.3x5.4 SMT
C2	Murata GRM155F51C104ZA01D	0.1uF Y5V 16V		0402
C3	Murata GRM2165C1H332JA01D	3300pF COG 5%		0805
	(low loss for integrator, COG acceptable, metal film is better)			
C4	Murata GRM188R71H223MA01D	0.022uF X7R 20%		0603
C5-C7	Murata GRM155R71E103KA01D	0.01uF X7R 10%		0402
C8	Nichicon F931A106MAA	10 uF 10V		3.2 by 1.6 SMT
R1	Panasonic ERJ-M1WTF2M0U	0.002 1%	2512	(current sense type)
R2-3		220K 1%	1206	
R4		270 1%	0603	
R5		22K	0603	
R6		100K	0603	
R7, R21, R22		470	0603	
R8		330K	0603	
R9		470K	0603	
R10		7.5K	0603	
R11		47K	0603	
R12		150K	0603	
R13		10K	0603	
R14-R20		1K	1206	
P1	NORCOMP 182-009-212-531		DB-9 for computer serial port	
P2, P3	Phoenix Contact MKDS 5/2-9.5 1714971		Suitable for AC line connection	

28 LEAD 5MM X 5MM X 0.90MM QFN

DIMENSIONS				
DIM.	INCH		MM.	
	MIN.	MAX.	MIN.	MAX.
A	.031	.039	.80	1.0
A1	0	.002	0	.05
A2	.008 REF.		,200 REF.	
b	.007	.012	.18	.30
D	.197 BSC		5.00 BSC	
D2	.118	.128	3.00	3.25
E	.197 BSC		5.00 BSC	
E2	.118	.128	3.00	3.25
e	.0197 BSC		.500 BSC	
L	.0177	.0256	.45	.65
N	28		28	



BOTTOM VIEW

3. MOLDED PACKAGE SHALL CONFORM TO JEDEC STANDARD CONFIGURATION MO-220 VARIATION VHHD-1.

2. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5M-1994.

1. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

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