Pushbutton PowerPath™ Controller with Supervisor

FEATURES

- **Pushbutton On/Off Control**
- **Automatic Low Loss Switchover Between DC Sources**
- **Wide Operating Voltage Range: 2.7V to 28V**
- **Low 25µA Shutdown Current**
- **Guaranteed Threshold Accuracy: ±1.5% of Monitored Voltage Over Temperature**
- Adjustable Pushbutton On/Off Timers
- Simple Interface Allows Graceful µP Shutdown
- Extendable Housekeeping Wait Time Prior to Shutdown
- 200ms Reset Delay and 1.6s Watchdog Timeout
- ±8kV HBM ESD on $\overline{PB}$ Input
- 20-pin TSSOP and QFN (4mm × 4mm) Packages

APPLICATIONS

- Desktop and Notebook Computers
- Portable Instrumentations
- Cell Phones, PDA and Handheld Computers
- Servers and Computer Peripherals
- Battery Backup Systems

DESCRIPTION

The LTC®2952 is a power management device that features three main functions: pushbutton on/off control of system power, ideal diode PowerPath controllers and system monitoring. The LTC2952's pushbutton input, which provides on/off control of system power, has independently adjustable ON and OFF debounce times. A simple microprocessor interface involving an interrupt signal allows for proper system housekeeping prior to power-down.

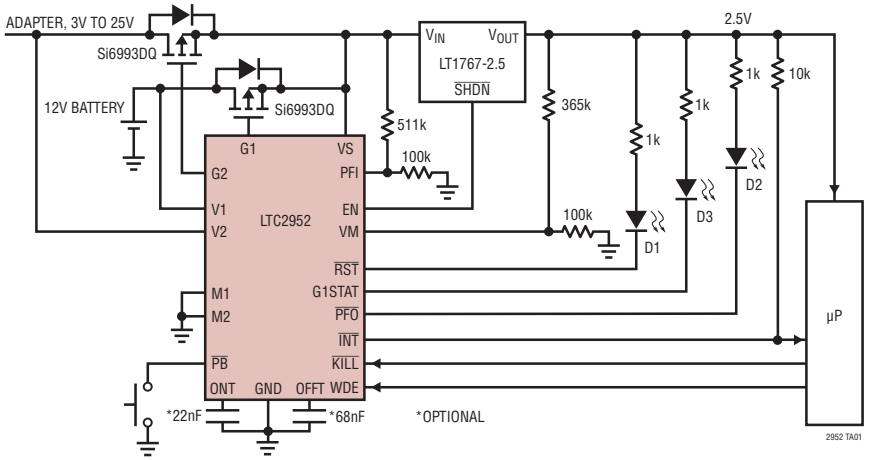
The ideal diode PowerPath controllers provide automatic low loss switchover between two DC sources by regulating two external P-channel MOSFETs to have a small 20mV forward drop.

High reliability systems may utilize the LTC2952's monitoring features to ensure system integrity. These features include: power-fail, voltage monitoring and µP watchdog.

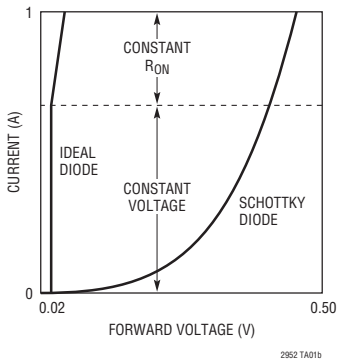
The LTC2952 operates over a wide operating voltage range to accommodate a large variety of input power supplies. The part's combination of low 20mV external MOSFET regulation and very low standby current matches battery powered and power conscious application requirements.

TYPICAL APPLICATION

Pushbutton Controller with Automatic Switchover Between Adapter and Battery



Ideal Diode vs Schottky Diode Forward Voltage Drop



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages
- V1, V2, VS ..... –0.3V to 30V

Input Voltages
- $\overline{PB}$ ..... –6V to MAX (V1, V2, VS) V
- ONT, OFFT ..... –0.3V to 3V
- M1, M2, PFI, VM, WDE, $\overline{KILL}$ ..... –0.3V to 7V

Output Voltages
- G1, G2, EN ..... –0.3V to MAX (V1, V2, VS) V
- G1STAT, $\overline{PFO}$, $\overline{RST}$, $\overline{INT}$ ..... –0.3V to 7V

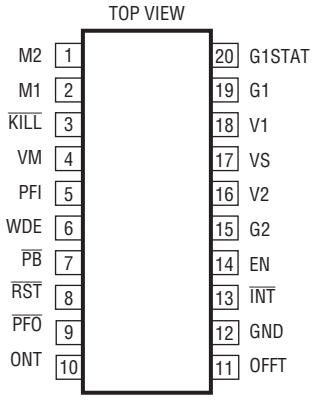
Input Currents
- $\overline{PB}$ ..... –1mA to 100µA

Operating Temperature Range
- LTC2952C ..... 0°C to 70°C
- LTC2952I ..... –40°C to 85°C

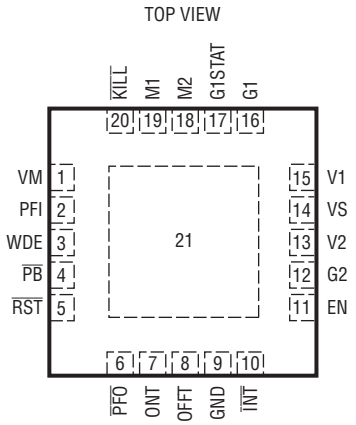
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



F PACKAGE
20-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 90°C/W



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 21), PCB GND CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2952CF#PBF	LTC2952CF#TRPBF	LTC2952CF	20-Lead Plastic TSSOP	0°C to 70°C
LTC2952IF#PBF	LTC2952IF#TRPBF	LTC2952IF	20-Lead Plastic TSSOP	–40°C to 85°C
LTC2952CUF#PBF	LTC2952CUF#TRPBF	2952	20-Lead 4mm × 4mm Plastic QFN	0°C to 70°C
LTC2952IUF#PBF	LTC2952IUF#TRPBF	2952	20-Lead 4mm × 4mm Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V1 = V2 = VS = 2.7V to 28V unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{MAX}	Operating Supply Voltage	V1, V2 or VS	●	2.7		28	V
I_{IN_OFF}	Quiescent Supply Current Both Ideal Diodes Switched Off (M1 = Open, M2 = 0V)	V1 = 2.7V to 28V, V2 = 0V, VS = Open or V2 = 2.7V to 28V, V1 = 0V, VS = Open. Measured Current at V1 or V2.	●		24	60	µA
		V1 = 2.7V to 28V, V2 = 3.5V, VS = Open. Measured Current at V1.	●		5	15	µA
		V1 = 2.7V to 28V, V2 = 3.5V, VS = Open. Measured Current at V2.	●		23	50	µA
I_{IN_ON}	Quiescent Supply Current Both Ideal Diodes Switched On (M1 = 0V, M2 = 0V)	V1 = VS = 2.7V to 28V, V2 = 0V or V2 = VS = 2.7V to 28V, V1 = 0V. Measured Combined Current at V1 and VS or V2 and VS.	●		65	170	µA
$V2_{PREF\_TH}$	V2 Preferential Threshold Voltage (M1 = Open, M2 = 0V) (Note 4)	V1 = 28V, VS = Open.	●		3.3	3.8	V
I_{LEAK}	V1, V2 and VS Inter Pin Leakage to the Highest Supply	V1 = 28V, V2 = VS = 0V; V1 = VS = 0V, V2 = 28V; V1 = V2 = 0V, VS = 28V				±3	µA
Ideal Diode Function							
V_{FR}	Ideal Diode PowerPath Forward Regulation Voltage	(V1 or V2) – VS, 2.7V ≤ (V1 or V2) ≤ 28V	●	10	20	35	mV
V_{RTO}	Ideal Diode PowerPath Fast Reverse Turn-Off Threshold Voltage	(V1 or V2) – VS, 2.7V ≤ (V1 or V2) ≤ 28V $\Delta I_G \leq -100\mu A/mV$	●	–20	–35	–64	mV
$I_{G(SRC)}$	Gate Turn-Off Current	G1 = G2 = V_{MAX} – 1.5V	●	–2	–5	–10	µA
$I_{G(SNK)}$	Gate Turn-On Current	V1 = V2 = 2.7V to 28V, VS = (V1 or V2) – 40mV, G1 = G2 = V_{MAX} –1.5V.	●	2	5	10	µA
$I_{G(FASTSRC)}$	Gate Fast Turn-Off Source Current	V1 = V2 = 2.7V to 28V, VS = (V1 or V2) + 0.1V, G1 = G2 = V_{MAX} –1.5V.	●	–0.5	–2.5	–10	mA
$I_{G(FASTSNK)}$	Gate Fast Turn-On Sink Current	V1 = V2 = 5V to 28V, VS = (V1 or V2) – 0.1V, G1 = G2 = V_{MAX} – 1.5V.	●	0.3	0.7	2	mA
$V_{G(ON)}$	Gate Clamp Voltage	I_{GX} = 2µA, V_X = 8V to 28V, VS = V_X – 0.1V Measure V_X – V_{GX}	●	6	7	8	V
$V_{G(OFF)}$	Gate Off Voltage	I_{GX} = –2µA, V_X = 2.7V to 28V, VS = V_X + 0.1V Measure V_{MAX} – V_{GX}	●		0.2	0.4	V
$t_{G(ON)}$	Gate Turn-On Time	$V_{G(OFF)}$ to $V_{GS} \leq -3V$, C_{GATE} = 1nF (Note 5), V1 = V2 = 12V		0.1	2.5	10	µs
$t_{G(OFF)}$	Gate Turn-Off Time	$V_{G(ON)}$ to $V_{GS} \geq -1.5V$, C_{GATE} = 1nF (Note 6), V1 = V2 = 12V		0.1	2.5	10	µs
Pushbutton Pin ($\overline{PB}$)							
$V_{\overline{PB}(VOC)}$	$\overline{PB}$ Open-Circuit Voltage	$I_{\overline{PB}}$ = –1µA	●	1	4	6	V
$I_{\overline{PB}}$	$\overline{PB}$ Input Current	$V_{\overline{PB}(VOC)} < V_{\overline{PB}} \leq 28V$ $0V \leq V_{\overline{PB}} < V_{\overline{PB}(VOC)}$	● ●	 –1	 –10	±1 –25	µA µA
$V_{TH\_\overline{PB}}$	$\overline{PB}$ Input Threshold Voltage	$\overline{PB}$ Falling From High to Low	●	0.65	0.77	0.8	V
$V_{HYS\_\overline{PB}}$	$\overline{PB}$ Input Hysteresis		●	10	25	150	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V1 = V2 = VS = 2.7V TO 28V unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Debounce Time Pins (ONT, OFFT)							
$I_{ONT,OFFT}$	ONT/OFFT Pull-Up/Pull-Down Current When Timer Is Active	V_{ONT}, V_{OFFT} = 0V (Pull-Up), V_{ONT}, V_{OFFT} = 1.5V (Pull-Down)	●	±1.6	±2.0	±2.4	µA
$t_{DB,ON/OFF}$	Internal Default On-Time/Off-Time	$t_{DB,ON}$: C_{ONT} = Open, Measured Time Between $\overline{PB}$ Low → EN High, $t_{DB,OFF}$: Measured Time Between $\overline{PB}$ Low → INT High	●	18	26	34	ms
$t_{ONT,OFFT}$	Additional Adjustable Turn-On/Turn-Off Time (Note 7)	C_{ONT} = 1500pF, C_{OFFT} = 1500pF	●	10	15	20	ms
Accurate Comparator Input Pins (VM, PFI, M1, M2, $\overline{KILL}$)							
V_{TH_VM}	VM Input Reset Threshold	Both Falling and Rising	●	0.492	0.500	0.508	V
V_{TH}	PFI, M1, M2, $\overline{KILL}$ Input Threshold Voltage	Falling	●	0.492	0.500	0.508	V
V_{HYS}	PFI, M1, M2, $\overline{KILL}$ Input Hysteresis		●	5	15	25	mV
I_{IN_LKG}	VM, PFI, M2, $\overline{KILL}$ Input Current	V = 0.5V	●			±0.1	µA
I_{M1_SRC}	M1 Input Pull-Up Current	M1 = 1V	●	–1.5	–3	–5	µA
$V_{M1(VOC)}$	M1 Voltage Open-Circuit		●	1	4	6	V
I_{M1_LKG}	M1 Input Leak Current	M1 = 6V	●			±0.1	µA
Watchdog/Extend Pin (WDE)							
$V_{WDE(H,TH)}$	Input High Threshold Voltage		●			1.5	V
$V_{WDE(L,TH)}$	Input Low Threshold Voltage		●	0.3			V
$I_{WDE(IN,HL)}$	High Low Input Current (Note 8)		●			±25	µA
$I_{WDE(IN,HZ)}$	Hi-Z Input Current	V_{WDE} = 0.7V, 1.1V	●	±10			µA
Open-Drain Output Pins (G1STAT, $\overline{INT}$, $\overline{RST}$, $\overline{PFO}$)							
I_{OUT_LKG}	Leakage Current	V_{PIN} = 5V	●			±1	µA
V_{OL}	Voltage Output Low	I_{PIN} = 1mA	●			0.4	V
High Voltage Open-Drain Output Pin (EN)							
$I_{EN(LKG)}$	EN Leakage Current	V_{EN} = 28V, EN Sink Current Off	●			±1	µA
$V_{EN(VOL)}$	EN Voltage Output Low	I_{EN} = 3mA	●			0.4	V
		V1 = 1.2V and/or V2 = 1.2V, I_{EN} = 100µA	●		0.05	0.3	V
Voltage Monitor/Watchdog Timing							
t_{RST}	Reset Timeout Period		●	140	200	260	ms
t_{WDE}	Watchdog Timeout Period		●	1.1	1.6	2.1	s
$t_{WDE(PW\ MIN)}$	Minimum Period Between Consecutive Edges		●		5	10	µs
$t_{VM(UV)}$	VM Undervoltage Detect to $\overline{RST}$	VM Less Than V_{TH_VM} by More Than 1%			150		µs
t_{PFI}	PFI Delay to $\overline{PFO}$	PFI More or Less Than V_{PFI_TH} by More Than 1%			150		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V1 = V2 = VS = 2.7V to 28V unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
µP Handshake Timing							
$t_{\overline{INT}(MIN)}$	$\overline{INT}$ Minimum Pulse Width	Minimum Measured Time $\overline{PB}$ Rising to $\overline{INT}$ Rising	●	10	50	250	µs
$t_{\overline{KILL}(PW)}$	$\overline{KILL}$ Minimum Pulse Width	Full Swing Pulse From 5V to 0V	●		150	500	µs
$t_{\overline{KILL},ON\ BLANK}$	$\overline{KILL}$ On Blanking (Note 9)	$\overline{KILL}$ = 0V, Measured Time Between EN Rising → EN Falling	●	270	400	530	ms
$t_{\overline{KILL},\ OFF\ WAIT}$	$\overline{KILL}$ Wait Time (Note 10)	$\overline{KILL}$ = 1V, $C_{OFFT\ =\ OPEN}$, Measured Time Between $\overline{INT}$ Falling → EN Falling	●	270	400	530	ms
$t_{EN,\ LOCKOUT}$	Enable Lockout Time (Note 11)	Measured Time Between EN Falling → EN Rising	●	270	400	530	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The greatest of V1, V2 or VS is the internal supply voltage (V_{MAX}).

Note 3: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 4: $V2_{PREF\_TH}$ is the minimum voltage level at which V2 becomes the preferential source of quiescent current when both of the ideal diodes are off.

Note 5: VS is stepped from (V1 or V2) + 0.2V to (V1 or V2) – 0.2V to trigger the event. The gate voltages are initially $V_{G(OFF)}$.

Note 6: VS is stepped from V_X – 0.2V to V_X + 0.2V to trigger the event. Gate voltages are initially clamped at $V_{G(ON)}$.

Note 7: The adjustable turn-on and turn-off timer period is the adjustable debounce period following the Internal default-on and default-off timer period, respectively.

Note 8: The input current to the three-state WDE pin are the pull-up and the pull-down current when the pin is either set to 3.3V or GND, respectively. In the open state, the maximum pull-up or pull-down leakage current permissible is 10µA.

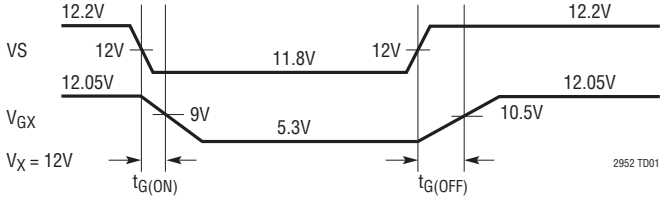
Note 9: The turn-on $\overline{KILL}$ blanking time is the waiting period immediately following the EN pin switching high; at the end of this period the input to the $\overline{KILL}$ needs to be high to indicate that the system has powered up properly, otherwise the EN pin is immediately switched low.

Note 10: The $\overline{KILL}$ wait time during the power-down process is the wait period immediately following a valid turn-off command until the EN pin switches low.

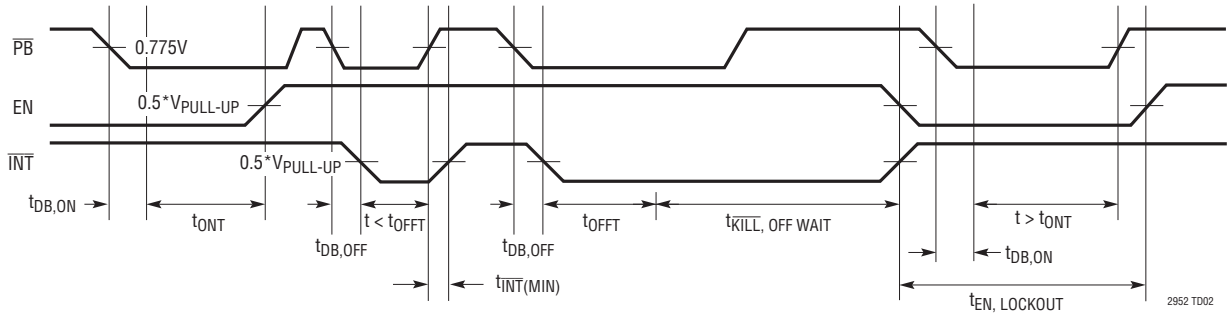
Note 11: The enable lockout time is the minimum wait time between the last falling edge and the next rising edge on the EN pin.

TIMING DIAGRAMS

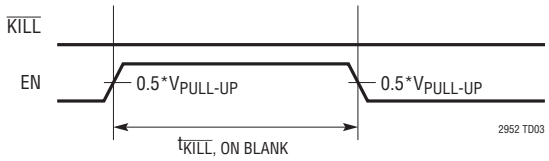
Ideal Diode Function – Gate Turn-On and Turn-Off Time



Pushbutton Debounce Times, $\overline{KILL}$ Wait Time and Enable Lockout Time with $\overline{KILL}$ Above Threshold

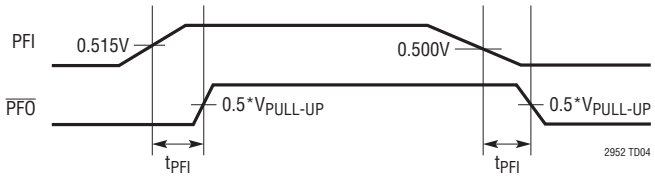


$\overline{KILL}$ On Blanking with $\overline{KILL}$ Below Threshold

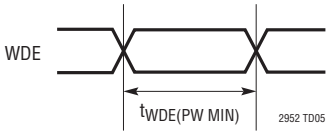


TIMING DIAGRAMS

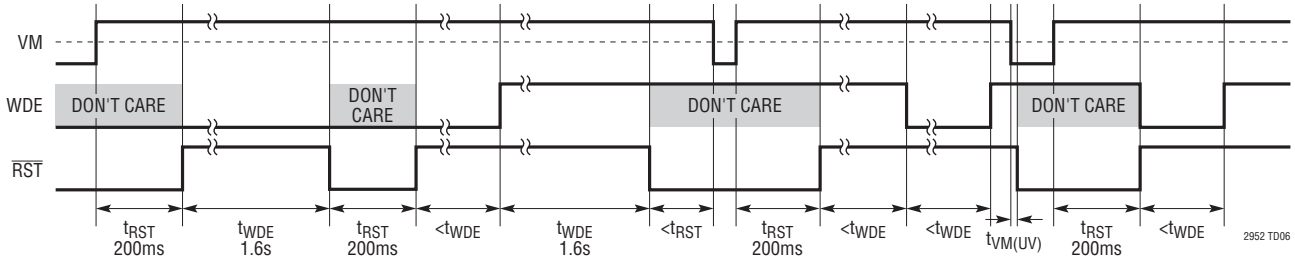
PFI and $\overline{PFO}$



WDE Minimum Pulse Width

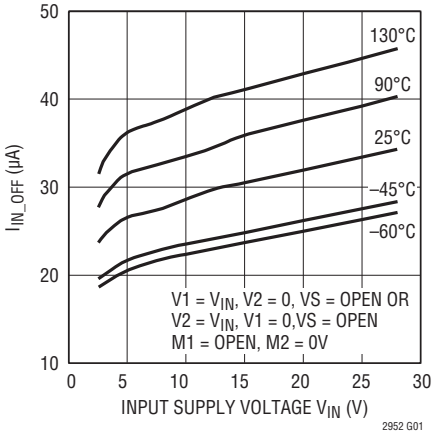


VM, WDE and $\overline{RST}$

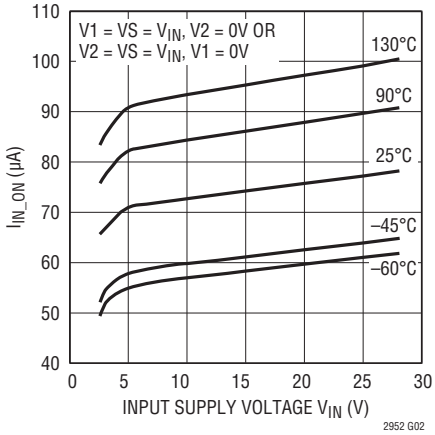


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

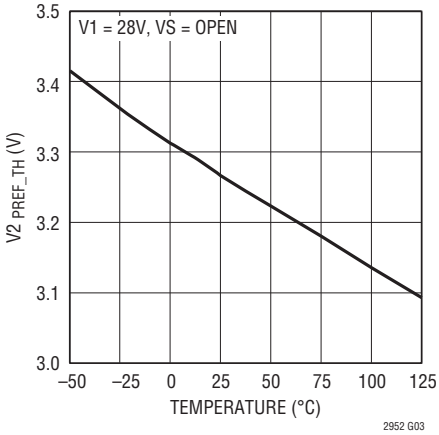
I_{IN-OFF} vs Input Supply Voltage at Different Temperatures



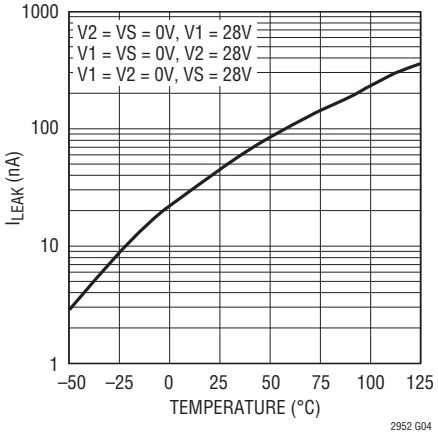
I_{IN-ON} vs Input Supply Voltage at Different Temperatures



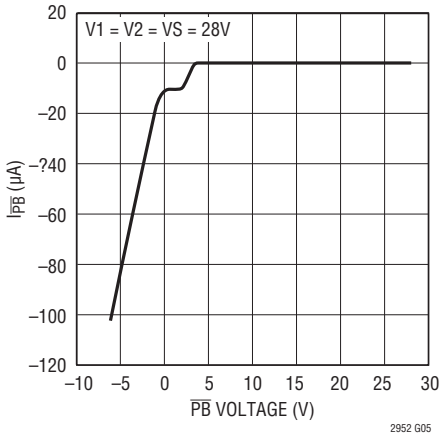
V2 Preferential Threshold vs Temperature



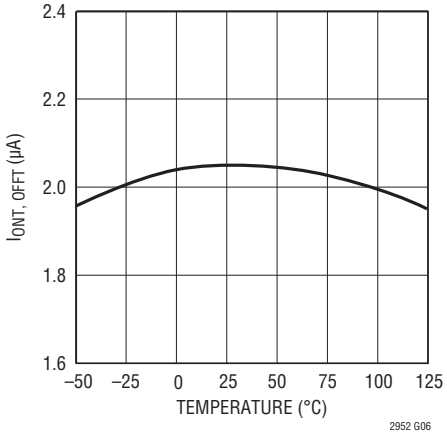
Worst Case Supply to Supply Leakage vs Temperature



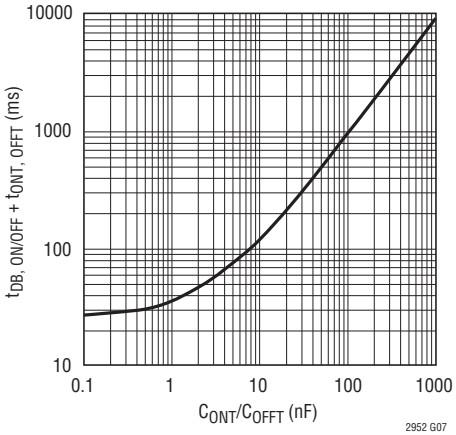
$\overline{PB}$ Current vs $\overline{PB}$ Voltage



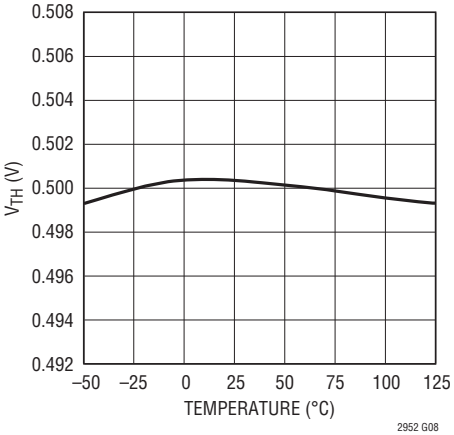
ONT/OFFT Pull-Up/Pull-Down Current vs Temperature



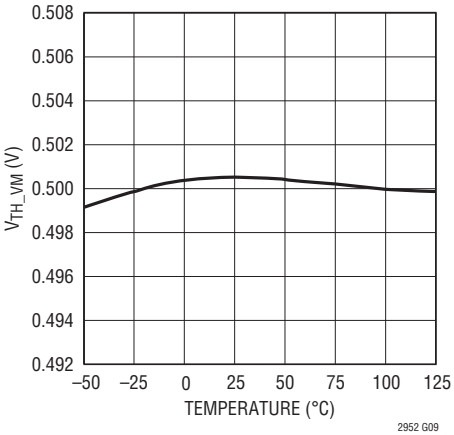
Total Turn-On/Turn-Off Time vs ONT/OFFT Capacitors Value



$\overline{KILL}$, PFI, M1 and M2 Falling Input Threshold Voltage vs Temperature



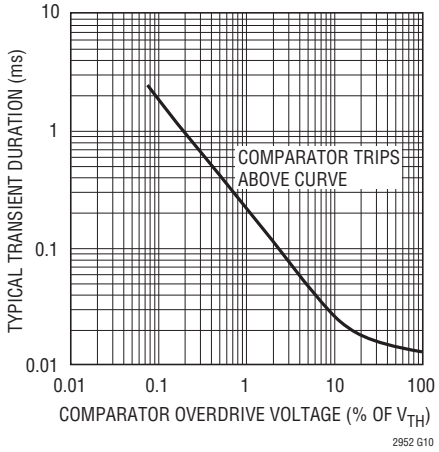
VM Input Reset Threshold Voltage vs Temperature



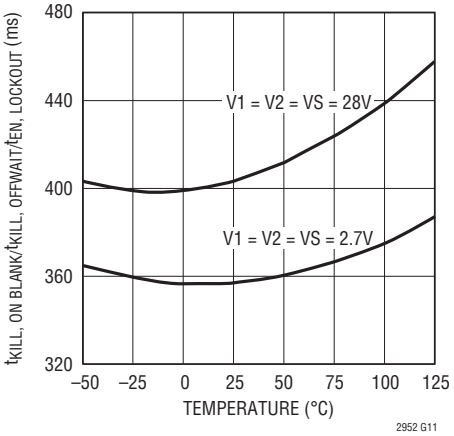
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

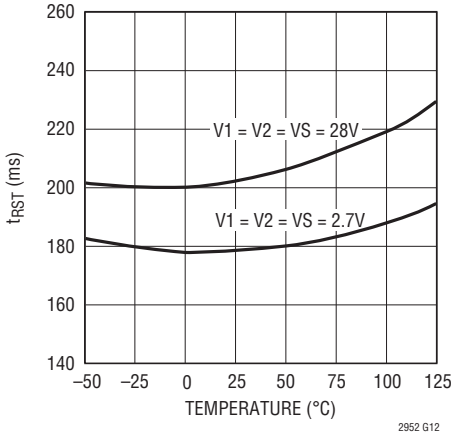
Typical Transient Duration vs Comparator Overdrive (VM, $\overline{KILL}$, PFI, M1 and M2)



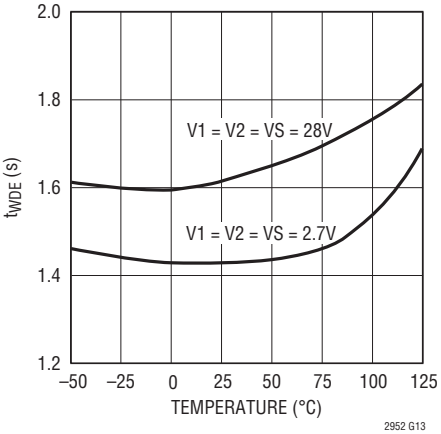
$\overline{KILL}$ On Blanking, $\overline{KILL}$ Wait Time, Enable Lockout Time vs Temperature at Different Input Voltages



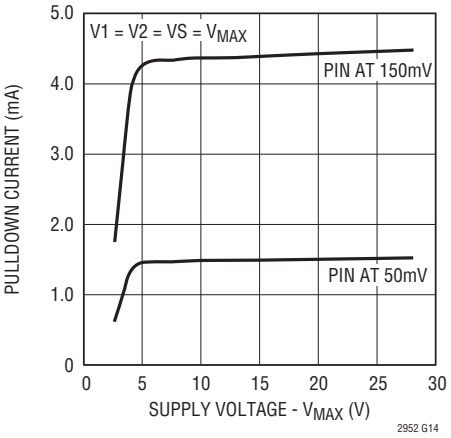
Reset Timeout Period vs Temperature at Different Input Voltages



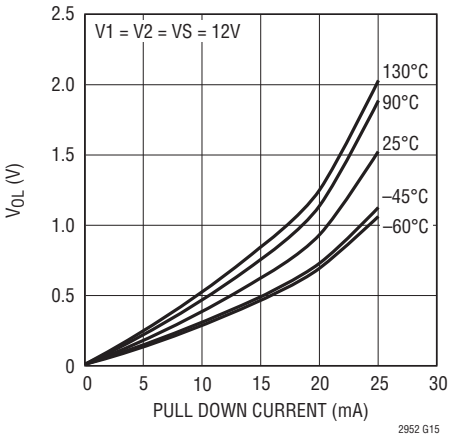
Watchdog Time Period vs Temperature at Different Input Voltages



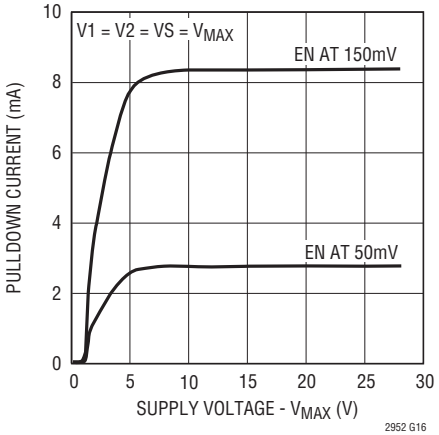
G1STAT, $\overline{PFO}$, $\overline{INT}$ and $\overline{RST}$ Pull-Down Current vs Supply Voltage



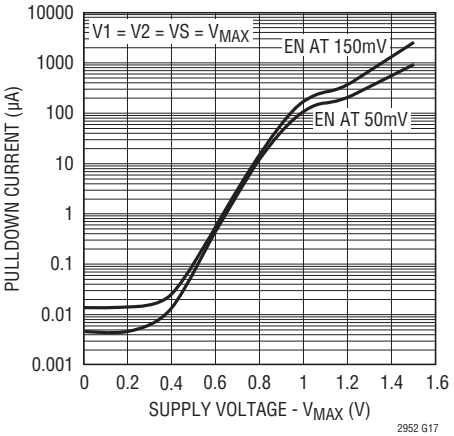
G1STAT, $\overline{PFO}$, $\overline{INT}$ and $\overline{RST}$ Voltage Output Low vs Pull-Down Current at Different Temperatures



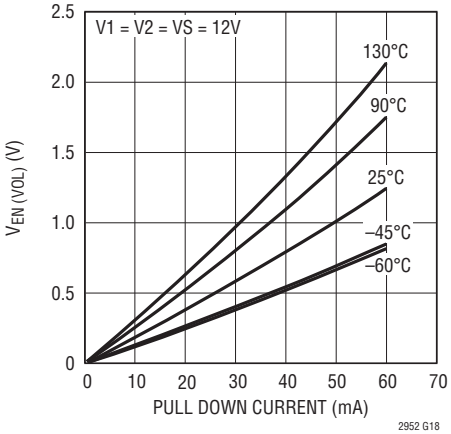
EN Pull-Down Current vs Supply Voltage



EN Pull-Down Current vs Supply Voltage



EN Voltage Output Low vs Pull-Down Current at Different Temperatures



PIN FUNCTIONS (TSSOP/QFN)

EN (Pin 14/Pin 11): DC/DC Enable Output. This pin is a high voltage open-drain pull-down used to control system power. EN pin goes high impedance after an initial turn-on command (via either the digital on or a valid pushbutton on—refer to the Applications Information section). EN pin pulls low at the end of a valid power-down sequence, or when $\overline{KILL}$ pin is driven low anytime after a valid power-up sequence.

Exposed Pad (Pin 21, QFN Package): The exposed pad may be left open or connected to device ground.

G1 (Pin 19/Pin 16): Primary P-Channel MOSFET Gate Drive Output. When the primary ideal diode function is enabled and in regulation, the ideal diode controller drives this pin to maintain a forward voltage (V_{FR}) of 20mV between the V1 and VS pins. When another power source is driving the VS pin, causing the voltage level at the VS pin to be greater than the voltage level at the V1 pin or when the primary ideal diode driver is disabled via the mode select input pins, this pin pulls up to the MAX (V1, VS) voltage, turning off the primary P-channel power switch. Leave this pin open when primary ideal diode function is not used.

G1STAT (Pin 20/Pin 17): Open-Drain Primary Ideal Diode Status Output. When the primary P-channel power switch is off, the G1STAT pin will go from an open state to a strong pull-down. This pin can be used to signal the state of the primary ideal diode PowerPath to a microcontroller. Leave this pin open or tied to GND when unused.

G2 (Pin 15/Pin 12): Secondary P-Channel MOSFET Gate Drive Output. When the secondary ideal diode function is enabled and in regulation, the ideal diode controller drives this pin to maintain a forward voltage (V_{FR}) of 20mV between the V2 and VS pins. When another power source is driving the VS pin, causing the voltage level at the VS pin to be greater than the voltage level at the V2 pin or when the secondary ideal diode driver is disabled via the mode select input pins, this pin pulls up to the MAX (V2, VS) voltage, turning off the secondary P-channel power switch. Leave this pin open when secondary ideal diode function is not used.

GND (Pin 12/Pin 9): Device Ground.

$\overline{INT}$ (Pin 13/Pin 10): Interrupt Output. This pin is an open-drain pull-down pin used to signal the system that a power shutdown is imminent. The $\overline{INT}$ pin asserts low 26ms after the initial falling edge of the pushbutton off event and during the power-down sequence. Leave this pin open or tied to GND if interrupt signal is unused.

$\overline{KILL}$ (Pin 3/Pin 20): System Power Shutdown Input. Setting this pin low asserts the EN pin low. In modes where M1 is above threshold, setting this pin low also shuts off the ideal diodes. During system turn-on, input to this pin is ignored until 500ms ($t_{\overline{KILL},ON\ BLANK}$) after the EN pin first becomes high impedance. This pin has an accurate 0.5V falling threshold and can be used as a voltage monitor input.

M1 (Pin 2/Pin 19): Mode Select Input 1. Input to an accurate comparator with 0.5V falling threshold and 15mV hysteresis. Has a 3µA internal pull-up to an internal supply (4V). Together with M2 determines the ideal PowerPath and on/off control behavior of the part. Refer to the Operation and Applications Information sections for configurations based on the voltage levels at M1 and M2.

M2 (Pin 1/Pin 18): Mode Select Input 2. High impedance input to an accurate comparator with 0.5V falling threshold and 15mV hysteresis. When M1 is low, M2 controls whether the primary (G1) ideal diode function is enabled. When M1 is high, M2 acts as a digital on/off control input: A rising edge on this pin is interpreted as a turn-on command and a falling edge is interpreted as a turn-off command. Refer to the Operation and Applications Information sections for configurations based on the voltage levels at M1 and M2.

OFFT (Pin 11/Pin 8): Off Timing Input. Attach 110pF of external capacitance (C_{OFFT}) to GND for each additional millisecond of turn-off debounce time beyond the internally set 26ms. Leave open if additional debounce time is not needed.

ONT (Pin 10/Pin 7): On Timing Input. Attach 110pF of external capacitance (C_{ONT}) to GND for each additional millisecond of turn-on debounce time beyond the internally set 26ms. Leave open if additional debounce time is not needed.

$\overline{PB}$ (Pin 7/Pin 4): Pushbutton Input. Input to a comparator with 0.775V falling threshold and 25mV hysteresis. $\overline{PB}$ has a 10µA internal pull-up to an internal supply (4V). This

PIN FUNCTIONS (TSSOP/QFN)

pin provides on/off power supply control via the EN pin, which is typically connected to an external DC/DC converter. Setting the $\overline{PB}$ pin low for a time determined by the ONT timing capacitor toggles the EN pin high impedance. Letting this pin toggle high and then setting this pin low again for 26ms asserts $\overline{INT}$ low. After the $\overline{INT}$ pin asserts low, if the $\overline{PB}$ pin is still held low for a time determined by the OFFT timing capacitor, the process of turning off the system power begins. At the end of the turn-off process, the EN pin is set low. Leave this pin open if pushbutton function is not used.

PFI (Pin 5/Pin 2): Power Fail Input. High impedance input to an accurate comparator with a 0.5V falling threshold and 15mV hysteresis. This pin controls the state of the $\overline{PFO}$ output pin. Tie to device GND if power fail monitoring function is not used.

$\overline{PFO}$ (Pin 9/Pin 6): Power Fail Output. This pin is an open-drain pull-down which pulls low when the PFI input is below 0.5V. Leave this pin open or tied to GND if power fail monitoring function is not used.

$\overline{RST}$ (Pin 8/Pin 5): Reset Output. This pin is an open-drain pull-down. Pulls low when VM input is below 0.5V and held low for 200ms after VM input is above 0.5V. Also pulls low for 200ms when the watchdog timer (1.6s) is allowed to time out. Leave this pin open or tied to GND if voltage monitoring function is not used.

V1 (Pin 18/Pin 15): Primary Input Supply Voltage: 2.7V to 28V. Supplies power to the internal circuitry and is the anode input of the primary ideal diode driver (the cathode input to the ideal diode drivers is the VS pin). A battery or other primary power source usually provides power to this input. Minimize the capacitance on this pin in applications where the pin can be high impedance (disconnected or inherent high source impedance). Otherwise, an optional bypass capacitor to ground in the range of 0.1µF to 10µF can be used.

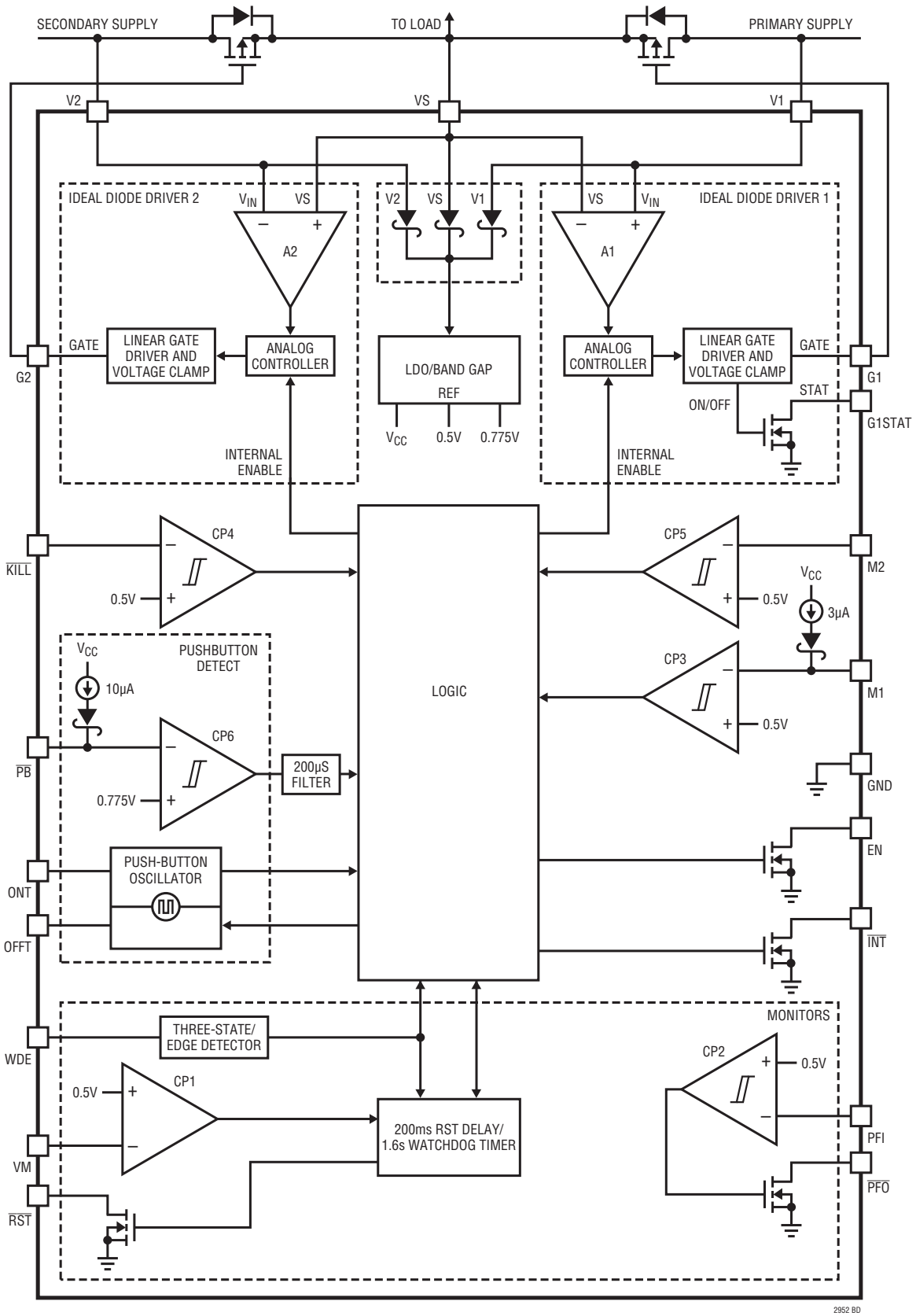
V2 (Pin 16/Pin 13): Secondary Input Supply Voltage: 2.7V to 28V. Supplies power to the internal circuitry and is the anode input of the secondary ideal diode driver (the cathode input to the ideal diode drivers is the VS pin). A secondary power source such as a wall adapter, usually provides power to this input. Minimize the capacitance on this pin in applications where the pin can be high impedance (disconnected or inherent high source impedance). Otherwise, an optional bypass capacitor to ground in the range of 0.1µF to 10µF can be used.

VM (Pin 4/Pin 1): Voltage Monitor Input. High impedance input to an accurate comparator with a 0.5V threshold. Together with the WDE pin controls the state of the $\overline{RST}$ output pin. Tie to device GND if voltage monitoring function is not used.

VS (Pin 17/Pin 14): Power Sense Input. This pin supplies power to the internal circuitry and is the cathode input to the ideal diode drivers (the anode inputs to the ideal diode drivers are the V1 and V2 pins). Bypass this pin to ground with one or more capacitors of at least 0.1µF.

WDE (Pin 6/Pin 3): Watchdog/Extend Input. A three-state input pin. A rising or falling edge must occur on this pin within a 1.6s watchdog timeout period (while the $\overline{RST}$ output is high impedance), to prevent the $\overline{RST}$ pin from going low. The watchdog function of this pin is disabled when both of the ideal diode drivers are disabled in certain PowerPath configurations (refer to the Application Information section). During a shutdown process: a rising or falling edge on this WDE pin within the 500ms $t_{\overline{KILL},OFF\ WAIT}$ period extends the waiting period another 500ms before the EN line is set low. This extend process can be repeated indefinitely in order to provide as much time as possible for the microprocessor to do its housekeeping functions before a power shutdown. Leave open or drive in Hi-Z state with a three-state buffer to disable watchdog or extend function or both.

BLOCK DIAGRAM



OPERATION

The LTC2952 is designed to simplify applications requiring management of multiple power sources. The three main features of the part are: pushbutton control, ideal diode PowerPath controllers and system monitoring. The Block Diagram on the previous page shows the part divided into its main functional blocks.

The pushbutton detect block is responsible for debouncing any pushbutton event on the $\overline{PB}$ pin. Note that the ON and OFF debounce times can be configured independently by using two separate capacitors on the ONT and OFFT pins respectively. A valid pushbutton on event will set the EN pin high impedance and a valid off event will drive the EN pin low.

In a typical application the EN pin is tied to the shutdown pin of a DC/DC converter. Therefore, by toggling the EN pin, the pushbutton pin has a direct control over the enabling/disabling of an external DC/DC converter. This control of system turn-on/off is done in a graceful manner which ensures proper system power-up and power-down.

The ideal diode drivers regulate two external P-channel MOSFETs to achieve low loss switchover between two DC sources. Each driver regulates the gate of the PFET such that the voltage drop across its source and drain is 20mV. When the load current is larger than the PFET ability to deliver such current with a 20mV drop across its source and drain, the voltage at the gate clamps at $V_{G(ON)}$ and the PFET behaves like a fixed value resistor.

Besides providing ideal diode PowerPath controllers and control of system power turn-on/off, the LTC2952 also provides system monitoring function via the VM, WDE, $\overline{RST}$ and PFI, $\overline{PFO}$ pins. The voltage monitoring (VM) and the watchdog (WDE) input pins determine the state of the $\overline{RST}$ output with 200ms reset time and 1.6s watchdog time. The PFI and $\overline{PFO}$ pins are the input and output of an accurate comparator that can be used as an early power fail monitor.

The $\overline{KILL}$, M1 and M2 pins are the inputs to accurate comparators with 0.5V threshold. The outputs of these comparators interact with the logic block to alter the ideal diode PowerPath controllers and the pushbutton control behavior. Specifically, the $\overline{KILL}$ input provides the system with a capability to turn off system power at any point during operation. The M1 and M2 pins are mode pins that configure the part to have different behaviors in the PowerPath switchover of the two DC sources.

Figure 1 shows the four different typical configurations of the LTC2952. In configuration A, both of the ideal-diode PowerPath controllers are always enabled which results in an automatic switchover between the two DC sources. configuration C is similar to A except for the pushbutton input which now controls both the EN pin and the ideal diode PowerPath controllers.

In configurations B and D, M2 is used as a voltage monitor. In B, when the M2 input is above its threshold the primary ideal diode PowerPath is disabled. In D, M2 needs to be above threshold before $\overline{PB}$ has control over the EN pin and the ideal diode PowerPath controllers. Furthermore in D, the rising and falling edges on M2 are interpreted as turn-on and turn-off commands, respectively.

OPERATION

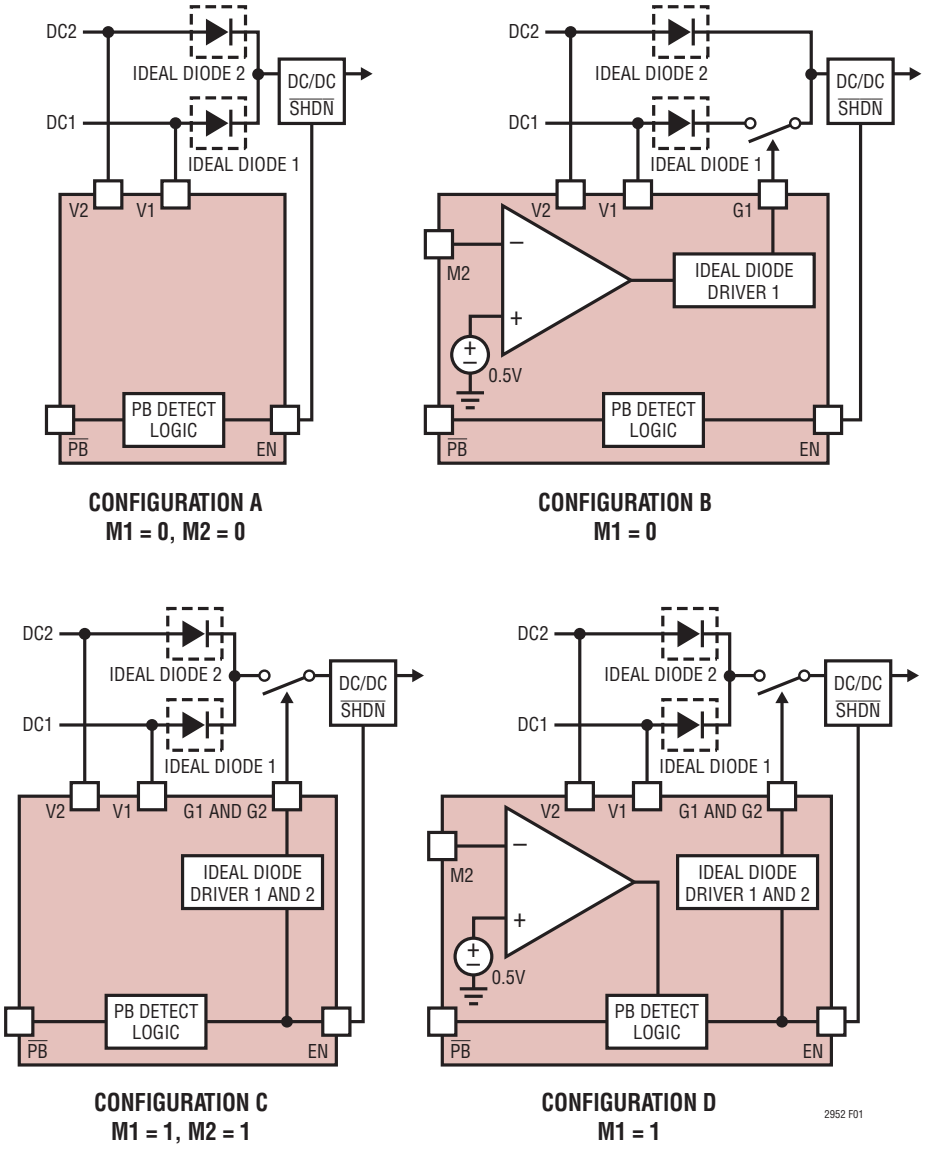


Figure 1. Four Different Typical PowerPath Configurations

APPLICATIONS INFORMATION

The LTC2952 is a versatile power management IC with pushbutton on/off control and system supervisory features. The power management function features ideal diode PowerPath control that provides low loss switchover between two DC sources. This PowerPath control behavior is configurable to satisfy various application requirements.

The LTC2952's pushbutton input has independently adjustable ON and OFF debounce times that control the toggling of a low leakage open-drain enable output and in some configurations, the ideal diode PowerPath operation. A simple interface allows for digital on/off control and proper system housekeeping prior to power-down.

The LTC2952 also features robust and accurate system supervisory functions that fit high reliability system applications. These supervisory functions include power-fail, voltage monitoring and watchdog reset functions which can be used to monitor power status and ensure system integrity.

The Ideal Diode Drivers

In a typical application, each of the ideal diode drivers is connected to drive an external P-channel MOSFET as shown in the Block Diagram and Figure 2. When power is available at V_{IN} and the ideal diode driver is enabled, the ideal diode driver regulates the voltage at the GATE to maintain a 20mV difference between V_{IN} and VS. As the load current varies, the GATE voltage is controlled to maintain the 20mV difference.

If the load current exceeds the external PFET's ability to deliver the current with a 20mV V_{DS}, then the voltage at the GATE clamps and the PFET behaves as a fixed resistor causing the forward voltage to increase slightly as the load current increases. When the VS pin is externally pulled up above the voltage level at V_{IN}, the ideal diode driver shuts the external PFET off to prevent reverse conduction. Thus when both the primary and secondary ideal diode drivers are enabled, the two ideal diode drivers work together to bring VS to within 20mV of the higher of either V1 or V2.

The G1STAT pin indicates the status of the primary ideal diode driver. If the external PFET connected to the primary driver is providing power to VS, the G1STAT pin is in a high impedance state and when the PFET connected to the primary driver is shut-off, the G1STAT pin pulls low.

PowerPath CONFIGURATIONS

Configuration A: Pushbutton Controller with Automatic Switchover Between WALL Adapter and Battery

In this particular configuration both of the M1 and M2 pins are connected to ground. These connections set up the LTC2952 to operate with both of the ideal diodes enabled all the time.

In this application, power from the VS node to the system is controlled through the EN pin connected to a shutdown

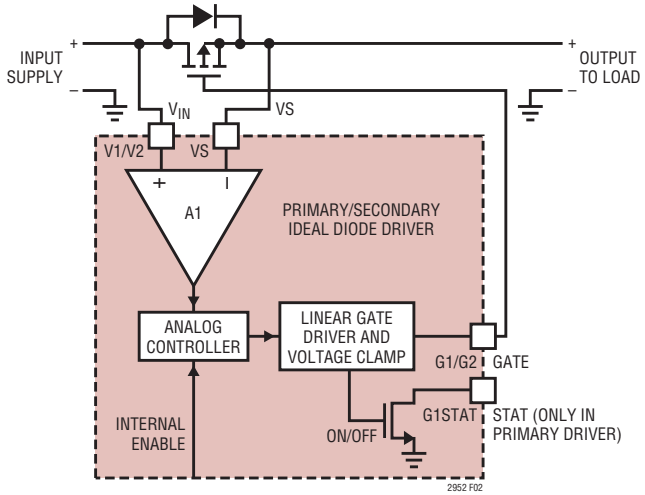


Figure 2. Detailed Ideal Diode Driver Functional Block Diagram

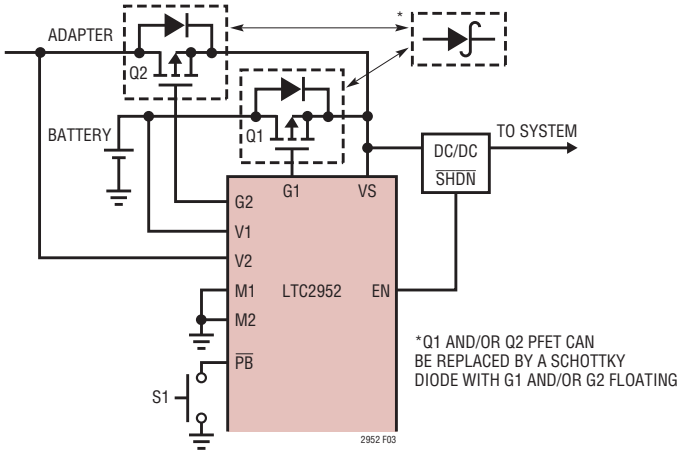


Figure 3. PowerPath Configuration A

APPLICATIONS INFORMATION

pin of a DC/DC converter. The $\overline{PB}$ input achieves PowerPath control by toggling this EN pin.

Note that in this application both of the ideal diodes are enabled all the time, therefore either Q1 or Q2 can be replaced by Schottky diodes as long as the voltage drop across the Schottky diodes and their reverse leakage currents are acceptable.

Configuration B: Pushbutton Controller with Preferential WALL Adapter Operation and Automatic Switchover to Battery

In this configuration (Figure 4) the M1 pin is connected to ground and the M2 pin is used as a monitor on the wall adapter input to alter the behavior of the ideal diode drivers. When the wall adapter voltage is below the trip threshold, both of the ideal diodes are enabled.

When the wall adapter voltage is above the trip threshold, the primary ideal diode driver is disabled (shutting off Q1 and Q3) and the secondary ideal diode driver is enabled (turning on Q2). This means the load current will be supplied from the wall adapter (V2) regardless of the voltage level at the battery (V1).

If the wall adapter voltage trip threshold is set lower than the battery input voltage level and the wall adapter input can go high impedance, the capacitance on V2 needs to be minimized. This is to ensure proper operation when the wall adapter goes high impedance and Q1, Q3 is instantly turned on.

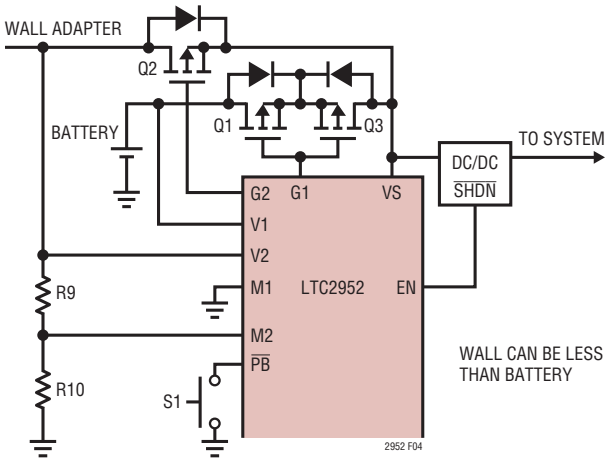


Figure 4. PowerPath Configuration B

Noting the possible current path through the PFET body diode, a back-to-back PFET configuration must be used for Q1, Q3 to make sure that no current will flow from the battery (V1) to the VS pin even if the wall adapter (V2) voltage is less than the battery (V1) voltage.

Configuration C: Pushbutton Control of Ideal Diode Drivers

In this configuration the M2 pin is tied to the M1 pin. Since the M1 pin has a 3µA internal pull-up current, this current causes both M1 and M2 to pull high. This allows the $\overline{PB}$ pin to have complete control of both the ideal diode drivers and the EN pin.

The first valid pushbutton input turns on both of the ideal diode drivers causing the VS pin to be driven to the higher of either the wall adapter or the battery input – providing power to the system directly. Conversely, a valid pushbutton off input turns off the ideal diodes after the shutdown sequence involving an interrupt to the system.

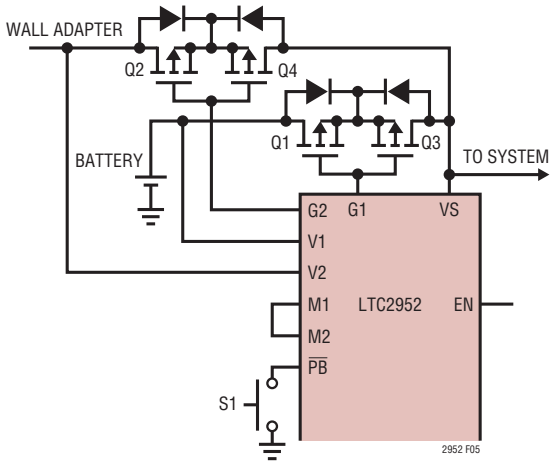


Figure 5. PowerPath Configuration C

Configuration D: Battery Backup with Pushbutton PowerPath Controller

In this configuration shown in Figure 6, the M1 pin is left floating allowing its own 3µA internal pull-up to pull itself above threshold. With M1 high, the device operates such that rising and falling edges on the M2 pin are interpreted as digital on and off commands respectively.

In Figure 6, the M2 pin monitors the wall adapter voltage. When power is first applied to the wall adapter so that the voltage at the M2 pin rises above its rising trip threshold

APPLICATIONS INFORMATION

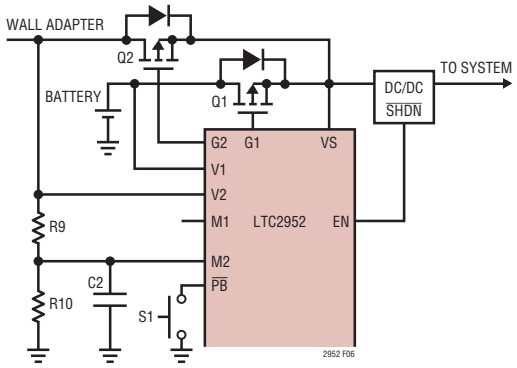


Figure 6. PowerPath Configuration D

(0.515V), both of the ideal diode drivers and the DC/DC converter are enabled. Thus, power is delivered to the system.

As soon as the wall adapter voltage falls below its trip threshold, a shutdown sequence is immediately started. At the end of the shutdown sequence, the ideal diode drivers and the DC/DC converter are disabled. Thus, power is cut off from the load and the system is in shutdown.

Note that once power is delivered to the system, the $\overline{PB}$ pin can be used to turn off the power. If $\overline{PB}$ is used to turn off the power in this configuration, there are two methods to turn the power back on: a valid pushbutton on event at the $\overline{PB}$ pin or a recycling of the wall adapter voltage (bringing the voltage level at the M2 pin down below and then back up above its threshold – a digital on command).

Also note that in this application, the voltage threshold of the wall adapter input (being monitored at the M2 pin) is usually set higher than the battery input voltage. Therefore, the only time when power is drawn from the battery (V1 pin) to the load is during the shutdown sequence when the voltage at the wall adapter input (V2 pin) has collapsed below the battery input voltage level.

Reverse Battery Protection

To protect the LTC2952 from a reverse battery connection, place a 1k resistor in series with the respective supply pin intended for battery connection (V1 and/or V2) and remove any capacitance on the protected pin. Figure 7 shows a configuration with a reverse battery protection on the V1 pin. This resistor will limit the amount of current that flows out of the V1 pin when a battery is connected in reverse and protect the part.

Note however, this reverse battery protection resistor should not be too large in value since the V1 and V2 pins are also used as the anode sense pins of the ideal diode drivers. When the ideal diode driver is on, the VS pin supplies most of the quiescent current of the part (60µA typ) and the supply pin supplies the remaining quiescent current (20µA typ). Therefore, the recommended 1k reverse battery protection resistor amounts to an additional 20mV (1k • 20µA) drop across the P-channel MOSFET.

In Figure 7, when the battery voltage is larger than the wall adapter voltage, the battery supplies the load current to the DC/DC converter. The ideal diode driver regulates G1 to maintain a fixed voltage drop from V1 to VS of 20mV (typ). Since there is a 20mV drop across the reverse battery protection resistor (R1) then the regulated voltage drop from the battery to the VS pin is 40mV (typ).

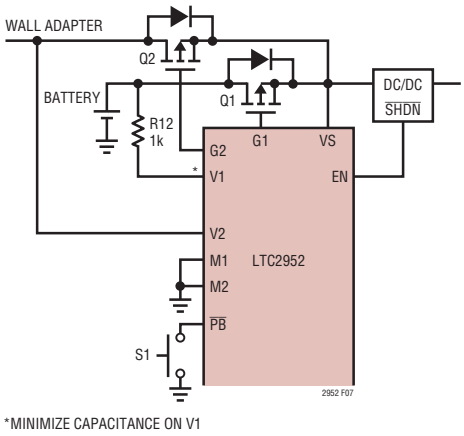


Figure 7. Reverse Battery Protection on V1

Pushbutton Input and Circuitry

The $\overline{PB}$ pin is a high impedance input to an accurate comparator with a 10µA pull-up to an LDO regulated internal supply of 4V. The $\overline{PB}$ input comparator has a 0.775V falling trip threshold with 25mV hysteresis. Protection circuitry allows the $\overline{PB}$ pin to operate over wide range from –6V to 28V with an ESD HBM rating of ±8kV.

The pushbutton circuitry debounces the input into the $\overline{PB}$ pin that sets an internal ON/OFF signal. This signal initiates a turn ON/OFF power sequence.

APPLICATIONS INFORMATION

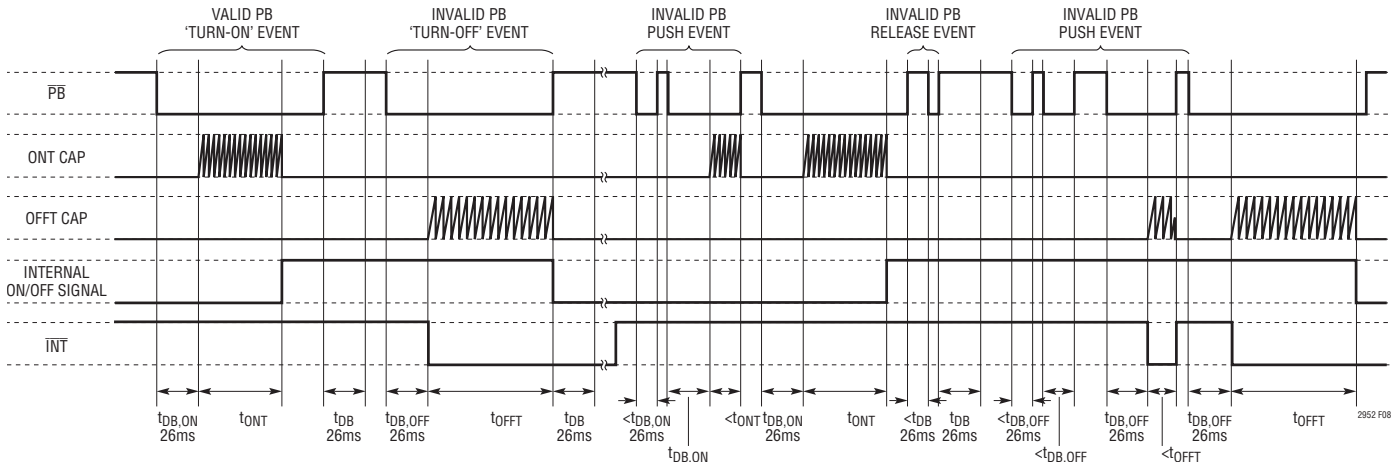


Figure 8. Pushbutton Debounce Timing Diagram

The timing diagram in Figure 8 shows the $\overline{PB}$ pin being debounced and setting an internal ON/OFF signal. Note that a high at the internal ON/OFF signal indicates that the last event was a turn-on command and a low at the internal ON/OFF signal indicates that the last event was a turn-off command. Here specifically the turn-on command is a result of a pushbutton on event and the turn-off command is a result of a pushbutton off event.

Note that a complete pushbutton consists of a push event and a release event. The push event (falling edge) on and off debounce durations on the $\overline{PB}$ pin can be increased beyond the fixed internal 26ms by placing a capacitor on the ONT and OFFT pins respectively. The following equations describe the additional debounce time that a push event at the $\overline{PB}$ pin must satisfy before it is recognized as a valid pushbutton on or off.

$$t_{ONT} = C_{ONT} \bullet (9.3M\Omega)$$

$$t_{OFFT} = C_{OFFT} \bullet (9.3M\Omega)$$

C_{ONT} and C_{OFFT} are the ONT and OFFT external programming capacitors respectively.

Note that during the push event of the pushbutton off, the $\overline{INT}$ pin is asserted low after the initial 26ms debounce duration. The $\overline{INT}$ pin asserts low when the $\overline{PB}$ pin is held low during the OFFT debounce duration and during the shutdown sequence. If the $\overline{PB}$ pin pulls high before the OFFT time ends, the $\overline{INT}$ pin immediately turns high impedance. On the other hand, if the $\overline{PB}$ pin is still held low at the end of the OFFT time, the $\overline{INT}$ pin continues to assert low throughout the ensuing shutdown sequence.

On a release event (rising edge) of the pushbutton switch following a valid push event, the $\overline{PB}$ pin must be continuously held above its rising threshold (0.8V) for a fixed 26ms internal debounce time.

In a typical application, the $\overline{PB}$ pin is connected to a pushbutton switch. If the switch exhibits high leakage current (>10µA), connecting an external pull-up resistor to V1, V2 and/or VS (depending on the application) is recommended. Furthermore, if the pushbutton switch is physically located far from the LTC2952's $\overline{PB}$ pin, signals may couple onto the high impedance $\overline{PB}$ input. Placing a 0.1µF capacitor from the $\overline{PB}$ pin to ground reduces the impact of signal coupling. Additionally, parasitic series inductance may cause undesirable ringing at the $\overline{PB}$ pin. This can be minimized by placing a 5k resistor in series and located next to the switch.

APPLICATIONS INFORMATION

Accurate Comparator Input Pins VM, PFI, $\overline{KILL}$, M1 and M2

VM, PFI, $\overline{KILL}$, M1 and M2 are high impedance input pins to accurate comparators with a falling threshold of 0.500V. Note the following differences between some of these pins: the VM pin comparator has no hysteresis while the other comparators have 15mV hysteresis and the M1 pin has a 3µA pull-up current while the other input pins do not.

Figure 9 shows the configuration of a typical application when VM, PFI, $\overline{KILL}$ or M2 pin connects to a tap point on an external resistive divider between a positive voltage and ground.

Calculate the falling trip voltage from the resistor divider value using:

$$V_{FALLING-TRIP} = 0.5V\left(1+\frac{R1}{R2}\right)$$

Table 1 shows suggested 1% resistor values for various applications.

Table 1. Suggested 1% Resistor Values for the Accurate Comparators (–6.5% Nominal Threshold)

V_{SUPPLY} (V)	V_{TRIP} (V)	R1 (kΩ)	R2 (kΩ)
12	11.25	2150	100
10	9.4	1780	100
8	7.5	1400	100
7.5	7	1300	100
6	5.6	1020	100
5	4.725	845	100
3.3	3.055	511	100
3	2.82	464	100
2.5	2.325	365	100
1.8	1.685	237	100
1.5	1.410	182	100
1.2	1.120	124	100
1.0	0.933	86.6	100
0.9	0.840	68.1	100
0.8	0.750	49.9	100
0.7	0.655	30.9	100
0.6	0.561	12.1	100

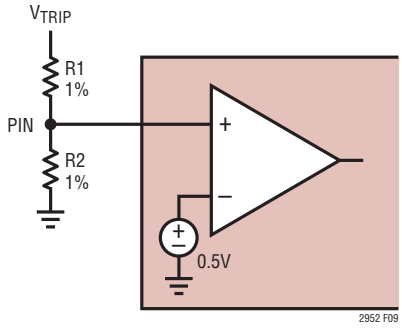


Figure 9. Setting the Comparator Trip Point

In a typical application the M1 pin is usually either connected to ground or left floating. When left floating, the internal 3µA pull-up drives the M1 pin high above its rising threshold (0.515V). Note that this 3µA pull-up current can be used to pull up any or all of the other high impedance input pins. For example, connect the M2 pin to the M1 pin to pull both up above their rising thresholds, as shown in Figure 5.

The Voltage Monitor and Watchdog Function

The first voltage monitor input is PFI. As mentioned before, this pin is a high impedance input to an accurate comparator with 15mV hysteresis. When the voltage at PFI is higher than its rising threshold (0.515V), the $\overline{PFO}$ pin is high impedance. Conversely, when the voltage level at PFI is lower than its falling threshold (0.500V), the $\overline{PFO}$ pin strongly pulls down to GND.

The second voltage monitor input is VM. The VM pin together with the WDE pin (acting as a watchdog monitor pin) affects the state of the $\overline{RST}$ output pin. The VM pin is also a high impedance input to an accurate comparator. However, the VM comparator has no hysteresis and hence the same rising and falling threshold (0.500V).

When the voltage level at VM is less than 0.5V, the $\overline{RST}$ pin strongly pulls down to GND. When the voltage level at VM first rises above 0.5V, the $\overline{RST}$ output pin is held low for another 200ms (t_{RST}) before turning high impedance.

After the $\overline{RST}$ pin becomes high impedance, if the WDE input pin is not left in a Hi-Z state, the watchdog timer is started. The watchdog timer is reset every time there is an edge (high to low or low to high transition) on the

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WDE pin. The watchdog timer can expire due to any of the following conditions:

1. No valid edge on the WDE pin in a t_{WDE} (1.6s) time period after the $\overline{RST}$ pin transitions from pulling low to high impedance.
2. No valid edge on the WDE pin in a t_{WDE} (1.6s) time period since the last valid edge on the WDE pin while the $\overline{RST}$ pin is high impedance.

As shown in the Timing Diagrams section, when the watchdog timer is allowed to expire while voltage at the VM pin is higher than 0.5V, the $\overline{RST}$ pin strongly pulls down to ground for t_{RST} (200ms) before again becoming high impedance for t_{WDE} (1.6s). This will continue unless there is an edge at the WDE pin, the voltage at VM goes below 0.5V, or the watchdog function is disabled (by leaving the WDE in a Hi-Z state).

In certain PowerPath configurations where both of the ideal diode drivers are disabled, the watchdog function of the WDE pin is also disabled. Examples of such configurations are configuration C (Figure 5) and configuration D (Figure 6) when both of the ideal diode can be turned off due to a valid pushbutton off or a digital off command.

Power-On/Power-Off Sequence

Figure 10 shows a normal power-on and power-off timing diagram. Note that in this timing diagram only the clean internal ON/OFF signal is shown. A transition at this internal ON/OFF signal can be caused by a valid debounced pushbutton ON/OFF or a digital ON/OFF through the mode input pins (M1/M2).

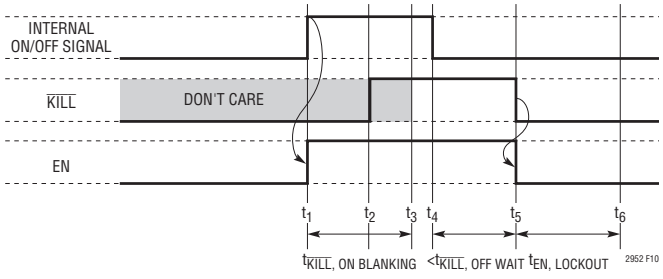

Figure 10. Power-On and Power-Off Sequence with $\overline{KILL}$ Deasserting EN During $\overline{KILL}$ Off Wait Time

In this timing sequence, the $\overline{KILL}$ pin has been set low since power is first applied to the LTC2952. As soon as the internal ON/OFF signal transitions high (t_1), the EN pin goes high impedance and an internal 500ms ($t_{\overline{KILL},\ ON\ BLANK}$) timer starts. During this 500ms $\overline{KILL}$ On Blanking period, the input to $\overline{KILL}$ pin is ignored and the EN pin remains in its high impedance state. This $\overline{KILL}$ On Blanking period is designed to give the system sufficient time to power up properly.

Once the µP/system powers on, it sets the $\overline{KILL}$ pin high (t_2) indicating that proper power-up sequence is completed. Failure to set $\overline{KILL}$ pin high at the end of the 500ms $\overline{KILL}$ On Blanking time (t_3) will result in immediate system shutdown (see Aborted Power-On Sequence segment). After the $\overline{KILL}$ On Blanking time expires, the system is now in normal operation with power turned on.

When the internal ON/OFF signal transitions low (t_4), a shutdown sequence is immediately started. From the start of the shutdown sequence, the system power will turn off in 500ms ($t_{\overline{KILL},\ OFF\ WAIT}$), unless an edge (a high-to-low or low-to-high transition) at the WDE pin is detected within the 500ms period to extend the wait period for another 500ms.

This $\overline{KILL}$ Off Wait time (500ms/cycle) is designed to allow the system to finish performing its housekeeping tasks before shutdown. Once the µP finishes performing its power-down operations, it can either let the 500ms $\overline{KILL}$ Off Wait time expire on its own or set the $\overline{KILL}$ pin low (t_5) immediately terminating the $\overline{KILL}$ Off Wait time. When the $\overline{KILL}$ Off Wait time expires, the LTC2952 sets EN low, turning off the DC/DC converter connected to the EN pin.

When the DC/DC converter is turned off (EN goes low), it can take a significant amount of time for its output level to decay to ground. In order to guarantee that the µP has always powered down properly before it is restarted, another 500ms (Enable Lockout time, $t_{EN,\ LOCKOUT}$) timer is started to allow for the DC/DC converter output power level to power down completely to ground. During this Enable Lockout time, the EN pin remains in its low state.

At the end of the 500ms Enable Lockout time (t_6), the LTC2952 goes into its reset state with the EN pin remains strongly pulling down.

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Aborted Power-On Sequence

The power-on sequence is aborted when the µP fails to set the $\overline{KILL}$ pin high before the 500ms $\overline{KILL}$ On Blanking time expires, as shown in the timing diagram in Figure 11. When the $\overline{KILL}$ On Blanking timer expires (t_7), the $\overline{KILL}$ pin is still low indicating that the µP/system has failed to power on successfully. When the system failed to set the $\overline{KILL}$ pin high within the specified 500ms time window, the LTC2952 pulls the EN pin low (thus turning off the DC/DC converter) and as a side effect resets the internal ON/OFF signal.

$\overline{KILL}$ Power Turn-Off During Normal Operation

Once the system has powered on and is operating normally, the system can turn off power by setting $\overline{KILL}$ low, as shown in the timing diagram in Figure 12. At t_9, $\overline{KILL}$ is set low and this immediately causes the LTC2952 to pull EN low, turning off the DC/DC converter.

Extended Power During Turn-Off

In the shutdown process, the availability of power can be extended by providing edges to the WDE pin during the $\overline{KILL}$ Off Wait time. The timing diagram in Figure 13 is similar to the power-on/power-off sequence timing diagram (Figure 10) except for the edges on the WDE pin during the shutdown process. At time t_{10}, the internal ON/OFF signal transitions low. When this happens, the DC/DC converter providing power to the system will be shut off in 500ms unless the WDE pin is toggled.

When the WDE pin transitions at t_{11}, the LTC2952 resets the 500ms $\overline{KILL}$ Off Wait timer. Before this second 500ms wait time expires, the WDE pin transitions again (this time from high to low) at t_{12}, causing the 500ms timer to reset again. Finally, the third 500ms timer which starts at t_{12} expires without any further extension at t_{13} causing the EN pin to go low, shutting down the DC/DC converter.

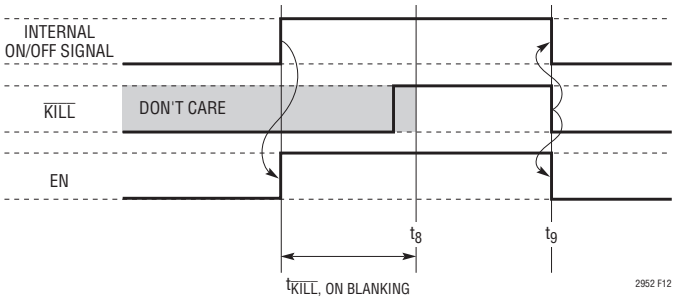


Figure 12. $\overline{KILL}$ Initiated Shutdown

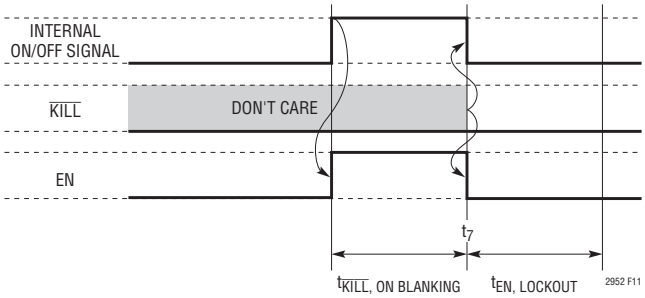


Figure 11. Aborted Power-On Sequence

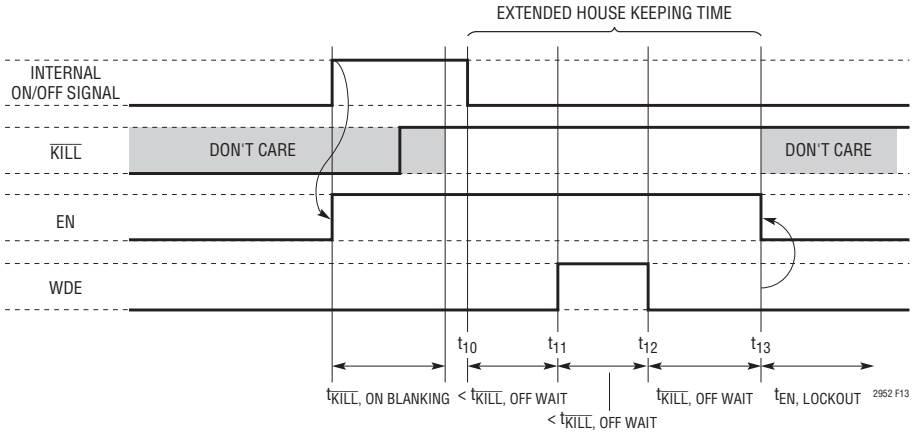


Figure 13. Power-On/Power-Off Sequence with Extended Shutdown/Housekeeping Wait Time

APPLICATIONS INFORMATION

Setting Up Different Configurations

The various configurations discussed previously are summarized in Table 2, including the ideal diode PowerPath state (ID1-primary, ID2-secondary). Note that an input above 0.515V (typical rising threshold) on the M1 and M2 pins is indicated with a 1 and an input below 0.500V (typical falling threshold) is represented by a 0. Also, an enabled ideal diode driver is indicated with a 1 and a disabled driver is indicated with a 0.

Table 2. Mode Table

MODE	DESCRIPTION	M1	M2	EN	ID1	ID2
0	Both Diodes Enabled	0	0	0	1	1
1	Both Diodes Enabled	0	0	1	1	1
2	Primary Diode Off, Secondary Diode On	0	1	0	0	1
3	Primary Diode Off, Secondary Diode On	0	1	1	0	1
4	PowerPath Off, PB Overwrite	1	0	0	0	0
5	Transitional PowerPath Off, PB Overwrite	1	0	1	1	1
6	Pushbutton PowerPath Off	1	1	0	0	0
7	Pushbutton PowerPath On	1	1	1	1	1

In addition to the mode table, the mode transition diagram in Figure 14 shows all possible interactions between the events on the pins ($\overline{PB}$, M1 and M2) and the different modes of the LTC2952 PowerPath behavior. Using Table 2 and Figure 14, it is possible to configure the LTC2952 in many different ways beyond the four discussed in the Operation and Applications Information sections.

In modes 0 and 1, both of the ideal diode drivers are enabled all the time. A valid pushbutton toggles the mode between 0 and 1 (changing the state of the EN pin) without ever turning off of the ideal diodes. These modes are used in configuration A and B (Figures 3 and 4).

In modes 2 and 3, only V2 provides power to the load connected at VS because the primary ideal diode driver is disabled and only the secondary ideal diode driver is enabled. These modes are used in configuration B (Figure 4).

In modes 4 and 5 both of the ideal diodes are disabled and the input to the $\overline{PB}$ pin is ignored. Note that mode 5 is a transitional mode. If there is no change at the M1 and M2 pin while in mode 5, the mode eventually transitions into mode 4 after a proper shutdown sequence.

A rising edge at M1 in mode 1 or a falling edge at M2 in mode 7 is recognized as a digital off command, which causes a transition to mode 5. When a digital off command is received, the EN pin is driven low and the ideal diodes are disabled after a proper shutdown sequence involving the interrupt alert to the µP ($\overline{INT}$ pin driven low)—refer to the earlier sections for details on the shutdown sequence.

Note that since the $\overline{PB}$ input is ignored in both mode 4 and 5, the only way to turn on the PowerPath from these two modes is a transition from 0 to 1 at the M2 pin. A transition from 0 to 1 at the M2 pin in modes 4 or 5 is interpreted as a digital on command. This digital on command causes the mode to transition from mode 4 or 5 to mode 7. In mode 7, both of the ideal diodes are enabled and the EN pin goes high impedance. Modes 4, 5 and 7 are used in configuration D (Figure 6).

Notice that in mode 7, both the M2 pin and the $\overline{PB}$ pin have direct control over the EN pin. A transition from 1 to 0 at the M2 pin in mode 7 is recognized as a digital off command. This digital off command causes a transition to mode 4 after a proper shutdown sequence. On the other hand, a valid pushbutton off mode 7 transitions the part to mode 6 after a proper shutdown sequence. In both mode 4 and mode 6 the EN pin is driven low. Modes 6 and 7 are used in configuration C (Figure 5).

In mode 4 the ideal diode driver circuitry is disabled, the EN pin is driven low, and the PB input is ignored. On the other hand, in mode 6, although both of the primary and secondary ideal diodes are disabled and the EN pin is set low, the PB input is not ignored. A valid pushbutton transitions the part from mode 6 to mode 7, turning on both the ideal diodes and setting the EN pin high impedance (turning on the DC/DC converter).

APPLICATIONS INFORMATION

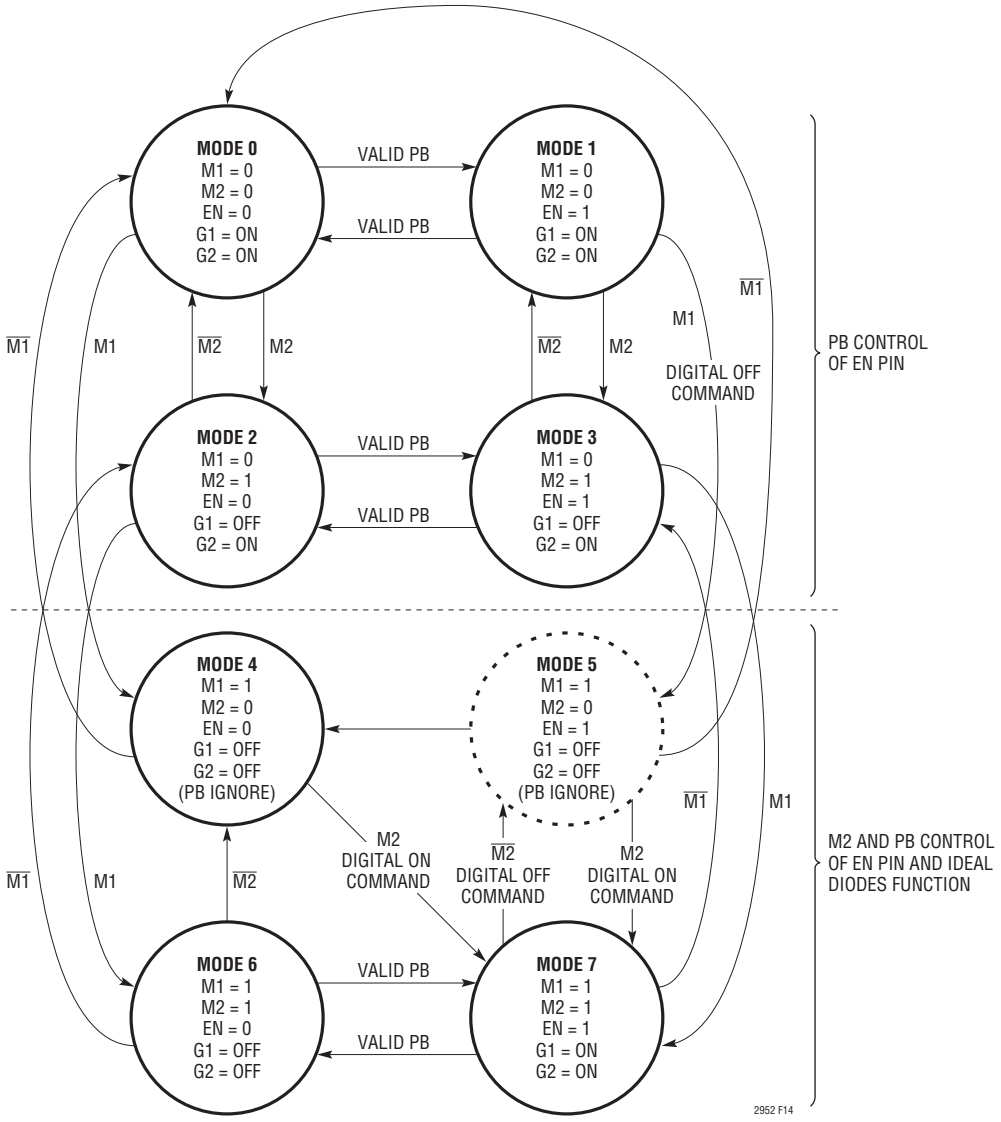
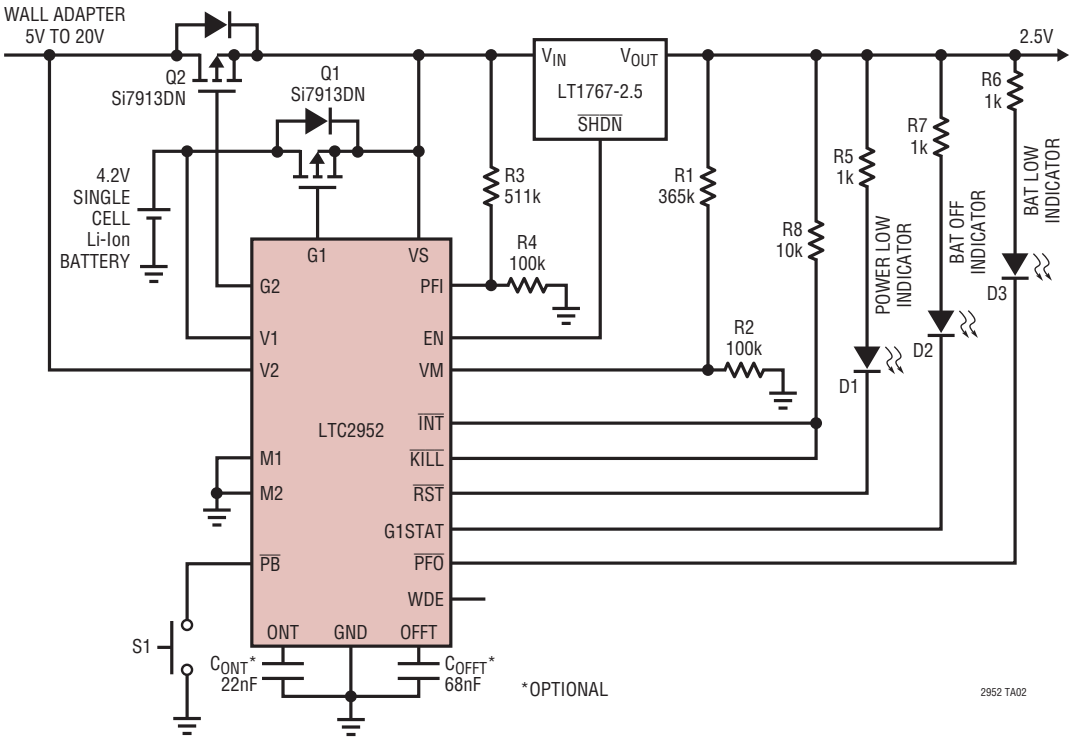


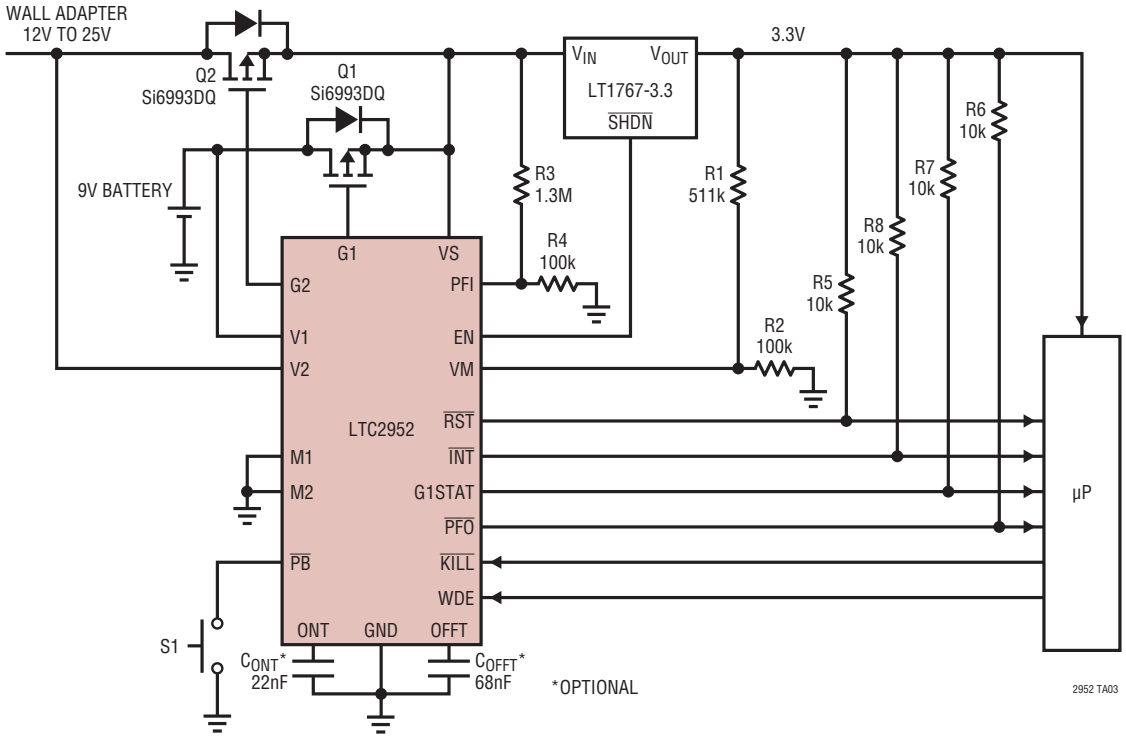
Figure 14. Mode Transition Diagram

TYPICAL APPLICATIONS

Wall Adapter and Battery Automatic Load Switchover with Simple On/Off Pushbutton Control and Voltage Monitors for System Power without µP

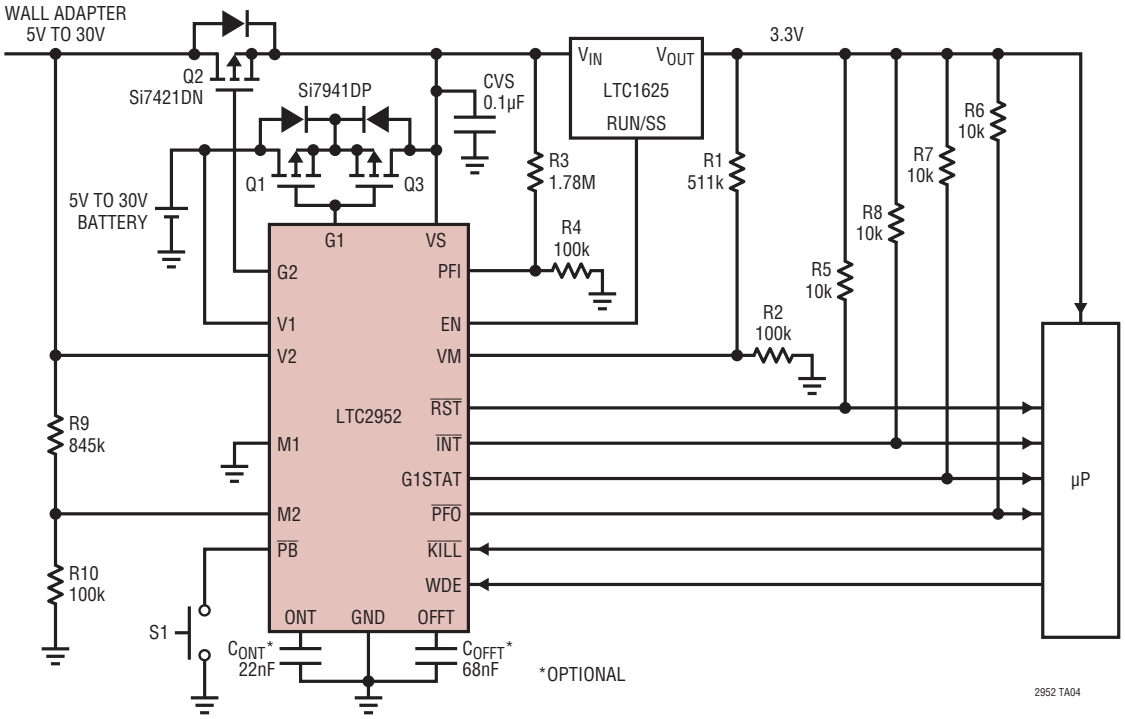


Wall Adapter and Battery Automatic Load Switchover with Pushbutton Control, Voltage Monitors and Watchdog

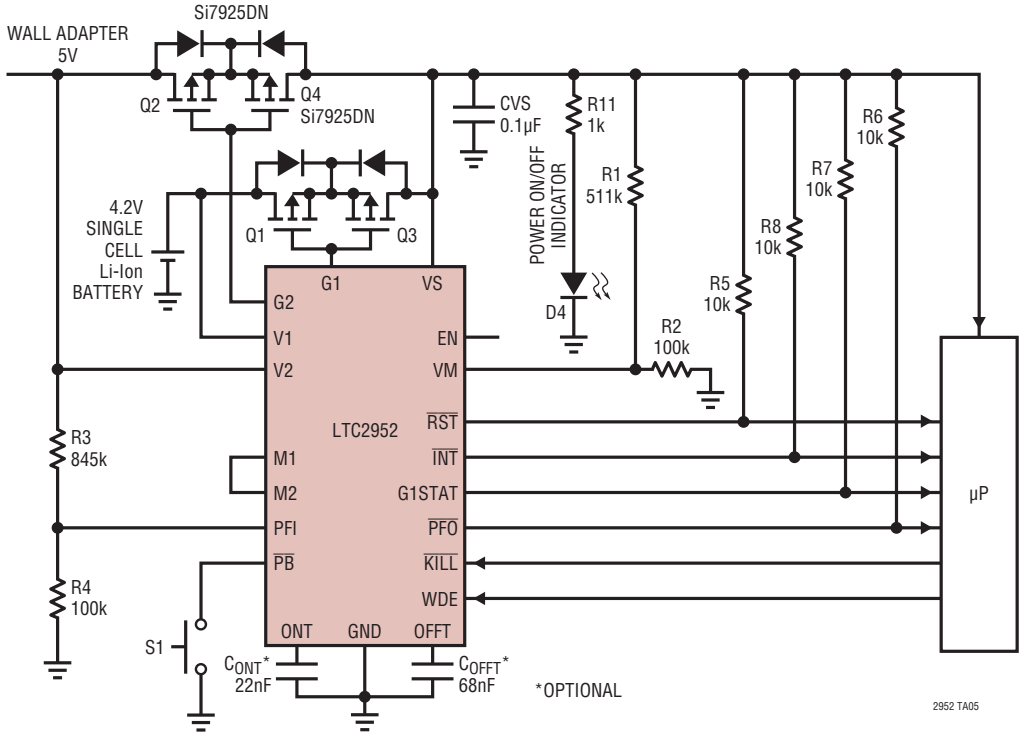


TYPICAL APPLICATIONS

Uninterruptible Power Supply with Preferential Wall Adapter Operation and Automatic Load Switchover to Battery with Pushbutton Control, Voltage Monitors and Watchdog

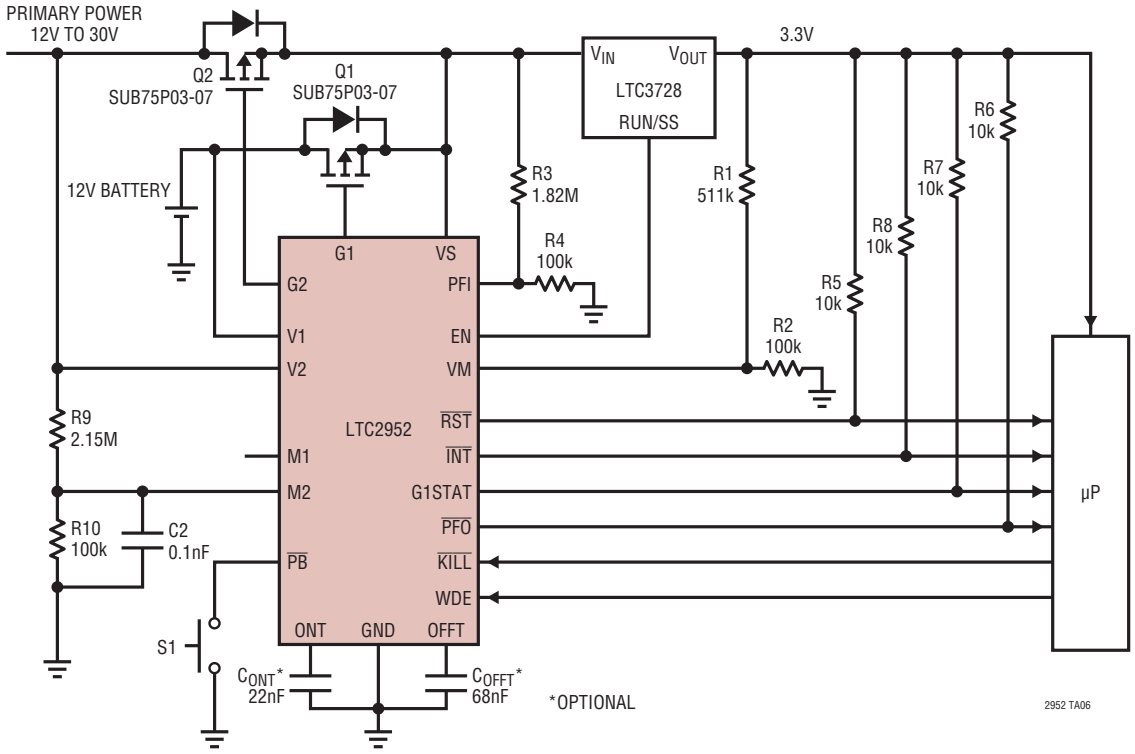


Direct PowerPath Control with Pushbutton Control, Voltage Monitors and Watchdog



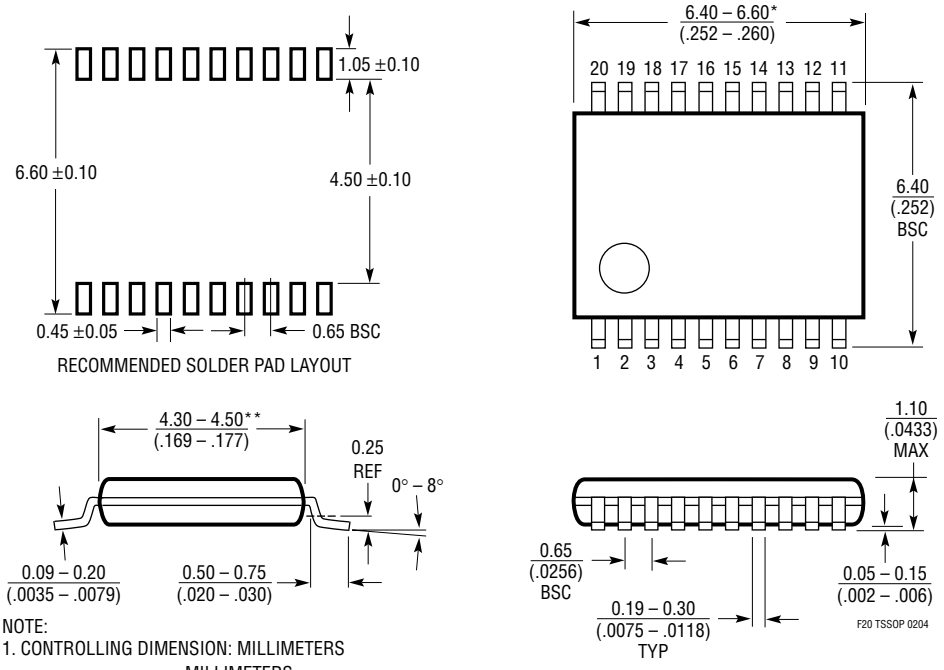
TYPICAL APPLICATIONS

Critical System with Primary Supply and Temporary Battery Backup with Pushbutton Control, Voltage Monitors and Watchdog



PACKAGE DESCRIPTION

F Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1650)



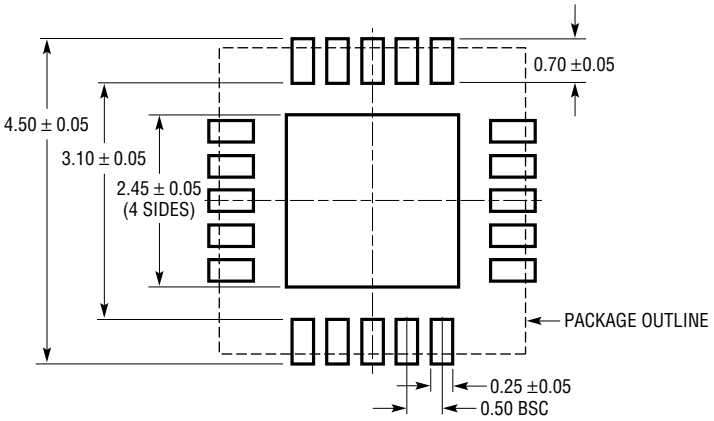
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

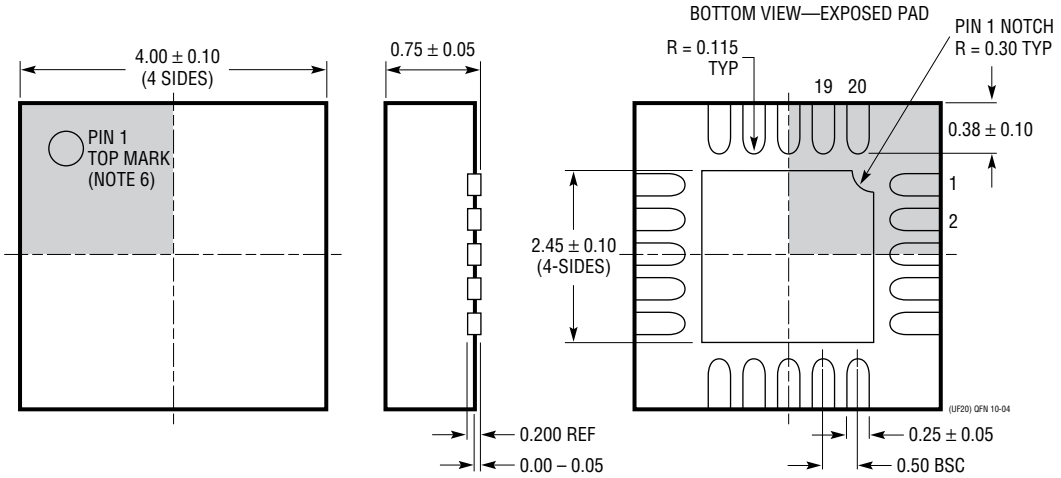
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



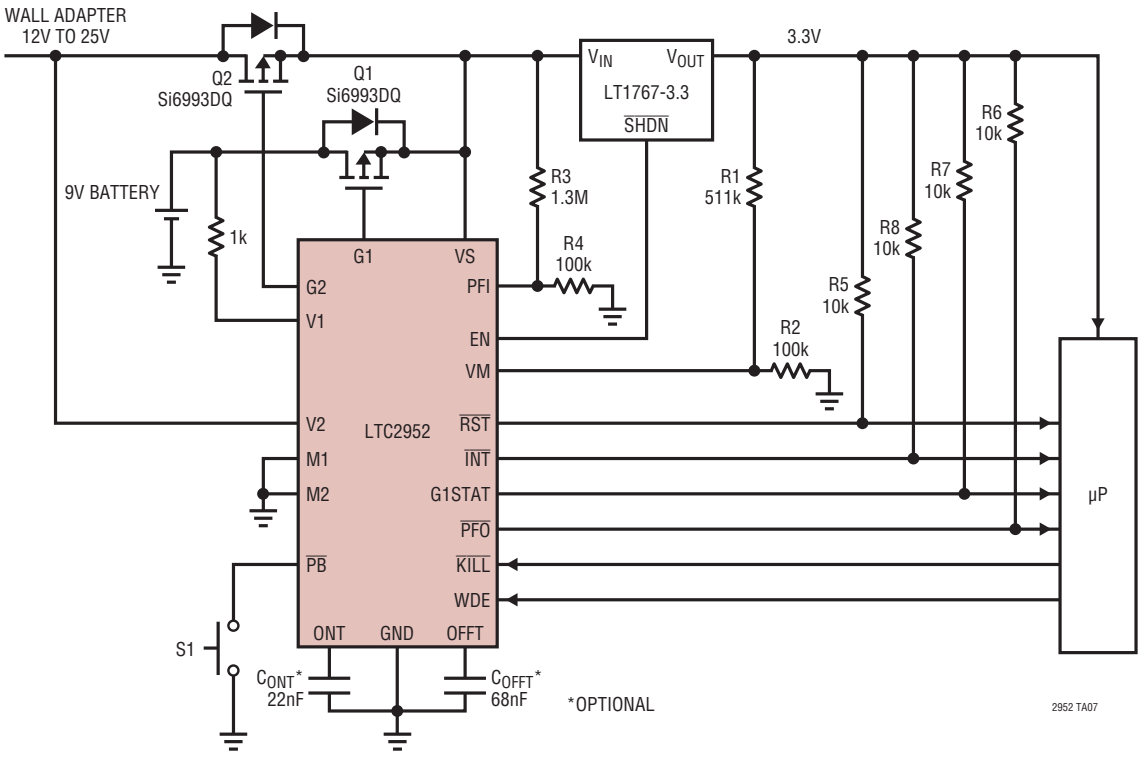
NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/10	Revised Configuration B of Figure 1	14

TYPICAL APPLICATION

Wall Adapter and Battery Automatic Load Switchover with Reverse Battery Protection



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1479	PowerPath Controller for Dual Battery Systems	Complete PowerPath Management for Two Batteries; DC Power Source, Charger and Backup
LTC1726	Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ	Adjustable RESET and Watchdog Timeout
LTC2900	Programmable Quad Supply Monitor	Adjustable RESET, 10-Lead MSOP and DFN Packages
LTC2901	Programmable Quad Supply Monitor	Adjustable RESET and Watchdog Timer, 16-Lead SSOP Package
LTC2902	Programmable Quad Supply Monitor	Adjustable RESET and Tolerance, 16-Lead SSOP Package
LTC2903	Precision Quad Supply Monitor	6-Lead SOT-23 Package
LTC2904/ LTC2905	Three-State Programmable Precision Dual Supply Monitor	Adjustable Tolerance, 8-Lead SOT-23 and DFN Packages
LTC2906/ LTC2907	Dual Supply Monitor with One Pin-Selectable Threshold and One Adjustable Input	0.5V Adjustable Threshold and Three Supply Tolerances, 8-Lead SOT-23 and DFN Packages
LTC2908	Precision Six Supply Monitors	0.5V Adjustable Threshold, RESET, 8-Lead SOT-23 and DFN Packages
LTC2950/ LTTC2951	Pushbutton On/Off Controller	µP Pushbutton Controller Interface with Programmable Debounce On and Off Timing, 8-Lead SOT23 and DFN Packages
LTC4411	SOT-23 Ideal Diode	2.6A Forward Current, 28mV Regulated Forward Voltage
LTC4412HV	PowerPath Controller in ThinSOT™	Efficient Diode-ORing, Automatic Switching, 3V to 36V

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