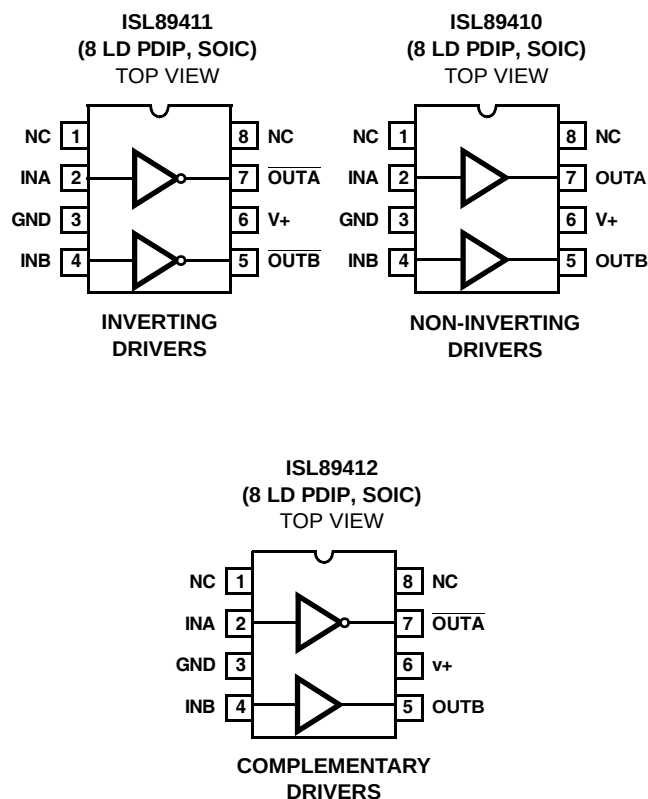


High Speed, Dual Channel Power MOSFET Drivers

The ISL89410, ISL89411, ISL89412 ICs are similar to the EL7202, EL7212, EL7222 series but with greater VDD ratings. These are very high speed matched dual drivers capable of delivering peak currents of 2.0A into highly capacitive loads. The high speed performance is achieved by means of a proprietary “Turbo-Driver” circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10-fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.

Pinouts



Features

- Industry Standard Driver Replacement
- Improved Response Times
- Matched Rise and Fall Times
- Reduced Clock Skew
- Low Output Impedance
- Low Input Capacitance
- High Noise Immunity
- Improved Clocking Rate
- Low Supply Current
- Wide Operating Voltage Range
- Pb-Free Available (RoHS compliant)

Applications

- Clock/line Drivers
- CCD Drivers
- Ultra-Sound Transducer Drivers
- Power MOSFET Drivers
- Switch Mode Power Supplies
- Class D Switching Amplifiers
- Ultrasonic and RF Generators
- Pulsed Circuits

Pin Descriptions

SYMBOL	PIN DESCRIPTIONS
V ₊	Power voltage from 4.5V to 18V.
GND	Power voltage return
INA, INB	Logic inputs.
$\overline{\text{OUTA}}$ OUTA	Non-inverted output for ISL89410. Inverted output for ISL89411 and ISL89412.
$\overline{\text{OUTB}}$ OUTB	Non-inverted output for ISL89410 and ISL89412. Inverted output for ISL89411.
NC	These pins must be left unconnected.

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL89410IP	ISL 89410IP	-40 to +85	8 Ld PDIP	MDP0031
ISL89410IBZ (Note)	89410 IBZ	-40 to +85	8 Ld SOIC (Pb-free)	MDP0027
ISL89410IBZ-T13* (Note)	89410 IBZ	-40 to +85	8 Ld SOIC (Tape and Reel) (Pb-free)	MDP0027
ISL89411IP	ISL 89411IP	-40 to +85	8 Ld PDIP	MDP0031
ISL89411IPZ (Note)	ISL 89411IPZ	-40 to +85	8 Ld PDIP** (Pb-free)	MDP0031
ISL89411IBZ (Note)	89411 IBZ	-40 to +85	8 Ld SOIC (Pb-free)	MDP0027
ISL89411IBZ-T13* (Note)	89411 IBZ	-40 to +85	8 Ld SOIC (Tape and Reel) (Pb-free)	MDP0027
ISL89412IP	ISL 89412IP	-40 to +85	8 Ld PDIP	MDP0031
ISL89412IBZ (Note)	89412 IBZ	-40 to +85	8 Ld SOIC (Pb-free)	MDP0027
ISL89412IBZ-T13* (Note)	89412 IBZ	-40 to +85	8 Ld SOIC (Tape and Reel) (Pb-free)	MDP0027

*Please refer to TB347 for details on reel specifications.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply (V+ to GND) 19.0V
 Input Pins -0.3V to +0.3V above V+
 Combined Peak Output Current 4A

Maximum Recommended Operating Conditions

Recommended Operating V+ Range 4.5V to 18.0V
 Input Pins 0V to V+

Thermal Information

Operating Junction Temperature +125°C
 Power Dissipation
 8 Ld SOIC 570mW
 8 Ld PDIP* 1050mW
 Storage Temperature Range -65°C to +150°C
 Ambient Operating Temperature -40°C to +85°C
 Pb-Free Reflow Profile see link below
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications $T_A = +25^\circ\text{C}$, $V = 18\text{V}$ unless otherwise specified; Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ\text{C}$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V_{IH}	Logic "1" Input Voltage		2.4			V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	μA
V_{IL}	Logic "0" Input Voltage				0.8	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	μA
V_{HVS}	Input Hysteresis			0.3		V
OUTPUT						
R_{OH}	Pull-Up Resistance	$I_{OUT} = -100\text{mA}$		3	6	Ω
R_{OL}	Pull-Down Resistance	$I_{OUT} = +100\text{mA}$		4	6	Ω
I_{PK}	Peak Output Current	Source		2		A
		Sink		2		A
I_{DC}	Continuous Output Current	Source/Sink	100			mA
POWER SUPPLY						
I_S	Power Supply Current	Inputs High/ISL89410		4.5	7.5	mA
		Inputs High/ISL89411		1	2.5	mA
		Inputs High/ISL89412		2.5	5.0	mA
V_S	Operating Voltage		4.5		18	V

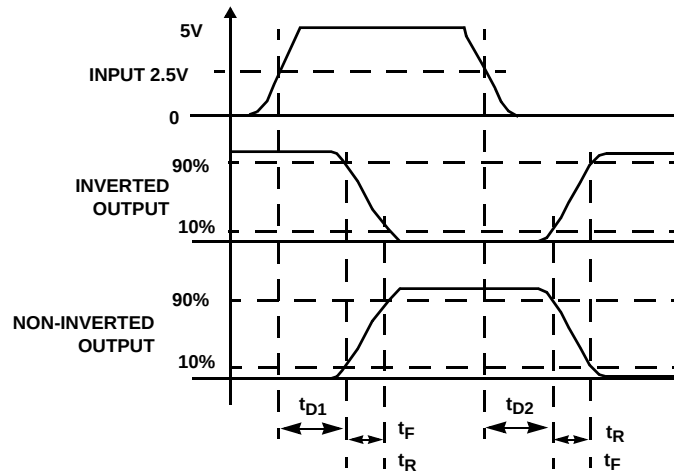
AC Electrical Specifications $T_A = +25^\circ\text{C}$, $V = 18\text{V}$ unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_R	Rise Time (Note 1)	$C_L = 500\text{pF}$		7.5		ns
		$C_L = 1000\text{pF}$		10	20	ns
t_F	Fall Time (Note 1)	$C_L = 500\text{pF}$		10		ns
		$C_L = 1000\text{pF}$		13	20	ns
t_{D1}	Turn-On Delay Time (Note 1)	See "Timing Table" on page 4		18	25	ns
t_{D2}	Turn-Off Delay Time (Note 1)	See "Timing Table" on page 4		20	25	ns

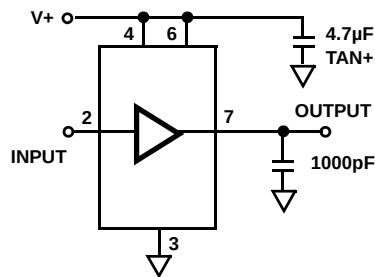
NOTE:

1. All AC Electrical Specifications are established by characterization and are not production tested.

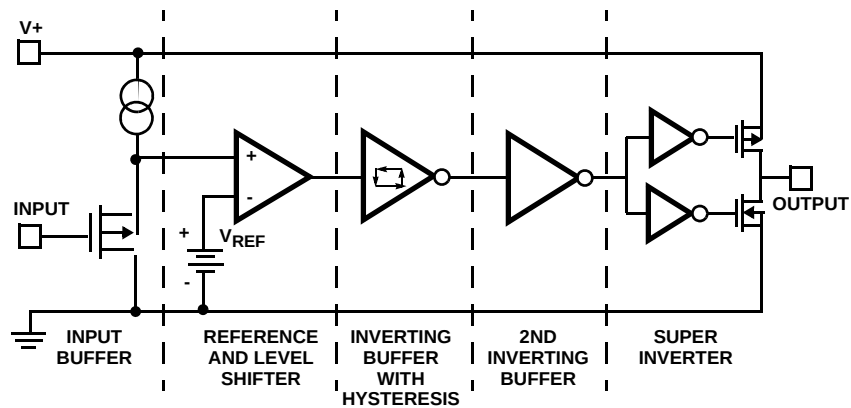
Timing Table



Standard Test Configuration



Simplified Schematic



Typical Performance Curves

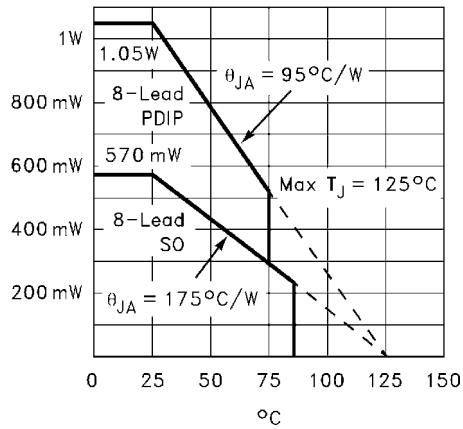


FIGURE 1. MAX POWER/DERATING CURVES

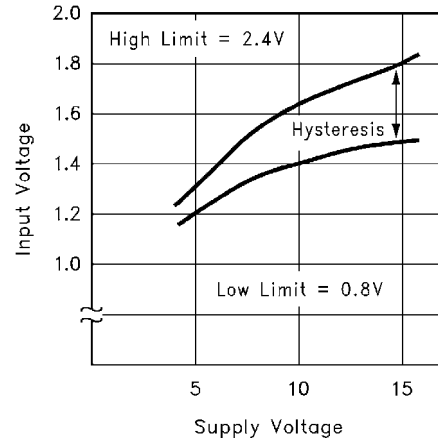


FIGURE 2. SWITCH THRESHOLD vs SUPPLY VOLTAGE

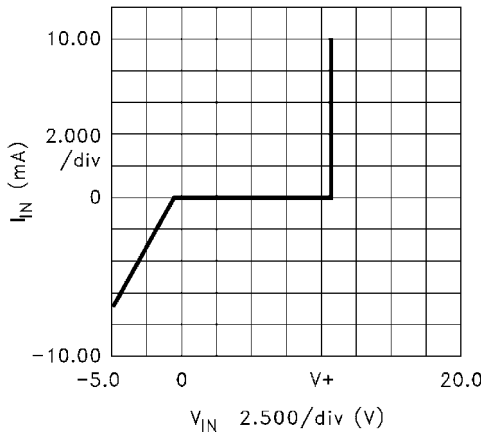


FIGURE 3. INPUT CURRENT vs VOLTAGE

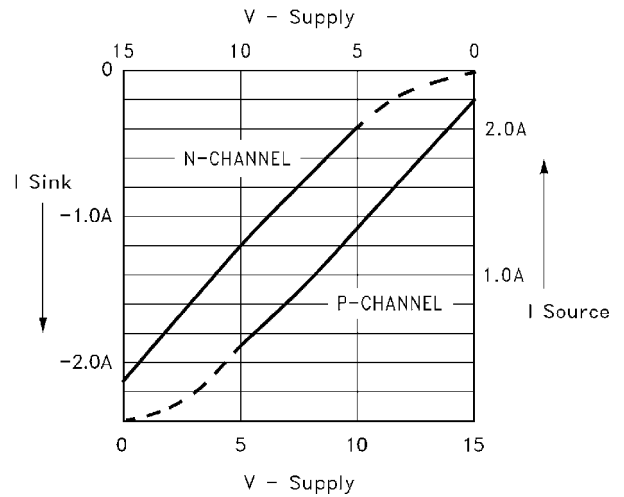


FIGURE 4. PEAK DRIVE vs SUPPLY VOLTAGE

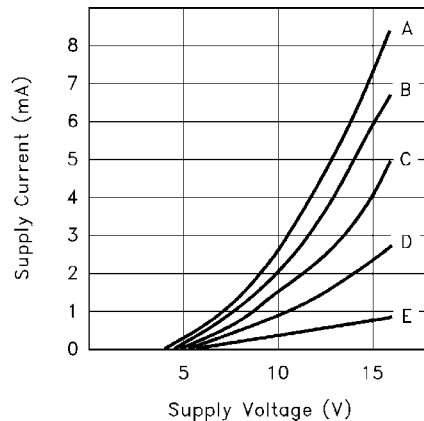


FIGURE 5. QUIESCENT SUPPLY CURRENT

CASE:

Device	Input Level	Curve
ISL89410	GND	A
	GND, V+	B
	V+	C
ISL89411	GND	C
	GND, V+	D
	V+	E
ISL89412	GND	B
	GND, V+	C
	V+	D

Typical Performance Curves (Continued)

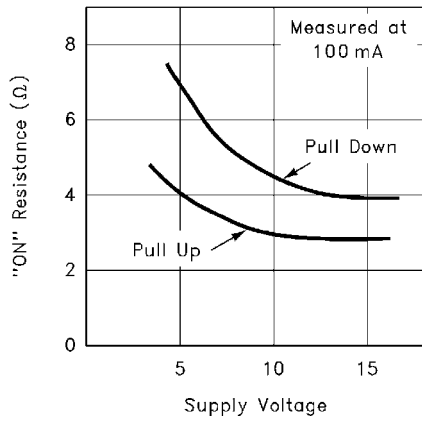


FIGURE 6. "ON" RESISTANCE vs SUPPLY VOLTAGE

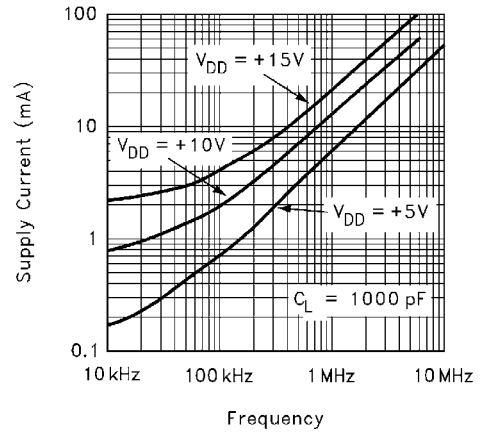


FIGURE 7. AVERAGE SUPPLY CURRENT vs VOLTAGE AND FREQUENCY

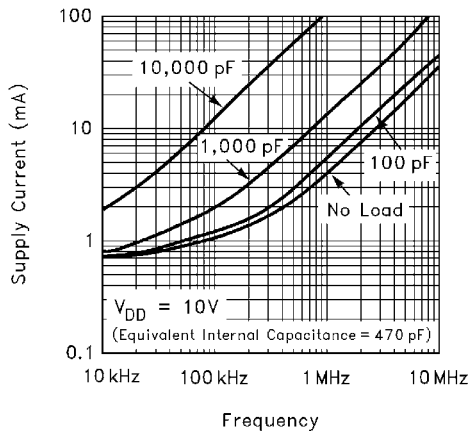


FIGURE 8. AVERAGE SUPPLY CURRENT vs CAPACITIVE LOAD

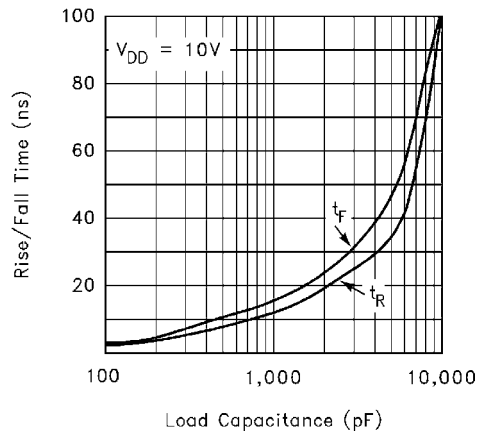


FIGURE 9. RISE/FALL TIME vs LOAD

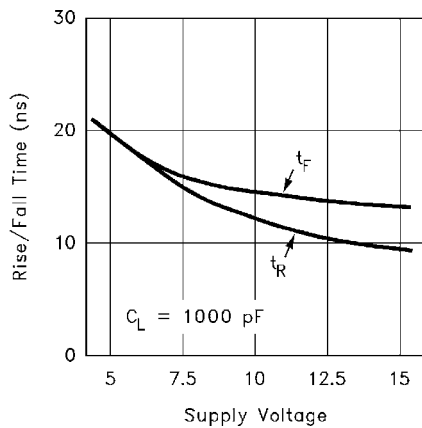


FIGURE 10. RISE/FALL TIME vs SUPPLY VOLTAGE

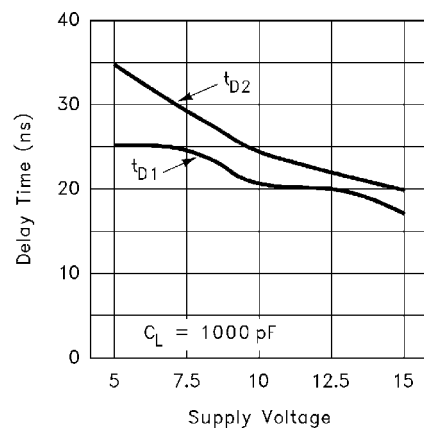


FIGURE 11. PROPAGATION DELAY vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

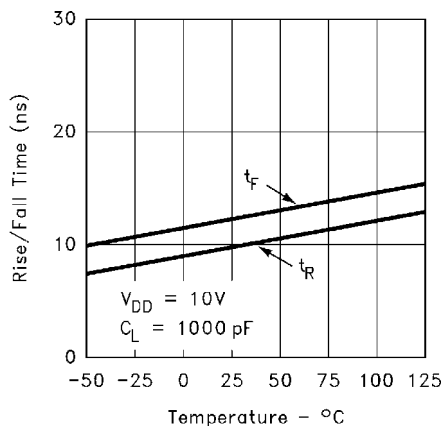


FIGURE 12. RISE/FALL TIME vs TEMPERATURE

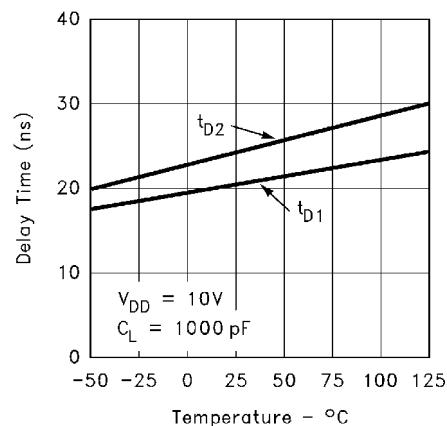
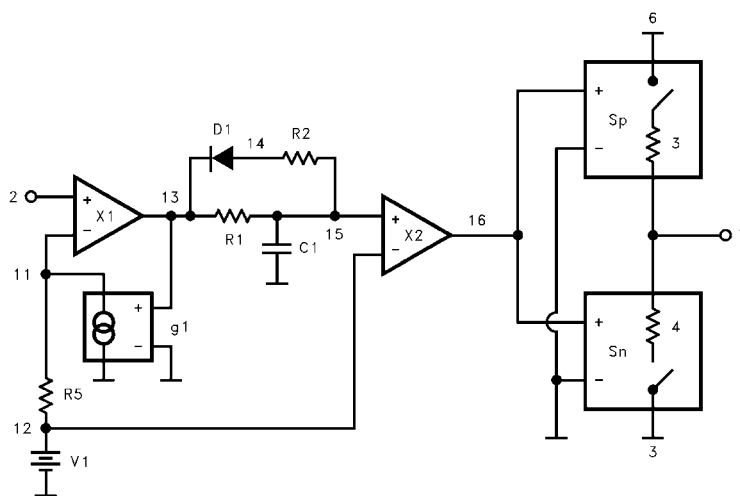


FIGURE 13. DELAY vs TEMPERATURE

ISL89411 Macro Model



**** ISL89411 Model ****

```

*          input
*          |   gnd
*          |   |   Vsupply
*          |   |   Vout
*          |   |   |
.subckt M89411 2   3   6   7
V1 12 3 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 3 43.3 pF
D1 14 13 dmod
X1 13 11 2 3 comp1
X2 16 12 15 3 comp1
sp 6 7 16 3 spmod
sn 7 3 16 3 snmod
g1 11 0 13 0 938μ
.model dmod d
.model spmod vswitch ron3 roff2meg von1 voff1.5
.model snmod vswitch ron4 roff2meg von3 voff2
.ends M89411
    
```

```
.subckt comp1 out inp inm vss
e1 out vss table { (v(inp) v(inm))* 5000} (0,0) (3.2,3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends comp1
```

Application Guidelines

It is important to minimize inductance to the power FET by keeping the output drive current loop as short as possible. Also, the decoupling capacitor, C_q , should be a high quality ceramic capacitor with a Q that should be a least 10x the gate Q of the power FET. A ground plane under this circuit is also recommended.

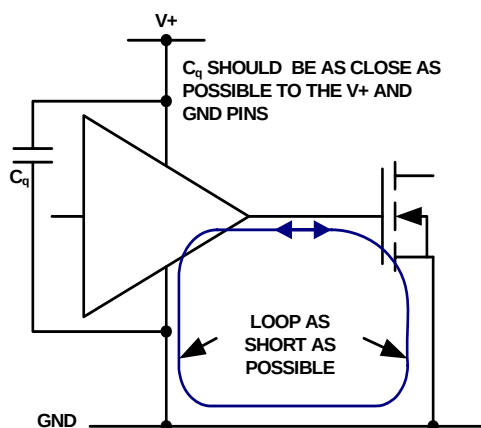


FIGURE 14. RECOMMENDED LAYOUT METHODS

In applications where it is difficult to place the driver very close to the power FET (which may result with excessive parasitic inductance), it then may be necessary to add an external gate resistor to dampen the inductive ring. If this resistor must be too large in value to be effective, then as an alternative, Schottky diodes can be added to clamp the ring voltage to V_+ or GND.

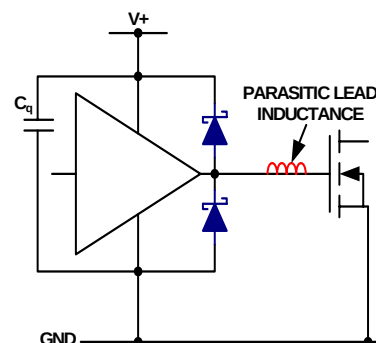


FIGURE 15. SUGGESTED CONFIGURATION FOR DRIVING INDUCTIVE LOADS

Where high supply voltage operation is required (15V to 18V), input signals with a minimum of 3.3V input drive is suggested and a minimum rise/fall time of 100ns. This is recommended to minimize the internal bias current power dissipation.

Excessive power dissipation in the driver can result when driving highly capacitive FET gates at high frequencies. These gate power losses are defined by Equation 1:

$$P = 2 \cdot Q_C \cdot V_{gs} \cdot f_{SW} \quad (\text{EQ. 1})$$

where:

P = Power

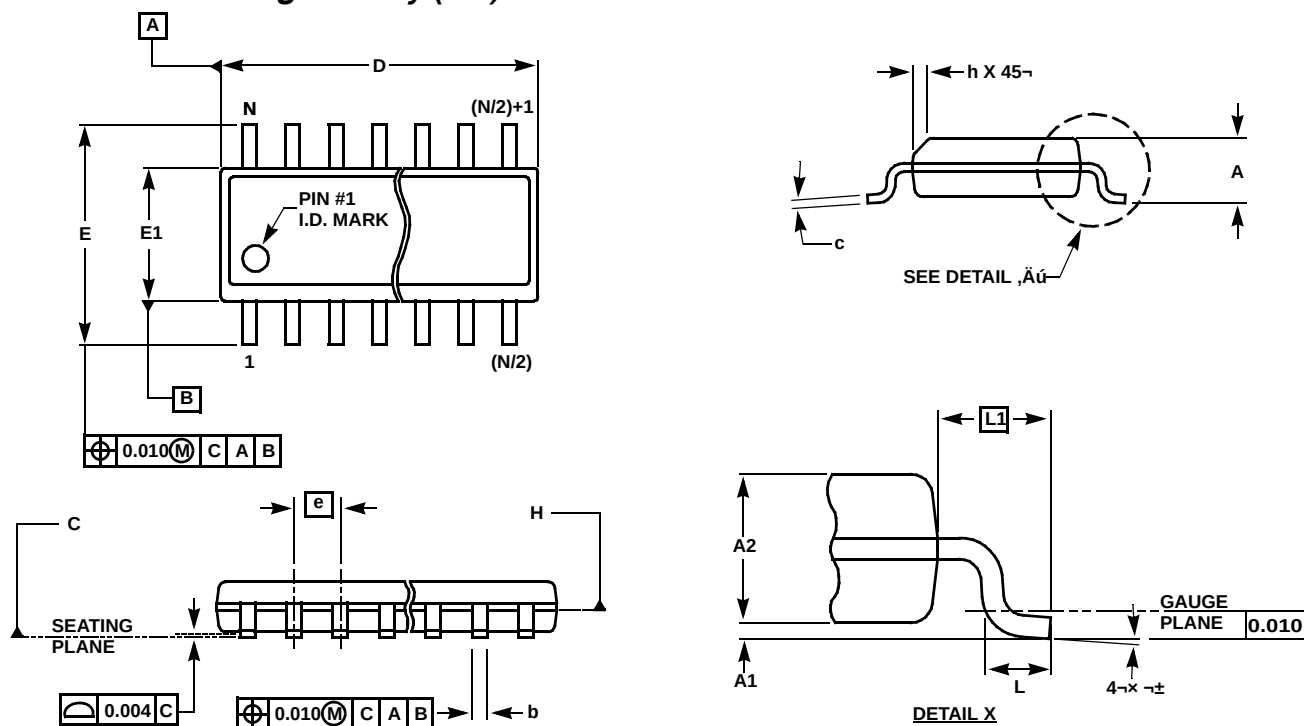
Q_C = Charge of the Power FET at V_{gs}

V_{gs} = Gate drive voltage (V_+)

f_{SW} = switching Frequency

Adding a gate resistor to the output of the driver will transfer some of the driver dissipation to the resistor. Another possible solution is to lower the gate driver voltage which also lowers Q_C .

Small Outline Package Family (SO)



MDP0027

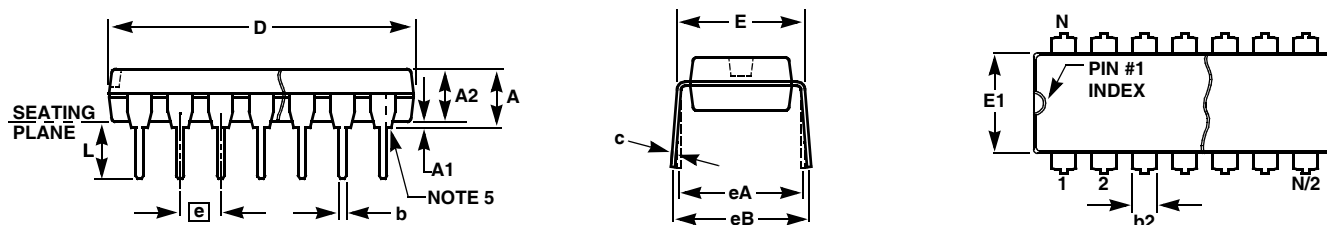
SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	± 0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	± 0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	± 0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	± 0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	± 0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	± 0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	± 0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	± 0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Plastic Dual-In-Line Packages (PDIP)**MDP0031****PLASTIC DUAL-IN-LINE PACKAGE**

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	± 0.005	
b	0.018	0.018	0.018	0.018	0.018	± 0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	± 0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	± 0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	± 0.025	
L	0.125	0.125	0.125	0.125	0.125	± 0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

NOTES:

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

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