Data Acquisition

A/D Converters/ DVM Circuits

D/A Converters

D/A Current Switches

†The ICL7136 is recommended for all applications which currently employ the ICL7126.

Integrating Analog-to-Digital Converters for Display

Maximum Electrical Specification at 25°C unless otherwise noted.

Model	ICL7136	ICL7137	ICL7135	ICL7129	ICL7106/ICL7116	ICL7107/ICL7117
Resolution	±3½ Digit	±3½ Digit	±4½ Digit	±4½ Digit	±3½ Digit	±3½ Digit
Accuracy						
Non-Linearity	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count
Zero Input Reading	±0.000	±0.000	±0.000	±0.000	±0.000	±0.000
Ratiometric Reading	±1.000	±1.000	±1.000	±0.9997	±1.000	±1.000
$V_{IN} = V_{REF}$	±1 Count	±1 Count	±1 Count	±3 Counts	±1 Count	±1 Count
Rollover Error	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count
Stability						
Offset vs. Temperature	1μV/°C	1μV/°C	1μV/°C	1μV/°C	1μV/°C	1μV/°C
Gain vs. Temperature	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C
Conversion Time	0.1 to 3 conv/sec	0.1 to 3 conv/sec	0.1 to 15 conv/sec	0.1 to 6 conv/sec	0.1 to 15 conv/sec	0.1 to 15 conv/sec
Analog Input						
Voltage Range	±200mV to ±2V	±200mV to ±2V	±2V	±200mV to ±2V	±200mV to ±2V	±200mV to ±2V
Impedance	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$
Leakage Current	2pA	2pA	3pA	1pA	2pA	3pA
Noise (peak-to-peak)	15μV typ.	15μV typ.	15μV typ.	7μV typ.	15μV typ.	15μV typ.
Digital Input	—	—	—	Decimal Points Continuity Hold, Range Select	Display Hold (7116)	Display Hold (7117)
Digital Outputs						
Format	Direct 7 Segment LCD Display	Direct 7 Segment LCD Display	Multiplex BCD	4½ Digit Triplexed LCD Display Drive w/Decimal Points, Low Battery and Continuity Indicators	Direct 7 Segment LCD Display	Direct 7 Segment LED Display
Logic Level	AC:4.5V Down from V+	AC:4.5V Down from V+	TTL/CMOS		AC:4.5V Down from V+	Comm Anode DTL/TTL/CMOS
Power Supply						
Voltage	+9V	±5V	±5V	+9V	+9V	±5V
Current	100μA	200μA	1.8mA	1.8mA	1.8mA	1.8mA
Package	40 pin DIP	40 pin DIP	28 pin DIP	40 pin DIP	40 pin DIP	40 pin DIP

*Also available LD110/111/114 (not recommended for new designs), and ICL7126 (recommended use ICL7136).

Integrating Analog-to-Digital Converters for Data Acquisition

Type	Single Chip	Two Chip System***	
Model	**ICL7109**	**ICL8052A/8068 ICL7104-14**	**ICL8052A/8068 ICL7104-16**
Resolution	±12-Bit Binary	±14-Bit	±16-Bit
Accuracy	±1 Count	±1 Count	±1 Count
Microprocessor Compatible	Yes	Yes	Yes
Output	Programmable: 1. Latched parallel 3 state Binary 2. Controlled 2-8 bit bytes	Programmable: 1. Latched parallel 3 state Binary 2. Controlled 2-8 Bit Byte for ICL7104-12/14 3-8 Bit Byte for ICL7104-16	
Control Lines	Run/Hold, Busy, Byte Enables, Mode, Load, Send Enable, Out of Range		
Conversion Time	10ms	80ms	330ms
UART Compatible	Yes	Yes	Yes
Noise (Typical)	15μV	2μV (8068)	2μV (8068)
Input Current	10pA	30pA (8052)	30pA (8052)
Input Voltage Range	+400mV to +4.1V	+100mV to +10V	−200mV to −10V

***ICL8052/8068 and ICL8053 can be combined as analog portion of dual-slope A/D converter under μp control. See ICL8052/8068 and ICL 7104-16 for performance characteristics.

Digital-to-Analog Converters*

Maximum Electrical Specification at 25°C unless otherwise noted.

Model	ICL7134U/B	7145	7146	AD7523	AD7533	AD7520 (7530)	AD7520 (7531)	AD7541
Resolution	14 bit	16 bit	12 bit	8 bit	10 bit	10 bit	12 bit	12 bit
Accuracy	J/K/L	J/K	J/K	J/K/L	J/K/L	J/K/L	J/K/L	J/K/L
Linearity	0.01/0.006/0.003%	0.006/0.003%	0.01%	0.2%/0.1%/0.05%	0.2%/0.1%/0.05%	0.02%/0.01%/0.05%	0.2%/0.1%/0.5%	0.02%/0.01%/0.01%
Zero Offset	10 nA	10 mV	120 µV	50 µA	200 nA	200 nA (300 nA)	200 nA (300 nA)	50 nA
Full Scale Reading	0.003%	0.04/0.02% FSR	0.04/0.02% FSR	1.5% max	1.4%	0.3% typ	0.3% typ	0.3%
Stability								
Gain vs. Temperature	5 ppm/°C	1 ppm/°C typ	5 ppm/°C typ	10 ppm/°C	10 ppm/°C	10 ppm/°C	10 ppm/°C	10 ppm/°C
Linearity vs. Temperature	1 ppm/°C	1 ppm/°C typ	1 ppm/°C typ	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C
Setting Time To 1/2 LSB	0.9 µs typ	3 µs	10 µ	150 ns	600 ns typ	500 ns typ	500 ns typ	1 µs
Input Code Logic Compatibility option	DTL/TTL/CMOS Binary (U); 2's Complement (B)	DTL/TTL/CMOS 2's Complement	DTL/TTL/CMOS Binary or 2's Complement	DTL/TTL/CMOS Binary Offset Binary	DTL/TTL/CMOS Binary Offset Binary	DTL/TTL/CMOS Binary Offset Binary	DTL/TTL/CMOS Binary Offset Binary	DTL/TTL/CMOS Binary Offset Binary
Power Supply								
Voltage	+3.5 to +6.0V	4.5 to 5.5V	±4.5 to 5.5V	+6 to +16V	+5 to +15V	+5 to +15V	+5 to +15V	+5 to +16V
Current	2mA	1.2mA	5mA	100 µA	2mA	2mA	2mA	2mA
Package	28 pin DIP	28 pin DIP	28 pin DIP	16 pin DIP	16 pin DIP	16 pin DIP	18 pin DIP	18 pin DIP

*R2R Ladder Multiplying Type

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Successive Approximation Analog-to-Digital Converters

Model	ADC0801-4	ICL7115
Resolution	8 bit	14 bit binary
Accuracy	± ¼/½/½/1 LSB	± ½ LSB
Microprocessor Compatible	Yes	Yes
Output	Programmable: 1. Latched parallel 3 state Binary	Programmable: 1. Two latched bytes
	2. One 8 bit byte	2. 15 bit parallel
Control Lines	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, BUS
Conversion Time	100µs	40µs
UART Compatible	Yes	No
Input Voltage Range	5V span	0 - 5V

Quad Current Switches ICL8018/8019/8020

High speed precision current switches for use in current summing D/A converters. Can be purchased individually or in matched sets with accuracies of 0.01% (ICL8018), 0.1% (ICL8019), or 1.0% (ICL8020)

Sample and Hold

Type	V_{analog} (V_{p-p})	t_{acq}** (µs)	V_{inject}** (mV)	V_{os} (mV)	Drift Rate (mV/sec)
IH5110	±7.5	6	5	40	5
IH5111	±10	6	5	40	5
IH5112	±7.5	6	5	10	5
IH5113	±10	6	5	10	5
IH5114	±7.5	6	5	5	5
IH5115	±10	6	5	5	5

**C_{STO} = 0.01 µF

Monolithic Voltage Converter—The ICL7660

Converts positive voltage into negative over a range of + 1.5V through + 10V. May be cascaded for higher negative output voltages, paralleled for greater output current, used as a positive voltage multiplier, or any combination of the above. Typical supply current is 170 µA, and output source resistance is 55Ω at T_A = 25°C and I_O = 20 mA

ADC0801–ADC0804

8-Bit Microprocessor Compatible A/D Converters

FEATURES

- MCS-48 and MCS-80/85 bus compatible–no interfacing logic required
- Conversion time < 100μs
- Easy interface to all microprocessors
- Will operate "stand alone"
- Differential analog voltage inputs
- Works with bandgap voltage references
- TTL compatible inputs and outputs
- On-chip clock generator
- 0V to 5V analog voltage input range (single +5V supply)
- No zero-adjust required

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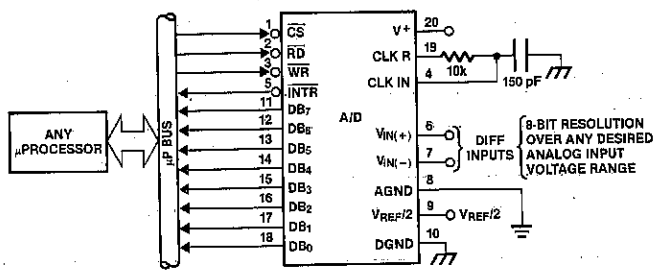
GENERAL DESCRIPTION

The ADC0801 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, hence no interfacing logic is required.

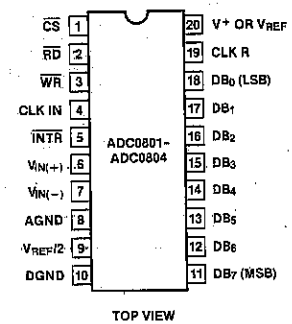
The differential analog voltage input has good common-mode-rejection, and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0801 family is available in the industry standard 20 pin CERDIP package.

TYPICAL APPLICATION



PIN CONFIGURATION



(Outline dwg. JP)

ORDERING INFORMATION

PART	ERROR	TEMPERATURE RANGE	PACKAGE	ORDER NUMBER
ADC0801	± 1/4 bit adjusted full-scale	0°C to +70°C	20 pin CERDIP	ADC0801LCN
		−40°C to +85°C	20 pin CERDIP	ADC0801LCD
		−55°C to +125°C	20 pin CERDIP	ADC0801LD
ADC0802	± 1/2 bit no adjust	0°C to +70°C	20 pin CERDIP	ADC0802LCN
		−40°C to +85°C	20 pin CERDIP	ADC0802LCD
		−55°C to +125°C	20 pin CERDIP	ADC0802LD
ADC0803	± 1/2 bit adjusted full-scale	0°C to +70°C	20 pin CERDIP	ADC0803LCN
		−40°C to +85°C	20 pin CERDIP	ADC0803LCD
		−55°C to +125°C	20 pin CERDIP	ADC0803LD
ADC0804	± 1 bit no adjust	0°C to +70°C	20 pin CERDIP	ADC0804LCN
		−40°C to +85°C	20 pin CERDIP	ADC0804LCD

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Voltage at Any Input ..... −0.3V to (V+ + 0.3V)
Storage Temperature Range ..... −65°C to +150°C
Package Dissipation at T_A = +25°C ..... 875 mW
Lead Temperature (Soldering, 10 seconds) ..... 300°C

OPERATING RATINGS

Temperature Range
ADC0801/02/03LD ..... −55°C to +125°C
ADC0801/02/03/04LCD ..... −40°C to +85°C
ADC0801/02/03/04LCN ..... 0°C to +70°C
Supply Voltage Range ..... 4.5V to 6.3V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYSTEM ELECTRICAL CHARACTERISTICS (Notes 1 and 7)

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $T_{MIN} \le T_A \le T_{MAX}$ and $f_{CLK} = 640kHz$ unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC0801: Total Adjusted Error	With Full Scale Adjust			±1/4	LSB
ADC0802: Total Unadjusted Error	Completely Unadjusted			±1/2	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			±1/2	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND − 0.05		V^+ + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	$V^+ = 5V \pm 10\%$ Over Allowed Input Voltage Range		±1/16	±1/8	LSB

AC ELECTRICAL CHARACTERISTICS

Timing Specifications: $V^+ = 5V$ and $T_A = +25°C$ unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	f_{CLK}	$V^+ = 6V$ (Note 3) $V^+ = 5V$	100 100	640 640	1280 800	kHz kHz
Clock Periods per Conversion (Note 4)	t_{conv}		66		73	
Conversion Rate In Free-Running Mode	CR	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0V, f_{CLK} = 640kHz			8888	conv/s
Width of $\overline{WR}$ Input (Start Pulse Width)	$t_{W(\overline{WR})l}$	$\overline{CS}$ = 0V (Note 5)	100			ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	t_{acc}	C_L = 100pF (Use Bus Driver IC for Larger C_L)		135	200	ns
3-State Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	t_{1h}, t_{0h}	C_L = 10 pF, R_L = 10k (See **3-State Test Circuits**)		125	250	ns
Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$	t_{WI}, t_{RI}			300	450	ns
Input Capacitance of Logic Control Inputs	C_{IN}			5	7.5	pF
3-State Output Capacitance (Data Buffers)	C_{OUT}			5	7.5	pF

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DC ELECTRICAL CHARACTERISTICS

Digital Levels and DC Specifications: $V^+ = 5V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL INPUTS (Note 6)						
Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{INH}	$V^+ = 5.25V$	2.0		V^+	V
Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{INL}	$V^+ = 4.75V$			0.8	V
CLK IN (Pin 4) Positive Going Threshold Voltage	V_{CLK}^+		2.7	3.1	3.5	V
CLK IN (Pin 4) Negative Going Threshold Voltage	V_{CLK}^-		1.5	1.8	2.1	V
CLK IN (Pin 4) Hysteresis $(V_{CLK}^+) - (V_{CLK}^-)$	V_H		0.6	1.3	2.0	V
Logical "1" Input Current (All Inputs)	I_{INHI}	$V_{IN} = 5V$		0.005	1	μA
Logical "0" Input Current (All Inputs)	I_{INLO}	$V_{IN} = 0V$	−1	−0.005		μA
Supply Current (Includes Ladder Current)	I^+	$f_{CLK} = 640kHz$, $T_A = +25°C$ and $\overline{CS}$ = HI		1.3	2.5	mA
DATA OUTPUTS AND $\overline{INTR}$						
Logical "0" Output Voltage	V_{OL}	$I_O = 1.6mA$ $V^+ = 4.75V$			0.4	V
Logical "1" Output Voltage	V_{OH}	$I_O = -360\mu A$ $V^+ = 4.75V$	2.4			V
3-State Disabled Output Leakage (All Data Buffers)	I_{LO}	$V_{OUT} = 0V$	−3			μA
		$V_{OUT} = 5V$			3	μA
Output Short Circuit Current		$T_A = +25°C$				
	I_{SOURCE}	V_{OUT} Short to Gnd	4.5	6		mA
	I_{SINK}	V_{OUT} Short to V^+	9.0	16		mA

Note 1: All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.

Note 2: For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see **Block Diagram**) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V^+ supply. Be careful, during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.

Note 3: With $V^+ = 6V$, the digital logic interfaces are no longer TTL compatible.

Note 4: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.

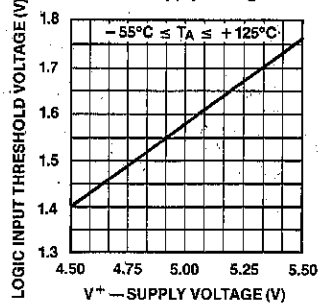
Note 5: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see **Timing Diagrams**).

Note 6: CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.

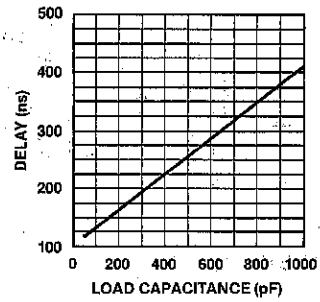
Note 7: None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See **Zero Error** below.

TYPICAL PERFORMANCE CHARACTERISTICS

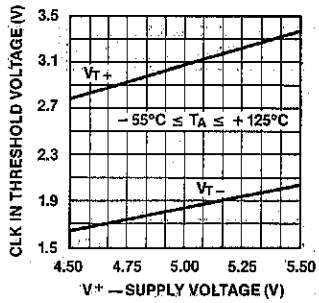
Logic Input Threshold Voltage vs Supply Voltage



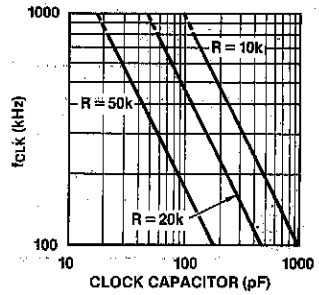
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs Load Capacitance



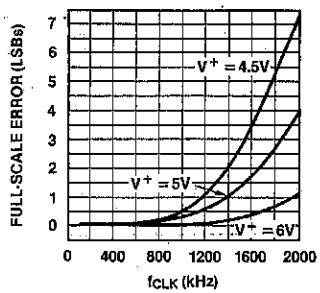
CLK IN Schmitt Trip Levels vs Supply Voltage



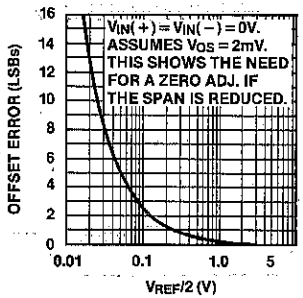
f_{CLK} vs Clock Capacitor



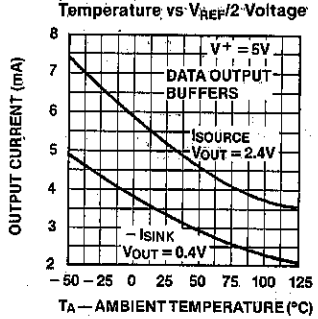
Full-Scale Error vs f_{CLK}



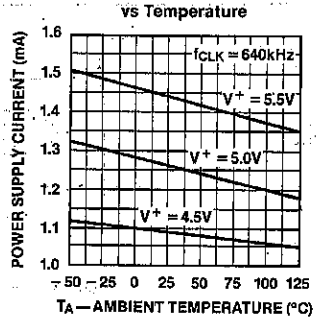
Effect of Unadjusted Offset Error



Output Current vs Temperature vs $V_{REF}/2$ Voltage

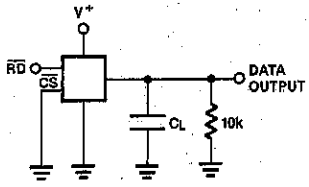


Power Supply Current vs Temperature

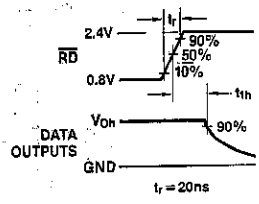


3-STATE TEST CIRCUITS AND WAVEFORMS

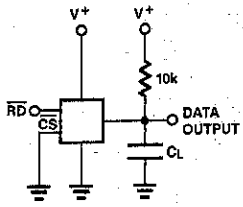
t_{1h}



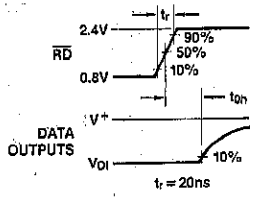
t_{1h}, $C_L = 10pF$



t_{0h}

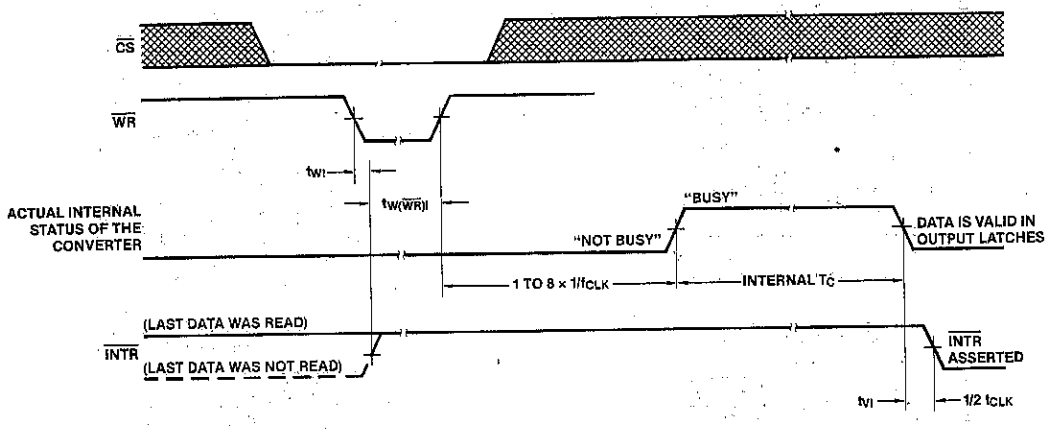


t_{0h}, $C_L = 10pF$

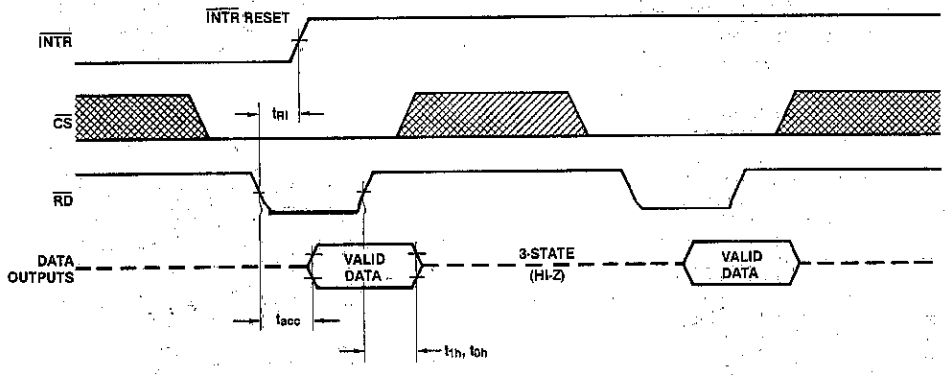


TIMING DIAGRAMS

Start Conversion



Output Enable and Reset $\overline{INTR}$



Note: All timing is measured from the 50% voltage points.

UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 1a. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D – 1, D, and D + 1. For the perfect A/D, not only will center-value (A – 1, A, A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±1/2 LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ±1/2 LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

Figure 1b shows the worst case transfer function for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±1/4 LSB. In other words, if we apply an analog input equal to the center-value ±1/4 LSB, the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than 1/2 LSB.

The error curve of Figure 1c shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 1a is +1/2 LSB because the digital code appeared 1/2 LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude, unless the device has missing codes.

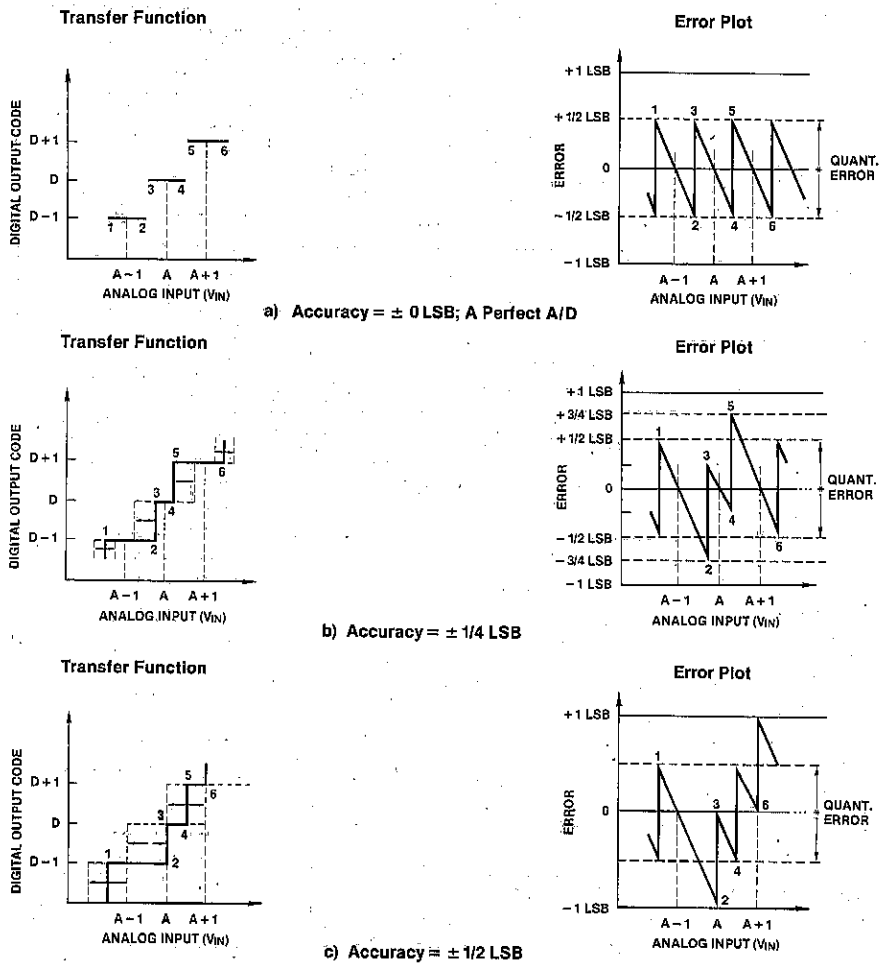


Figure 1. Clarifying the Error Specs of an A/D Converter

FUNCTIONAL DESCRIPTION

A functional diagram of the ADC0801 series of A/D converters is shown in Figure 2. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines. The device operates on the successive approximation principle (see A016 and A020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage $[V_{IN(+)} - V_{IN(-)}]$ matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to-low transition of the $\overline{WR}$ input, the internal SAR latches and the shift-register stages are reset, and the $\overline{INTR}$ output will be set high. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.* After the requisite number of clock pulses to complete the conversion, the $\overline{INTR}$ pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A $\overline{RD}$ operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line high again. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

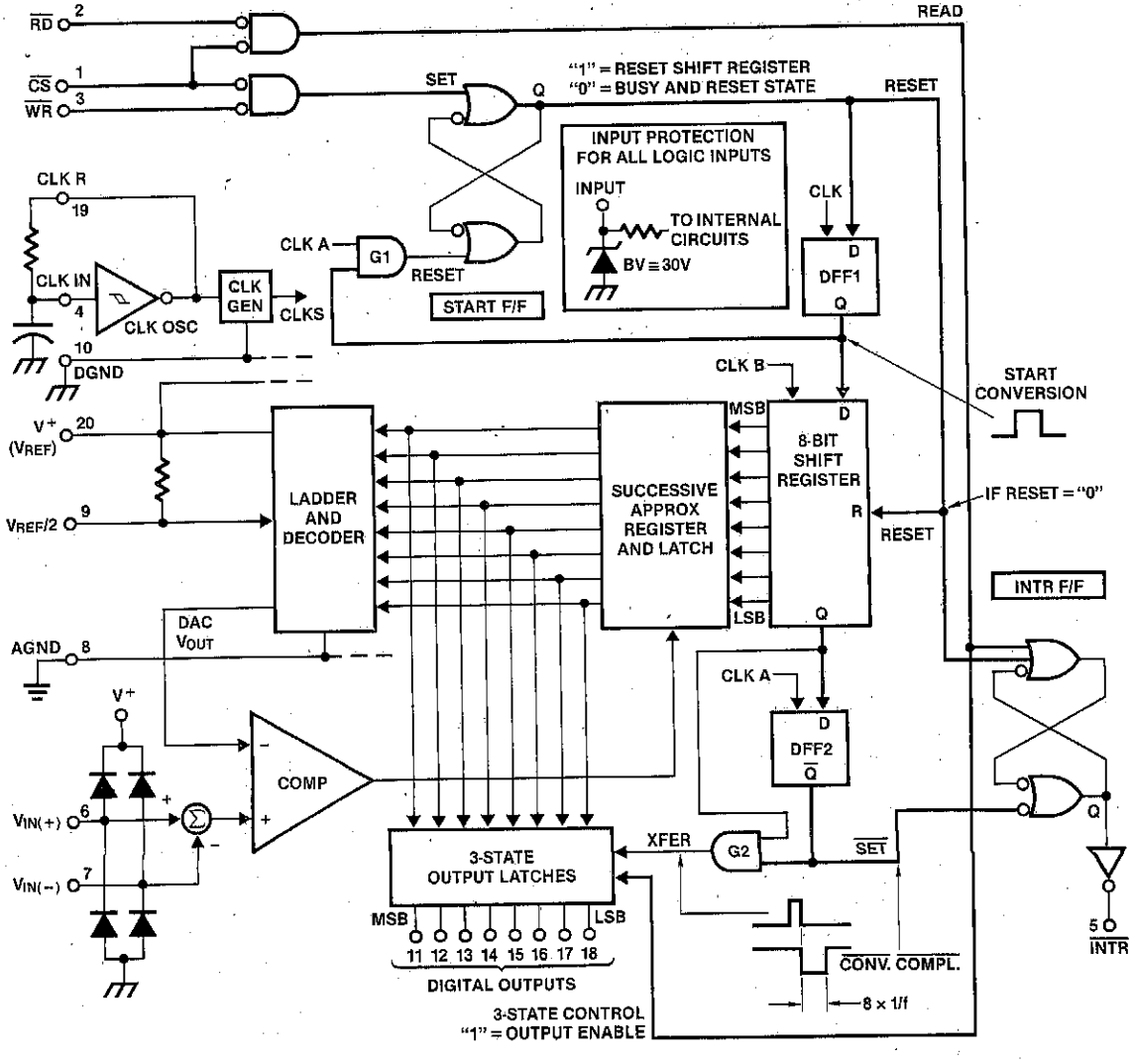


Figure 2. Block Diagram of ADC0801-ADC0804

Digital Details

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt ($\overline{INTR}$) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide $\overline{CS}$ and $\overline{WR}$ signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the 3-state output latches. When DFF2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the $\overline{INTR}$ F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the 3-state output latches will be enabled to provide the 8-bit digital outputs.

Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the $\overline{WR}$ input (pin 3). The Output Enable function is achieved by an active low pulse at the $\overline{RD}$ input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by 1/2 LSB (see Figure 1a).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA–20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)\ (2\pi f_{cm}) \left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

For example, with a 60Hz common-mode frequency, f_{cm}, and a 640kHz A/D clock, f_{CLK}, keeping this error to 1/4 LSB (~5mV) would allow a common-mode voltage, V_P, given by:

$$V_P = \frac{[\Delta V_e(MAX)(f_{CLK})]}{(2\pi f_{cm})\ (4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\ (640 \times 10^3)}{(6.28)\ (60)\ (4.5)} \simeq 1.9V$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see **Reference Voltage Span Adjust**).

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not inherently cause errors* as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full-scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately 5μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (>1kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor ($\leq 1k\Omega$) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications, ($\leq 1k\Omega$), a 0.1μF bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5kΩ. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see **Analog Input Current**). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full-scale adjustment of the A/D (see **Full-Scale Adjustment**) with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 3.

Notice that the reference voltage for the IC is either 1/2 of the voltage which is applied to the V+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

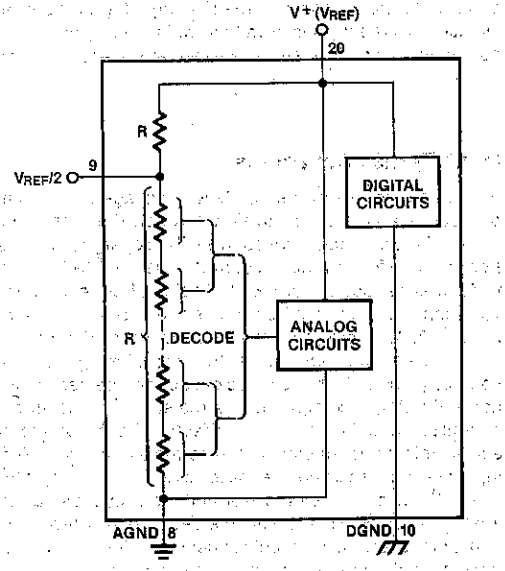


Figure 3. The $V_{REFERENCE}$ Design on the IC

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to 1/2 of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 4. For expanded scale inputs, the circuits of Figures 5 and 6 can be used.

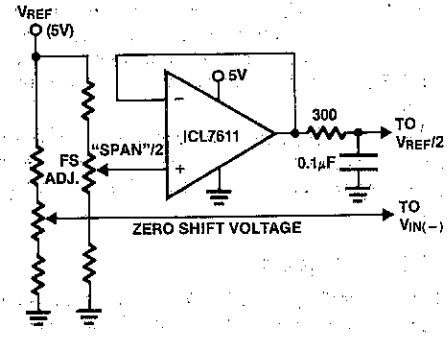


Figure 4. Offsetting the Zero of the ADC0801 and Performing an Input Range (Span) Adjustment

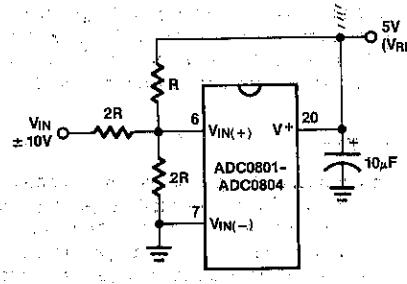


Figure 5. Handling ±10V Analog Input Range

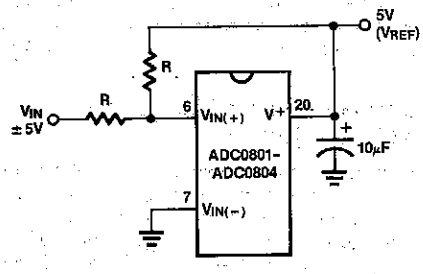


Figure 6. Handling ±5V Analog Input Range

Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of ±10mV will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1 LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see **Applications** section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal 1/2 LSB value (1/2 LSB = 9.8mV for $V_{REF}/2 = 2.500V$).

Full-Scale Adjust

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full-scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}\,\text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 7.

Heavy capacitive or DC loading of the CLocK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power T^2L buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard T^2L buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 8 for details.

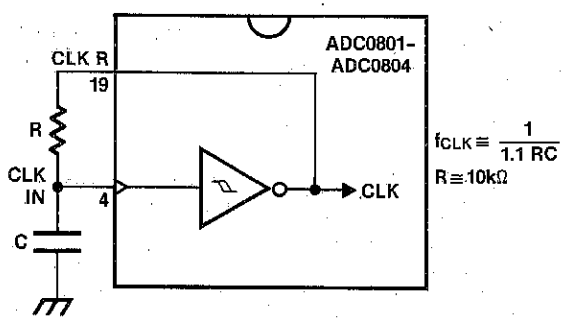


Figure 7. Self-Clocking the A/D

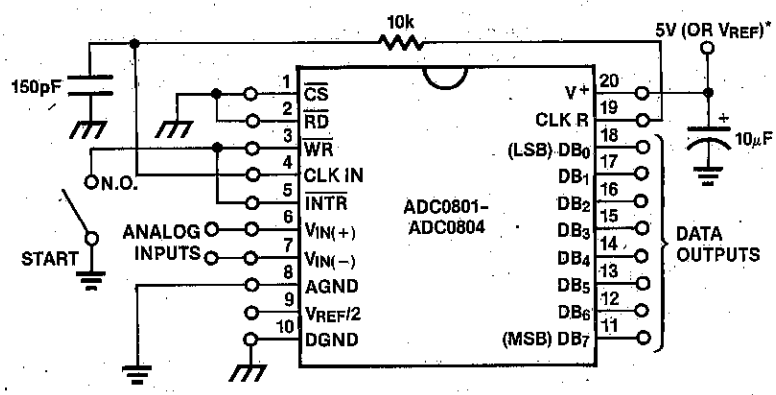


Figure 8. Free-Running Connection

4

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in 3-state (high-impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see **Typical Performance Characteristics**).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be 3-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V+ pin and values of 1μF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see **Zero Error** for measurement). Further information can be found in AN18.

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 9.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560V and a V+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090V (5.120 – 1½ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF}/2$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

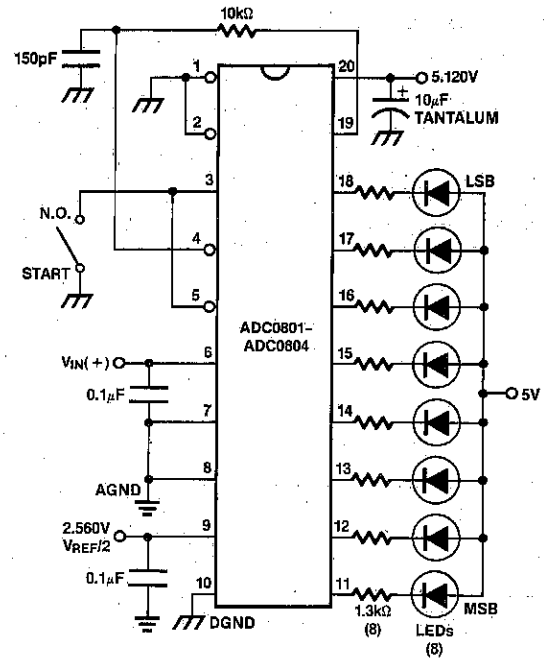


Figure 9. Basic Tester for the A/D

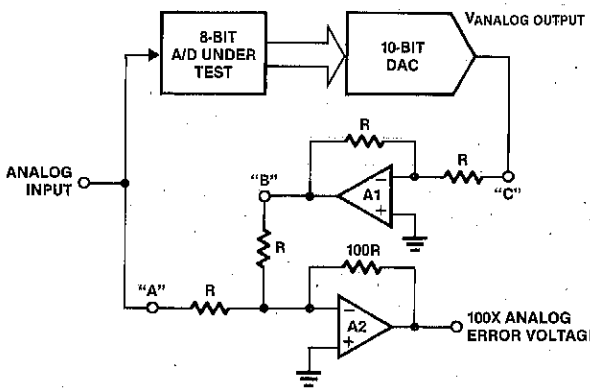


Figure 10. A/D Tester with Analog Error Output. This circuit can be used to generate "error plots" of Figure 1.

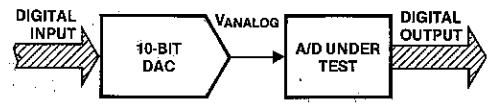


Figure 11. Basic "Digital" A/D Tester

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full-scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right)(5.12)\,V.$$

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so

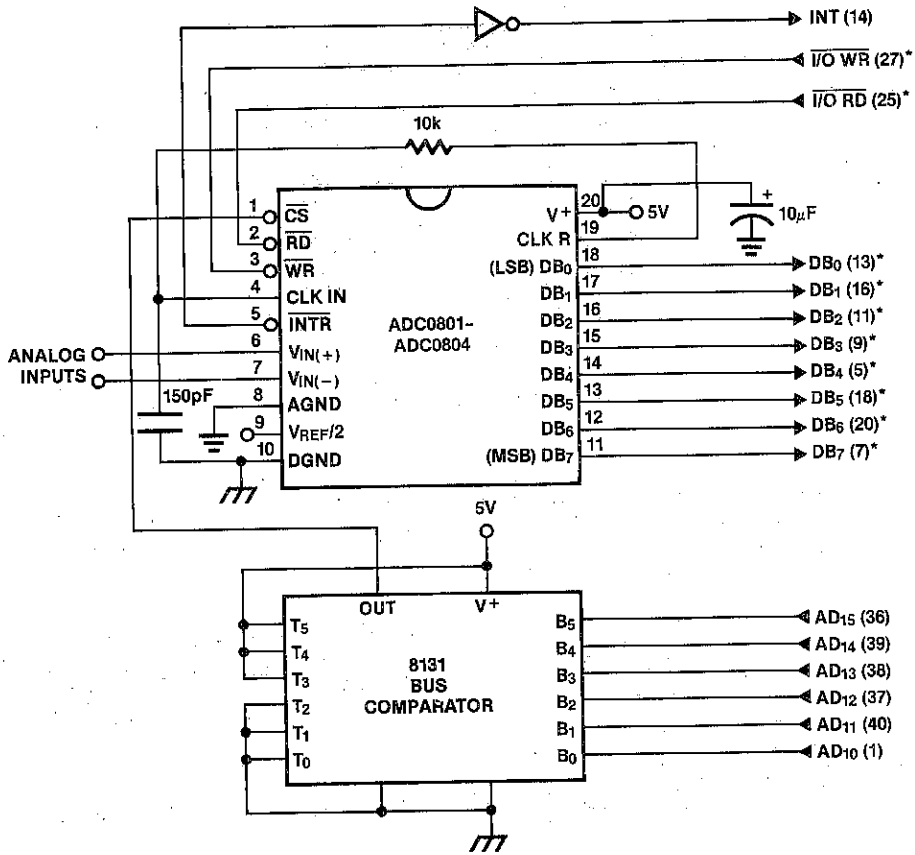
$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256}\right)(5.12) = 3.64V.$$

Figures 10 and 11 show more sophisticated test circuits.

APPLICATIONS

Interfacing MCS-48, and MCS-80/85 Processors

This converter has been designed to directly interface with an MCS-80/85 microprocessor or system. The 3-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 — A7 (or address bits A8 — A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See A020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 12.



*Note: Pin numbers for 8228 system controller; others are 8080A

Figure 12. ADC0801 to 8080A CPU Interface

The standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control busses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 13. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an IO/$\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 13 can again be used, with IO/$\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO}$/M for an I/O-mapped connection.

Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 14 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using 1/2 DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 15 the ADC0801 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

- **A016** "Selecting A/D Converters," by Dave Fullagar.
- **A018** "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- **A020** "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.
- **A030** "The ICL7104—A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.
- **R005** "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

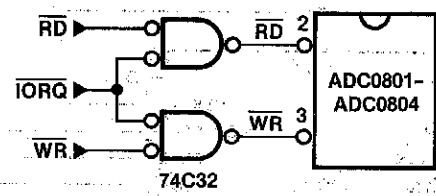
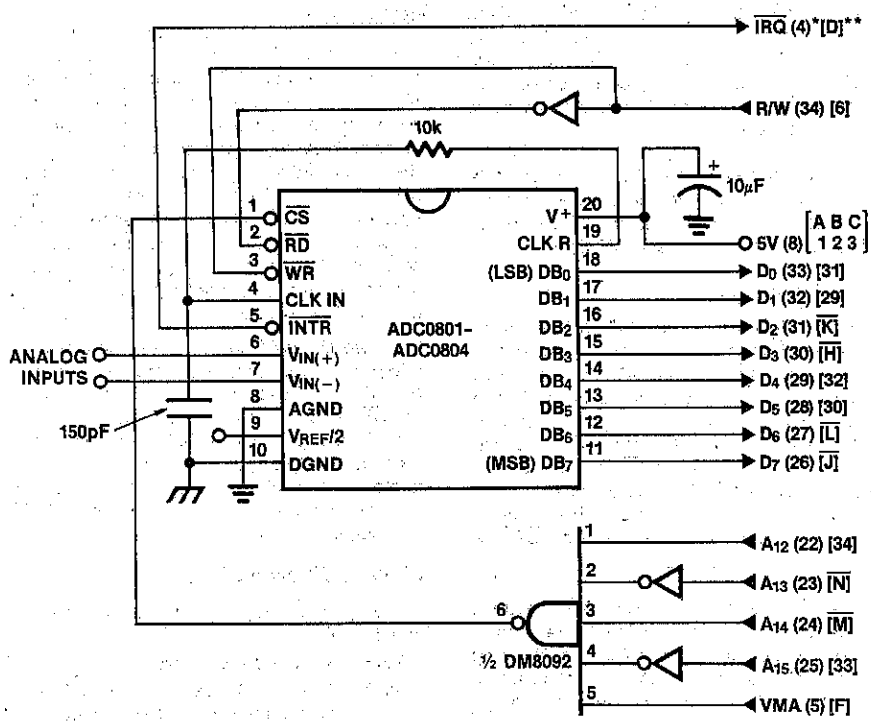


Figure 13. Mapping the A/D as an I/O device for use with the Z-80 CPU



*Note 1: Numbers in parentheses refer to MC6800 CPU pinout.
**Note 2: Numbers or letters in brackets refer to standard MC6800 system common bus code.

Figure 14. ADC0801 to MC6800 CPU Interface

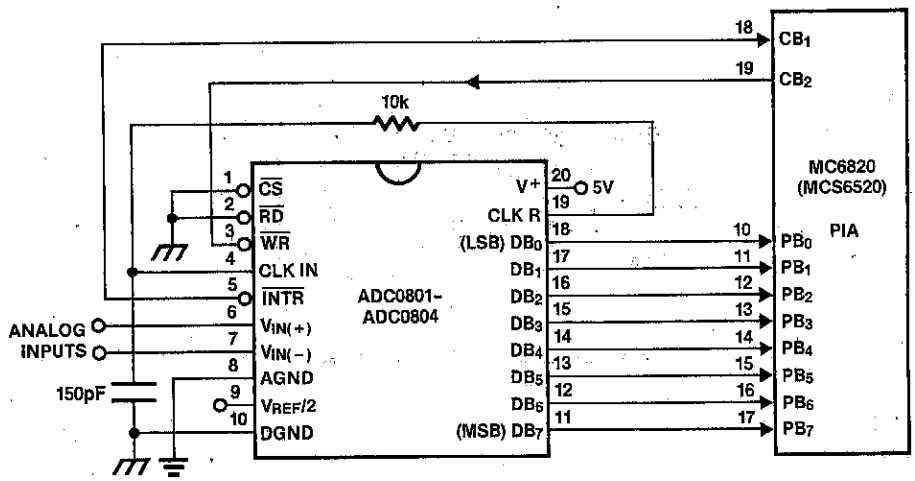
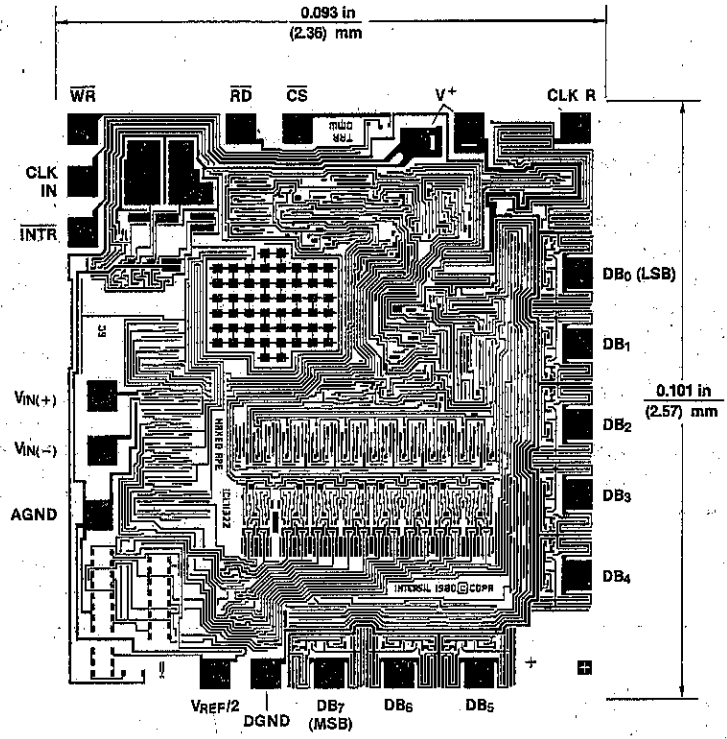


Figure 15. ADC0801 to MC6820 PIA Interface

CHIP TOPOGRAPHY



ICL7106/7107

3½-Digit Single Chip A/D Converter

FEATURES

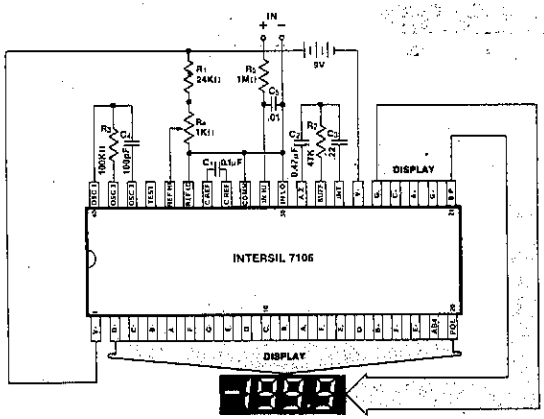
- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA typical input current.**
- **True differential input and reference.**
- **Direct display drive - no external components required. — LCD ICL7106**
  — LED ICL7107
- **Low noise - less than 15μV p-p.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**
- **Evaluation Kit available.**

4

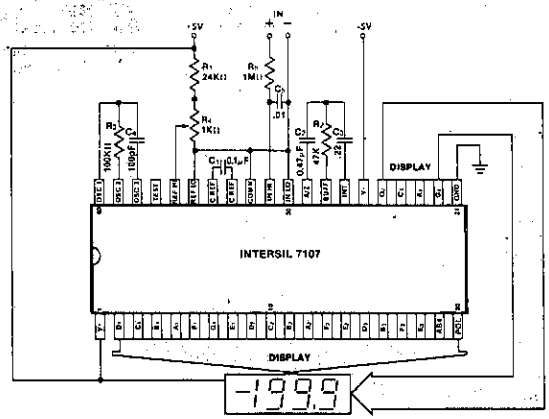
GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3½-digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and roll-over error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7106), enabling a high performance panel meter to be built with the addition of only 7 passive components and a display.



ICL7106 with Liquid Crystal Display

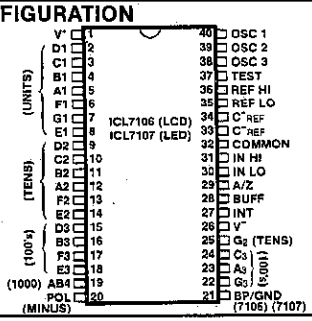


ICL7107 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7106	40 pin ceramic DIP	0°C to +70°C	ICL7106CDL
7106	40 pin plastic DIP	0°C to +70°C	ICL7106CPL
7106	40 pin CERDIP	0°C to +70°C	ICL7106CJL
7107	40 pin CERDIP	0°C to +70°C	ICL7107CJL
7107	40 pin ceramic DIP	0°C to +70°C	ICL7107CDL
7107	40 pin plastic DIP	0°C to +70°C	ICL7107CPL
7106 Kit 7107 Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware.		ICL7106EV/Kit ICL7107EV/Kit

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V^+ to V^- 15V
- ICL7107, V^+ to GND ..... +6V
- ICL7107, V^- to GND ..... −9V

Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7106 ..... TEST to V^+
- ICL7107 ..... GND to V^+

Power Dissipation (Note 2)
- Ceramic Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN}$ = 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current | Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment voltage = 3V	5 10	8.0 16		mA mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25° C, f_{clock} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

TEST CIRCUITS

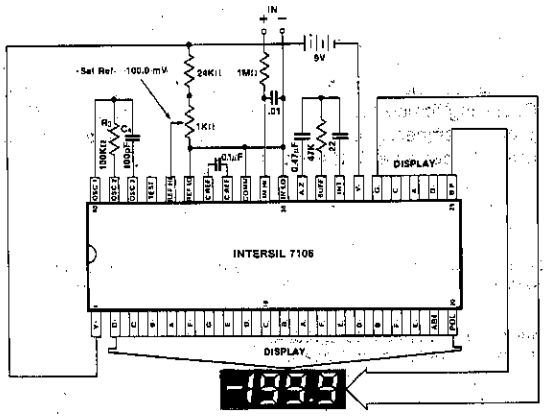


Figure 1: 7106

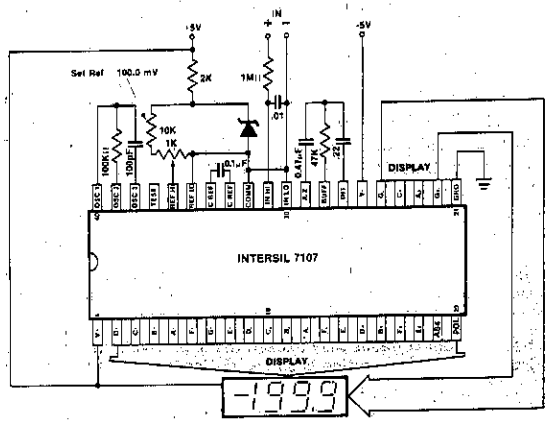


Figure 2: 7107

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

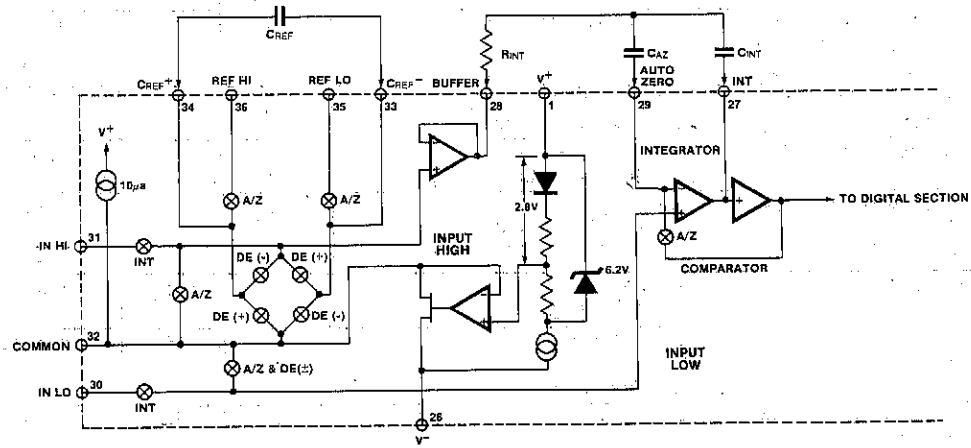


Figure 3: Analog Section of 7106/7107

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $(\frac{V_{IN}}{V_{REF}})$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80μVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

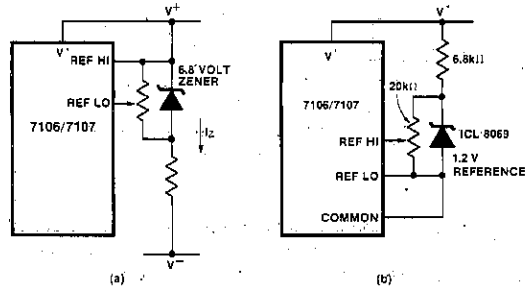


Figure 4: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

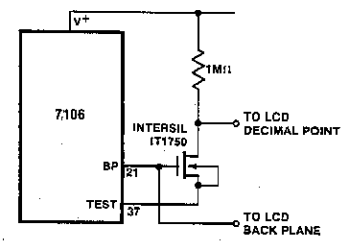


Figure 5: Simple Inverter for Fixed Decimal Point

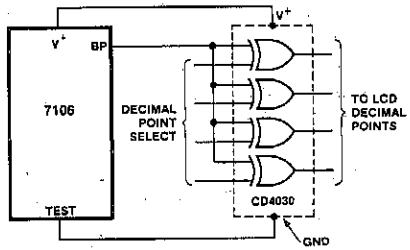


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled high (to V^+) all segments will be turned on and the display should read - 1888. The TEST pin will sink about 10mA under these conditions.

Caution: on the 7106, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7106 and 7107, respectively. In the 7106, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the 7107. It is identical to the 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

4

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

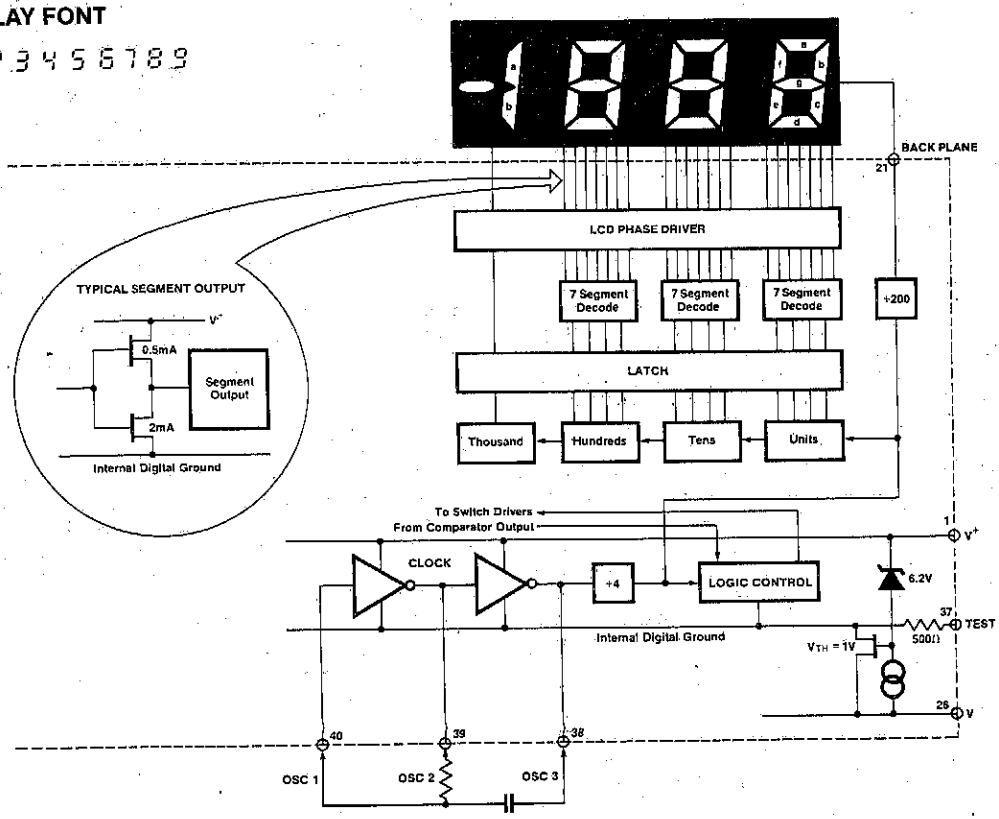


Figure 7: Digital Section 7106

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

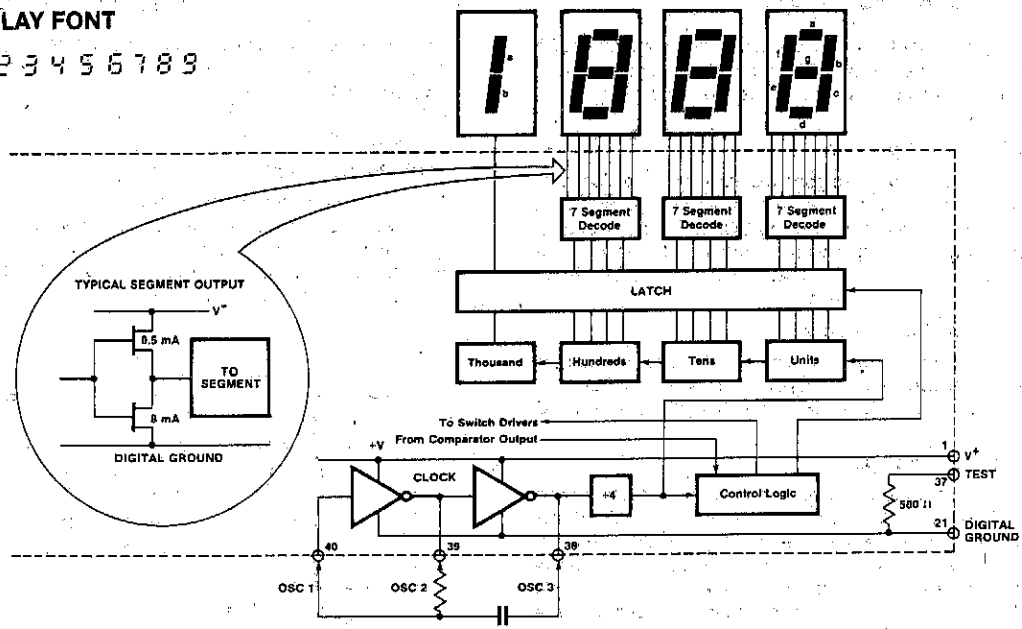


Figure 8: Digital Section 7107

4

System Timing

Figure 9 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

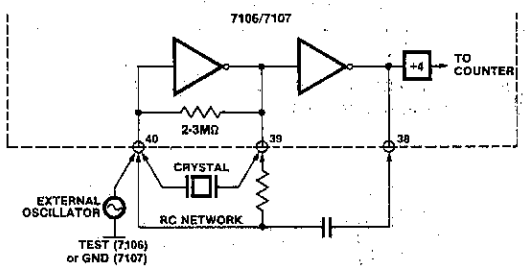


Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3 kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3 kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470KΩ is near optimum and similarly a 47KΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7106 or the 7107, when the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7107 with ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise

is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 100KΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select $V_{REF} = .341V$. Suitable values for integrating resistor and capacitor would be 120KΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this sytem occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7. 7107 Power Supplies

The 7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

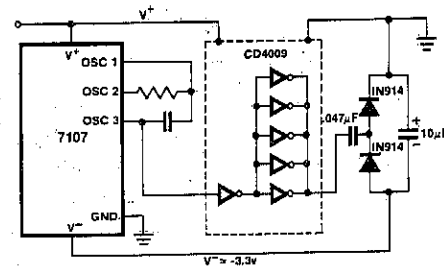


Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7106 and 7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

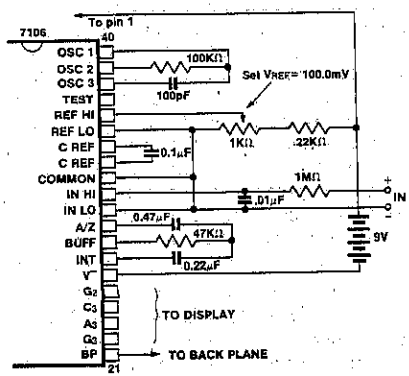


Figure 11: 7106 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

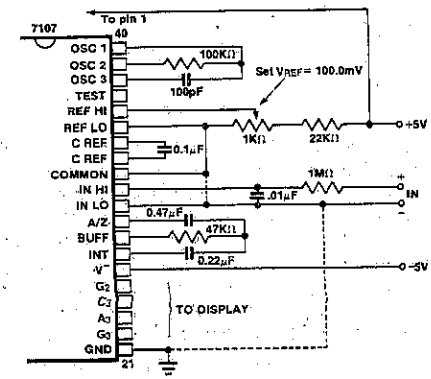


Figure 12: 7107 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

TYPICAL APPLICATIONS (Contd.)

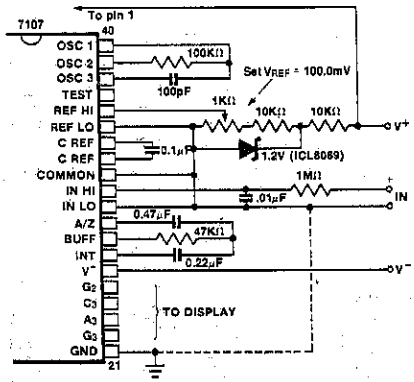


Figure 13: 7107 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply ground) and the pre-regulator is over-ridden.

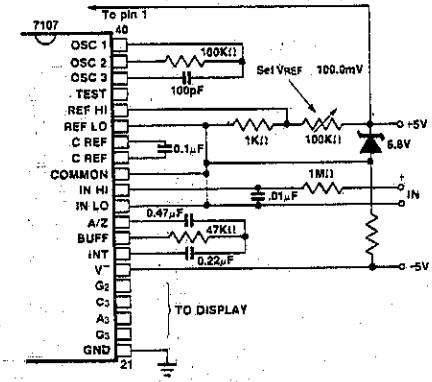


Figure 14: 7107 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 12, IN LO may be tied to either COMMON or GND.

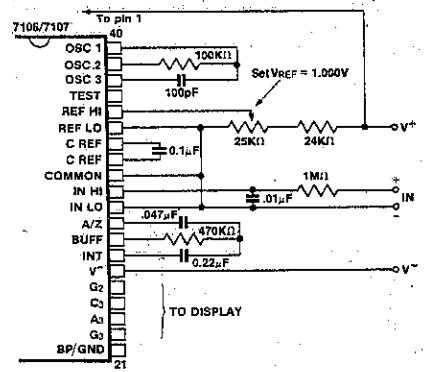


Figure 15: 7106/7107: Recommended component values for 2.000V full scale.

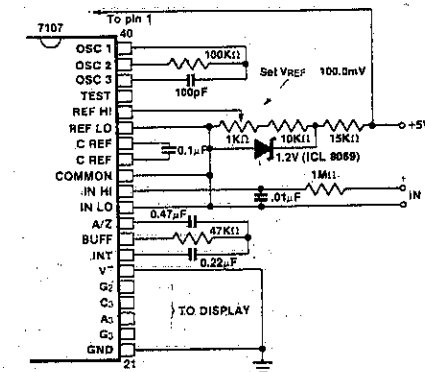


Figure 16: 7107 operated from single +5V supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

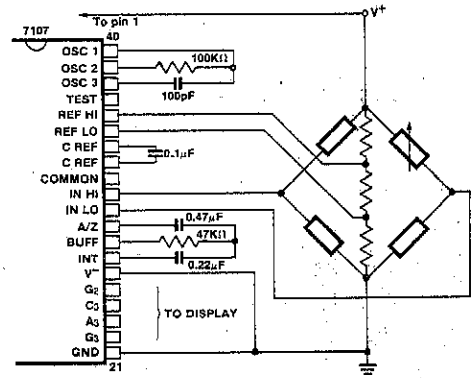


Figure 17: 7107 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

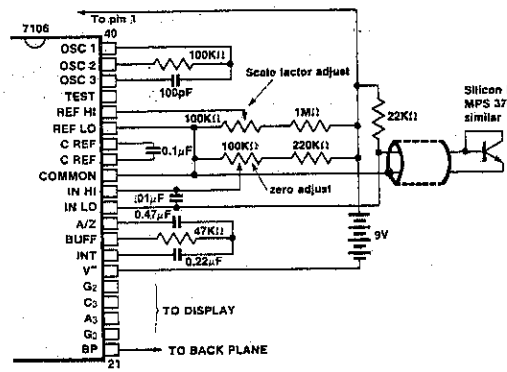


Figure 18: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

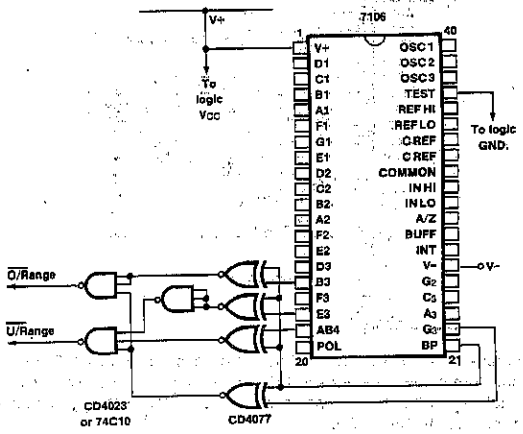


Figure 19: Circuit for developing Underrange and Overrange signals from 7106 outputs.

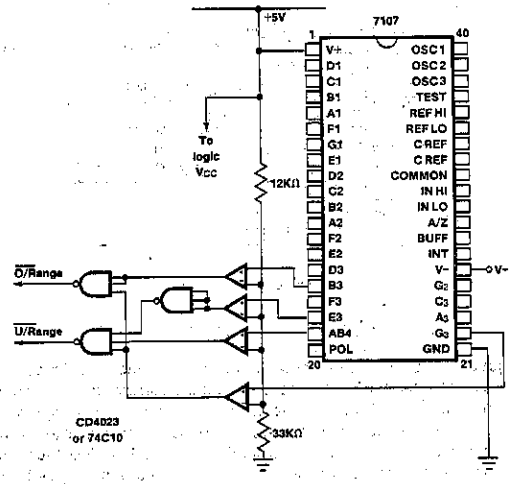


Figure 20: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

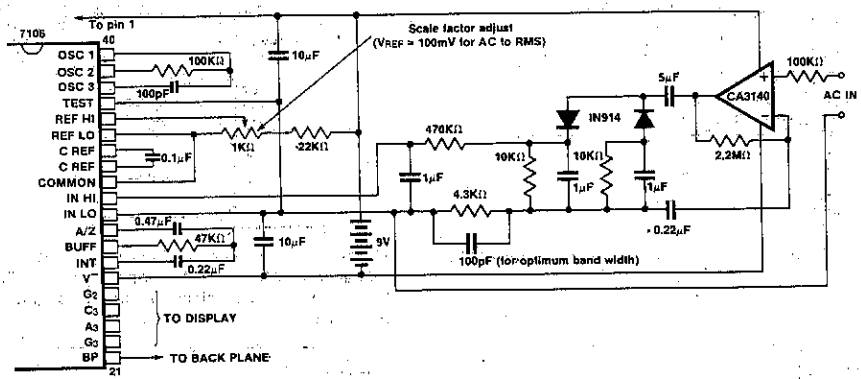


Figure 21: AC to DC Converter with 7106. TEST is used as a common mode reference level to ensure compatibility with most op-amps.

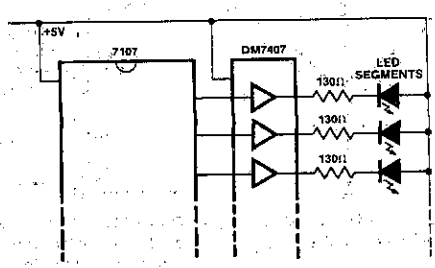


Figure 22: Display Buffering for increased drive current. Requires four DM7407 Hex Buffers. Each buffer is capable of sinking 40 mA.

7106/7107 EVALUATION KITS

After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

APPLICATION NOTES

A016 "Selecting A/D Converters", by David Fullagar.
A017 "The Integrating A/D Converter", by Lee Evans.
A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards", by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

ICL7109 12 Bit Binary A/D Converter for Microprocessor Interfaces

FEATURES

- **12 bit binary (plus polarity and overrange) dual slope integrating analog-to-digital converter.**
- **Byte-organized TTL-compatible three-state outputs and UART handshake mode for simple parallel or serial interfacing to microprocessor systems.**
- **RUN/HOLD input and STATUS output can be used to monitor and control conversion timing.**
- **True differential input and differential reference.**
- **Low noise — typically 15μV p-p.**
- **1pA typical input current.**
- **Operates at up to 30 conversions per second.**
- **On-chip oscillator operates with inexpensive 3.58MHz TV crystal giving 7.5 conversions per second for 60Hz rejection. May also be operated as RC oscillator for other clock frequencies.**
- **Fabricated using MAX-CMOS™ technology combining analog and digital functions on a single low power LSI CMOS chip.**
- **All inputs fully protected against static discharge; no special handling precautions necessary.**

GENERAL DESCRIPTION

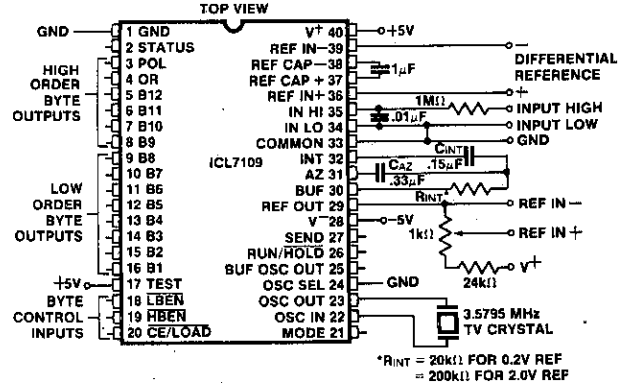
The ICL7109 is a high performance, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

The ICL7109 provides the user with the high accuracy, low noise, low drift, versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than 1μV/°C, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

PIN CONFIGURATION AND TEST CIRCUIT:

(See Figure 1 for typical connection to a UART or Microcomputer)



(OUTLINE DWGS DL, JL, PL)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7109	−55°C to +125°C	40-Pin Ceramic DIP	ICL7109MDL
7109	−20°C to +85°C	40-Pin Ceramic DIP	ICL7109IDL
7109	−20°C to +85°C	40-Pin CERDIP	ICL7109IJL
7109	0°C to 70°C	40-Pin Plastic DIP	ICL7109CPL

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply Voltage (GND to V^-) ..... -9V
Analog Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Digital Input Voltage ..... $V^+ + 0.3V$
(Pins 2-27) (Note 2) ..... GND - 0.3V
Power Dissipation (Note 3)
  Ceramic Package ..... 1W @ +85°C
  Plastic Package ..... 500mW @ +70°C
Operating Temperature
  Ceramic Package (MDL) ..... $-55°C \le T_A \le +125°C$
  (IDL) ..... $-25°C \le T_A \le +85°C$
  Plastic Package (CPL) ..... $0°C \le T_A \le +70°C$
Storage Temperature ..... $-55°C \le T_A \le +125°C$
Lead Temperature (soldering, 60 sec.) ..... +300°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE I OPERATING CHARACTERISTICS

All parameters with $V^+ = +5V$, $V- = -5V$, GND = 0V, $T_A = 25°C$, unless otherwise indicated.
Test circuit as shown on page 1.

4

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		V_{IN} = 0.0V Full Scale = 409.6mW	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	VCMR	Input Hi, Input Lo, Common	V-+1.5		V+-1.0	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale - 409.6mV		15		μV
Leakage current at Input	I_{LK}	V_{IN} = 0 All devices 25°C ICL7109CPL 0°C ≤ T_A ≤ +70°C ICL7109IDC -25°C ≤ T_A ≤ +85°C ICL7109MDL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV = > 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}	Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C
Input Common Mode Range	V_{CM}	IN HI, IN LO, COMMON	V^- +1.5	V+ -0.5 to V- +1.0	V+ -1.0	V

DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		V_{OH}	I_{OUT} = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage		V_{OL}	I_{OUT} = 1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current			Pins 18, 19, 20 V_{OUT} = V^+ –3V MODE input at GND		5		μA
Control I/O Loading			$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18			50	pF
Input High Voltage		V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			Pins 26, 27 V_{OUT} = V^+ –3V		5		μA
Input Pull-up Current			Pins 17, 24 V_{OUT} = V^+ –3V		25		μA
Input Pull-down Current			Pin 21 V_{OUT} = GND +3V		5		μA
Oscillator Output Current	High	O_{OH}	V_{OUT} = 2.5V		1		mA
	Low	O_{OL}	V_{OUT} = 2.5V		1.5		mA
Buffered Oscillator Output Current	High	BO_{OH}	V_{OUT} = 2.5V		2		mA
	Low	BO_{OL}	V_{OUT} = 2.5V		5		mA
MODE Input Pulse Width		t_W		50			ns

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA

Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.

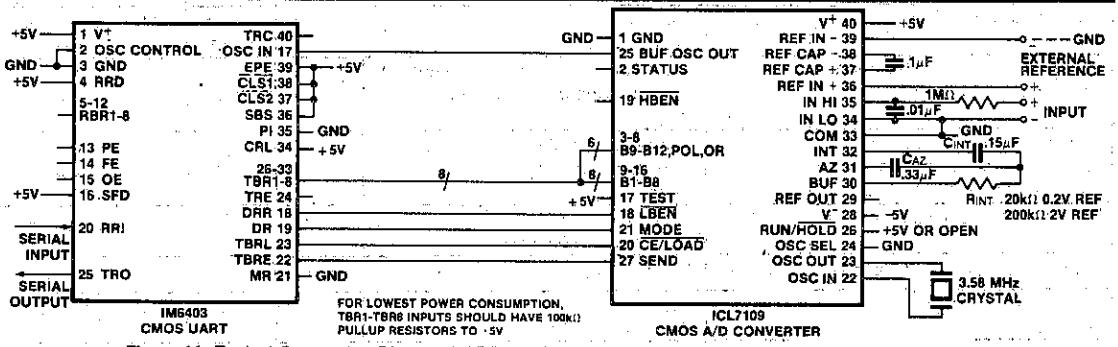


Figure 1A. Typical Connection Diagram UART Interface – To transmit latest result, send any word to UART

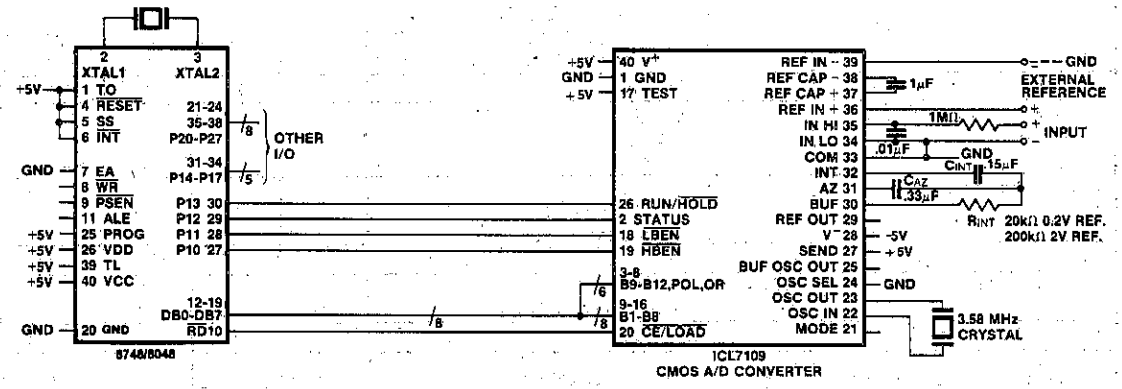


Figure 1B: Typical Connection Diagram Parallel Interface With MCS-48 Microcomputer

TABLE 2 - Pin Assignment and Function Description

PIN	SYMBOL	DESCRIPTION		
1	GND	Digital Ground, 0V, Ground return for all digital logic		
2	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.		
3	POL	Polarity - HI for Positive Input.		All three state output data bits
4	OR	Overrange - HI if Overranged.		
5	B12	Bit 12 (Most Significant Bit)		
6	B11	Bit 11	HI = true	
7	B10	Bit 10		
8	B9	Bit 9		
9	B8	Bit 8		
10	B7	Bit 7		
11	B6	Bit 6		
12	B5	Bit 5		
13	B4	Bit 4		
14	B3	Bit 3		
15	B2	Bit 2		
16	B1	Bit 1 (Least Significant Bit)		
17	TEST	Input High - Normal Operation. Input Low - Forces all bit outputs high. Note: This input is used for test purposes only. Tie high if not used.		
18	$\overline{LBEN}$	Low Byte Enable - With Mode (Pin 21) low, and $\overline{CE/LOAD}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. - With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 7, 8, 9.		
19	$\overline{HBEN}$	High Byte Enable - With Mode (Pin 21) low, and $\overline{CE/LOAD}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. - With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 7, 8, 9.		
20	$\overline{CE/LOAD}$	Chip Enable Load - With Mode (Pin 21) low, $\overline{CE/LOAD}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. - With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 7, 8, 9.		

PIN	SYMBOL	DESCRIPTION
21	MODE	Input Low - Direct output mode where $\overline{CE/LOAD}$ (Pin 20), $\overline{HBEN}$ (Pin 19) and $\overline{LBEN}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High - Causes immediate entry into handshake mode and output of data as in Figure 9. Input High - Enables $\overline{CE/LOAD}$ (Pin 20), $\overline{HBEN}$ (Pin 19), and $\overline{LBEN}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversion completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SEL	Oscillator Select - Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator - clock will be same phase and duty cycle as BUF OSC OUT. - Input low configures OSC IN, OSC OUT for crystal oscillator - clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/HOLD	Input High - Conversions continuously performed every 8192 clock pulses. Input Low - Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input - Used in handshake mode to indicate ability of an external device to accept data. Connect to + 5V if not used.
28	V^-	Analog Negative Supply - Nominally -5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output - Nominally 2.8V down from V^+ (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Node - Inside foil of C_{AZ}
32	INTEGRATOR	Integrator Output - Outside foil of C_{INT}
33	COMMON	Analog Common - System is Auto-Zeroed to COMMON
34	INPUT LO	Differential Input Low Side
35	INPUT HI	Differential Input High Side
36	REF IN +	Differential Reference Input Positive
37	REF CAP +	Reference Capacitor Positive
38	REF CAP	Reference Capacitor Negative
39	REF IN -	Differential Reference Input Negative
40	V^+	Positive Supply Voltage - Nominally +5V with respect to GND (Pin 1).

Note: All digital levels are positive true.

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent circuit of the Analog Section of the ICL7109. When the RUN/HOLD input is left open or connected to V^+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 3. They are (1) Auto-Zero (AZ), (2) Signal Integrate (INT) and (3) Deintegrate (DE).

1. **Auto-Zero Phase**

During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. **Signal Integrate Phase**

During signal integrate the auto-zero loop is opened, the internal short is removed and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time of 2048 clock periods. Note that this differential voltage can be within the common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

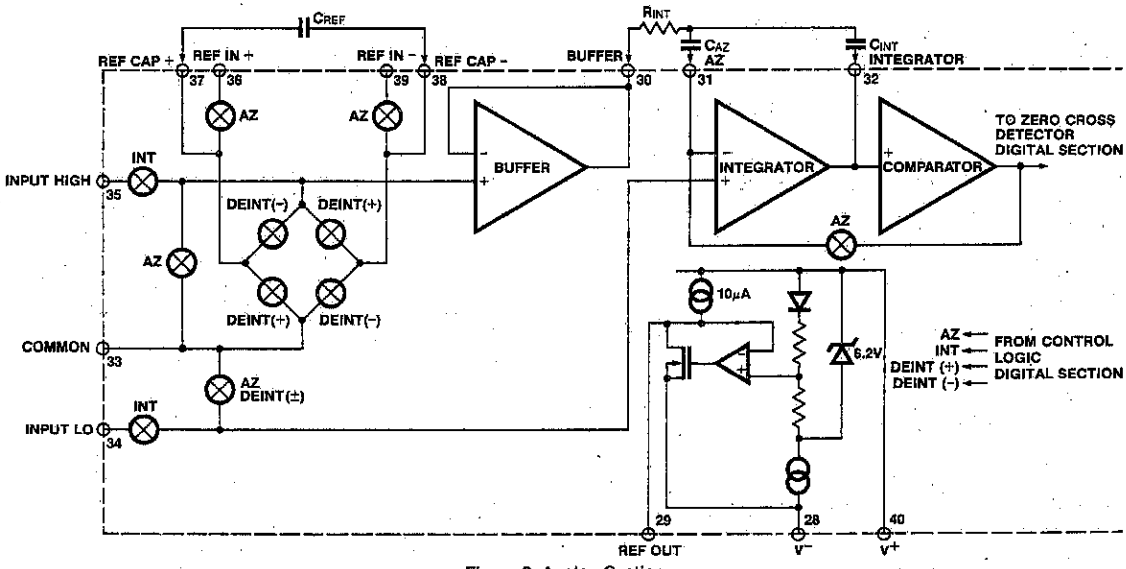


Figure 2: Analog Section

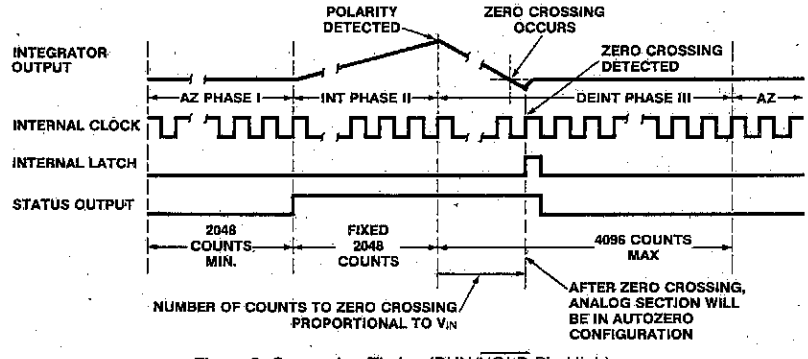


Figure 3: Conversion Timing (RUN/$\overline{HOLD}$ Pin High)

3. **De-Integrate Phase**

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.5 volts above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and –5V, this allows a 4V full scale integrator swing positive or negative maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (–) input voltage will give a roll-over error. However, by

selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection below).

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, supplies of ±6V may be used.

1. **Integrating Resistor**

   Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.096 volt full scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

2. **Integrating Capacitor**

   The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3 volt from either supply). For the ICL7109 with ±5 volt supplies and analog common connected to GND, a ±3.5 to ±4 volt integrator output swing is nominal. For 7-1/2 conversions per second (61.72KHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15μF and 0.33μF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{(2048 \times \text{clock period})\,(20\mu A)}{\text{integrator output voltage swing}}$$

   An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. For the military temperature range, Teflon® capacitors are recommended. While their dielectric absorption characteristics vary somewhat from unit to unit, selected devices should give less than 0.5 count of error due to dielectric absorption.

3. **Auto-Zero Capacitor**

   The size of the auto-zero capacitor has some influence on the noise of the system; a big capacitor, giving less noise. However, it cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and more important the error that exists at the end of an auto-zero cycle. For 409.6mv full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

   For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon®, or equivalent, capacitors are recommended above 85°C for their low leakage characteristics.

4. **Reference Capacitor**

   A 1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the reference low is not at analog common) and a 409.6mV scale is used, a larger value is required to prevent roll-over error. Generally 10μF will hold the roll-over error to 0.5 count in this instance. Again, Teflon®, or equivalent capacitors should be used for temperatures above 85°C for their low leakage characteristics.

5. **Reference Voltage**

   The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. Thus for a normalized scale, a reference of 2.048V should be used for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 34k and 0.15μF. This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

6. **Reference Sources**

   The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error.

For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80ppm/°C typ. When using the onboard reference, REF OUT (Pin 29) should be connected to REF – (pin 39), and REF + should be connected to the wiper of a precision potentiometer between REF OUT and V^+. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048mV reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between REF OUT and V^+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink enough current to destroy the device. This can be avoided by placing a 1kΩ resistor in series with pin 39.

4

DETAILED DESCRIPTION

Digital Selection

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic, as shown in the Block Diagram, Figure 4.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in Table 1 "Operating Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V^+ (high). Inputs driven from TTL gates should have 3-5kΩ pull-up resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/$\overline{\text{HOLD}}$ Input

When the RUN/$\overline{\text{HOLD}}$ input is high, or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If RUN/$\overline{\text{HOLD}}$ goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If RUN/$\overline{\text{HOLD}}$ stays or goes low, the converter will ensure minimum Auto-Zero time, and then wait in Auto-Zero until the RUN/$\overline{\text{HOLD}}$ input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at RUN/$\overline{\text{HOLD}}$. See Figure 5 for details.

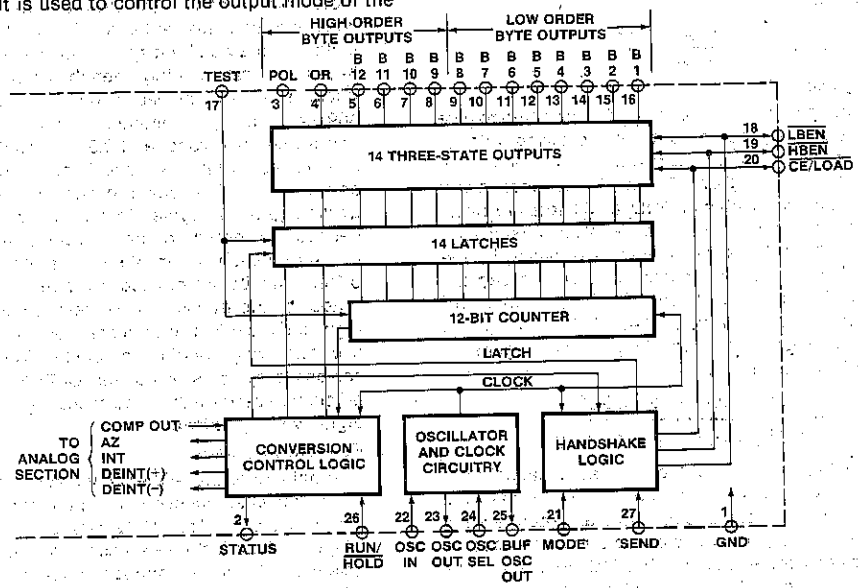


Figure 4: Digital Section

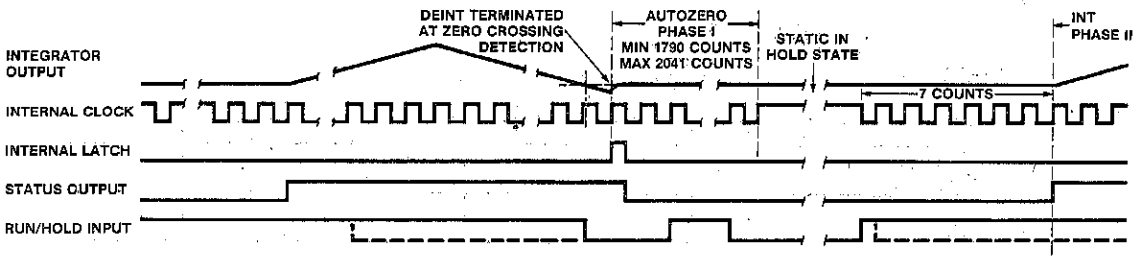


Figure 5: Run/Hold Operation

Using the RUN/HOLD input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in auto-zero with RUN/HOLD low. When RUN/HOLD goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). RUN/HOLD may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion.

Alternately, RUN/HOLD can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/HOLD input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A032 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/HOLD input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/HOLD to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated, on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled "Interfacing." The timing requirements for these outputs are shown in Figure 6 and Table 3.

Table 3 - Direct Mode Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{BEA}	Byte Enable Width	350	220		ns
t_{DAB}	Data Access Time from Byte Enable		210	350	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	400	260		ns
t_{DAC}	Data Access Time from Chip Enable		260	400	ns
t_{DHC}	Data Hold Time from Chip Enable		240	400	ns

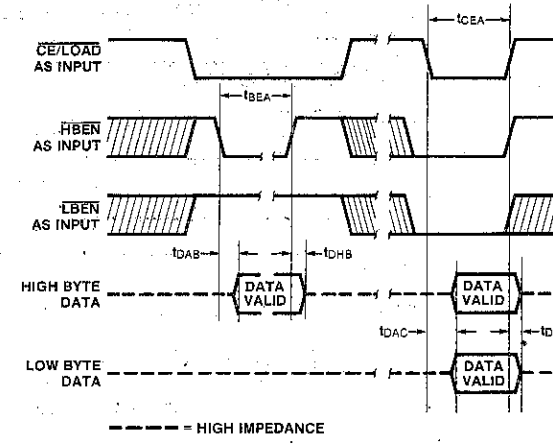


Figure 6: Direct Mode Output Timing

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7109 provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (See Figures 7 and 8). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry

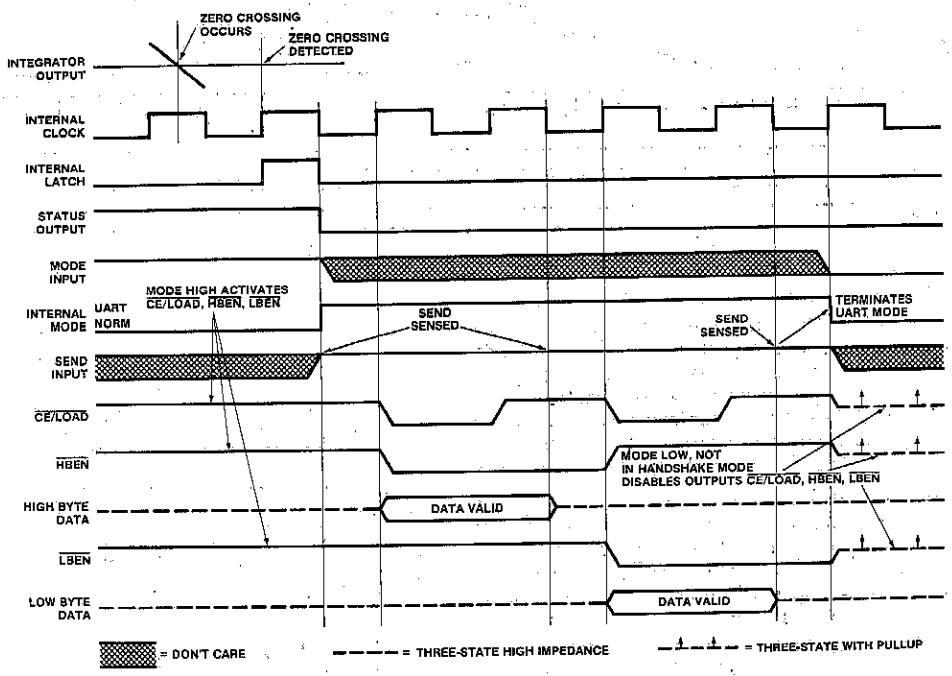


Figure 7: Handshake With Send Held Positive

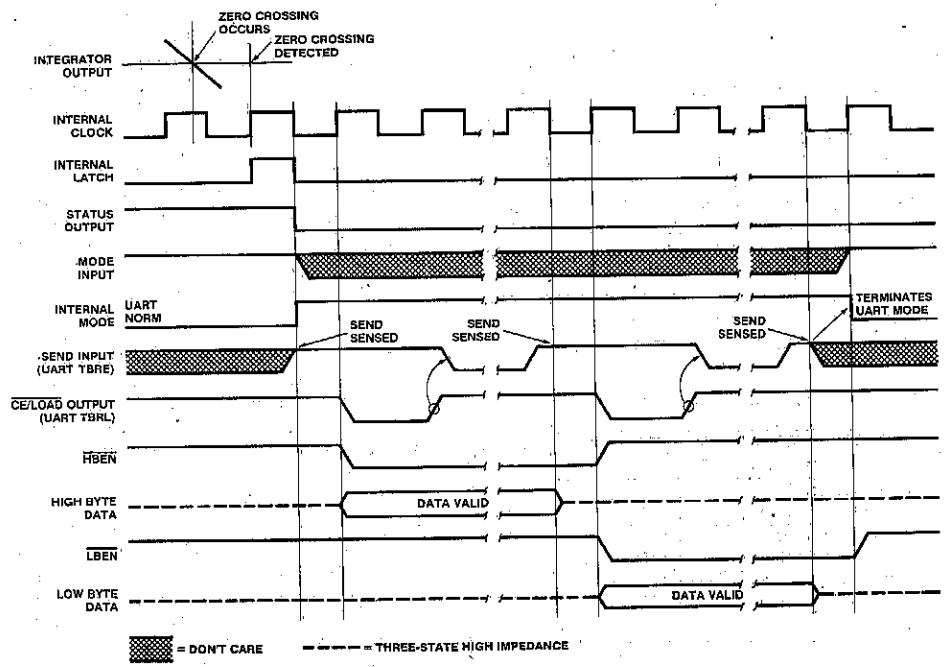


Figure 8: Handshake - Typical UART Interface Timing

into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 9) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 7, 8, and 9).

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

Figure 7 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{CE/LOAD}$, $\overline{LBEN}$ and $\overline{HBEN}$ terminals are active as outputs). The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{CE/LOAD}$ and the $\overline{HBEN}$ outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The $\overline{CE/LOAD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte enable remains low for two clock periods. Thus the $\overline{CE/LOAD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{CE/LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 8 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE/LOAD}$ terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The $\overline{CE/LOAD}$ and $\overline{HBEN}$ terminals will go low after SEND is sensed, and the high order byte outputs become active. When $\overline{CE/LOAD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7109

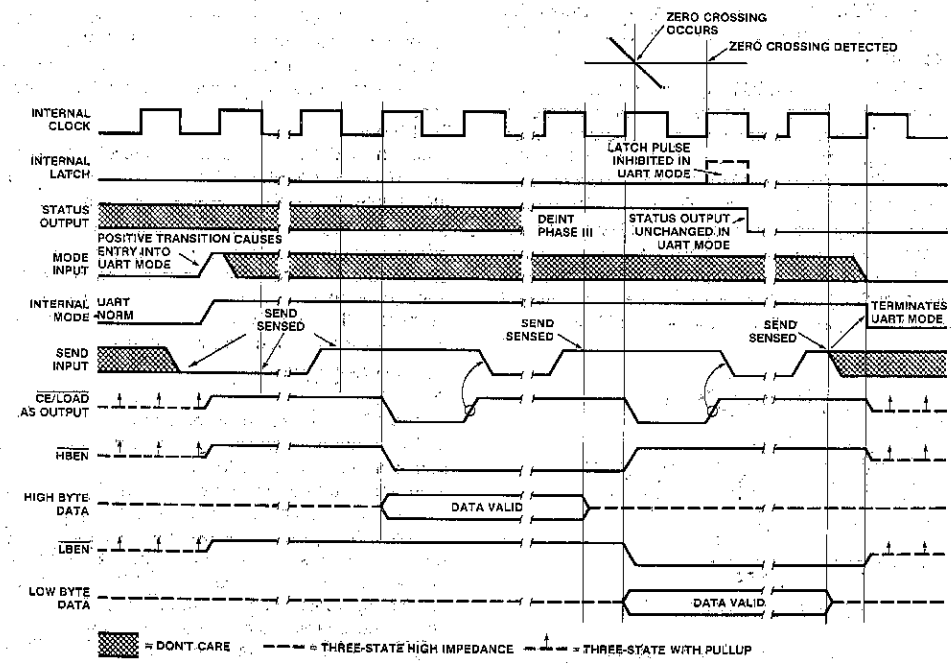


Figure 9: Handshake Triggered By Mode

internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE/LOAD}$ and $\overline{LBEN}$ outputs go low, and the low order byte outputs become active. Similarly, when the $\overline{CE/LOAD}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the $\overline{CE/LOAD}$, $\overline{HBEN}$, and $\overline{LBEN}$ terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/$\overline{HOLD}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

4

Oscillator

The ICL7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 10. The circuit will oscillate at a frequency given by f = 0.45/RC. A 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period (but not less than 50pF).

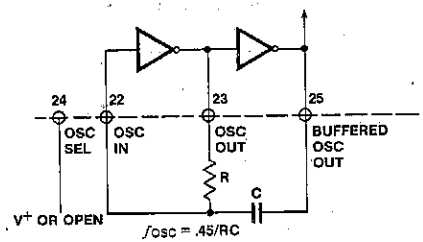


Figure 10: RC Oscillator

When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 11, the

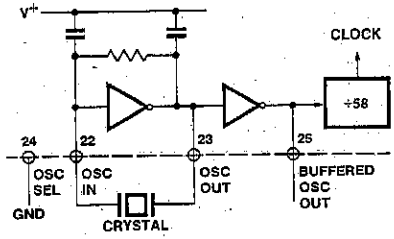


Figure 11: Crystal Oscillator

oscillator will operate with most crystals in the 1 to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. Using an inexpensive 3.58MHz TV crystal, this division ratio provides an integration time given by:

$$T = (2048 \text{ clock periods}) \times \left(\frac{58}{3.58\text{MHz}}\right) = 33.18\text{ms}$$

This time is very close to two 60Hz periods or 33.33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.

If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive, and when driving more than one slave device, external buffering should be used.

Test Input

When the TEST input is taken to a level halfway between V^+ and GND, the counter output latches are enabled, allowing the counter contents to be examined anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the 1/2 (V^+–GND) voltage (or to V^+) and one clock is applied, all the counter outputs will be clocked to the low state. This allows easy testing of the counter and its outputs.

INTERFACING

Direct Mode

Figure 12 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ICL7109 to parallel data lines. The $\overline{CE/LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable as in Figure 12A. Figure 12B shows a configuration where the two byte enables are connected together. In this configuration, the $\overline{CE/LOAD}$ serves as a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 12C shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE/LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors.

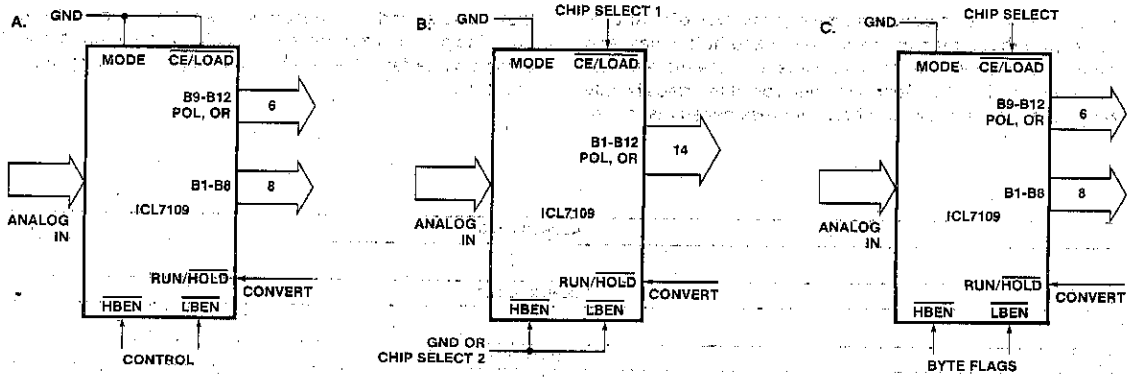


Figure 12: Direct Mode Chip and Byte Enable Combinations

Figure 13 shows an approach to interfacing several ICL7109s to a bus, ganging the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together, and using the $\overline{CE/LOAD}$ inputs (perhaps decoded from an address) to select the desired converter.

Some practical circuits utilizing the parallel three-state output capabilities of the ICL7109 are shown in Figures 14 through 19. Figure 14 shows a straightforward application to the Intel MCS-48, -80 and -85 systems via an 8255PPI, where the ICL7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated will lead to scrambled data. This will occur very rarely, in the proportion of setup-skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than 1/2 converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 15. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data. This application also shows the $\overline{RUN/HOLD}$ input being used to initiate conversions under software control.

A similar interface to Motorola MC6800 or MOS Technology MCS650X systems is shown in Figure 16. The high to low transition of the STATUS output generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the $\overline{RUN/HOLD}$ pin through Control Register B, allowing software-controlled initiation of conversions in this system also.

Figure 17 shows an interface to the Intersil IM6100 CMOS microprocessor family using the IM6101 PIE to control the data transfers. Here the data is read by the microprocessor in an 8-bit and a 6-bit word, directly from the ICL7109 to the microprocessor data bus. Again, the high to low transition of the STATUS output generates an interrupt leading to a software routine controlling the two read operations. As before, the $\overline{RUN/HOLD}$ input to the ICL7109 is shown as being under software control.

The three-state output capability of the ICL7109 allows direct interfacing to most microprocessor busses. Examples of this are shown in Figures 1, 18 and 19. It is necessary to

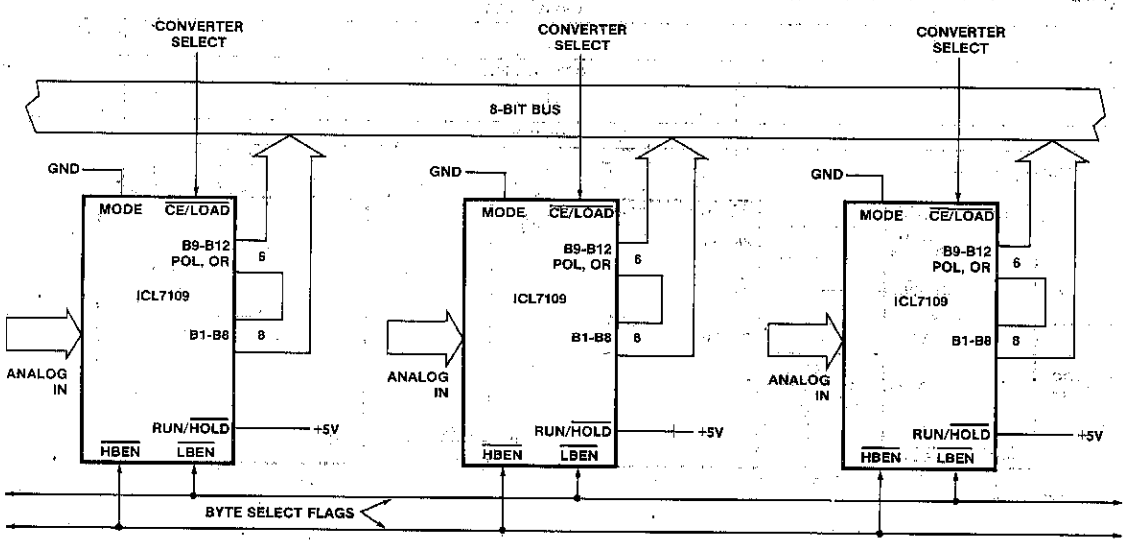


Figure 13: Three-stating Several 7109's to a Small Bus

carefully consider the system timing in this type of interface, to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long busses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

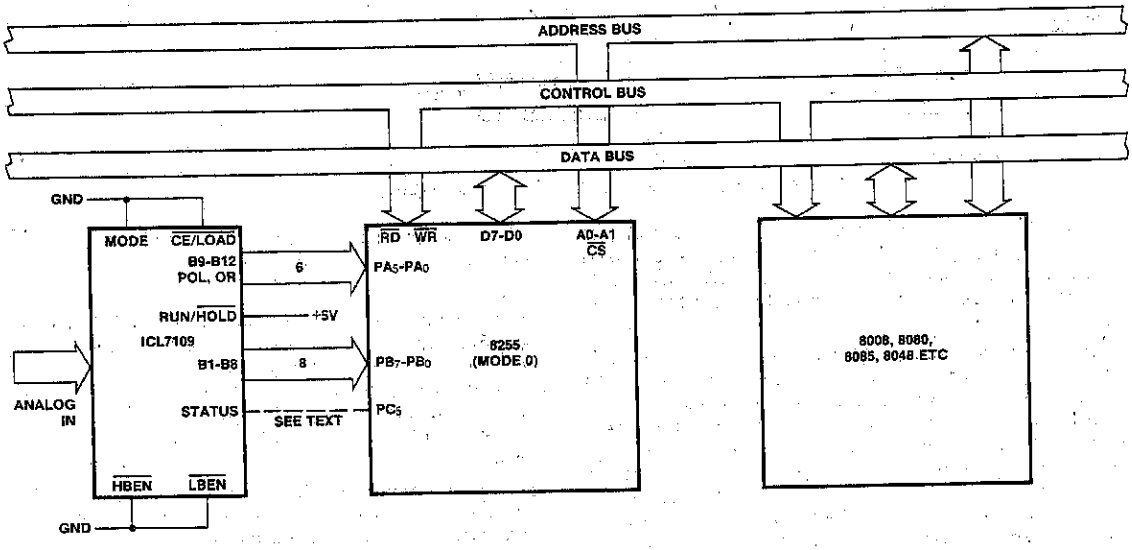


Figure 14: Full-time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

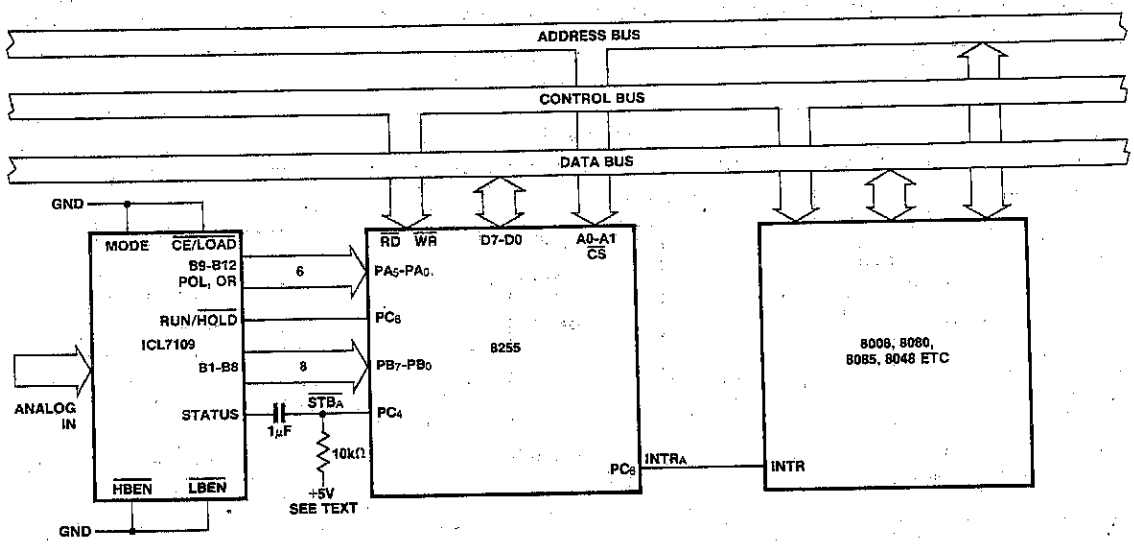


Figure 15: Full-time Parallel Interface to MCS-48, -80, -85 Microcomputers With Interrupt

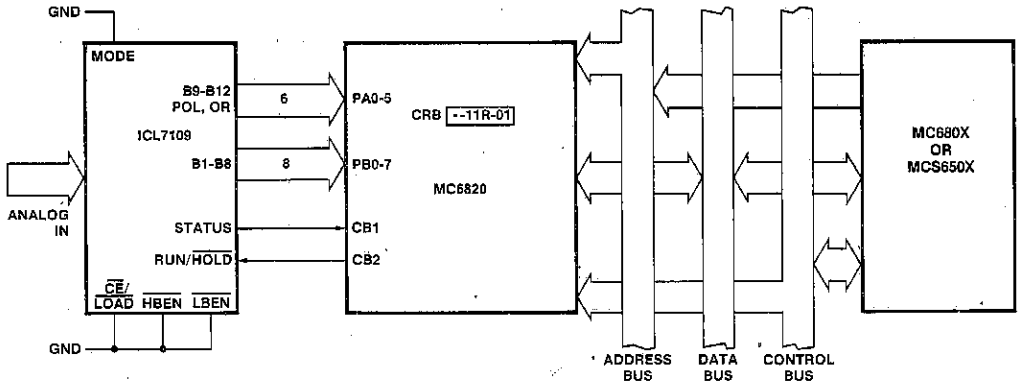


Figure 16: Full-time Parallel Interface to MC680X or MCS650X Microprocessors

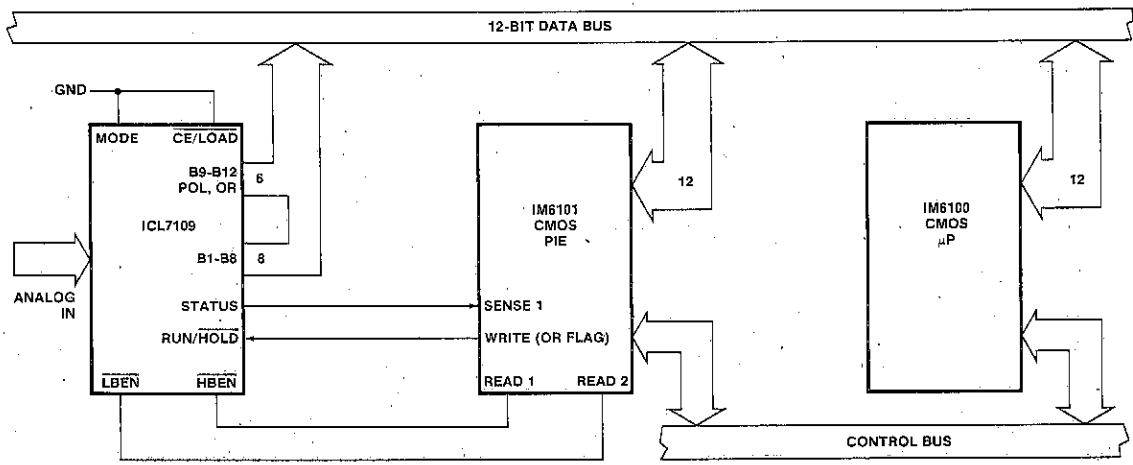


Figure 17: ICL7109-IM6100 Interface Using IM6101 PIE

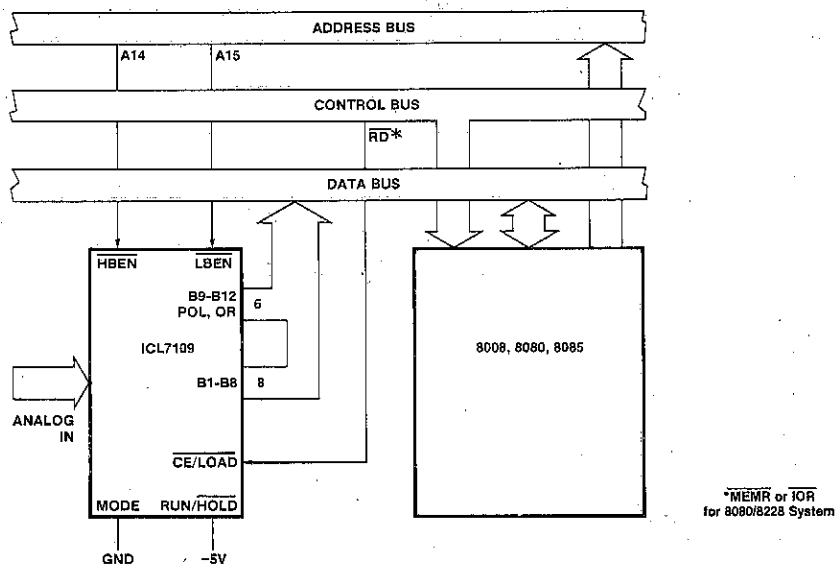


Figure 18: Direct Interface - ICL7109 to 8080/8085

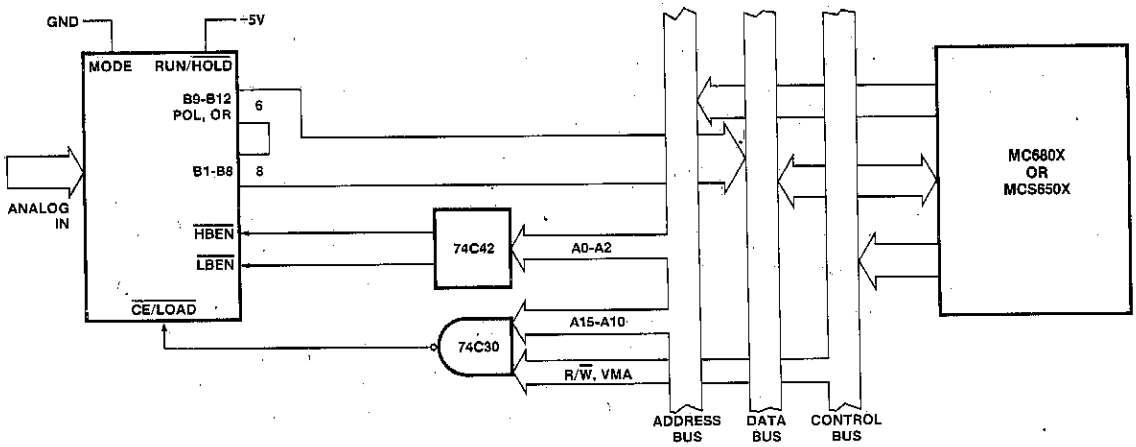


Figure 19: Direct ICL7109 - MC680X Bus Interface

Handshake Mode

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of $\overline{CE/LOAD}$, and the byte enables may be used as byte identification flags or as load enables.

Figure 20 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL7109, and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ICL7109 to sequence into the next byte. This figure shows the MODE input to the ICL7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/$\overline{HOLD}$ input to the ICL7109 may also be driven by a bit of the 8255 so that conversions may be obtained on command under software control. Note that one port of the 8255 is not used, and can service another peripheral device. The same arrangement can also be used with the 8155.

Figure 21 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/$\overline{HOLD}$ are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Intersil IM6402/6403 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown on page 3. In this circuit, any word received by the UART causes

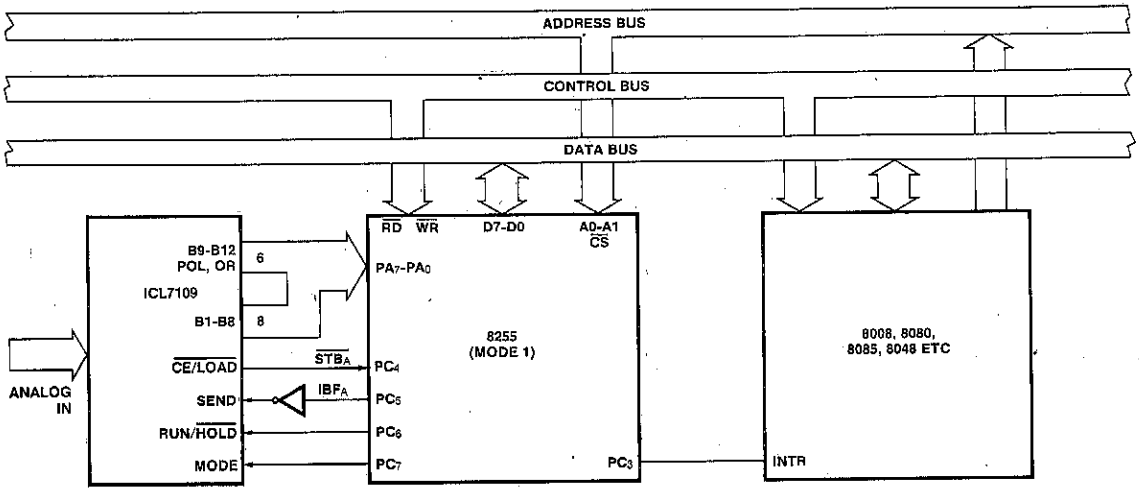


Figure 20: Handshake Interface - ICL7109 to MCS-48, -80, 85

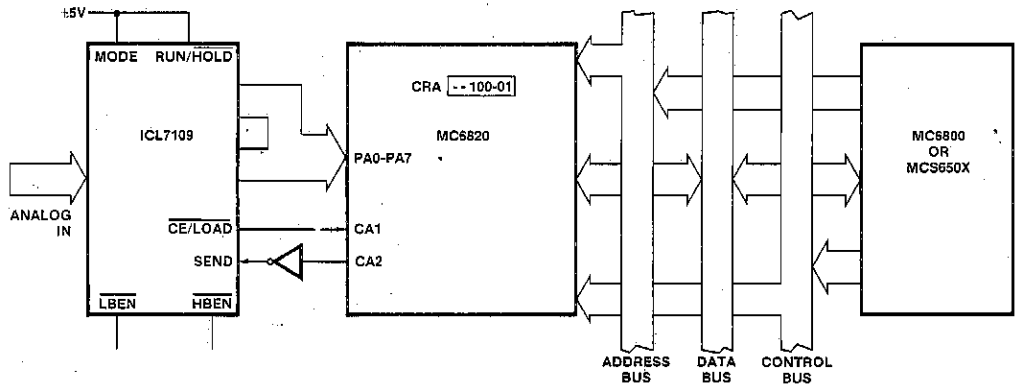


Figure 21: Handshake Interface - ICL7109 to MC6800, MCS650X

the UART DR (Data Ready) output to go high. This drives the MODE input to the ICL7109 high, triggering the ICL7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high and the second byte is output. When TBRE (SEND) goes high again, LBEN will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ICL7109 to the UART.

Figure 22 shows an extension of the one converter - one UART scheme of the Typical Connection to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ICL7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

The applications of the ICL7109 are not limited to those shown here. The purpose of these examples is to provide a starting point for users to develop useful systems, and to show some of the variety of interfaces and uses of the ICL7109. Many of the ideas suggested here may be used in combination; in particular the uses of the STATUS, RUN/HOLD, and MODE signals may be mixed.

4

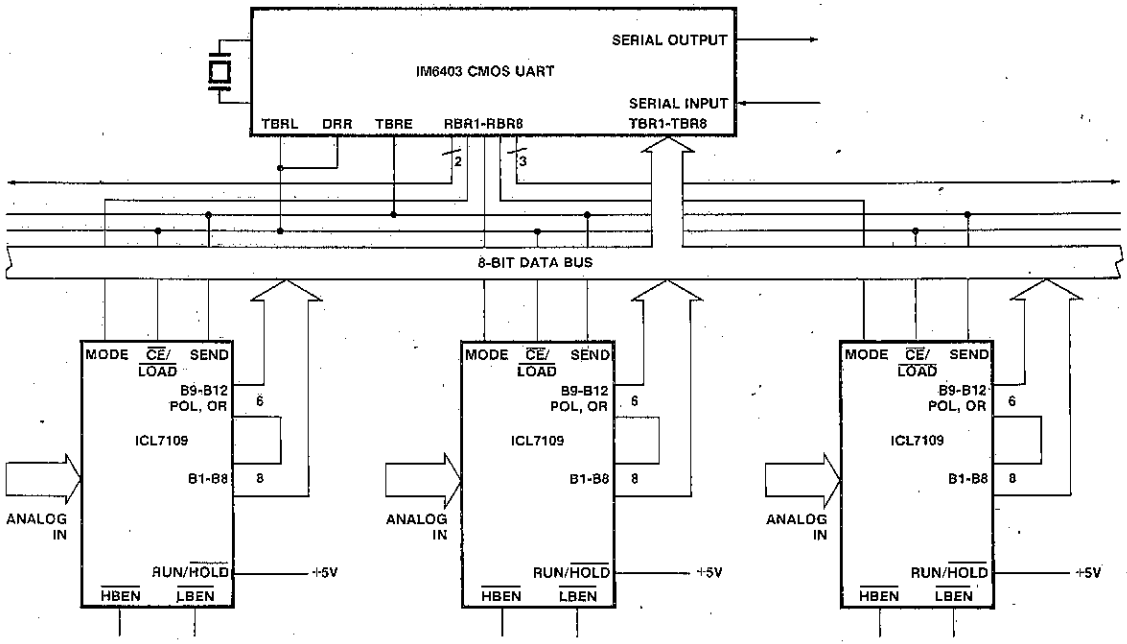


Figure 22: Multiplexing Converters with Mode Input

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converters," by Lee Evans
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family," by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

ICL7115

Fast CMOS Monolithic 14-Bit A/D Converter

FEATURES

- 14-bit linearity and resolution (0.003%)
- No missing codes
- Microprocessor compatible byte-organized buffered outputs
- Fast conversion (40μs)
- Auto-zeroed comparator for low offset voltage
- Low linearity and gain tempco (1ppm/°C, 4ppm/°C)
- Low power consumption (60mW)
- No gain or offset adjustment necessary (0.006% FS)
- Provides 3% useable overrange
- FORCE/SENSE and separate digital and analog ground pins for increased system accuracy

4

GENERAL DESCRIPTION

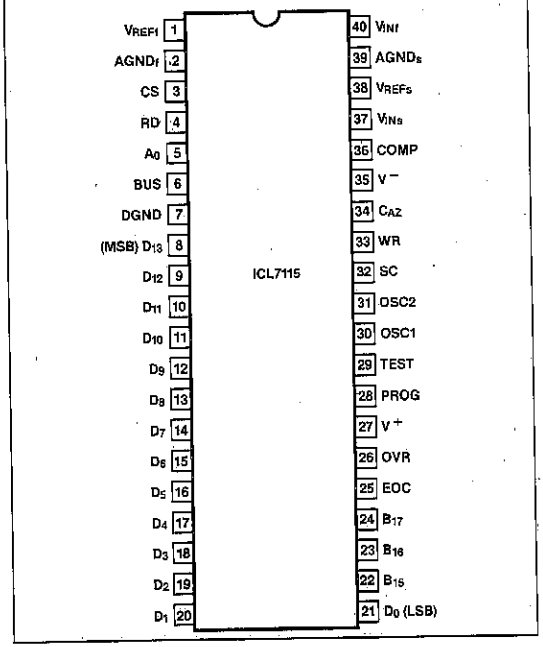
The ICL7115 is the first monolithic 14-bit accurate, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry with an on-chip PROM calibration table circuit to achieve 14-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is made easy by the use of standard WRite and ReaD cycle timing and control signals, combined with Chip Select and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8, 12, and 16-bit systems.

The ICL7115 provides separate Analog and Digital grounds. Analog ground, voltage reference and input voltage pins are separated into force and sense lines for increased system accuracy. Operating with ±5V supplies, the ICL7115 accepts 0V to +5V input with a −5V reference or 0V to −5V input with a +5V reference.

The ICL7115 is available in several versions with different accuracies, temperature ranges and packages. A Leadless Chip Carrier (LCC) package is also available; consult factory.

PIN CONFIGURATION (outline dwg JL)



ORDERING INFORMATION

ACCURACY	PACKAGE	TEMPERATURE	PART NUMBER
0.01%	40-Pin CERDIP	0°C to +70°C	ICL7115JCJL
0.01%	40-Pin CERDIP	−25°C to +85°C	ICL7115JIJL
0.01%	LCC	—	—
0.006%	40-Pin CERDIP	0°C to +70°C	ICL7115KCJL
0.006%	40-Pin CERDIP	−25°C to +85°C	ICL7115KIJL
0.006%	LCC	—	—
0.003%	40-Pin CERDIP	0°C to +70°C	ICL7115LCJL
0.003%	40-Pin CERDIP	−25°C to +85°C	ICL7115LIJL
0.003%	LCC	—	—

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND ..... −0.3V to +6.5V
Supply Voltage V^- to DGND ..... +0.3V to −6.5V
V_{REFs}, V_{REFf}, V_{INs}, V_{INf} to DGND ..... +25V to −25V
$AGND_s$, $AGND_f$ to DGND ..... +1V to −1V
Current in FORCE and SENSE Lines 25mA
Digital I/O Pin Voltages ..... −0.3V to V^+ +0.3V
PROG to DGND Voltage ..... V^- to V^+ +0.3V

Operating Temperature Range
ICL7115XCXX ..... 0°C to +70°C
ICL7115XIXX ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
derate above 70°C @ 100mW/°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Note 1: All voltages with respect to DGND, unless otherwise noted.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

$V^+ = +5.0V$, $V^- = -5.0V$, $V_{REFs} = +5.0V$, $T_A = +25°C$ unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		$\overline{SC}$ = High $\overline{SC}$ = Low	14 12			Bits
Total Unadjusted Error					1	LSB
Differential Non-Linearity		Full Operating Temperature Range		1/2		
Overall Accuracy (Note 3)		ICL7115J ICL7115K ICL7115L			0.01 0.006 0.003	% FSR
Full-Scale Error		$T_A = +25°C$ Operating Temperature Range (Note 2)		1/2 1	1 4	LSB ppm/°C
Zero Error		$T_A = +25°C$ Operating Temperature Range (Note 2)			1/8 4	LSB ppm/°C
Power Supply Rejection	PSRR	$T_A = +25°C$ Full Operating Temperature Range		1/16	1/8	LSB
V_{INs}, V_{REFs} Resistance	Z_{IN}, Z_{REF}	(Note 4) Operating Temperature Range	3	5 −300	7	kΩ ppm/°C
Low State Input Voltage	V_{il}	Operating Temperature Range			0.8	V
High State Input Voltage	V_{ih}	Operating Temperature Range	2.4			V
Logic Input Current	I_{iih}	$0 < V_{IN} < V^+$		1	10	μA
Low State Output Voltage	V_{ol}	$I_{OUT} = 3.2mA$ Operating Temperature Range			0.4	V
High State Output Voltage	V_{oh}	$I_{OUT} = -200\mu A$ Operating Temperature Range	2.8			V
Three-State Output Current	I_{ox}	$0 < V_{OUT} < V^+$		1		μA
Logic Input Capacitance	C_{in}	(Note 2)		15		pF
Logic Output Capacitance	C_{out}	Three-State (Note 2)		15		
Supply Voltage Range	V^+	Functional Operation	4.5		6.0	V
	V^-		−4.5		−6.0	
Supply Current	I^+	Excluding Ladder Current		5		mA
	I^-	$F_{CLK} = 1kHz$		5		

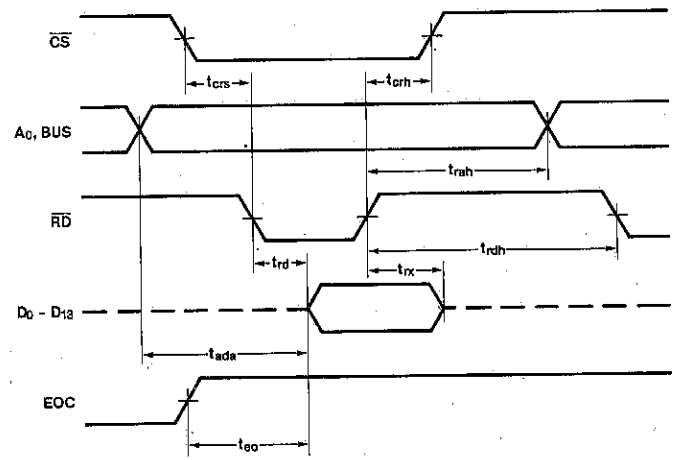
Note 2: Assumes all leads soldered or welded to printed circuit board.
Note 3: Full-scale range (FSR) is 10V (+5V to −5V).
Note 4: Guaranteed by design, not 100% tested in production.

AC ELECTRICAL CHARACTERISTICS $V^+ = +5.0V$, $V^- = -5.0V$, $T_A = +25°C$, unless otherwise noted

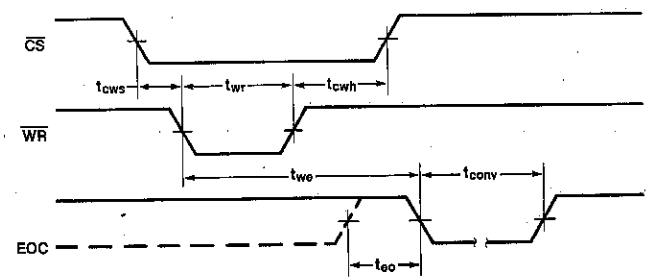
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Conversion Time	t_{conv}	$\overline{SC}$ = High			40	µs
		$\overline{SC}$ = Low			36	
Address to Data Access	t_{ada}			250		ns
ReaD Low to Data	t_{rd}			200		
ReaD High to Three-State	t_{rx}		20		100	
ReaD, Address Hold Time	t_{rah}				0	
ReaD Pulse Width High	t_{rdh}		200			
WRite Pulse Width Low	t_{wr}		200			
EOC High to Data	t_{ed}			200		
CS, WR Set-Up Time	t_{cws}				0	
CS, WR Hold Time	t_{cwh}				0	
CS, ReaD Set-Up Time	t_{crs}				0	
CS, ReaD Hold Time	t_{crh}				0	
EOC Pulse Width High	t_{eo}	Free-Run Mode		0.5		$1/f_{CLK}$
WRite Low to EOC Low	t_{we}	Wait Mode	1		2	

4

Read Cycle Timing



Write Cycle Timing



PIN DESCRIPTION TABLE

PIN	NAME	FUNCTION	
1	V_{REFf}	FORCE line for reference input	
2	$AGND_f$	FORCE input for analog ground	
3	$\overline{CS}$	Chip Select enables reading and writing (active low)	
4	$\overline{RD}$	ReaD (active low)	
5	A_0	Byte select (low = D_0 – D_7, high = D_8 – D_{13}, OVR)	
6	BUS	Bus select (low = outputs enabled by A_0, high = all outputs enabled together)	
7	DGND	Digital GrouND return	
8	D_{13}	Bit 13 (most significant)	High Byte
9	D_{12}	Bit 12	
10	D_{11}	Bit 11	
11	D_{10}	Bit 10	
12	D_9	Bit 9	
13	D_8	Bit 8	
14	D_7	Bit 7	Low Byte
15	D_6	Bit 6	
16	D_5	Bit 5	
17	D_4	Bit 4	
18	D_3	Bit 3	
19	D_2	Bit 2	
20	D_1	Bit 1	
21	D_0	Bit 0 (least significant)	

Output Data Bits (High = True)

PIN	NAME	FUNCTION
22	B_{15}	
23	B_{16}	Used for programming only (leave open)
24	B_{17}	
25	EOC	End Of Conversion flag (low = busy, high = conversion complete)
26	OVR	OVerRange flag (valid at end of conversion when output code exceeds full-scale, three-state output enabled with high byte)
27	V^+	Positive power supply input
28	PROG	Used for programming only. Tie to V^+ for normal operation
29	TEST	Used for programming only. Tie to V^+ for normal operation
30	OSC1	Oscillator inverter input
31	OSC2	Oscillator inverter output
32	$\overline{SC}$	Short cycle input (high = 14-bit, low = 12-bit operation)
33	WR	WRite pulse input (low starts new conversion)
34	C_{AZ}	Auto-zero capacitor connection
35	V^-	Negative power supply input
36	COMP	Used in test, tie to V^-
37	V_{INs}	SENSE line for input voltage
38	V_{REFs}	SENSE line for reference input
39	$AGND_s$	SENSE line for analog ground
40	V_{INf}	FORCE line for input voltage

4

I/O CONTROL TRUTH TABLE

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A_0	BUS	FUNCTION
0	0	x	x	x	Initiates a Conversion
1	x	x	x	x	Disables all Chip Commands
0	1	0	0	0	Low Byte is Enabled
0	1	0	1	0	High Byte is Enabled
0	1	0	x	1	Low and High Bytes Enabled Together
x	x	1	x	x	Disables Outputs (High-Impedance)

TRANSFER FUNCTION TABLE

INPUT VOLTAGE	EXPECTED OUTPUT CODE			
$V_{REF} = -5.0V$	OVR	MSB		LSB
0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0	0
+0.0003	0	0	0 0 0 0 0 0 0 0 0 0 0 0 1	1
+0.150	0	0	0 0 0 0 1 1 1 1 0 1 0 1	1
+2.4997	0	0	1 1 1 1 1 1 1 1 1 1 1 1 1	1
+2.500	0	1	0 0 0 0 0 0 0 0 0 0 0 0 0	0
+4.9994	0	1	1 1 1 1 1 1 1 1 1 1 1 1 1	0
+4.9997	0	1	1 1 1 1 1 1 1 1 1 1 1 1 1	1
+5.000	1	0	0 0 0 0 0 0 0 0 0 0 0 0 0	0
+5.0003	1	0	0 0 0 0 0 0 0 0 0 0 0 0 1	1
+5.150	1	0	0 0 0 0 1 1 1 1 0 1 0 1	1

DETAILED DESCRIPTION

The ICL7115 is basically a successive approximation A/D converter with an internal structure much more complex than a standard SAR-type converter. Figure 1 shows the functional block diagram of the ICL7115 14-bit A/D converter. The additional circuitry incorporated into the ICL7115 is used to perform error correction and to maintain the operating speed in the 40μs range.

The internal 17-bit DAC of the ICL7115 is designed around a radix of 1.85 rather than the traditional 2.00. This radix gives each bit of the DAC a weight of approximately 54% of the previous bit. The result is a useable range that extends to 3% beyond the full-scale input of the A/D. The actual value of each bit is measured and stored in the on-chip PROM. The absolute value of each bit weight then becomes relatively unimportant because of the error correction action of the ICL7115.

The output of the high-speed auto-zeroed comparator is fed to the data input of a 17-bit successive approximation register (SAR). This register is uniquely designed for the ICL7115 in that it tests bit pairs instead of individual bits in the manner of a standard SAR. At the beginning of the conversion cycle, the SAR turns on the MSB (B_{16}) and the MSB-4 bit (B_{12}). The sequence continues for each bit pair, B_x and B_{x-4}, until only the four LSBs remain. The sequence concludes by testing the four LSBs individually.

The SAR output is fed to the DAC register and to the preprogrammed 17-word by 17-bit PROM where it acts as PROM address. PROM data is fed to a 17-bit full-adder/accumulator where the decoded results from each successive phase of the conversion are summed with the previous results. After 20 clock cycles, the accumulator contains the final binary data which is latched and sent to the three-state output buffers. The accuracy of the A/D converter depends primarily upon the accuracy of the data that has been programmed into the PROM during the final test portion of the manufacturing process.

The error correcting algorithm built into the ICL7115 reduces the initial accuracy requirements of the DAC. The overlap in the testing of bit pairs reduces the accuracy requirements on the comparator which has been optimized for speed. Since the comparator is auto-zeroed, no external adjustment is required to get ZERO code for ZERO input voltage.

Twenty clock cycles are required for the complete 14-bit conversion. The auto-zero circuitry associated with the comparator is employed during the last three clock cycles of the conversion to cancel the effect of offset voltage. Also during this time, the SAR and accumulator are reset in preparation for the start of the next conversion. When the Short Cycle ($\overline{SC}$) input is low, 18 clock cycles are required to complete a 12-bit conversion.

The overflow output of the 17-bit full-adder is also the OVer-Range (OVR) output of the ICL7115. Unlike standard SAR-type A/D converters, the ICL7115 has the capability of providing valid useable data for inputs that exceed the full-scale range by as much as 3%.

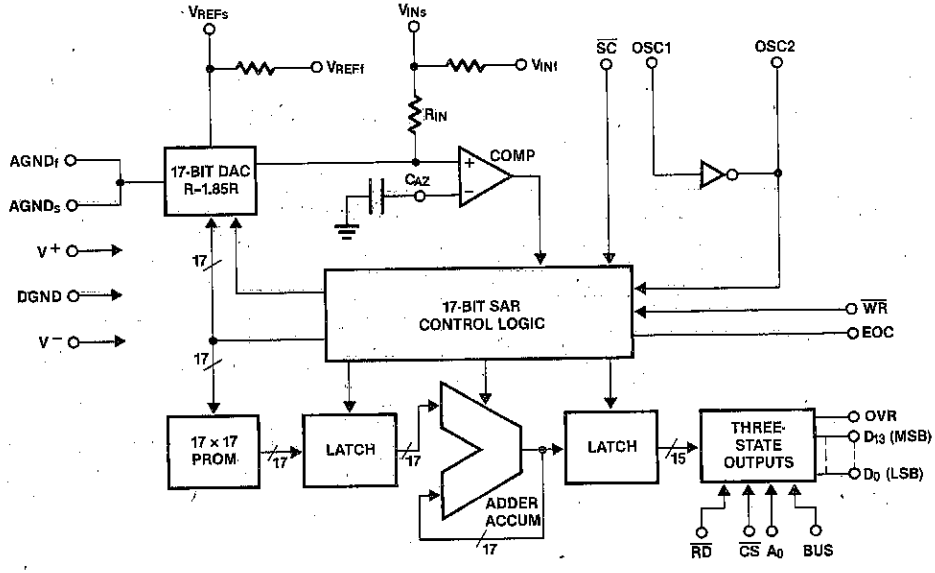


Figure 1. ICL7115 Functional Block Diagram

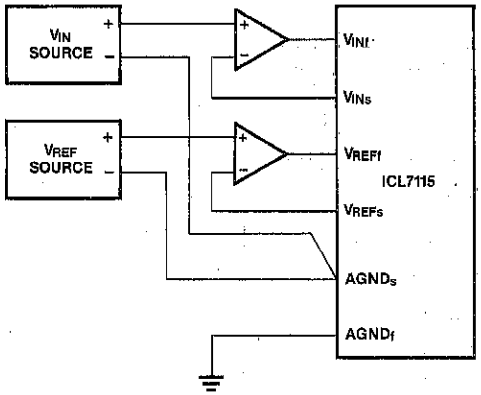


Figure 2. V_{IN} and V_{REF} Input Buffers

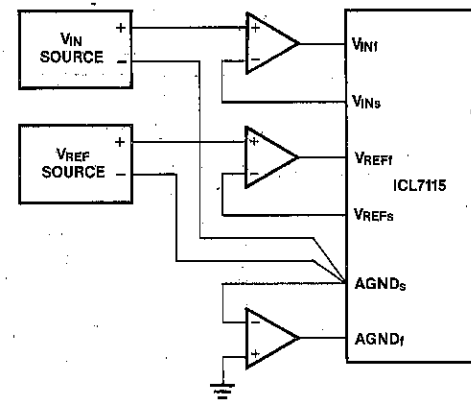


Figure 3. Using a Forced Ground

4

OPTIMIZING SYSTEM PERFORMANCE

In order to maintain full system accuracy when using A/D converters with more than 12 bits of resolution, special attention must be paid to grounding and the elimination of potential ground loops. A ground loop can be formed by allowing the return current from the ICL7115's DAC to flow through traces that are common to other analog circuitry. If care is not taken, this current can generate small unwanted voltages that add to or detract from the reference or input voltages of the A/D converter.

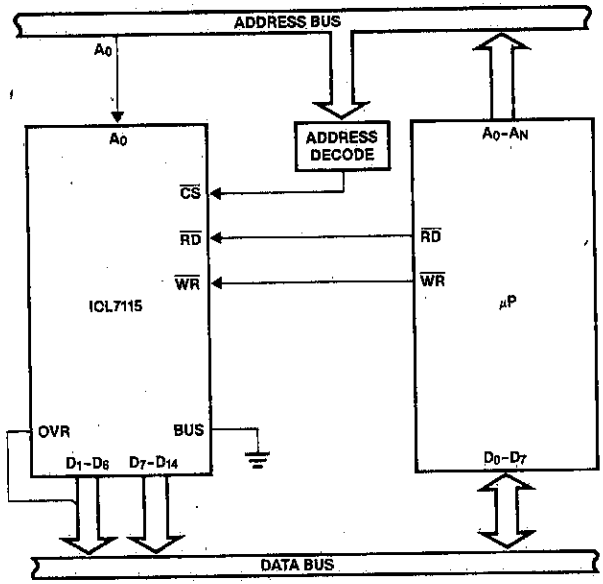
Ground loops can be eliminated by the use of the analog ground FORCE and SENSE lines provided on the ICL7115. Figures 2 and 3 illustrate the proper grounding technique for eliminating ground loops. Note that the input voltage *AND* the reference voltage are referred to the analog ground SENSE input. In Figure 2 the FORCE line is the only point that is connected to system analog ground. Figure 3 shows how an external op-amp can be used to force ground. In this example, only the non-inverting input of the op-amp is connected to system analog ground.

The FORCE and SENSE inputs for V_{IN} and V_{REF} are also shown driven by external op-amps. This technique eliminates the effect of small voltage drops which can appear between the input pin of the IC package and the actual resistor on the chip. If the small gauge wire and the bonds that connect the chip to its package have more than 300mΩ of total series resistance, the result can be a voltage error equivalent to 1 LSB. There is an inconsequential 200Ω resistor in series with the V_{IN} and V_{REF} FORCE inputs. If no op-amps are used for V_{IN} and V_{REF}, connections should be made directly to the SENSE lines. The external op-amps also serve to transform the relatively low impedance at the V_{IN} and V_{REF} pins into a high impedance. The input offset voltages of these amplifiers should be kept low in order to maintain the overall A/D converter system accuracy.

INTERFACING TO DIGITAL SYSTEMS

The ICL7115 provides three-state data output buffers, CS, RD, WR, and bus select inputs (A_0 and BUS) for interfacing to a wide variety of microcomputers and digital systems. The I/O Control Truth Table shows the functions of the digital control lines. The BUS select and A_0 lines are provided to enable the output data onto either 8-bit or 16-bit data busses. A conversion is initiated by a WR pulse (pin 33) when Chip Select (pin 3) is low. Data is enabled on the bus when the chip is selected and RD (pin 4) is low.

Figure 4 illustrates a typical interface to an 8-bit microcomputer. The "Start and Wait" operation requires the fewest external components and is initiated by a low level on the WR input to the ICL7115 after the I/O or memory-mapped address decoder has brought the CS input low. After executing a delay or utility routine for a period of time greater than the conversion time of the ICL7115, the processor issues two consecutive bus addresses to read output data into two bytes of memory. A low level on A_0 enables the LSBs and a high level enables the MSBs.



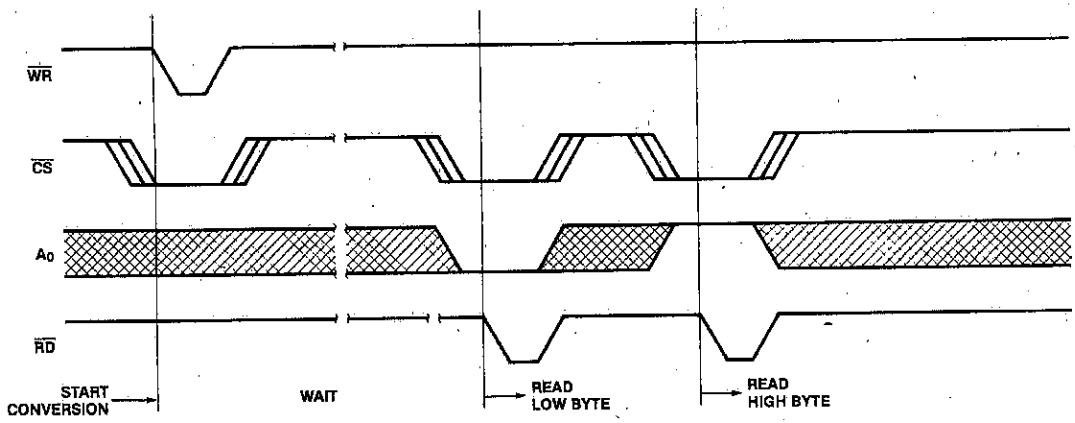


Figure 4. "Start and Wait" Operation

By adding a three-state buffer and two control gates, the End-of-Conversion (EOC) output can be used to control a "Start and Poll" interface (Figure 5). In this mode, the A_0 and $\overline{CS}$ lines connect the EOC output to the data bus along with the most significant byte of data. After pulsing the WR line to initiate a conversion, the microprocessor continually reads the most significant byte until it detects a high level on the EOC bit. The "Start and Poll" interface increases data throughput compared with the "Start and Wait" method by eliminating delays between the conversion termination and the microprocessor read operation.

Other interface configurations can be used to increase data throughput without monopolizing the microprocessor during waiting or polling operations by using the EOC line as an interrupt generator as shown in Figure 6. After the conversion cycle is initiated, the microprocessor can continue to execute routines that are independent of the A/D converter until the converter's output register actually holds valid data. For fastest data throughput, the ICL7115 can be connected directly to the data bus but controlled by way of a Direct Memory Access (DMA) controller as shown in Figure 7.

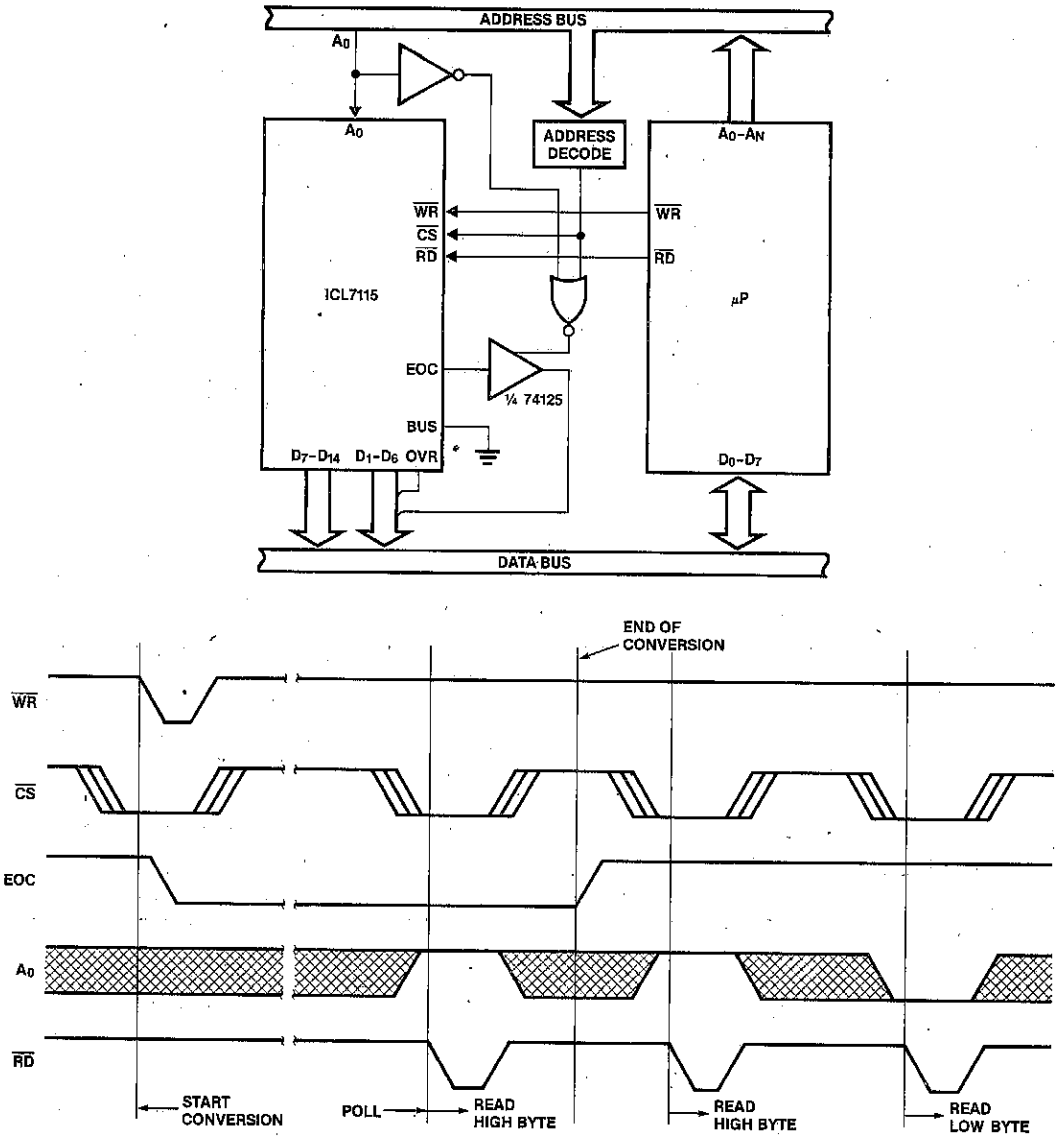
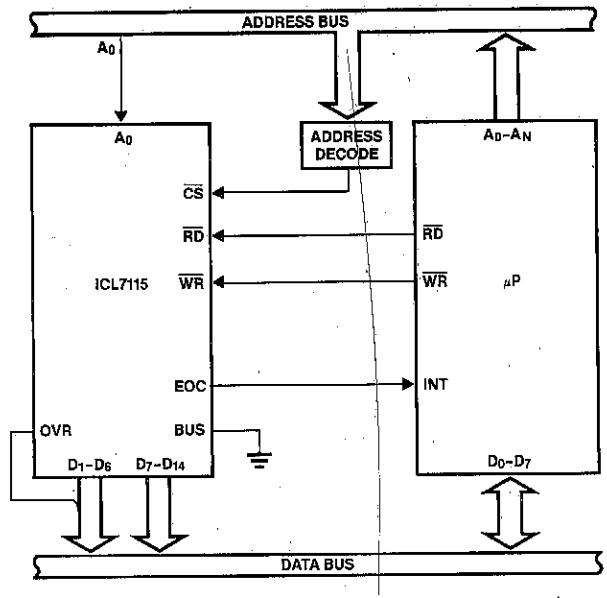


Figure 5. "Start and Poll" Operation



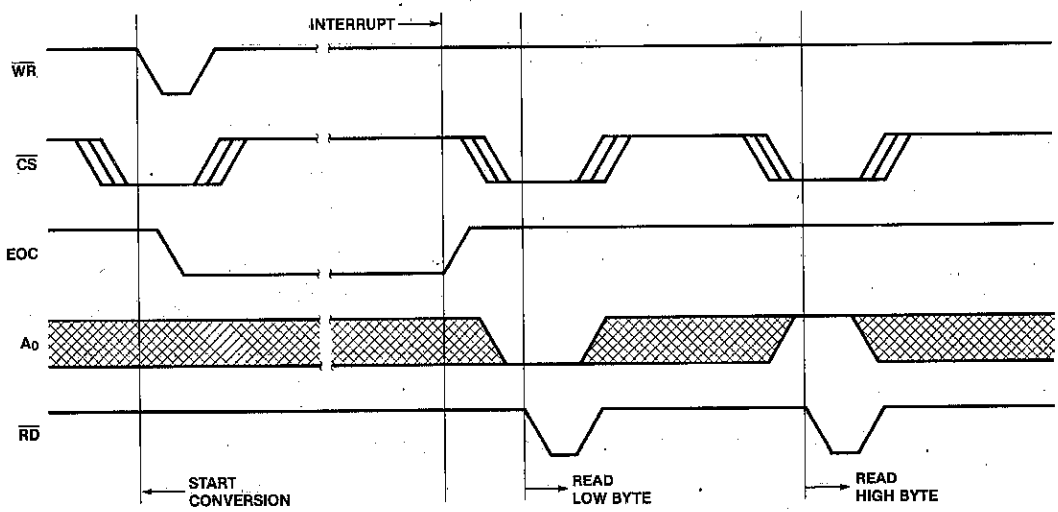
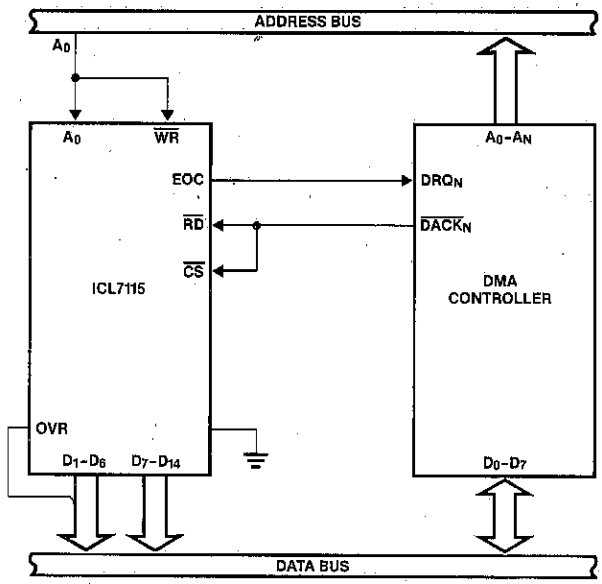


Figure 6. Using EOC as an Interrupt



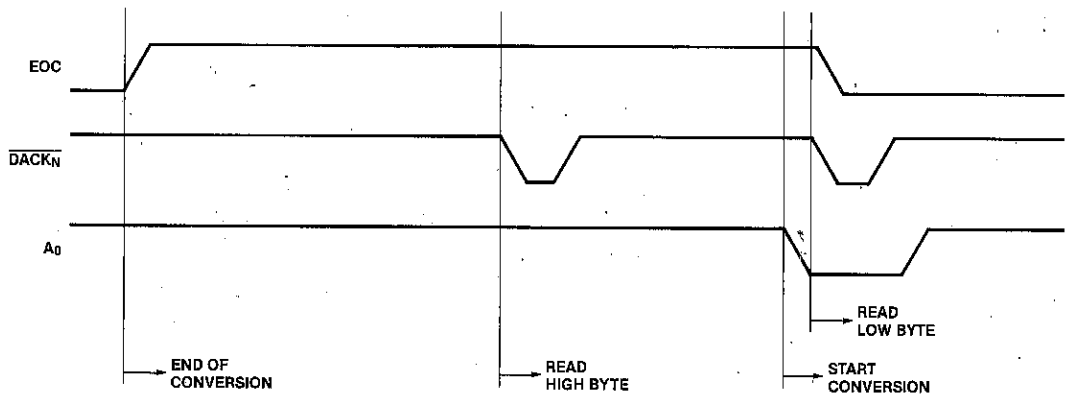


Figure 7. Data to Memory via DMA Controller

APPLICATIONS

Figure 8 shows a typical application of the ICL7115 14-bit A/D converter. A bipolar input voltage range of +5V to −5V is the result of using the current through R_2 to force a 1/2 scale offset on the input amplifier (A_2). The output of A_2 swings from 0V to −5V. The ICL8078-5D0 provides a very stable and accurate +5V for the reference buffer amplifier A_1. The overall gain of the A/D is varied by adjusting the 100kΩ trim resistor, R_5. Since the reference voltage will have a tempco of 1ppm/°C, typically, and the ICL7115 is automatically zeroed every conversion, the system gain and offset stability will be superb as long as stable external resistors are used.

In Figure 8, note that the 0.22μF auto-zero capacitor is connected directly between the C_{AZ} pin and analog ground SENSE. A_3 forces the analog ground of the ICL7115 to be the zero reference for the input signal. Its offset voltage is not important in this example because the voltage to be digitized is referred to the analog ground SENSE line rather than system analog ground.

The clock for the ICL7115 is taken from whatever system clock is available and divided down to the 500kHz level for a conversion time of 40μs. Output data is controlled by the BUS and A_0 inputs. Here they are set for 8-bit bus operation with BUS grounded and A_0 under the control of the address decode section of the external system.

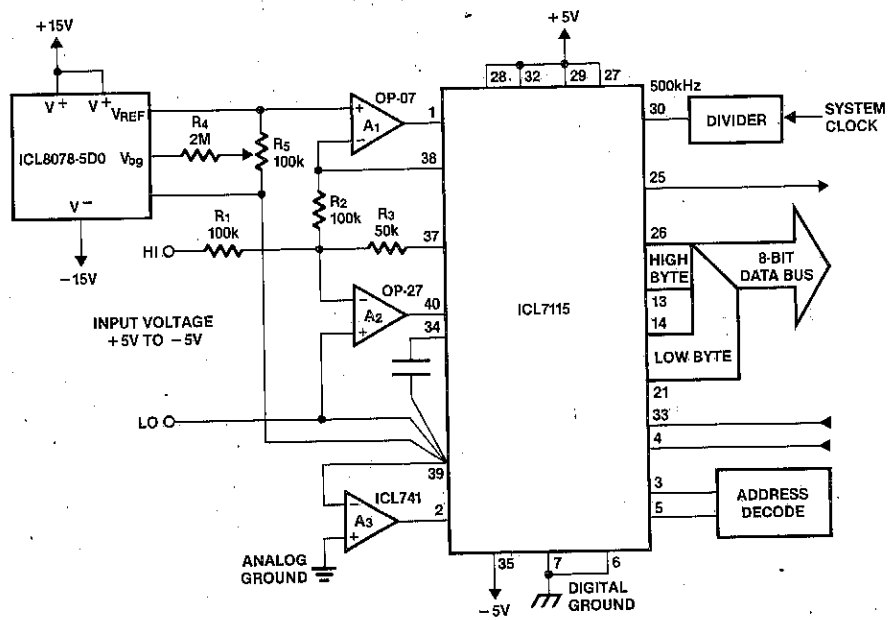


Figure 8. Typical Application with Bipolar Input Range, Forced Ground, and Heated-Substrate Reference

Because the ICL7115's internal accumulator generates accurate output data for input signals as much as 3% greater than full-scale, and because the converter's OVR output flags overrange inputs, a simple microprocessor routine can be employed to precisely measure and correct for system gain and offset errors. Figure 9 shows a typical data acquisition system that uses a 5.0V reference, input signal multiplexer, and input signal Track/Hold amplifier. Two of the multiplexer's input channels are dedicated to sampling the system analog ground and reference voltage. Here, as in Figure 8, bipolar operation is accommodated by an offset resistor between the reference voltage and the summing junction of A_1. A flip-flop in IC_3 sets IC_2's Track/Hold input after the microprocessor has initiated a WR command, and resets when EOC goes high at the end of the conversion.

The first step in the system calibration routine is to select the multiplexer channel that is connected to system analog ground and initiate a conversion cycle for the ICL7115. The results represent the system offset error which comes from the sum of the offsets from IC_1, IC_2, and A_1. Next the channel connected to the reference voltage is selected and measured. These results, minus the system offset error, represent the system full-scale range. A gain error correction factor can be derived from this data. Since the ICL7115 provides valid data for inputs that exceed full-scale by as much as 3%, the OVR output can be thought of as a valid 15th data bit. Whenever the OVR bit is high, however, the total 14-bit result should be checked to insure that it falls within 100% of full-scale and 103% of full-scale. Data beyond 103% of full-scale should be discarded.

The ICL7115 provides an internal inverter, OSC1 and OSC2, for crystal or ceramic resonator oscillator operation. The clock frequency is calculated from:

$$f_{CLK} = \frac{20}{t_{conv}} \text{ for 14-bit operation}$$

and

$$f_{CLK} = \frac{18}{t_{conv}} \text{ for 12-bit operation}$$

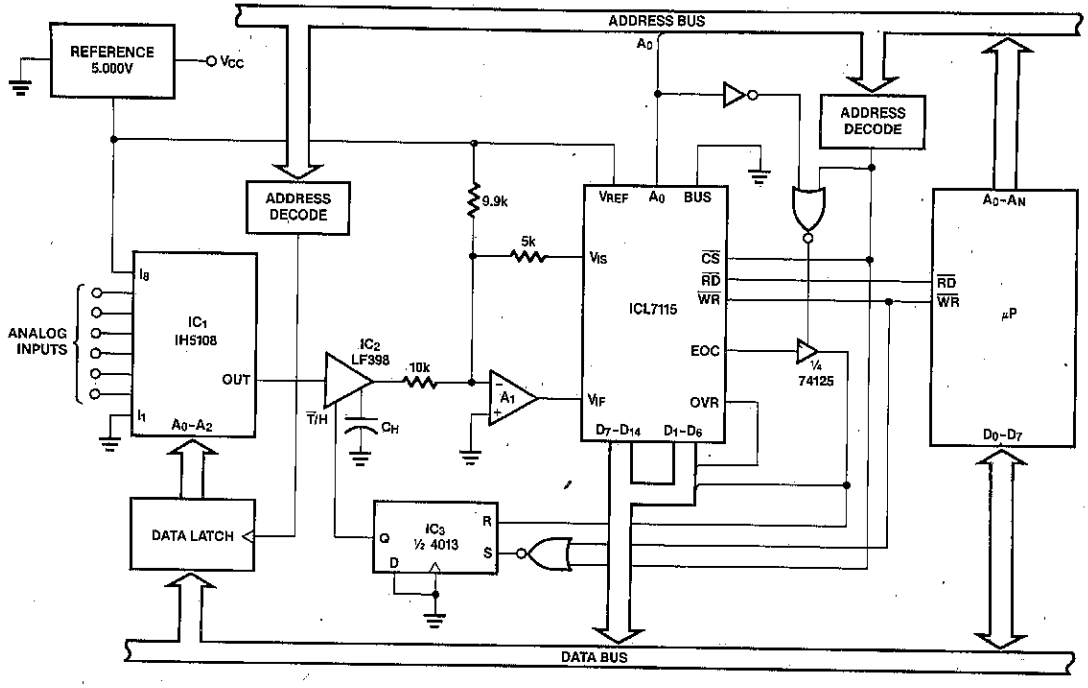
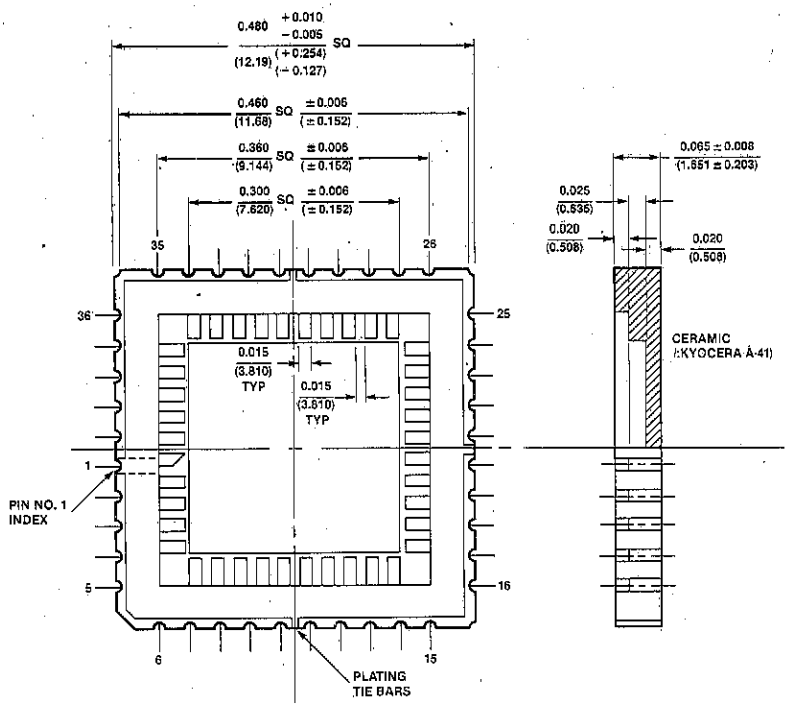
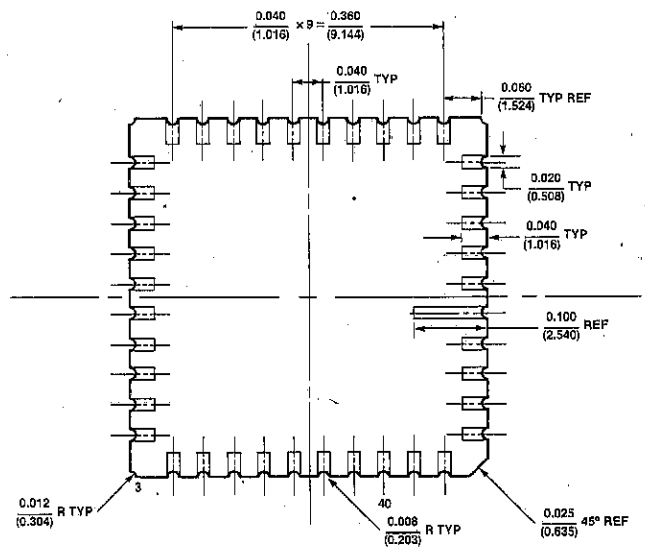


Figure 9. Multi-Channel Data Acquisition System with Zero and Reference Lines Brought to Multiplexer for System Gain and Offset Error Correction

PACKAGE OUTLINES All dimensions are in inches (millimeters)





Note 1: Finish: Gold plated 60 micro inches minimum thickness over nickel plated.
Note 2: Pin number 1 connected to die attach pad ground

Leadless Chip Carrier

ICL7116/7117

3½-Digit Single Chip A/D Converter with Display Hold

FEATURES

- **HOLD Reading Input allows indefinite display hold**
- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA input current typical.**
- **True differential input**
- **Direct display drive - no external components required. — LCD ICL7116**
  — LED ICL7117
- **Low noise - less than 15μV pk-pk typical.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**

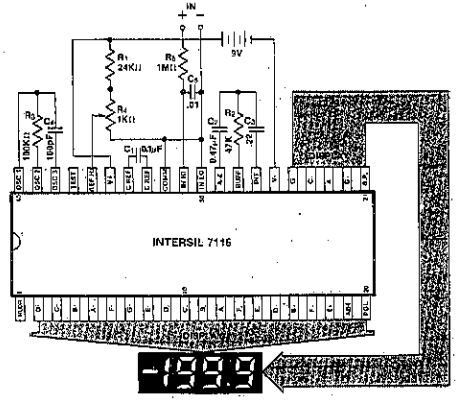
GENERAL DESCRIPTION

The Intersil ICL7116 and 7117 are high performance, low power 3-1/2 digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7116 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7117 will directly drive an instrument-size light emitting diode (LED) display.

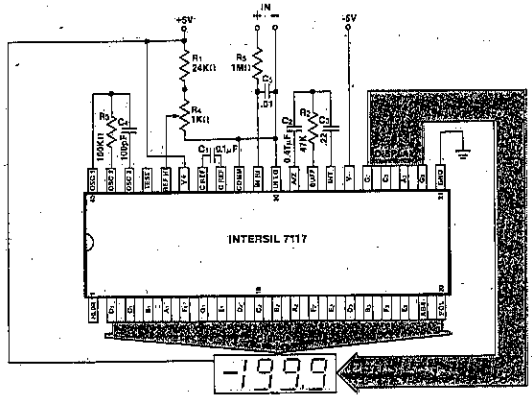
The 7116 and 7117 have almost all of the features of the 7106 and 7107 with the addition of a HOLD Reading input. With this input, it is possible to make a measurement and then retain the value on the display indefinitely. To make room for this feature the reference input has been referenced to Common rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the 7106 and 7107. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7116), enabling a high performance panel meter to be built with the addition of only seven passive components and a display.

4

TYPICAL CONNECTION DIAGRAMS



ICL7116 with Liquid Crystal Display

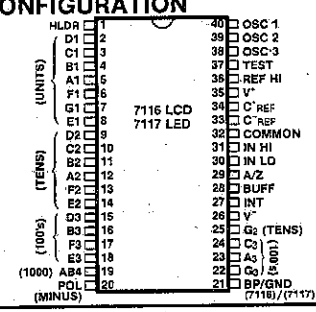


ICL7117 with LED Display

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7116	0°C to +70°C	40-Pin Ceramic DIP	ICL7116CDL
7116	0°C to +70°C	40-Pin Plastic DIP	ICL7116CPL
7116	0°C to +70°C	40 Pin CERDIP	ICL7116CJL
7117	0°C to +70°C	40-Pin Ceramic DIP	ICL7117CDL
7117	0°C to +70°C	40-Pin Plastic DIP	ICL7117CPL
7117	0°C to +70°C	40-Pin CERDIP	ICL7117CJL

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

ICL7116

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V to V^-
Reference Input Voltage (either input) ..... V to V^-
HLDR, Clock Input ..... Test to V^+
Power Dissipation (Note 2)
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

ICL7117

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
HLDR, Clock Input ..... Gnd to V^+
Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \cong$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or Full Scale = 2.000V	−1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	$V_{CM} = \pm 1V$, V_{IN} = 0V, Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0 0°C < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C < T_A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7117)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7117 only)			0.6	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25kΩ between COMMON & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25kΩ between COMMON & pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				TEST +1.5	V
V_{IL}, Pin 1 (7117 only)				GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ −1.5			V
7116 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	$V^+ - V^- = 9V$	4 4	5 5	6 6	V
7117 ONLY Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A = 25°C, f_{clock} = 48kHz. 7116 is tested in the circuit of Figure 1. 7117 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.

TEST CIRCUITS

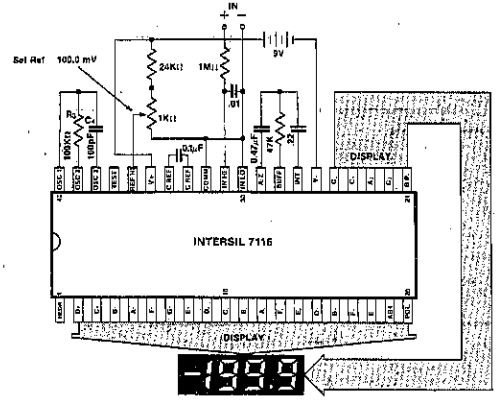


Figure 1: 7116

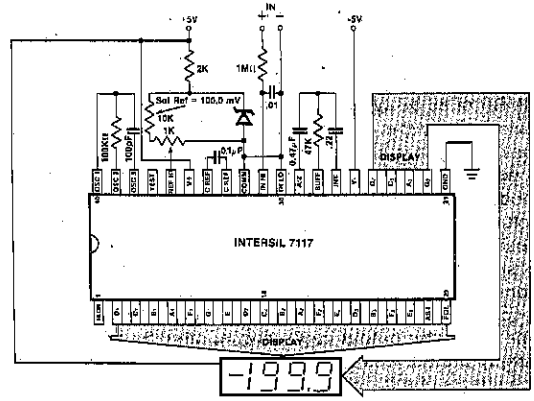


Figure 2: 7117

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

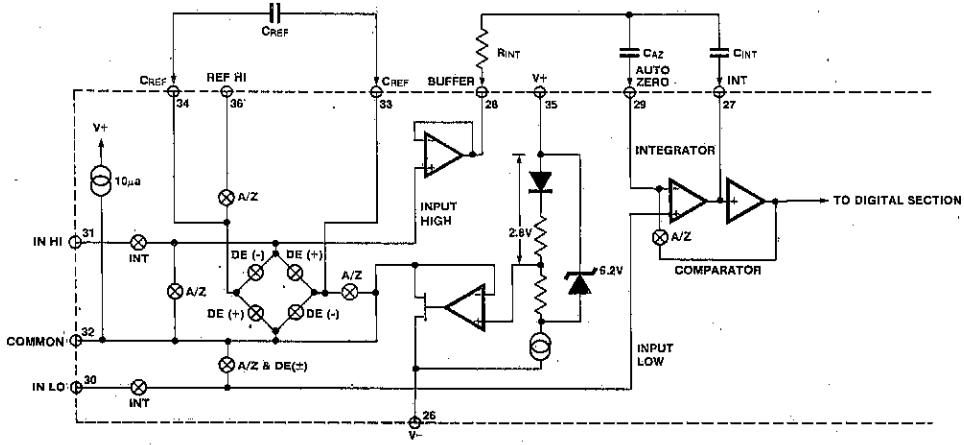


Figure 3: Analog Section of 7116/7117

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 ($\frac{Vin}{Vref}$).

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

Reference

The reference input must be generated as a positive voltage with respect to COMMON. Note that current flowing in the COMMON pins' internal resistance causes a slight shift in the effective reference voltage, disturbing ratiometric readings at low reference inputs. If possible, do not let this current vary.

4

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

Analog COMMON is also the voltage that input low returns to during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter.

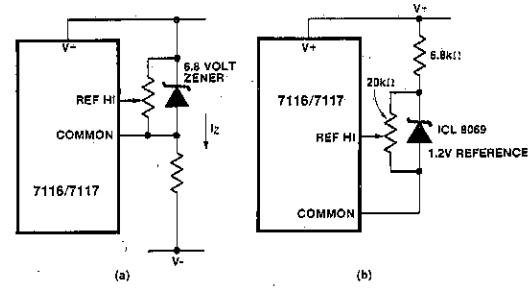


Figure 4: Using an External Reference

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

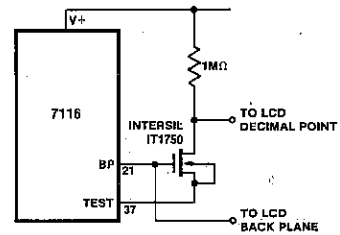


Figure 5: Simple Inverter for Fixed Decimal Point

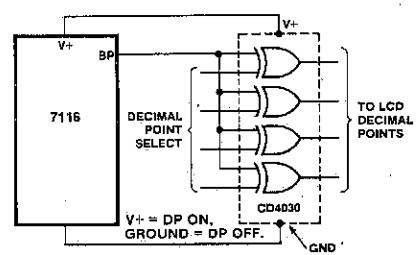


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled to high (to V^+) all segments will be turned on and the display should read - 1888. **[Caution: on the 7116, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.]**

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the 7117. It is identical except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16 mA.

In both devices the polarity indicator is ON for negative analog inputs. This can be reversed by simply reversing IN LO and IN HI.

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "HI". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input is CMOS compatible, and has a 70k typical resistance to either TEST (7116) or GROUND (7117).

4

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

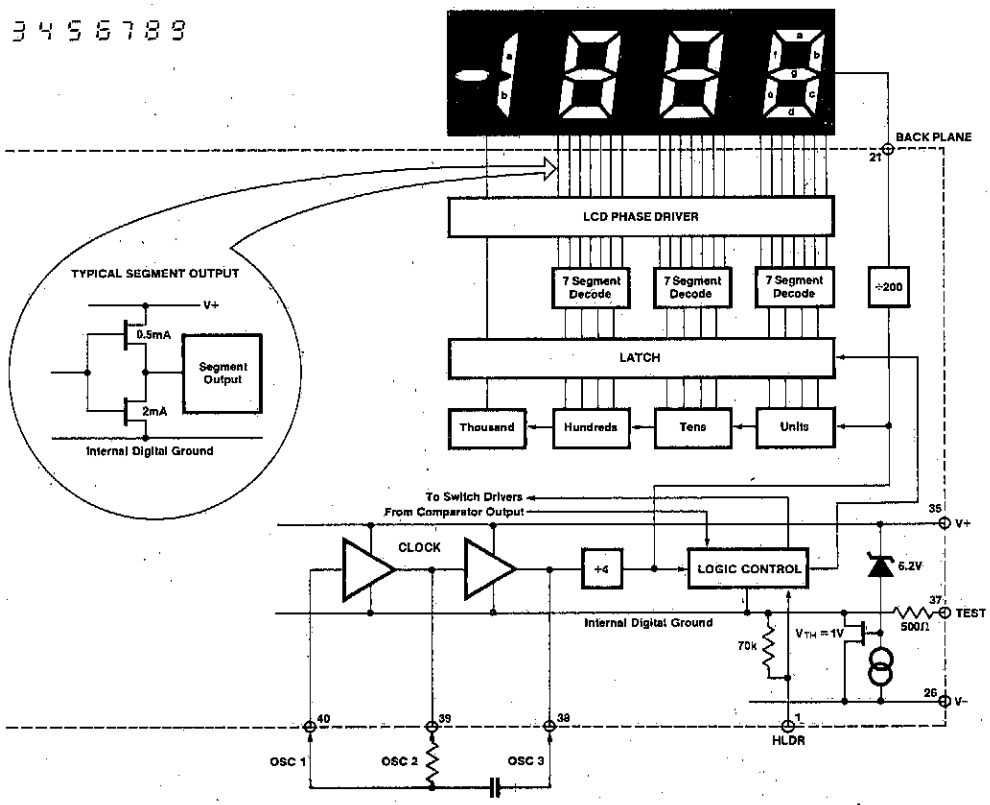


Figure 7: Digital Section 7116

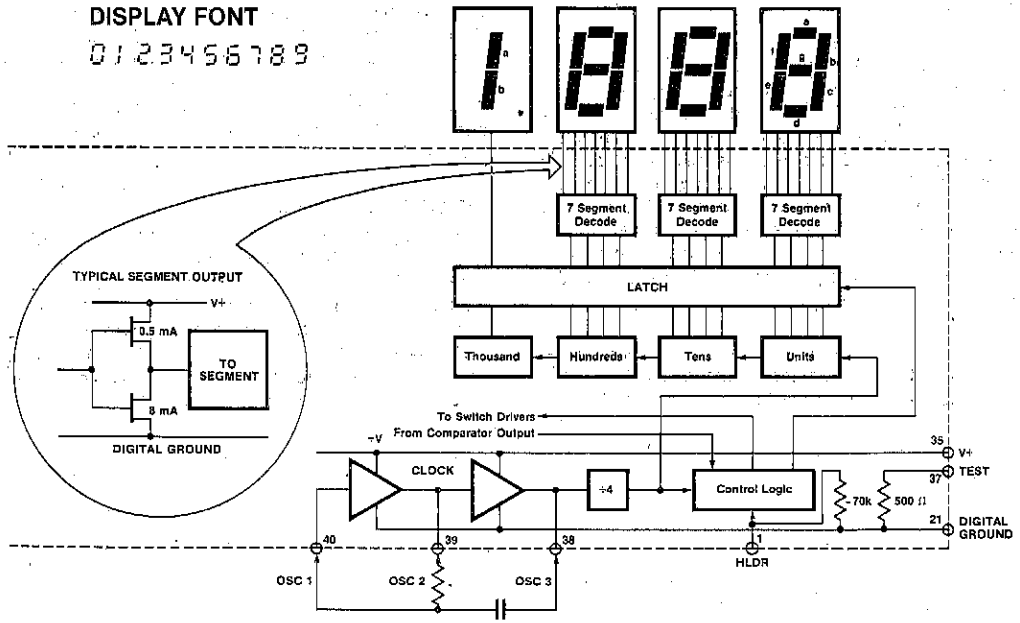


Figure 8: Digital Section 7117

4

System Timing

Figure 9 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

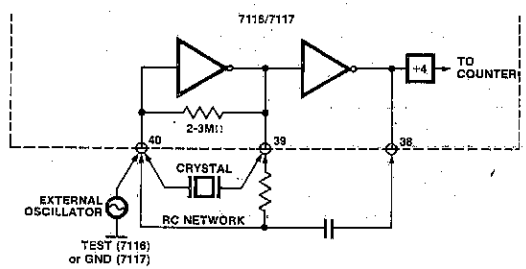


Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3 kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3 kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog COMMON is used as a reference, a nominal ±2volt full scale integrator swing is fine. For the 7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{INT} are 0.22 and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise

is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. If rollover errors occur a larger value, up to 1.0μF may be required.

5. Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} = 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7. 7117 Power Supplies

The 7117 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

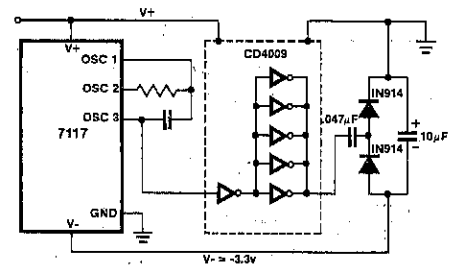


Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

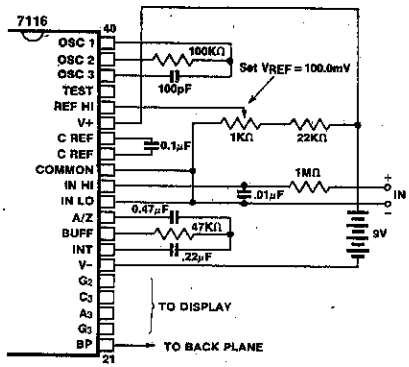


Figure 11: 7116 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

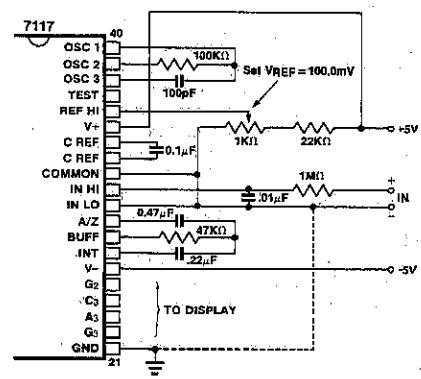


Figure 12: 7117 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common.)

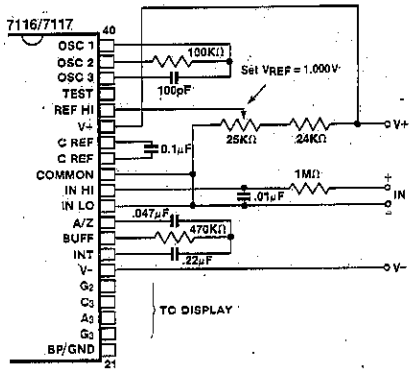


Figure 13: 7116/7117: Recommended component values for 2.000V full scale.

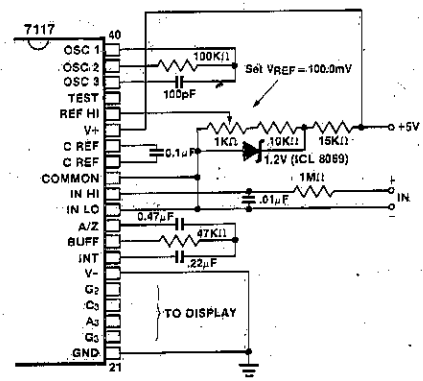


Figure 14: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

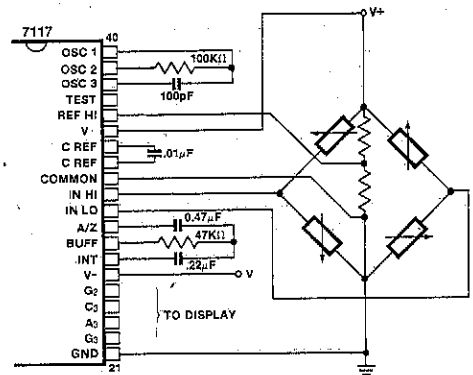


Figure 15: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

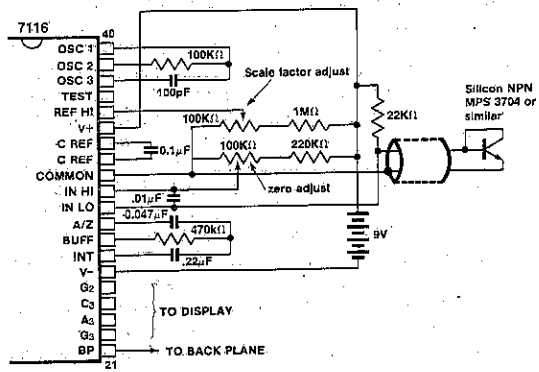


Figure 16: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar.
A017 "The Integrating A/D Converter," by Lee Evans.
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
A047 "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

ICL7126

Single-Chip 3½-Digit Low-Power A/D Converter

FEATURES

- Guaranteed zero reading for 0 Volts input on all scales
- True polarity at zero for precise null detection
- 1pA typical input current
- True differential input and reference
- Direct LCD display drive — no external components required
- Pin compatible with the ICL7106
- Low noise — less than 15μV p-p
- On-chip clock and reference
- Low power dissipation guaranteed less than 1mW
- No additional active circuits required
- Evaluation Kit available (ICL7126EV/KIT)
- 8,000 hours typical 9 Volt battery life

GENERAL DESCRIPTION

The Intersil ICL7126 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven segment decoders, display drivers, reference, and clock. The 7126 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is 100μA, ideally suited for 9V battery operation.

The 7126 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias-current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

The ICL7126 can be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

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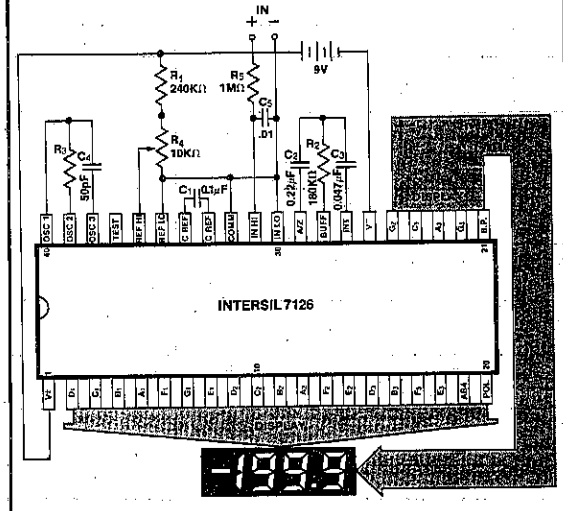
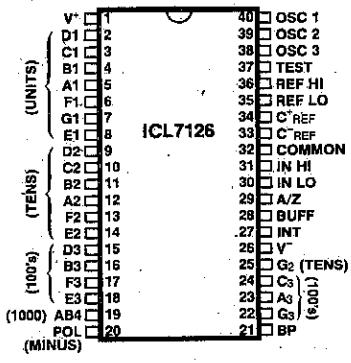


ICL7126 with Liquid Crystal Display

PIN CONFIGURATION



ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7126	0°C to +70°C	40-Pin Ceramic DIP	ICL7126CDL
7126	0°C to +70°C	40-Pin Plastic DIP	ICL7126CPL
7126	0°C to +70°C	40-Pin CERDIP	ICL7126CJL
7126 Kit		Evaluation Kits	ICL7126EV/KIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN}$ = 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0 0°C < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C < T_A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0 (Note 6)		50	100	μA
Analog COMMON Voltage (With respect to pos. supply)	250KΩ between Common & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (with respect to pos. Supply)	250KΩ between Common & pos. Supply		80		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Freq.		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion.
Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less then 50mV.
Note 6: During auto zero phase, current is 10-20μA higher. 48kHz oscillator, Figure 2, increases current by 8μA (typ).

TEST CIRCUITS

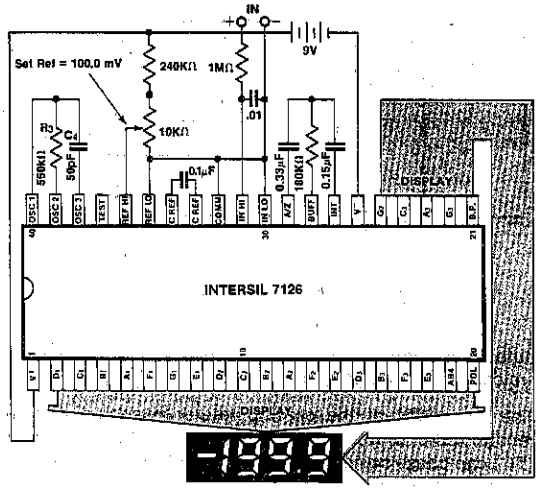


Figure 1: 7126 Clock Frequency 16kHz. (1 reading/sec)

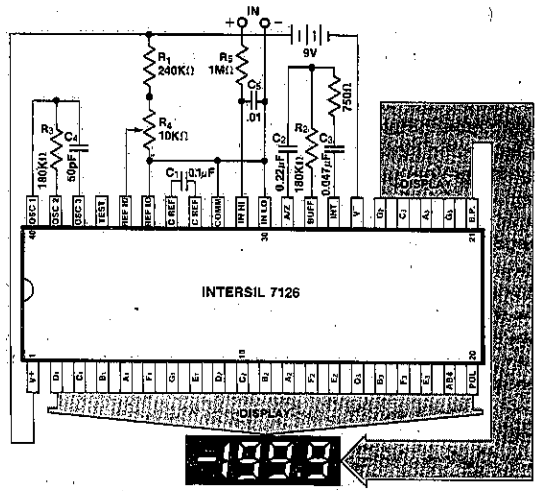


Figure 2: Clock Frequency 48kHZ. (3 readings/sec)

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DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

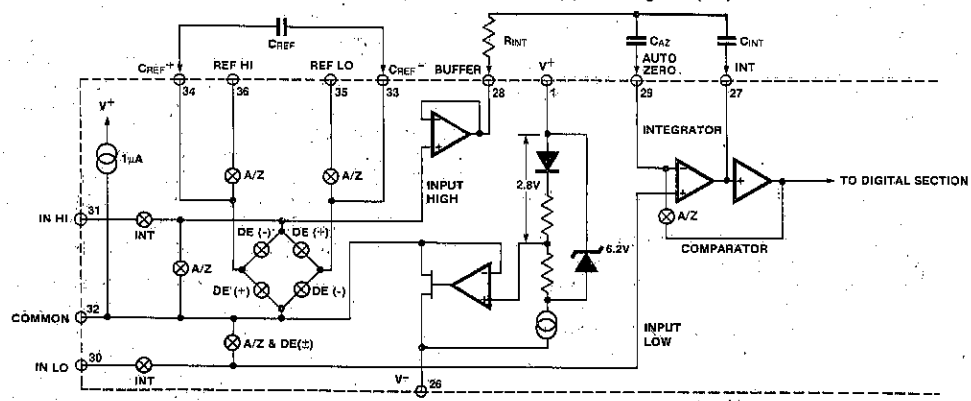

Figure 3: Analog Section of 7126

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less then 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $(\frac{V_{IN}}{V_{REF}})$.

Differential Input

The input can accept differential voltages anywhere within the common mode rante of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86 db typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (<7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low

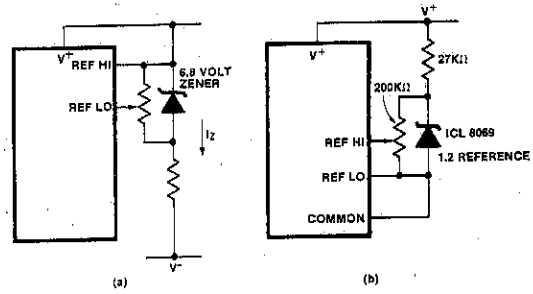

Figure 4: Using an External Reference

output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 100μA or more of current to hold the voltage 2.8 Volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

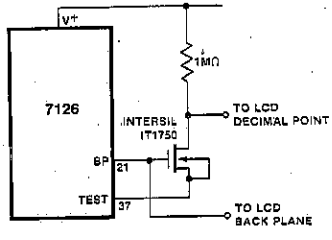

Figure 5: Simple Inverter for Fixed Decimal Point

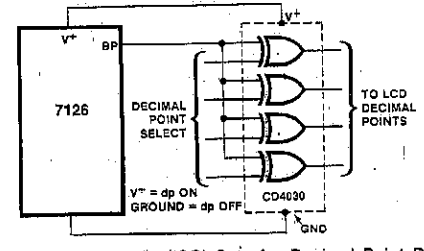

Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant D-C voltage (no square-wave) and may burn the LCD display if left in this mode for extended periods.

DIGITAL SECTION

Figure 7 shows the digital section for the 7126. An internal digital ground is generated from a 6 Volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 Volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

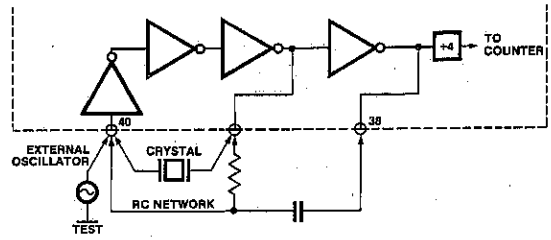

Figure 8: Clock Circuits

System Timing

Figure 8 shows the clocking arrangement used in the 7126. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000

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DISPLAY FONT

0 1 2 3 4 5 6 7 8 9

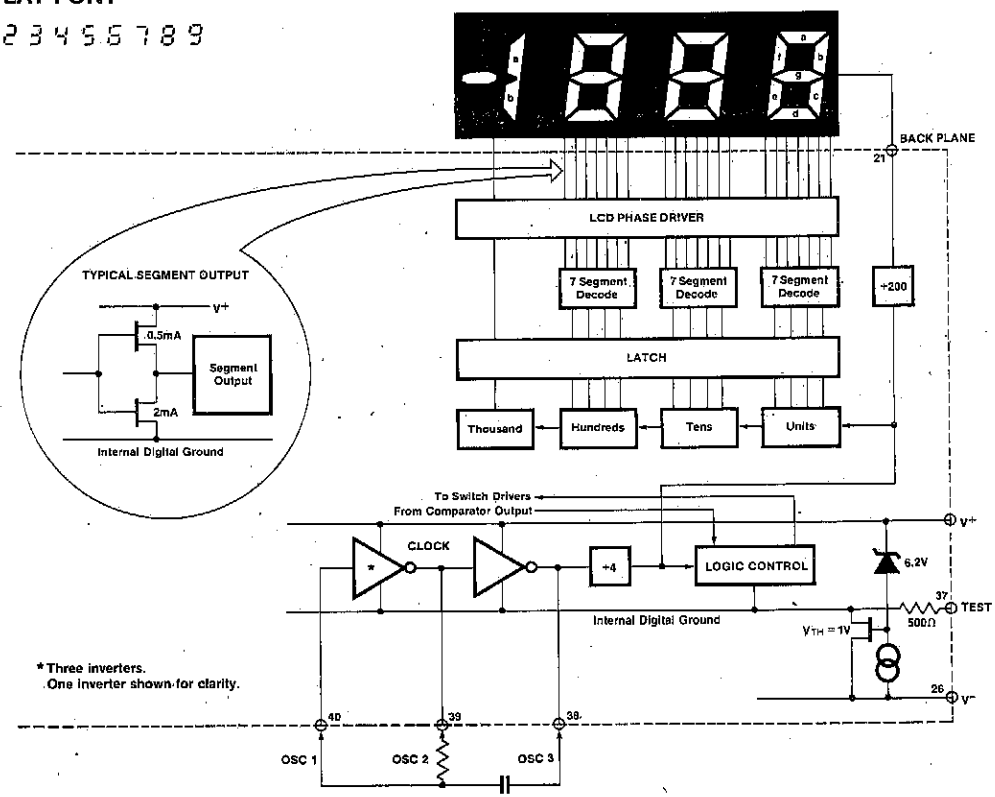


Figure 7: Digital Section

counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33-1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale, 1.8MΩ is near optimum and similarly 180kΩ for a 200.0mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1/sec (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay. See App. Note A017 for a description of the need and effects of this resistor.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32μF capacitor is recommended. On the 2 Volt scale, a 0.033μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications However, where a large common mode voltage exists (i.e., the REF LO pin is not analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{45}{RC}$. For 48kHz clock (3 readings/second), R = 180kΩ.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 Volt scale, V_{REF} should equal 100.0mV and 1.000 Volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. A suitable value for integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighting systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7126 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

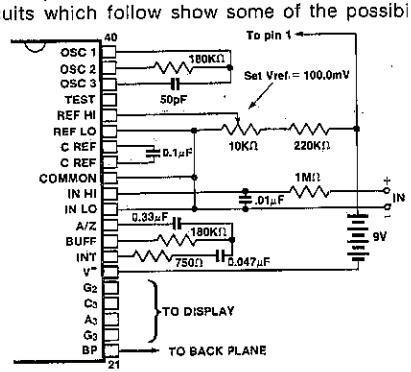


Figure 9: 7126 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).

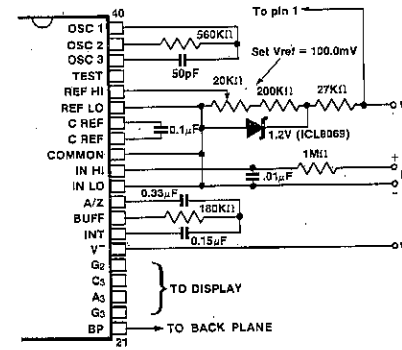


Figure 10: 7126 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading per second.

TYPICAL APPLICATIONS (Contd.)

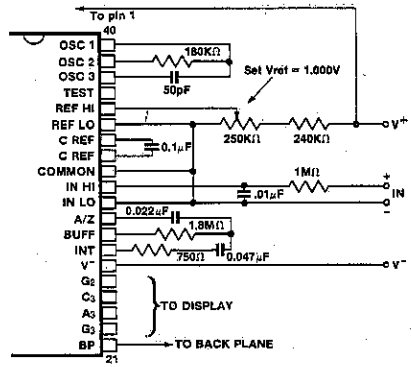


Figure 11: Recommended component values for 2.000V full scale, 3 readings per second. For 1 reading per second, delete 750Ω resistor, change C_{INT}, R_{OSC} to values of Fig. 10.

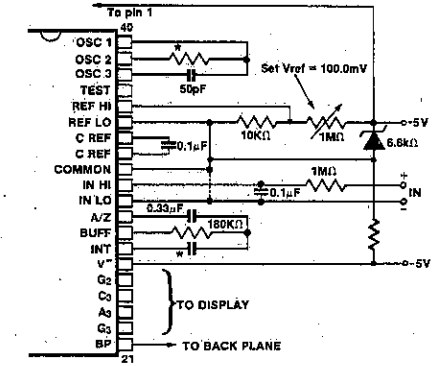


Figure 12: 7126 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

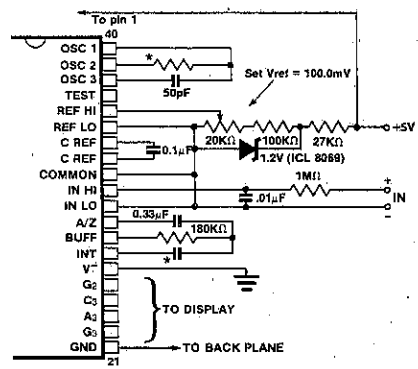


Figure 13: 7126 operated from single +5V supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

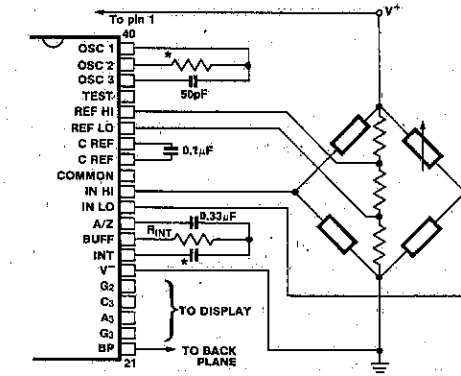


Figure 14: 7126 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

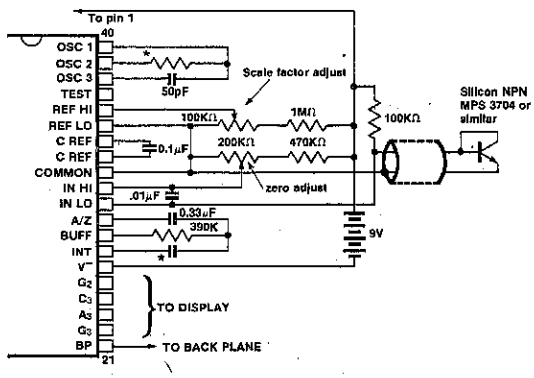


Figure 15: 7126 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

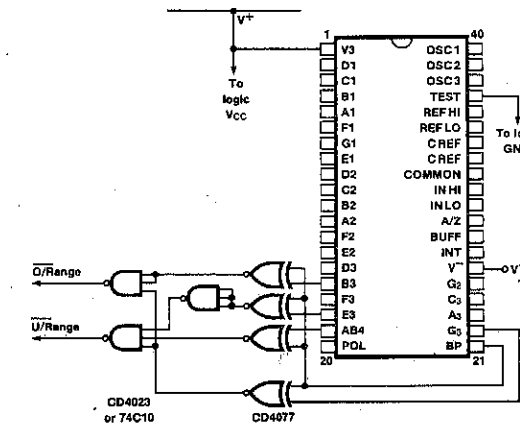


Figure 16: Circuit for developing Underrange and Overrange signals from 7126 outputs.

*Values depend on clock frequency. See Figure 9, 10, 11.

TYPICAL APPLICATIONS (Contd.)

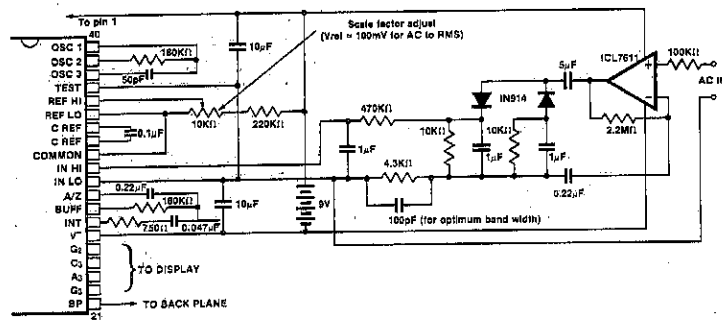


Figure 17: AC to DC Converter with 7126. Test is used as a common mode reference level to ensure compatibility with most op-amps.

APPLICATION NOTES

A016 "Selecting A/D Converters", by David Fullagar.
A017 "The Integrating A/D Converter", by Lee Evans.
A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards", by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

7126 EVALUATION KITS

After purchasing a sample of the 7126, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7126EV/KIT and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

ICL7129

4½-Digit Single-Chip A/D Converter

FEATURES

- ±19,999 count A/D converter accurate to ±1 count
- 10μV resolution on 200mV scale
- 110dB CMRR
- Direct LCD display drive
- True differential input and reference
- Low power consumption
- Decimal point drive outputs
- Overrange and underrange outputs
- Low battery detection and indication
- 10:1 range change input

ORDERING INFORMATION

PART	PACKAGE	TEMPERATURE	ORDER NUMBER
7129	40-Pin CERDIP	0°C to +70°C	ICL7129CJL
7129	40-Pin Plastic	0°C to +70°C	ICL7129CPL
7129	40-Pin Plastic	0°C to +70°C	ICL7129RCPL
7129	Dice	0°C to +70°C	ICL7129C/D
7129	Flat Pack		

GENERAL DESCRIPTION

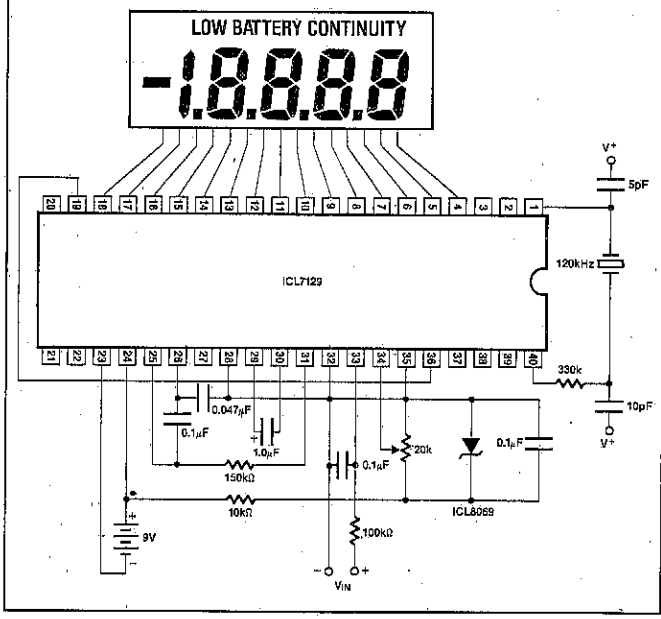
The Intersil ICL7129 is a very high-performance 4½-digit analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single-chip CMOS integrated circuit requires only a few passive components and a reference to operate. And it is ideal for high-resolution hand-held digital multimeter applications.

The performance of the ICL7129 has not been equaled before in a single-chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full-scale and resolution down to 10μV/count.

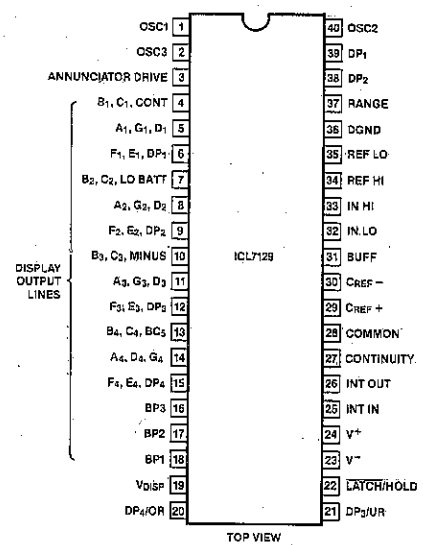
The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible signal. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

4

TYPICAL APPLICATION



PIN CONFIGURATION (outline dwg JL, PL)



ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (Note 1)
(IN HI or IN LO) ..... V^+ to V^-
V_{DISP} ..... V^+ to DGND – 0.3V
Digital Input Pins
1, 2, 19, 20, 21, 22, 27,
37, 38, 39, 40 ..... DGND to V^+

Power Dissipation (Note 2)
CERDIP package 1000mW
Plastic package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +160°C
Lead Soldering Temperature ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ±400μA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1mA.

Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V^+ to V^- = 9V, V_{REF} = 1.00V, T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0V 200mV Scale	–0000	0000	+0000	Reading
Zero Reading Drift	V_{IN} = 0V 0°C < T_A < +70°C		±0.5		μV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV RANGE = 2V	9998	9999	10000	Reading
Range Change, Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 1.0000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	–V_{IN} = +V_{IN} = 199mV		0.5	1.0	Counts
Linearity Error	200mV Scale		0.5		Counts
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale	(V^-) + 1.5		(V^+) – 0.5	V
Noise (p-p Value not Exceeding 95% of Time)	V_{IN} = 0V 200mV Scale		7.0		μV
Input Leakage Current	V_{IN} = 0V, Pin 32, 33		1	10	pA
Scale Factor Tempco	V_{IN} = 199mV 0°C < T_A < +70°C External V_{REF} = 0ppm/°C		2	5	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V		0.6		mA
COMMON Source Current	ΔCommon = –0.1V		12		μA
DGND Voltage	V^+ to Pin 36 V^+ to V^- = 9V	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V		1.2		mA
Supply Voltage Range	V^+ to V^-	6	9	14	V
Supply Current Excluding COMMON Current	V^+ to V^- = 9V		1.0	1.4	mA
Clock Frequency			120	360	kHz
Display Multiplex Rate	f_{CLK} = 120kHz		100		Hz
V_{DISP} Resistance	V_{DISP} to V^+		50		kΩ

ELECTRICAL CHARACTERISTICS (Continued) V^+ to V^- = 9V, V_{REF} = 1.00V, T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	 400	mV
Pull-Down Current	Pins 37, 38, 39		2	10	µA
"Weak Output" Current Sink, Source	Pin 20, 21		3/3		µA
	Pin 27 Sink/Source		3/9		
Pin 22 Source Current Pin 22 Sink Current			40 3		µA

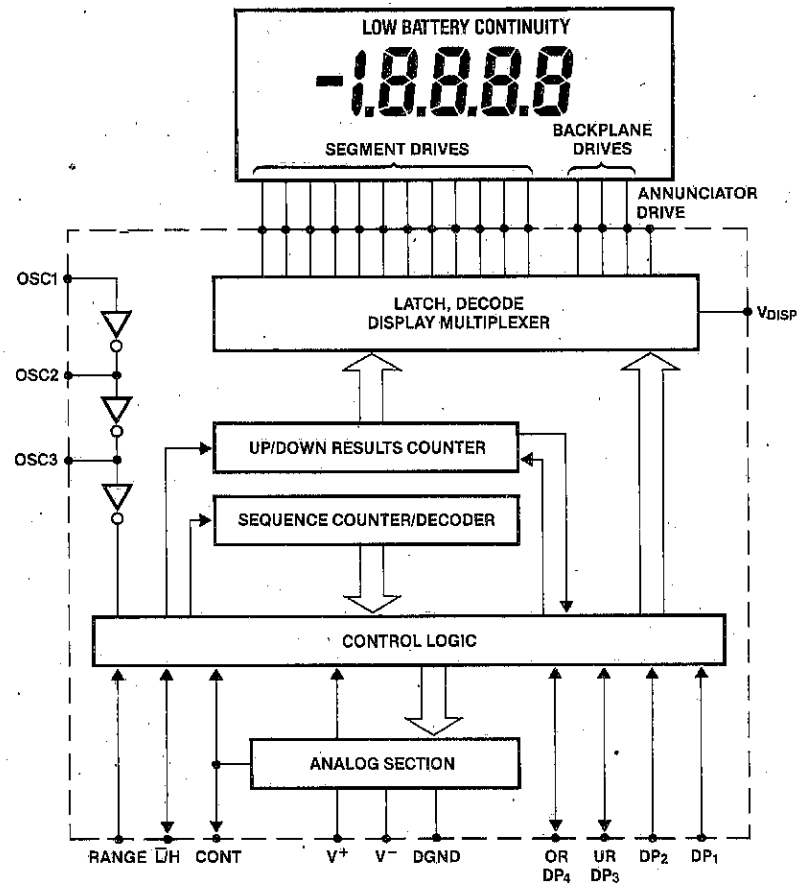


Figure 1. Simplified Block Diagram of ICL7129 Digital Section

Table 1. Pin Assignments and Functions

PIN	NAME	FUNCTION
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, D_4, G_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: Second most significant decimal point on when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{\text{LATCH}}$/HOLD	INPUT: When floating, A/D converter operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.

PIN	NAME	FUNCTION
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal, and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	$C_{REF}+$	Positive side of external reference capacitor.
30	$C_{REF}-$	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.
36	DGND	Ground reference for digital section.
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3μA pull-down. When HI, decimal point 1 will be on.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

DETAILED OPERATION DESCRIPTION

Intersil's ICL7129 is a uniquely designed single-chip A/D converter. It features a new "successive integration" technique to achieve 10μV resolution on a 200mV full-scale range. To achieve this resolution a 10:1 improvement in noise performance over previous monolithic CMOS A/D converters was accomplished. Previous integrating converters used an external capacitor to store an offset correction voltage. This technique worked well but greatly increased the equivalent noise bandwidth of the converter. The ICL7129 removes this source of error (noise) by not using an auto-zero capacitor. Offsets are instead cancelled using digital techniques. Savings in external parts cost are realized as well as improved noise performance and elimination of a source electromagnetic and electrostatic pick-up.

The overall block diagram of the ICL7129 is shown in Figure 1. The heart of this A/D converter is the sequence counter/decoder which drives the control logic and keeps track of the many separate phases required for each conversion cycle. The sequence counter is constantly running and is a separate counter from the up/down results counter which is activated only when the integrator is de-integrating. At the end of a conversion the data remaining in the results counter is latched, decoded and multiplexed to the liquid crystal display.

The analog section block diagram shown in Figure 2 includes all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the cycle. The input and reference switching schemes are very similar to those in other less accurate integrating A/D converters. There are 5 basic configurations used in the full conversion cycle. Figure 3 illustrates a typical waveform on the integrator output. INT, INT_1, and INT_2 all refer to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage.

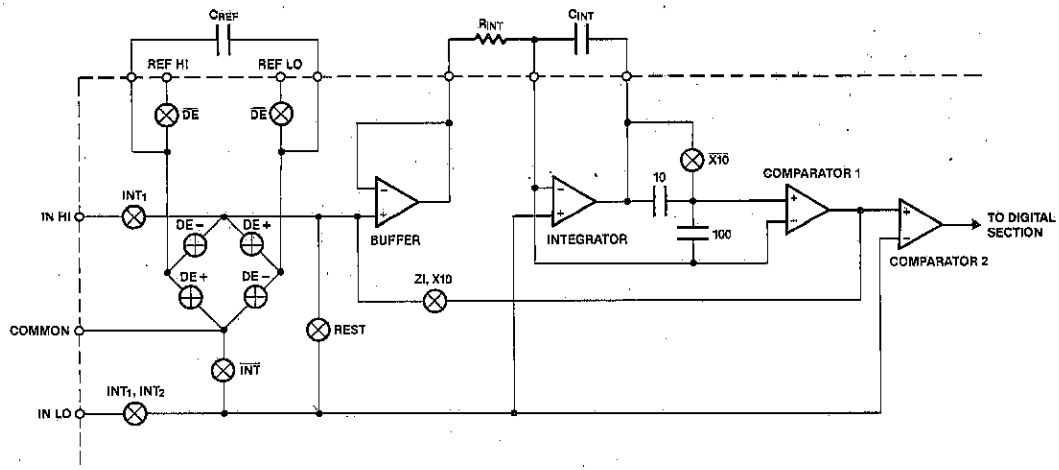


Figure 2. ICL7129 Analog Block Diagram

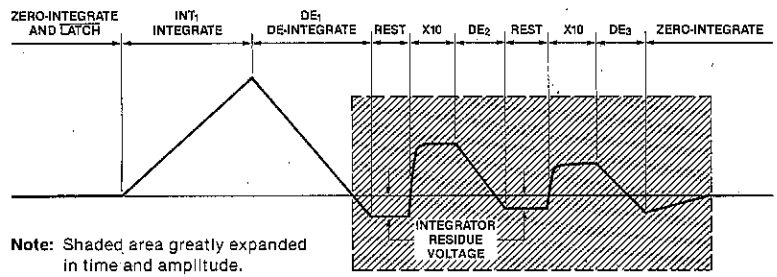


Figure 3. Integrator Waveform for Negative Input Voltage Showing Successive Integration Phases and Residue Voltage

DE_1, DE_2, and DE_3 are the de-integrate phases where the reference capacitor is switched in series with the buffer amplifier and the integrator ramps back down to the level it started from before integrating. However, since the de-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129 amplifies this overshoot by 10 and DE_2 begins. Similarly DE_2's overshoot is amplified by 10 and DE_3 begins. At the end of DE_3 the results counter holds a number with 5½ digits of resolution. This was obtained by feeding counts into the results counter at the 3½ digit level during DE_1, into the 4½ digit level during DE_2 and the 5½ digit level for DE_3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted and subtracting the results from the original reading. For this phase INT_2 switch is closed to give the same common-mode voltage as the measurement cycle. This assures excellent CMRR. At the end of the cycle the data in the up/down results counter is accurate to 0.005% of full-scale and is sent to the display driver for decoding and multiplexing.

COMMON, DGND, AND "LOW BATTERY"

The COMMON and DGND (Digital GrouND) outputs of the ICL7129 are generated from internal zener diodes (Figure 4). COMMON is included primarily to set the common-mode voltage for battery operation or for any system where the input signals float with respect to the power supplies. It also functions as a pre-regulator for an external precision reference voltage source. The voltage between DGND and V^+ is the supply voltage for the logic section of the ICL7129 including the display multiplexer and drivers. Both COMMON and DGND are capable of sinking current from external loads, but caution should be taken to insure that these outputs are not overloaded. Figure 5 shows the connection of external logic circuitry to the ICL7129. This connection will work providing that the supply current requirements of the logic do not exceed the current sink capability of the DGND pin. If more supply current is required, the buffer in Figure 6 can be used to keep the loading on DGND to a minimum. COMMON can source approximately 12μA while DGND has no source capability.

The "LOW BATTERY" annunciator of the display is turned on when the voltage between V^+ and V^- drops below 7.2V typically. The exact point at which this occurs is determined by the 6.3V zener diode and the threshold voltage of the n-channel transistor connected to the V^- rail in Figure 4. As the supply voltage decreases, the n-channel transistor connected to the V-rail eventually turns off and the "LOW BATTERY" input to the logic section is pulled HIGH, turning on the "LOW BATTERY" annunciator.

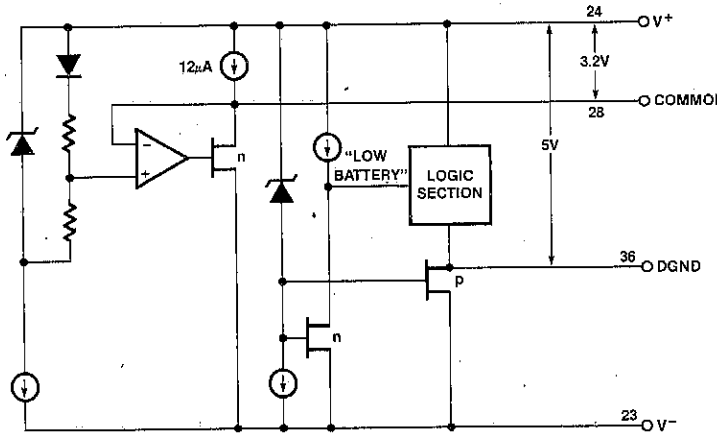


Figure 4. Biasing Structure for COMMON and DGND

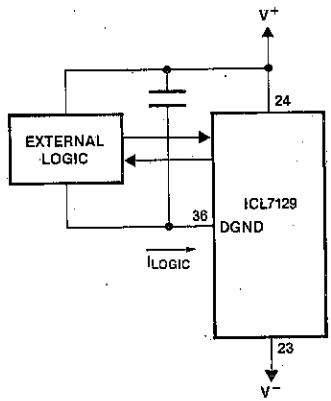


Figure 5. DGND Sink Current

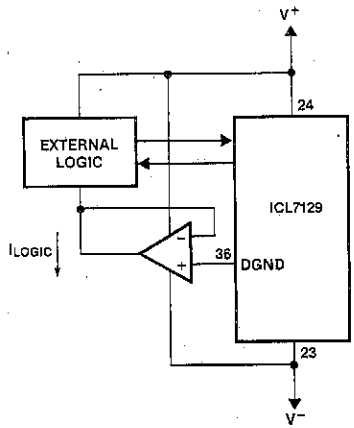


Figure 6. Buffered DGND

I/O PORTS

Four of the pins of the ICL7129 can be used as either inputs or outputs. The specific pin numbers and functions are described on the Pin Assignments and Functions (Table 1). If the output function of the pin is not desired in an application it can easily be overriden by connecting the pin to V^+ (HI) or DGND (LO). This connection will not damage the device because the output impedance of these pins is quite high. A simplified schematic of these input/output pins is shown in Figure 7. Since there is approximately 500kΩ in series with the output driver, the pin (when used as an output) can only drive very light loads such as 4000 series, 74CXX-type CMOS logic, or other high input impedance devices. The output drive capability of these four pins is limited to 3μA, nominally.

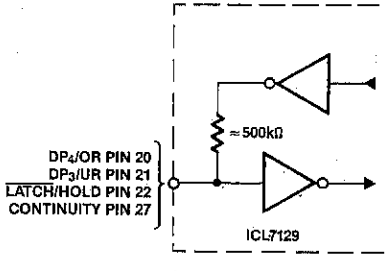


Figure 7. "Weak Output"

LATCH/HOLD, OVERRANGE, AND UNDERRANGE TIMING

The LATCH/HOLD output (pin 22) will be pulled low during the last 100 clock cycles of each full conversion cycle. During this time the final data from the ICL7129 counter is latched and transferred to the display decoder and multiplexer. The conversion cycle and LATCH/HOLD timing are directly related to the clock frequency. A full conversion cycle takes 30,000 clock cycles which is equivalent to 60,000 oscillator cycles. OverRange (OR pin 20) and UnderRange (UR pin 21) outputs are latched on the falling edge of LATCH/HOLD and remain in that state until the end of the next conversion cycle. In addition, digits 1 through 4 are blanked during overrange. All three of these pins are "weak outputs" and can be overridden with external drivers or pull-up resistors to enable their input functions as described in the Pin Assignments and Functions (Table 1).

INSTANT CONTINUITY

A comparator with a built-in 200mV offset is connected directly between INPUT HI and INPUT LO of the ICL7129 (Figure 8). The CONTINUITY output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This will also turn on the "CONTINUITY" annunciator on the display. The CONTINUITY output may be used to enable an external alarm or buzzer, thereby giving the ICL7129 an audible continuity checking capability. Since the CONTINUITY output is one of the four "weak outputs" of the ICL7129, the "continuity" annunciator on the display can be driven by an external source if desired. The continuity function can be overridden with a pull-down resistor connected between CONTINUITY pin and DGND (pin 36).

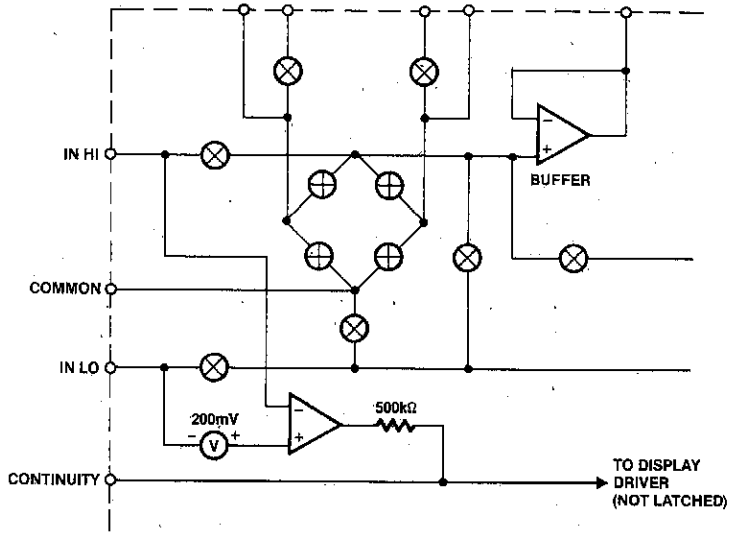


Figure 8. "Instant Continuity" Comparator and Output Structure

DISPLAY CONFIGURATION

The ICL7129 is designed to drive a triplexed liquid crystal display. This type of display has three backplanes and is driven in a multiplexed format similar to the ICM7231 display driver family. The specific display format is shown in Figure 9. Notice that the polarity sign, decimal points, "LOW BATTERY", and "CONTINUITY" annunciators are directly driven by the ICL7129. The individual segments and annunciators are addressed in a manner similar to row-column addressing. Each backplane (row) is connected to one-third of the total number of segments. BP1 has all F, A, and B segments of the four least significant digits. BP2 has all of the C, E, and G segments. BP3 has all D segments, decimal points, and annunciators. The segment lines (columns) are connected in groups of three bringing all segments of the display out on just 12 lines.

ANNUNCIATOR DRIVE

A special display driver output is provided on the ICL7129 which is intended to drive various kinds of annunciators on custom multiplexed liquid crystal displays. The ANNUNCIATOR DRIVE output (pin 3) is a squarewave signal running at the backplane frequency, approximately 100Hz. This signal swings from V_{DISP} to V^+ and is in sync with the three backplane outputs BP1, BP2, and BP3. Figure 10 shows these four outputs on the same time and voltage scales.

Any annunciator associated with any of the three backplanes can be turned on simply by connecting it to the ANNUNCIATOR DRIVE pin. To turn an annunciator off connect it to its backplane. An example of a display and annunciator drive scheme is shown in Figure 11.

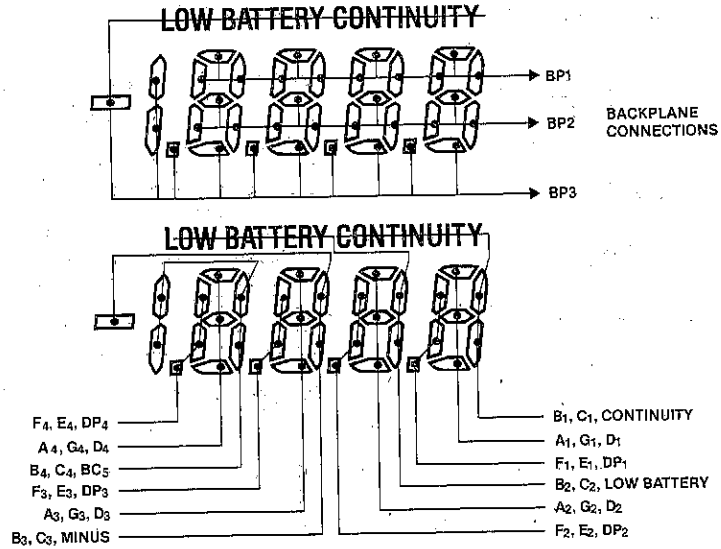


Figure 9. Triplexed Liquid Crystal Display Layout for ICL7129

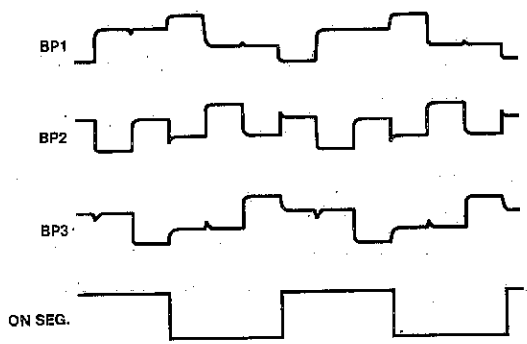


Figure 10. Typical Backplane and Annunciator Drive Waveforms

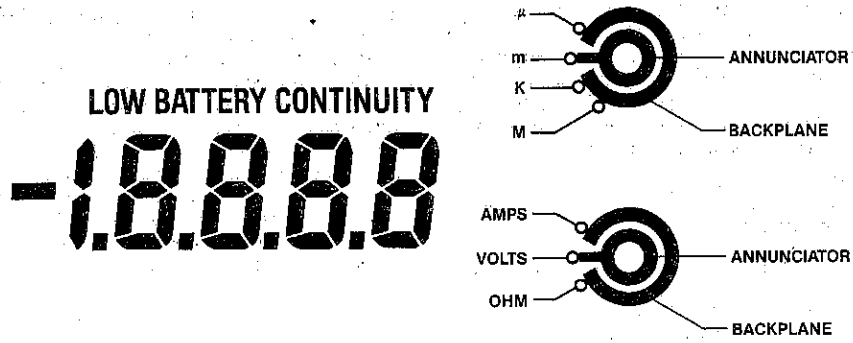


Figure 11. Multimeter Example Showing Use of Annunciator Drive Output

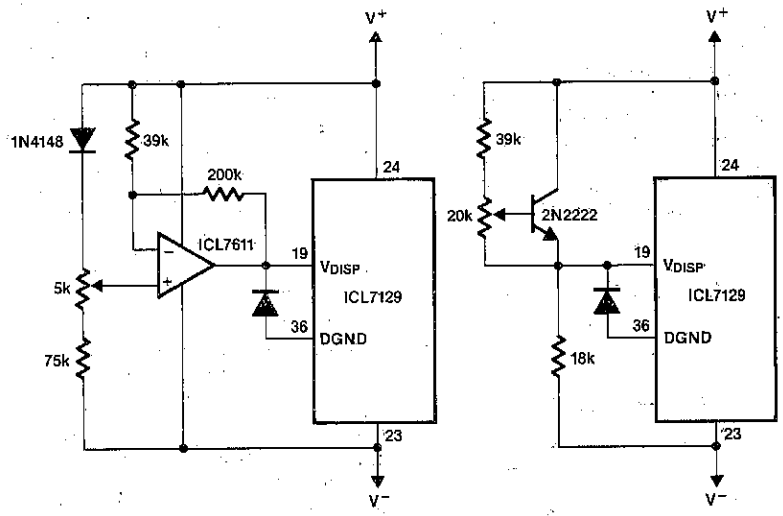


Figure 12. Two Methods for Temperature Compensating the Liquid Crystal Display

DISPLAY TEMPERATURE COMPENSATION

For most applications an adequate display can be obtained by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is encountered, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers can supply the temperature compensation requirements for their displays. Figure 12 shows two circuits that can be adjusted to give a temperature compensation of $\approx +10mV/°C$ between V^+ and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage to assure that no forward current is injected on the chip if V_{DISP} is more negative than DGND.

COMPONENT SELECTION

There are only three passive components around the ICL7129 that need special consideration in selection. They are the reference capacitor, integrator resistor, and integrator capacitor. There is no auto-zero capacitor like that found in earlier integrating A/D converter designs.

The integrating resistor is selected high enough to assure good current linearity from the buffer amplifier and integrator and low enough that PC board leakage is not a problem. A value of 150k should be optimum for most applications. The integrator capacitor is selected to give an optimum integrator swing at full-scale. A large integrator swing will reduce the effect of noise sources in the comparator but will affect

rollover error if the swing gets too close to the positive rail (≈0.7V). This gives an optimum swing of ≈2.5V at full-scale. For 150k integrating resistor and 2 conversions per second the value is 0.10μF. For different conversion rates, the value will change in inverse proportion. A second requirement for good linearity is that the capacitor have low dielectric absorption. Polypropylene caps give good performance at a reasonable price. Finally the foil side of the cap should be connected to the integrator output to shield against pick-up.

The only requirement for the reference cap is that it be low leakage. In order to reduce the effects of stray capacitance, a 1.0μF value is recommended.

CLOCK OSCILLATOR

The ICL7129 achieves its digital range changing by integrating the input signal for 1000 clock pulses (2,000 oscillator cycles) on the 2V scale and 10,000 clock pulses on the 200mV scale. To achieve complete rejection of 60Hz on both scales, an oscillator frequency of 120kHz is required, giving two conversions per second.

In low resolution applications, where the converter uses only 3½ digits and 100μV resolution, an R-C type oscillator is adequate. In this application a C of 51pF is recommended and the resistor value selected from $f_{OSC} = 0.45/RC$. However, when the converter is used to its full potential (4½ digits and 10μV resolution) a crystal oscillator is recommended to prevent the noise from increasing as the input signal is increased due to frequency jitter of the R-C oscillator. Both R-C and crystal oscillator circuits are shown in Figure 13.

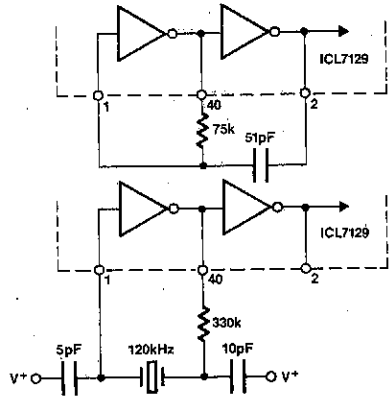


Figure 13. RC and Crystal Oscillator Circuits

POWERING THE ICL7129

The ICL7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies. Figures 14, 15, and 16 show various powering modes that may be used with the ICL7129.

The standard battery connection using a 9V battery is shown on the front page of this data sheet.

The power connection for systems with +5V and −5V supplies available is shown in Figure 14. Notice that measurements are with respect to ground. COMMON is not connected to INPUT LO but is used only as a pre-regulator for the external voltage reference.

It is important to notice that in Figure 14, digital ground of the ICL7129 (DGND pin 36) is **not** directly connected to power supply ground. DGND is set internally to approximately 5V less than the V^+ terminal and is not intended to be used as a power input pin. It may be used as the ground reference for external logic, as shown in Figure 5 and 6. In Figure 5, DGND is used as the negative supply rail for external logic provided that the supply current for the external logic does not cause excessive loading on DGND. The DGND output can be buffered as shown in Figure 6. Here, the logic supply current is shunted away from the ICL7129 keeping the load on DGND low. This treatment of the DGND output is necessary to insure compatibility when the external logic is used to interface directly with the logic inputs and outputs of the ICL7129.

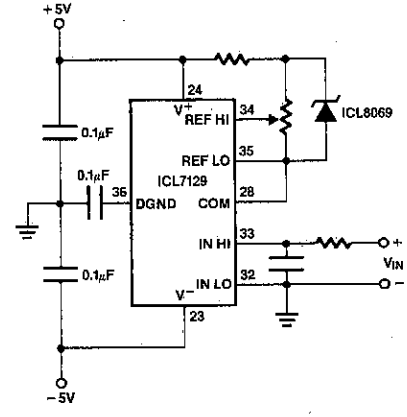


Figure 14. Powering the ICL7129 from +5V and −5V Power Supplies

When a battery voltage between 3.8V and 7V is desired for operation, a voltage doubling circuit should be used to bring the voltage on the ICL7129 up to a level within the power supply voltage range. This operating mode is shown in Figure 15.

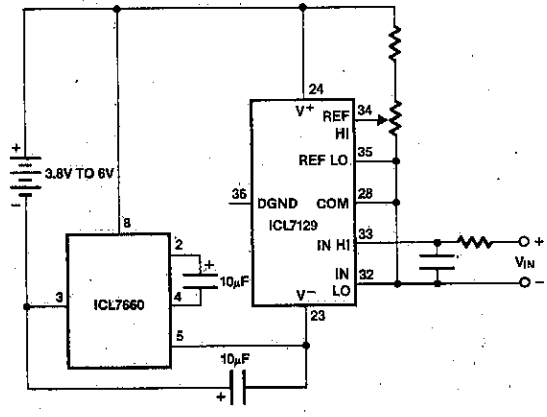


Figure 15. Powering the ICL7129 from a 3.8V to 6V Battery

Again measurements are made with respect to COMMON since the entire system is floating. Voltage doubling is accomplished by using an ICL7660 CMOS voltage converter and two inexpensive electrolytic capacitors. The same principle applies in Figure 16 where the ICL7129 is being used in a system with only a single +5V power supply. Here measurements are made with respect to power supply ground.

A single polarity power supply can be used to power the ICL7129 in applications where battery operation is not appropriate or convenient **only** if the power supply is **isolated** from system ground. Measurements must be made with respect to COMMON or some other voltage within its input common-mode range.

VOLTAGE REFERENCES

The COMMON output of the ICL7129 has a temperature coefficient of ±80ppm/°C typically. This voltage is only suitable as a reference voltage for applications where ambient temperature variations are expected to be minimal. When the ICL7129 is used in most environments, other voltage references should be considered. The diagram on the front page of this data sheet shows the ICL8069 1.2V band-gap voltage source used as the reference for the ICL7129 and the COMMON output as its pre-regulator. The reference voltage for the ICL7129 is set to 1.000V for both 2V and 200mV full-scale operation.

Figures 17 and 18 show two other methods for generating precision references that are compatible with the ICL7129. Both reference voltage and input voltage are connected to power supply ground. The use of a 6.2V reference diode is shown in Figure 18. The voltage drop across $R_1 \approx 2.8V$ to minimize rollover error caused by stray capacitance charging or discharging the reference capacitor. The reference voltage in this case is taken with respect to V^+ and is adjusted with the trim potentiometer connected to REF LO (pin 35).

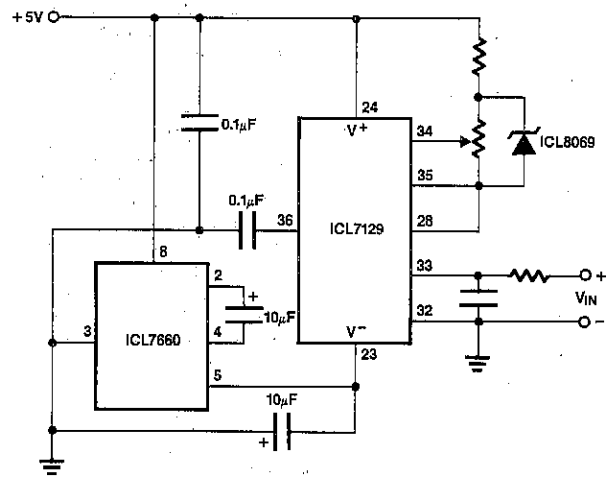


Figure 16. Powering the ICL7129 from a Single Polarity Power Supply

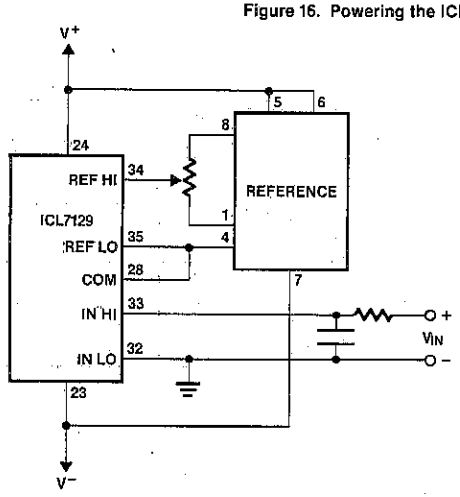


Figure 17. Using a Heated-Substrate 1.000V Reference with the ICL7129

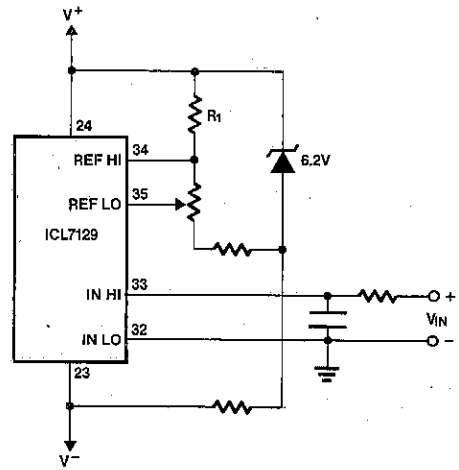


Figure 18. Using a 6.2V Reference Diode with the ICL7129

ICL7134

14-Bit μP-Compatible Multiplying D/A Converter

FEATURES

- 14-bit linearity (0.003% FSR)
- No gain adjustment necessary
- Microprocessor-compatible with double buffered inputs
- Bipolar application requires no extra adjustments or external resistors
- Output current settling-time 3μs max (0.9μs typ)
- Low linearity and gain temperature coefficients
- Low power dissipation
- Full four-quadrant multiplication
- Full temperature range operation

4

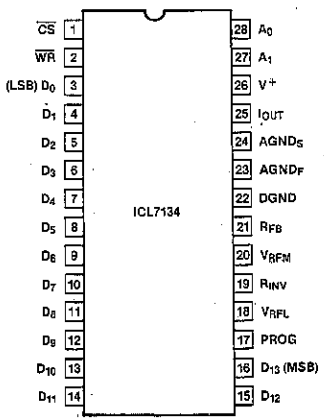
GENERAL DESCRIPTION

The ICL7134 combines a four-quadrant multiplying DAC using thin film resistors and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve true 14-bit linearity without laser trimming.

Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14-bit DAC register, which controls the output switches. The DAC register can also be loaded directly from the data inputs, in which case the registers are transparent.

The ICL7134 is supplied in two versions. The ICL7134U is programmed for unipolar operation while the ICL7134B is programmed for bipolar applications. The V_{REF} input to the most significant bit of the DAC is separated from the reference input to the remainder of the ladder. For unipolar use, the two reference inputs are tied together, while for bipolar operation, the polarity of the MSB reference is reversed, giving the DAC a true 2's complement input transfer function. Two resistors which facilitate the reference inversion are included on the chip, so only an external op-amp is needed. The PROM is coded to correct for errors in these resistors as well as the inversion of the MSB.

PIN CONFIGURATION



(outline dwg JI)

ORDERING INFORMATION

NON-LINEARITY	TEMPERATURE RANGE		
	0°C to +70°C	−25°C to +85°C	−55°C to +125°C
Bipolar Versions			
0.01% (12-bit)	ICL7134BJCJI	ICL7134BJIJI	ICL7134BJMJI
0.006% (13-bit)	ICL7134BKCJI	ICL7134BKIJI	ICL7134BKMJI
0.003% (14-bit)	ICL7134BLCJI	ICL7134BLIJI	ICL7134BLMJI
Unipolar Versions			
0.01% (12-bit)	ICL7134UJCJI	ICL7134UJIJI	ICL7134UJMJI
0.006% (13-bit)	ICL7134UKCJI	ICL7134UKIJI	ICL7134UKMJI
0.003% (14-bit)	ICL7134ULCJI	ICL7134ULIJI	ICL7134ULMJI

Package: 28-pin CERDIP only

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to DGND) ..... −0.3V to 7.5V
V_{RFL}, V_{RFM}, R_{INV}, R_{FB} to DGND ..... ±25V
I_{OUT}, $AGND_F$, $AGND_S$ ..... −0.1V to V^+
Current in $AGND_S$, $AGND_F$ 25mA
An, Dn, $\overline{WR}$, $\overline{CS}$, PROG ..... −0.3V to V^+ + 0.3V
Operating Temperature Range
ICL7134XXC ..... 0°C to +70°C
ICL7134XXI ..... −20°C to +85°C
ICL7134XXM ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation (Note 2) 500mW
Derate Linearly Above 70°C @ 10mW/°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: All voltages with respect to DGND.
Note 2: Assumes all leads soldered or welded to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

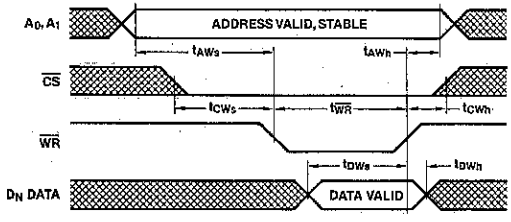
OPERATING CHARACTERISTICS (V^+ = 5V, V_{REF} = 10V, T_A = +25°C unless otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Resolution				14			Bits
Non-Linearity	J		Test Figure 1 (Notes 1 and 2)			0.010	% FSR
	K					0.006	% FSR
	L					0.003	% FSR
Non-Linearity Temperature Coefficient			Operating Temperature Range		1	2	ppm/°C
Gain Error	J		Test Figure 1 (Notes 1 and 2)			0.020	% FSR
	K					0.012	% FSR
	L					0.006	% FSR
Gain Error Temperature Coefficient					2	8	ppm/°C
Monotonicity	J			14			Bits
	K			14			Bits
	L			14			Bits
I_{OUT} Leakage Current		I_{OLK}	T_A = +25°C			10	nA
			Operating Temperature Range		50		
Power Supply Rejection		PSRR	T_A = +25°C, ΔV^+ = ±10%		1	50	ppm/V
			Operating Temperature Range			100	
Output Current Settling Time					0.9	3	µs
Feedthrough Error	ICL7134U		V_{REF} = ±10V, 2kHz Sinewave		250		µVp-p
	ICL7134B				500		
Reference Input Resistance		Z_{REF}	V_{RFL} = V_{RFM} (Unipolar Mode)	4.0		10	kΩ
Output Capacitance		C_{OUT}	DAC Register = All 0's		160		pF
			DAC Register = All 1's		235		
Output Noise			Equivalent Johnson Res.		7		kΩ
Low State Input		V_{INL}	Operating Temperature Range			0.8	V
High State Input		V_{INH}	Operating Temperature Range	2.4			V
Logic Input Current		I_{IIN}	$0 \le V_{IN} \le V^+$			1.0	µA
Logic Input Capacitance		C_{IIN}	(Note 3)		15		pF
Supply Voltage Range		V^+	Functional Operation	3.5		6.0	V
Supply Current		I^+	(Excluding Ladder)		0.06	0.5	mA
Long Term Stability			1000 Hours, +125°C (Note 3)		10		ppm/√month

Note 1: Full-Scale Range (FSR) is 10V for unipolar mode, 20V (±10V) for bipolar mode.
Note 2: Using internal feedback and reference inverting resistors.
Note 3: Guaranteed by design, not 100% tested in production.

AC CHARACTERISTICS (V^+ =5V, see Timing Diagram)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Address-WRite Set-Up Time (Min)	t_{AWs}				100	ns
Address-WRite Hold Time (Min)	t_{AWh}				0	
Chip Select-WRite Set-Up Time (Min)	t_{CWs}				0	
Chip Select-WRite Hold Time (Min)	t_{CWh}				0	
WRite Pulse Width Low (Min)	t_{WR}				200	
Data-WRite Set-Up Time (Min)	t_{DWs}				200	
Data-WRite Hold Time (Min)	t_{DWh}				0	



Timing Diagram

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a straight line function between endpoints. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to full-scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

Table 1. Pin Assignment and Function Description

PIN	SYMBOL	DESCRIPTION	
1	$\overline{CS}$	Chip Select (active low). Enables register write.	
2	$\overline{WR}$	WRite, (active low). Writes in register. Equivalent to $\overline{CS}$.	
3	D_0	Bit 0	Least significant.
4	D_1	Bit 1	Input Data Bits (High = True)
5	D_2	Bit 2	
6	D_3	Bit 3	
7	D_4	Bit 4	
8	D_5	Bit 5	
9	D_6	Bit 6	
10	D_7	Bit 7	
11	D_8	Bit 8	
12	D_9	Bit 9	
13	D_{10}	Bit 10	
14	D_{11}	Bit 11	
15	D_{12}	Bit 12	
16	D_{13}	Bit 13	Most significant.

PIN	SYMBOL	DESCRIPTION	
17	PROG	Used for programming only. Tie to +5V for normal operation.	
18	V_{RFL}	V_{REF} for lower bits.	
19	R_{INV}	Summing node for reference inverting amplifier.	
20	V_{RFM}	V_{REF} for MSB only (bipolar).	
21	R_{FB}	Feedback resistor for voltage output applications.	
22	DGND	Digital GrouND return.	
23	$AGND_F$	Analog GrouND force line. Use to carry current from internal Analog GrouND connections. Tied internally to $AGND_S$.	
24	$AGND_S$	Analog GrouND sense line. Reference point for external circuitry. Pin should carry minimal current; tied internally to $AGND_F$.	
25	I_{OUT}	Current output pin.	
26	V^+	Positive supply voltage.	
27	A_1	Address 1	Control register lines
28	A_0	Address 0	

TEST CIRCUITS (Unipolar operation shown)

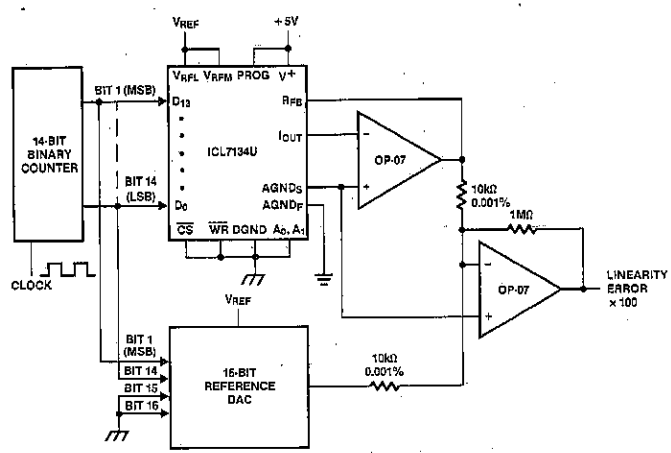


Figure 1. Non-Linearity

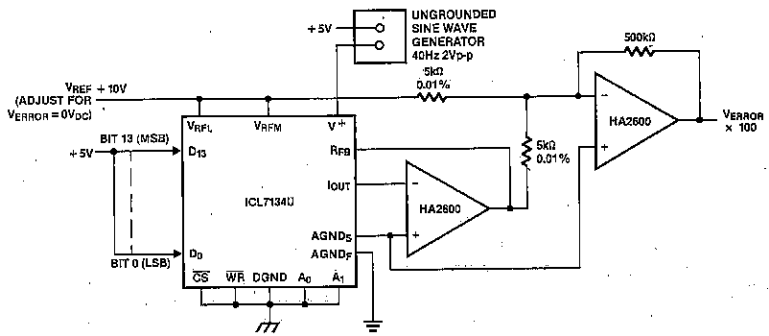


Figure 2. Power Supply Rejection

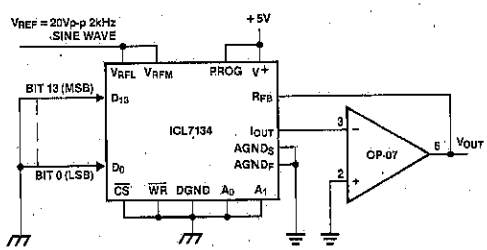


Figure 3. Feedthrough Error

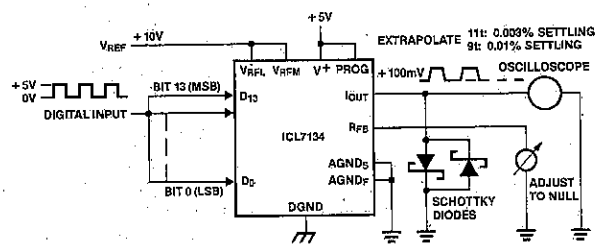


Figure 4. Output Current Settling Time

FUNCTIONAL DIAGRAM

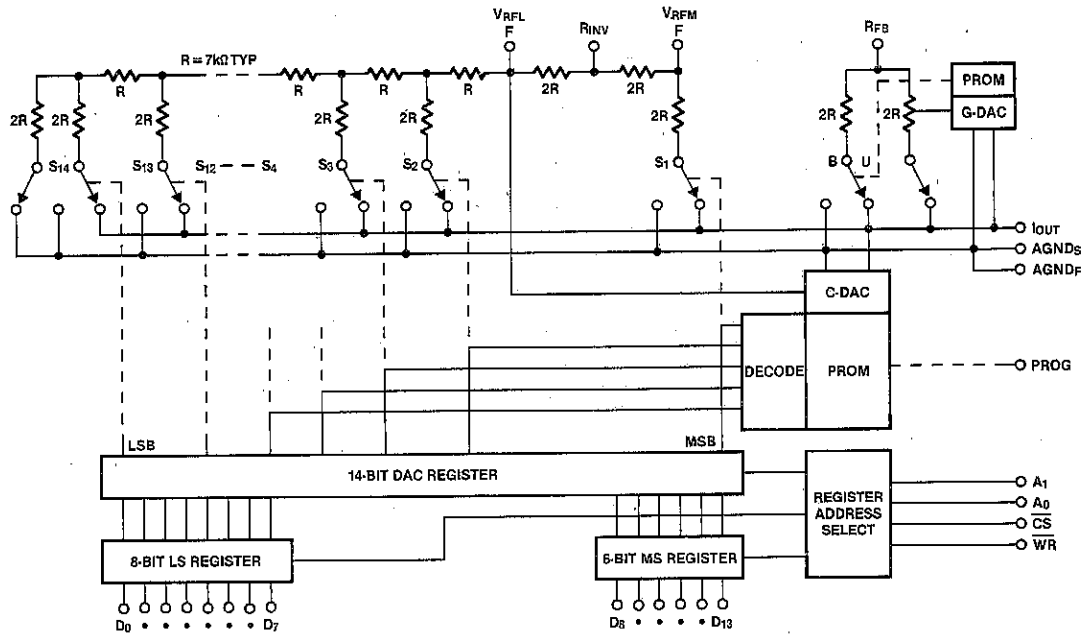


Figure 5. ICL7134 Functional Diagram

DETAILED DESCRIPTION

The ICL7134 consists of a 14-bit primary DAC, two PROM controlled correction DACs, input buffer registers, and microprocessor interface logic (Figure 5). The 14-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistances in the ladder, results in excellent temperature stability.

True 14-bit linearity is achieved by programming a floating polysilicon gate PROM array which controls two correction DAC circuits. A 6-bit gain correction DAC, or G-DAC, diverts up to 2% of the feedback resistor's current to Analog GrouND and reduces the gain error to less than 1 LSB, or 0.006%. The 5 most significant outputs of the DAC register address a 31-word PROM array that controls a 12-bit linearity correction DAC, or C-DAC. For every combination of the primary DAC's 5 most significant bits, a different C-DAC code is selected. This allows correction of superposition errors, caused by bit interaction on the primary resistor ladder's current output bus and by voltage non-linearity in the feedback resistor. Superposition errors cannot be corrected by any method which corrects individual bits only, such as laser trimming. Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging. These packaging shifts limit the accuracy that can be achieved using wafer level correction methods such as laser trimming, which has also been found to degrade the time stability of thin film resistors at the 14-bit level.

Analog Section

The ICL7134 inherently provides both unipolar and bipolar operation. The bipolar application circuit (Figure 6) requires one additional op-amp but no external resistors. The two on-chip resistors, R_{INV1} and R_{INV2}, together with the op-amp, form a voltage inverter which drives the MSB reference terminal, V_{RFM}, to $-V_{REF}$, where V_{REF} is the voltage applied at the less significant bits' reference terminal, V_{RFL}. This reverses the weight of the MSB, and gives the DAC a 2's complement transfer function. The op-amp and reference connection to V_{RFM} and V_{RFL} can be reversed, without affecting linearity, but a small gain error will be introduced. For unipolar operation the V_{RFM} and V_{RFL} terminals are both tied to V_{REF}, and the R_{INV} pin is left unconnected.

Since the PROM correction codes required are different for bipolar and unipolar operation, the ICL7134 is available in two different versions; the ICL7134U, which is corrected for unipolar operation, and the ICL7134B, which is programmed for bipolar application. The feedback resistance is also different in the two versions, and is switched under PROM control from 'R' in the unipolar device to '2R' in the bipolar part. These feedback resistors have a dummy (always ON) switch in series to compensate for the effect of the ladder switches. This greatly improves the gain temperature coefficient and the power supply rejection of the device.

Digital Section

Two levels of input buffer registers allow loading of data from an 8-bit or 16-bit data bus. The A_0 and A_1 pins select one of four operations: 1) load the LS-buffer register with the data at inputs D_0 to D_7; 2) load the MS-buffer register with the data at inputs D_8 to D_{13}; 3) load the DAC register with the contents of the MS and LS-buffer registers and 4) load the DAC register directly from the data input pins (see Table 2). The $\overline{CS}$ and $\overline{WR}$ pins must be low to allow data transfers to occur. When direct loading is selected ($\overline{CS}$, $\overline{WR}$, A_0 and A_1 low) the registers are transparent, and the data input pins control the DAC output directly. The other modes of operation allow double buffered loading of the DAC from an 8-bit bus.

These input data pins are also used to program the PROM under control of the PROG pin. This is done in manufacturing, and for normal read-only use the PROG pin should be tied to V^+ (+5V).

Table 2. Data Loading Controls

CONTROL I/P				ICL7134 OPERATION
A_0	A_1	$\overline{CS}$	$\overline{WR}$	
X	X	X	1	No operation, device not selected.
X	X	1	X	
0	0	0	0	Load all registers from data bus.
0	1	0	0	Load LS register from data bus.
1	0	0	0	Load MS register from data bus.
1	1	0	0	Load DAC register from MS and LS register.

Note: Data is latched on LO-HI transition of either $\overline{WR}$ or $\overline{CS}$.

APPLICATIONS

General Recommendations

Ground Loops

Careful consideration must be given to ground loops in any 14-bit accuracy system. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, the $AGND_F$ and $AGND_S$ pins. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 7. Thus output signals should be referenced to the sense pin $AGND_S$, as shown in the various application circuits.

Operational Amplifier Selection

To maintain static accuracy, the I_{OUT} potential must be exactly equal to the $AGND_S$ potential. Thus output amplifier selection is critical, in particular low input bias current (less than 2nA), low offset voltage drift (depending on the temperature range) and low offset voltage (less than 25μV) are advisable if the highest accuracy is needed. Maintaining a low input offset over a 0V to 10V range also requires that the output amplifier has a high open loop gain (A_{VOL} > 400k for effective input offset less than 25μV).

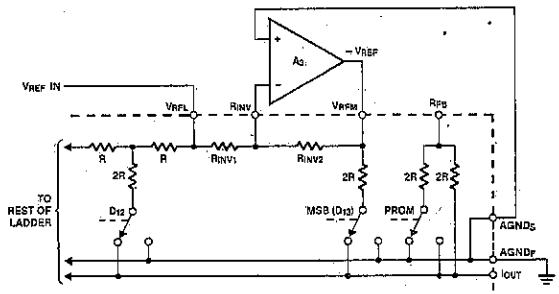


Figure 6. Bipolar Operation, with Inverted V_{REF} to MSB

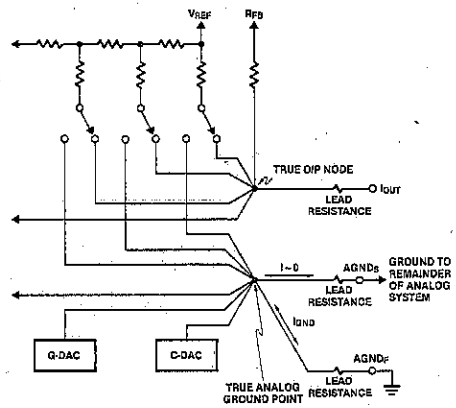


Figure 7. Eliminating Ground Loops

The reference inverting amplifier used in the bipolar mode circuit must also be selected carefully. If 14-bit accuracy is desired without adjustment, low input bias current (less than 1nA), low offset voltage (less than 50μV), and high gain (greater than 400k) are recommended. If a fixed reference voltage is used, the gain requirement can be relaxed. For highest accuracy (better than 13 bits), an additional op-amp may be needed to correct for IR drop on the Analog GrouND line (op-amp A_2 in Figure 9). This op-amp should be selected for low bias current (less than 2nA) and low offset voltage (less than 50μV).

The op-amp requirements can be readily met by use of an ICL7650 chopper stabilized device. For faster settling time, an HA26XX can be used with an ICL7650 providing automatic offset null (see A053 for details).

The output amplifier's non-inverting input should be tied directly to $AGND_S$. A bias current compensation resistor is of limited use since the output impedance at the summing node depends on the code being converted in an unpredictable way. If gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

4

Power Supplies

The V^+ (pin 25) power supply should have a low noise level, and no transients exceeding 7 volts. Note that the absolute maximum digital input voltage allowed is V^+, which therefore must be applied before digital inputs are allowed to go high. Unused digital inputs must be connected to GND or V^+ for proper operation.

Unipolar Binary Operation (ICL7134U)

The circuit configuration for unipolar mode operation (ICL7134U) is shown in Figure 8. With positive and negative V_{REF} values the circuit is capable of two-quadrant multiplication. The "digital input code/analog output value" table for unipolar mode is given in Table 3. The Schottky diode (HP5082-2811 or equivalent) protects I_{OUT} from negative excursions which could damage the device, and is only necessary with certain high speed amplifiers. For applications where the output reference ground point is established somewhere other than at the DAC, the circuit of Figure 9 can be used. Here, op-amp A_2 removes the slight error due to IR voltage drop between the internal Analog GrouND node and the external ground connection. For 13-bit or lower accuracy, omit A_2 and connect $AGND_F$ and $AGND_S$ directly to ground through as low a resistance as possible.

Table 3. Code Table - Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-1/2^{14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2+1/2^{14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2-1/2^{14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2^{14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Zero Offset Adjustment

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Adjust offset zero-adjust trim-pot of the operational amplifier A_2, if used, for a maximum of 0V ±50μV at $AGND_S$.
3. Adjust the offset zero-adjust trim-pot of the output op-amp, A_1, for a maximum of 0V ±50μV at V_{OUT}.

Gain Adjustment (Optional)

1. Connect all data inputs to V^+, connect $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Monitor V_{OUT} for a $-V_{REF}(1-1/2^{14})$ reading.
3. To decrease V_{OUT}, connect a series resistor of 100Ω or less between the reference voltage and the V_{RFM} and V_{RFL} terminals (pins 20 and 18).
4. To increase V_{OUT}, connect a series resistor of 100Ω or less between A_1 output and the R_{FB} terminal (pin 21).

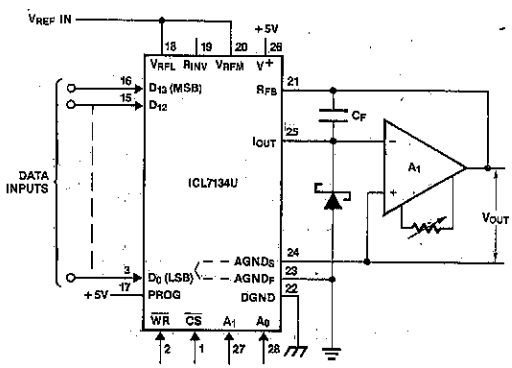


Figure 8. Unipolar Binary, Two-Quadrant Multiplying Circuit

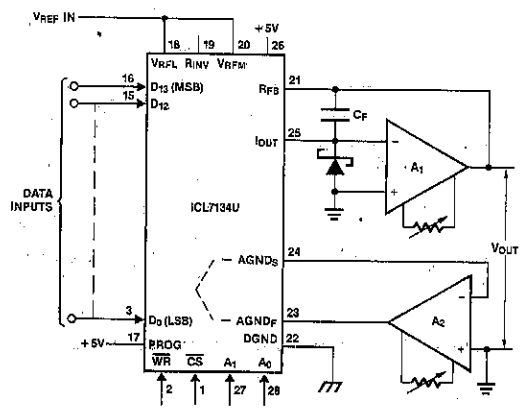


Figure 9. Unipolar Binary Operation with Forced Ground

Bipolar (2's Complement) Operation (ICL7134B)

The circuit configuration for bipolar mode operation (ICL7134B) is shown in Figure 10. Using 2's complement digital input codes and positive and negative reference voltage values, four-quadrant multiplication is obtained. The "digital input code/analog output value" table for bipolar mode is given in Table 4. Amplifier A_3, together with internal resistors R_{INV1} and R_{INV2}, forms a simple voltage inverter circuit. The MSB ladder leg sees a reference input of approximately $-V_{REF}$, so the MSB's weight is reversed from the polarity of the other bits. In addition, the ICL7134B's feedback resistance is switched to 2R under PROM control, so that the bipolar output range is $+V_{REF}$ to $-V_{REF}(1-1/2^{13})$. Again, the grounding arrangement of Figure 9 can be used, if necessary.

Table 4. Code Table -Bipolar (2's Complement) Operation

DIGITAL INPUT	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-1/2^{13})$
0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2^{13})$
0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1 1	$V_{REF}(1/2^{13})$
1 0 0 0 0 0 0 0 0 0 0 0 1	$V_{REF}(1-1/2^{13})$
1 0 0 0 0 0 0 0 0 0 0 0 0	V_{REF}

Offset Adjustment

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Adjust the offset zero-adjust trim-pot of the operational amplifier A_2, if used, for a maximum of 0V $\pm 50\mu V$ at $AGND_S$.
3. Set data to 00000....00. Adjust the offset zero-adjust trim-pot of the output op-amp A_1, for a maximum of 0V $\pm 50\mu V$ at V_{OUT}.
4. Connect D_{13} (MSB) data input to V^+.
5. Adjust the offset zero-adjust trim-pot of op-amp A_3 for a maximum of 0V $\pm 50\mu V$ at the R_{INV} terminal (pin 19).

Gain Adjustment (Optional)

1. Connect $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Connect D_0, D_1...D_{12} to V^+, D_{13} (MSB) to DGND.
3. Monitor V_{OUT} for a $-V_{REF}(1-1/2^{13})$ reading.
4. To increase V_{OUT}, connect a series resistor of 200Ω or less between the A_1 output and the R_{FB} terminal (pin 21).
5. To decrease V_{OUT}, connect a series resistor of 100Ω or less between the reference voltage and the V_{RFL} terminal (pin 18).

Processor Interfacing

The ease of interfacing to a processor can be seen from Figure 11, which shows the ICL7134 connected to an 8035 or any other MCS-48 processor such as an 8049. The data bus feeds into both register inputs; three port lines, in combination with the $\overline{WR}$ line, control the byte-wide loading into these registers and then the DAC register. A complete DAC set-up requires 4 write instructions to the port, to set up the address and $\overline{CS}$ lines, and 3 external data transfers, one a dummy for the final transfer to the DAC register.

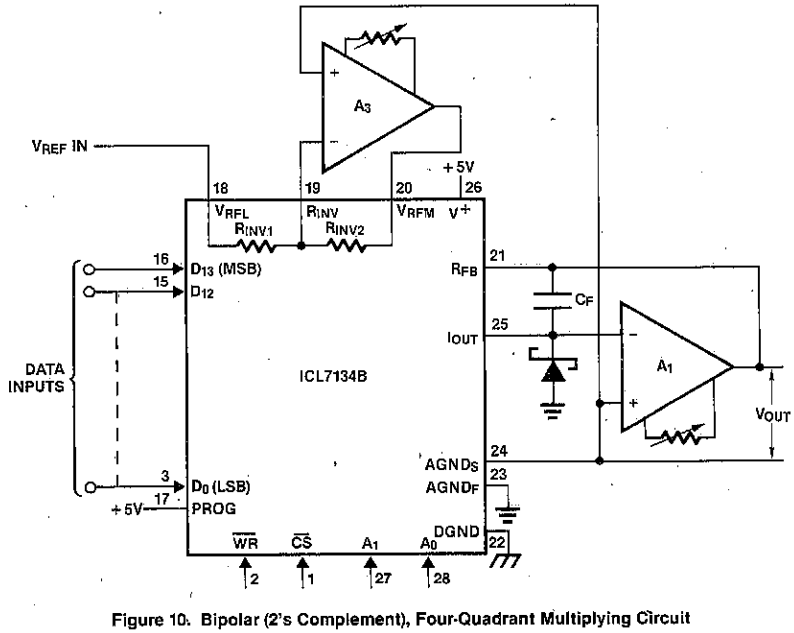


Figure 10. Bipolar (2's Complement), Four-Quadrant Multiplying Circuit

A similar arrangement can be used with the MCS-80 system, using an 8080A, 8228, and 8224 CPU set. Figure 12 shows the circuit, which can be arranged as a memory-mapped interface (using $\overline{MEMW}$) or as an I/O-mapped interface (using $\overline{I/O\ WRITE}$). See A020 and R005 for discussions of the relative merits of memory-mapped versus I/O-mapped interfacing, as well as some other ideas on interfacing with 8080 processors. The MCS-85 family 8085 processor has a very similar interface, except that the control lines available are slightly different, as shown in Figure 13. The decoding of the $\overline{IO/M}$ line, which controls memory-mapped or I/O-mapped operation, is arbitrary, and can be omitted if not necessary.

Neither the MC-680X nor MCS-650X processor families offer specific I/O operations. Figure 14 shows a suitable interface to either of these systems, using a direct connection. Several other decoding options can be used, depending on the other control signals generated in the system. Note that the MCS-650X family does not require VMA to be decoded with the address lines.

Figure 15 shows an interface to the Intersil IM6100 CMOS microprocessor family using the IM6101 PIE to control the data transfers. Here the data is read directly from the microprocessor data bus in an 8-bit and a 6-bit word. The flag lines control the data destination.

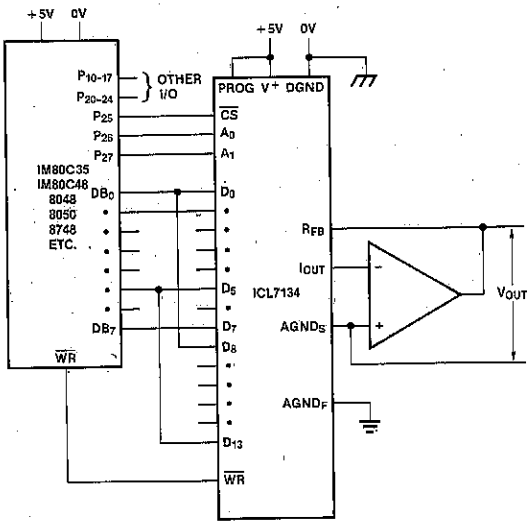


Figure 11. ICL7134 Interface to MCS-48 System

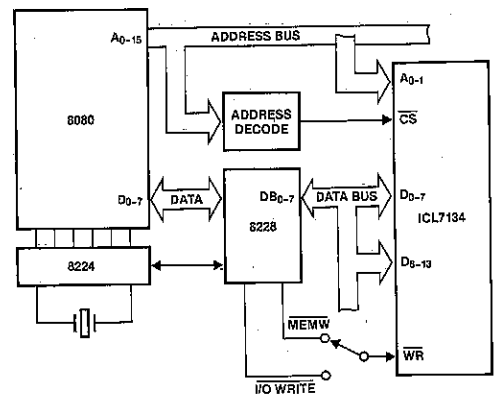


Figure 12. Interface to MCS-80 System

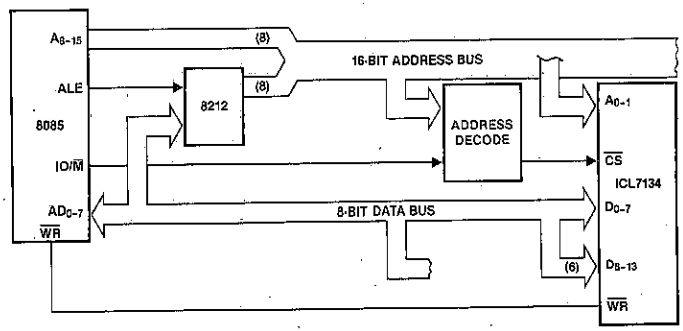


Figure 13. MCS-85 System Interface

Digital Feedthrough

All of the direct interfaces shown above can suffer from a capacitive coupling problem. The 14 data pins, and 4 control pins, all tied to active lines on a microprocessor bus, and in close proximity to the sensitive DAC circuitry, can couple pseudo-random spikes into the analog output. Careful board layout and shielding can minimize the problems (see **PC layout**), and clearly wire-wrap type sockets should never be used. Nevertheless, the inherent capacitance of the package alone can lead to unacceptable digital feedthrough in many cases. The only solution is to keep the digital input lines as inactive as possible. One easy way to do this is to use the peripheral interface circuitry available with all the systems previously discussed. These generally allow only 8 bits to be updated at any one time, but a little ingenuity will avoid difficulties with DAC steps that would result from partial updates. The problem can be solved for the MCS-48 family by tying the 14 port lines to the data input lines, with $\overline{CS}$, A_0 and A_1 held low, and using only the $\overline{WR}$ line to enter the data into the DAC (as shown in Figure 16). $\overline{WR}$ is well separated from the analog lines on the ICL7134, and is usually not a very active line in MCS-48 systems. Additional "protection" can be achieved by gating the processor $\overline{WR}$ line with another port line. The heavy use of port lines can be alleviated by use of the IM82C43 port expander. The same type of technique can be employed in the MCS-80/85 systems by using an 8255 PIA (peripheral interface adapter) (Figure 17) and in the MC-680X and MCS-650X systems by using an MC-6820 (MCS-6520) PIA.

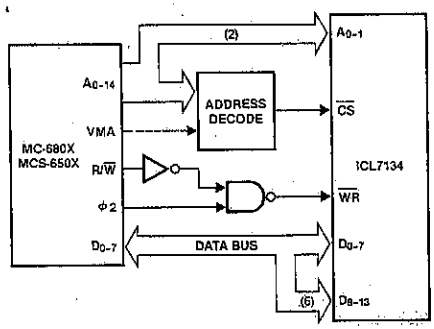


Figure 14. MCS-650X and MC-680X Families' Interface to ICL7134

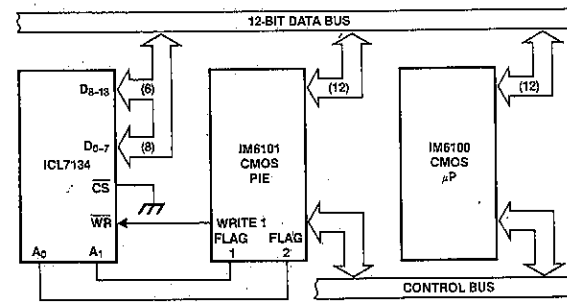


Figure 15. ICL7134 to IM6100 Interface Using IM6101 PIE

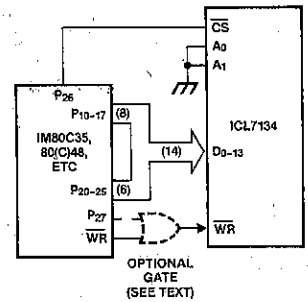


Figure 16. Avoiding Digital Feedthrough in an MCS-48 to ICL7134 Interface

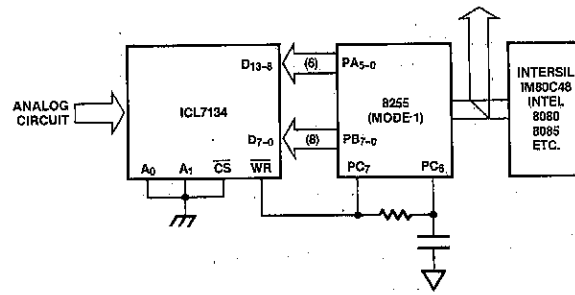


Figure 17. ICL7134 to MCS-48, -80, -85 Interface with Low Feedthrough

Successive Approximation A/D Converters

Figure 18 shows an ICL7134B-based circuit for a bipolar input high speed A/D converter, using two AM25L03s to form a 14-bit successive approximation register. The comparator is a two-stage circuit with an HA2605 front-end amplifier, used to reduce settling time problems at the summing node (see A020). Careful offset-nulling of this amplifier is needed, and if wide temperature range operation is desired, an auto-null circuit using an ICL7650 is probably advisable (see A053). The clock, using two Schmitt trigger TTL gates, runs at a slower rate for the first 8 bits, where settling-time is most critical, than for the last 6 bits. The short-cycle line is shown tied to the 15th bit; if fewer bits are required, it can be moved up accordingly. The circuit will free-run if the HOLD/$\overline{\text{RUN}}$ input is held low, but will stop after completing a conversion if the pin is high at that time. A low-going pulse will restart it. The STATUS output indicates when the device is operating, and the falling edge indicates the availability of new data. A unipolar version may be constructed by tying the MSB (D_{13}) on an ICL7134U to pin 14 on the first AM25L03, deleting the reference inversion amplifier A_4, and tying V_{RFM} to V_{RFL}.

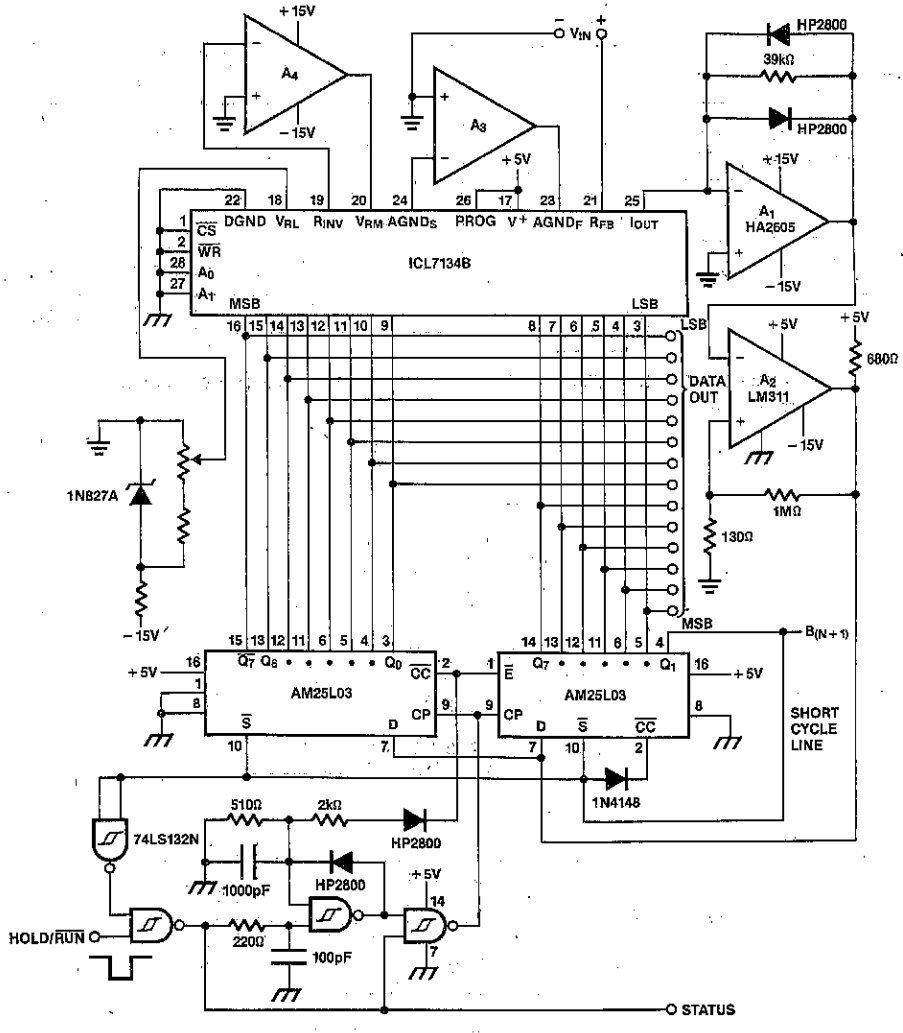


Figure 18. Successive Approximation A/D Converter

PC BOARD LAYOUT

Great care should be taken in the board layout to minimize ground loop and similar "hidden resistor" problems, as well as to minimize digital signal feedthrough. A suitable layout for the immediate vicinity of the ICL7134 is shown in Figure 19, and may be used as a guide.

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters," by Dave Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

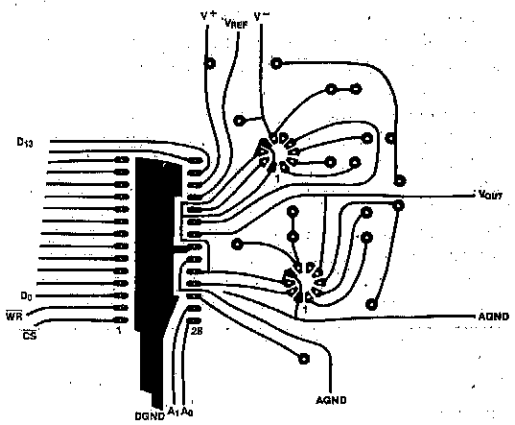
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.

A021 "Power A/D Converters Using the ICH8510," by Dick Wilenken.

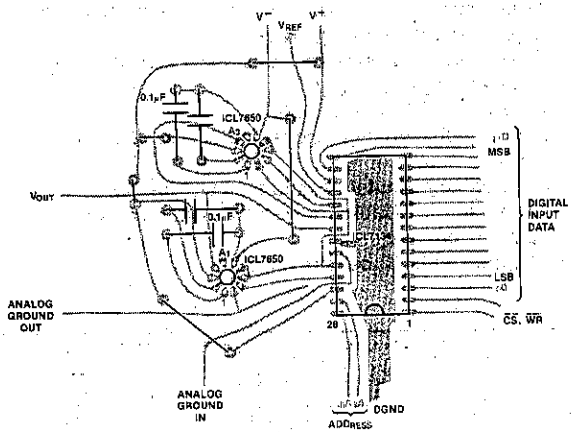
A030 "The ICL7104—A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

Most of these are available in the Intersil Data Acquisition Handbook, together with other material.



(a) Printed Circuit Side of Card (Single Sided Board)



(b) Top Side with Component Placement

Figure 19. Printed Circuit Board Layout (Bipolar Circuit, see Figure 10)

ICL7135

Precision 4½ Digit Single Chip A/D Converter

FEATURES

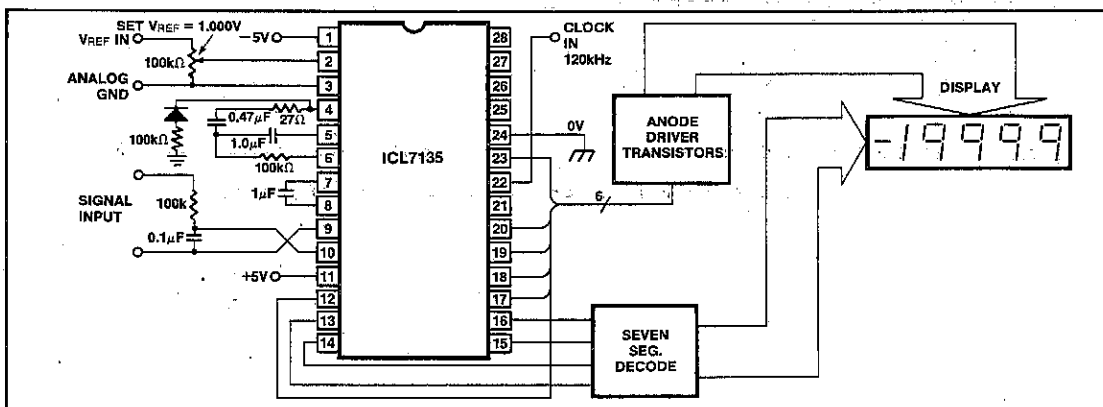
- **Accuracy guaranteed to ±1 count over entire ±20,000 counts (2.0000 volts full scale)**
- **Guaranteed zero reading for 0 volts input**
- **1 pA typical input current**
- **True differential input**
- **True polarity at zero count for precise null detection**
- **Single reference voltage required**
- **Over-range and under-range signals available for auto-ranging capability**
- **All outputs TTL compatible**
- **Blinking display gives visual indication of over-range**
- **Six auxillary inputs/outputs are available for interfacing to UARTs, microprocessors or other complex circuitry**
- **Multiplexed BCD output versatility**

4

GENERAL DESCRIPTION

The Intersil ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS I.C., with the exception of display drivers, reference, and a clock.

The Intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include STROBE, OVERRANGE, UNDER-RANGE, RUN/HOLD and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

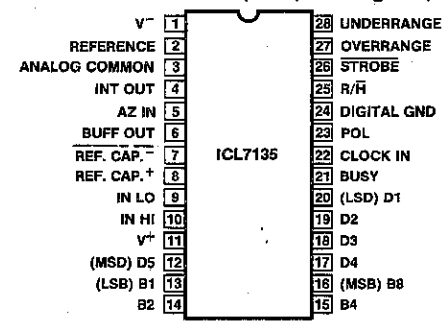


ICL7135 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7135	28-Pin CERDIP	0°C to +70°C	ICL7135CJI
7135	28-Pin Plastic DIP	0°C to +70°C	ICL7135CPI
EV/KIT	Evaluation Kit (PC Board, active, passive components)		ICL135EV/KIT

PIN CONFIGURATION (Outline dwgs JI, PI)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 2)
- Ceramic Package ..... 1000 mW
- Plastic Package ..... 800 mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Gnd to V^+

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7135 ELECTRICAL CHARACTERISTICS (Note 1)

$V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

		CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG		Zero Input Reading		$V_{IN} = 0.0V$ Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
		Ratiometric Reading (2)		$V_{IN} \equiv V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
		Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
		Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
		Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error
	(Note 1) (Note 2)	Noise (P-P value not exceeded 95% of time)	e_n	$V_{IN} = 0V$ Full scale = 2.000V		15		μV
		Leakage Current at Input	I_{ILK}	$V_{IN} = 0V$		1	10	pA
		Zero Reading Drift		$V_{IN} = 0V$ $0° \le T_A \le 70°C$		0.5	2	μV/°C
		Scale Factor Temperature Coefficient (3)	TC	$V_{IN} = +2V$ $0 \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL	INPUTS	Clock In, Run/$\overline{\text{Hold}}$, See Fig. 2	V_{INH} V_{INL} I_{INL} I_{INH}	 $V_{IN} = 0$ $V_{IN} = +5V$	2.8	2.2 1.6 0.02 0.1	 0.8 0.1 10	V mA μA
	OUTPUTS	All Outputs	V_{OL}	$I_{OL} = 1.6ma$		0.25	0.40	V
		B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OH}	$I_{OH} = -1mA$	2.4	4.2		V
		$\overline{\text{BUSY}}$, $\overline{\text{STROBE}}$, OVER-RANGE, UNDER-RANGE POLARITY	V_{OH}	$I_{OH} = -10\mu A$	4.9	4.99		V
	SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
		−5V Supply Range	V^-		−3	−5	−8	V
		+5V Supply Current	I^+	$f_C = 0$		1.1	3.0	mA
		−5V Supply Current	I^-	$f_C = 0$		0.8	3.0	
		Power Dissipation Capacitance	C_{PD}	vs. Clock Freq		40		pF
	Clock	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4-1/2 digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.
Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.
Note 3: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.
Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

TEST CIRCUIT

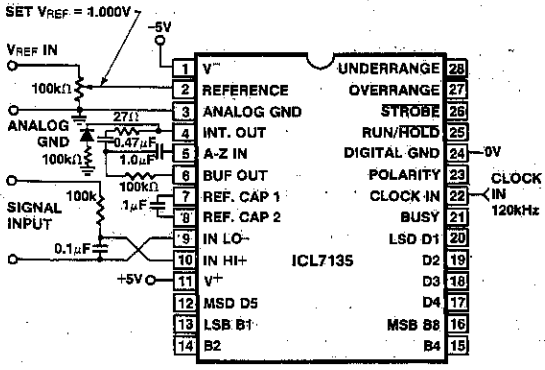


Figure 1: 7135 Test Circuit

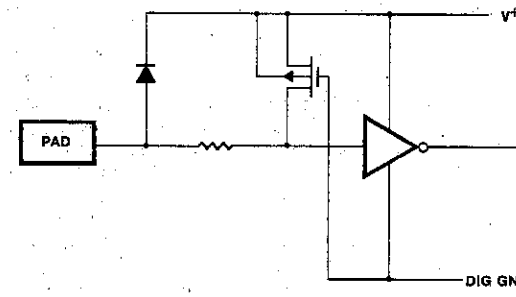


Figure 2: 7135 Digital Logic Input

DETAILED DESCRIPTION

Analog Section

4

Figure 3 shows the Block Diagram of the Analog Section for the ICL7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT), (3) deintegrate (DE) and (4) zero integrator (ZI).

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal-integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F/F.

3. De-Integrate phase

The Third phase is de-integrate, or reference integrate. Input Low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 10,000 ($\frac{V_{IN}}{V_{REF}}$).

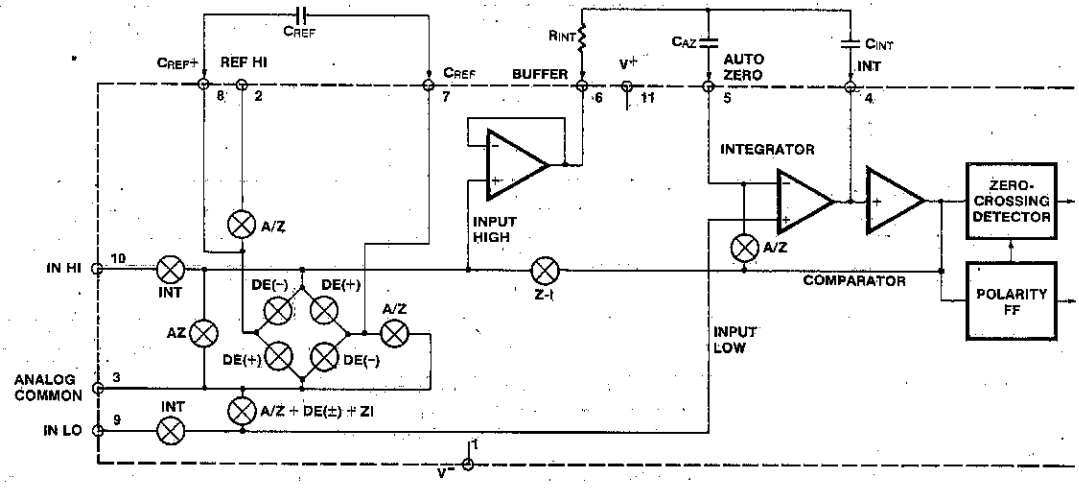


Figure 3: Analog Section of ICL7135

4. Zero Integrator phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog COMMON

Analog COMMON is used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Fig. 4.

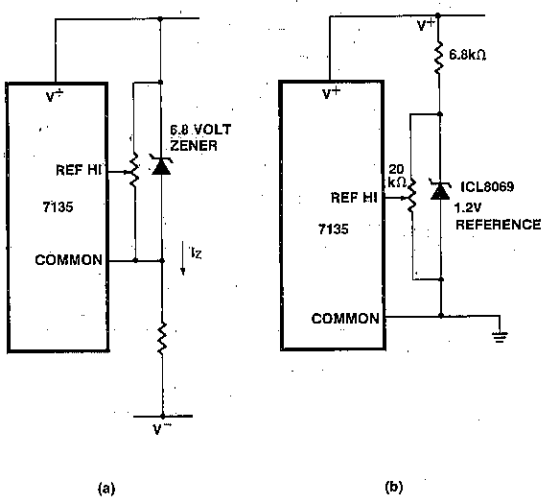


Figure 4: Using an External Reference

DETAILED DESCRIPTION

Digital Section

Figure 5 is the Digital Section of the 7135. It is identical to the 7103 except that the 4-1/2/3-1/2 digit pin has been eliminated (mask-option; consult factory). The 7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

1. RUN/$\overline{\text{HOLD}}$ (Pin 25). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002 clock pulses. If taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as R/$\overline{\text{H}}$ is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of auto zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if Run/$\overline{\text{Hold}}$ is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

2. $\overline{\text{STROBE}}$ (Pin 26). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going $\overline{\text{STROBE}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pules after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{STROBE}}$ pulse goes negative for 1/2 clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the $\overline{\text{STROBE}}$ goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last $\overline{\text{STROBE}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional $\overline{\text{STROBE}}$ pulses will be sent until a new measurement is available.

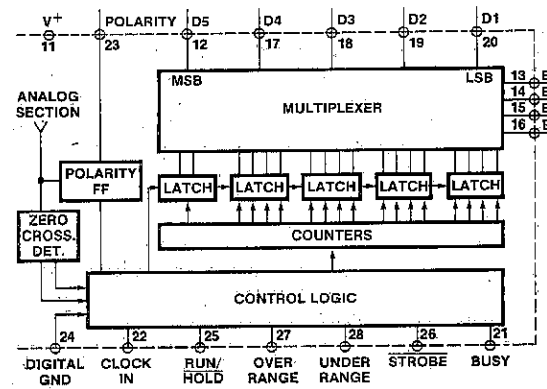


Figure 5: Digital Section 7135

3. BUSY (Pin 21). BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an over-range). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY, so it may also be considered a $(\overline{ZI + AZ})$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received - as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.

4. OVER-RANGE (Pin 27). This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F-F is set at the end of BUSY and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

5. UNDER-RANGE (Pin 28). This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.

6. POLARITY (Pin 23). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

7. Digit Drives (Pins 12, 17, 18, 19 and 20). Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned and this scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This can give a blinking display as a visual indication of over-range.

8. BCD (Pins 13, 14, 15 and 16). The Binary coded Decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the digit driver signal.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. Values of 5 to 40μA give good results, with a nominal of 20μA, and the exact value of integrating resistor may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is fine, and 0.47μF is nominal. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{integrator output voltage swing}} = \frac{(10{,}000)\,(\text{clock period})\,(20\mu A)}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

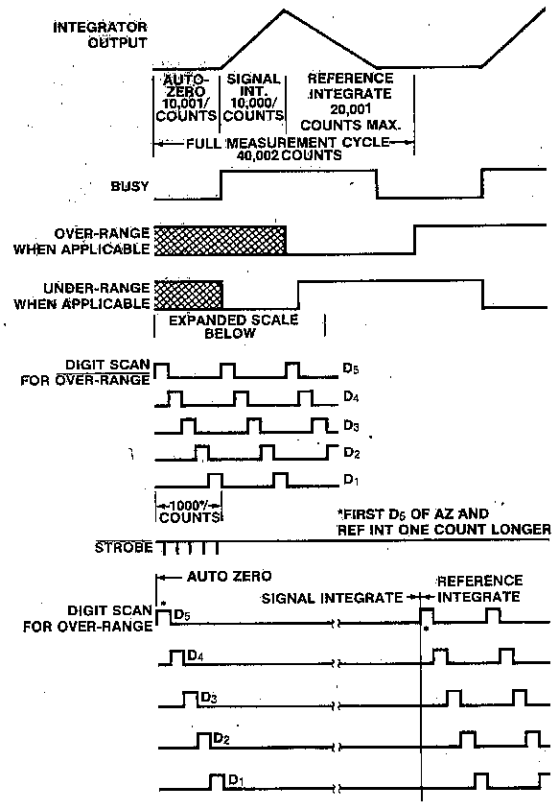


Figure 6: Timing Diagram for Outputs

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

Rollover Resistor and Diode

A small rollover error occurs in the 7135, but this can be easily corrected by adding a diode and resistor in series between the INTegrator OUTput and analog COMMON or ground. The value shown in the schematics is optimum for the recommended conditions, but if integrator swing or clock frequency is modified adjustment may be needed. The diode can be any silicon diode, such as a 1N914. These components can be eliminated if rollover error is not important, and may be altered in value to correct other (small) sources of rollover as needed.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3μs delay, and at a clock frequency of 160kHz (6μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50μV input, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant nonlinearities in the first few counts of the instrument - see Application Note A017.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, 166⅔kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

4

EVALUATING THE ERROR SOURCES

Errors from the "ideal" cycle are caused by:

1. Capacitor droop due to leakage.
2. Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity (dielectric absorption.)
6. Charge lost by C_{REF} in charging C_{stray}.
7. Charge lost by C_{AZ} and C_{INT} to charge C_{stray}.

Each of these errors is analyzed for its error contribution to the converter in application notes listed on the back page, specifically A017 and A032.

NOISE

The peak-to-peak noise around zero is approximately 15μV (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately 30μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

POWER SUPPLIES

The 7135 is designed to work from ±5V supplies. However, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.

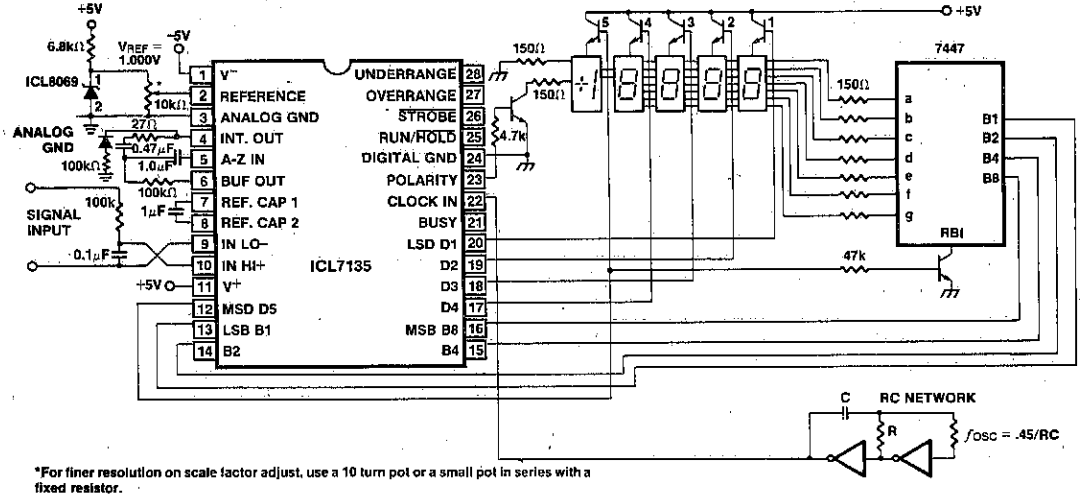
See "differential input" for a discussion of the effects this will have on the integrator swing without loss of linearity.

TYPICAL APPLICATIONS

The circuits which follow show some of the wide variety of possibilities, and serve to illustrate the exceptional versatility of this A/D converter.

Figure 7 shows the complete circuit for a 4-1/2 digit (±2.000V) full scale) A/D with LED readout using the ICL8069 as a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50μA. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The 1/2 digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder. The 2-gate clock circuit should use CMOS gates to maintain good power supply rejection.

Figure 8 is similar except the output drives a multiplexed common cathode LED Display with the 7-Common Emitter Transistor Array, for the digit driver transistors, making a lower component count possible. Both versions of the complete circuit will give a blinking display as a visual indication of overrange. A clock oscillator circuit using the ICM7555 CMOS timer is shown.



*For finer resolution on scale factor adjust, use a 10 turn pot or a small pot in series with a fixed resistor.

Figure 7: 4-1/2 Digit A-D Converter with a multiplexed common anode LED display

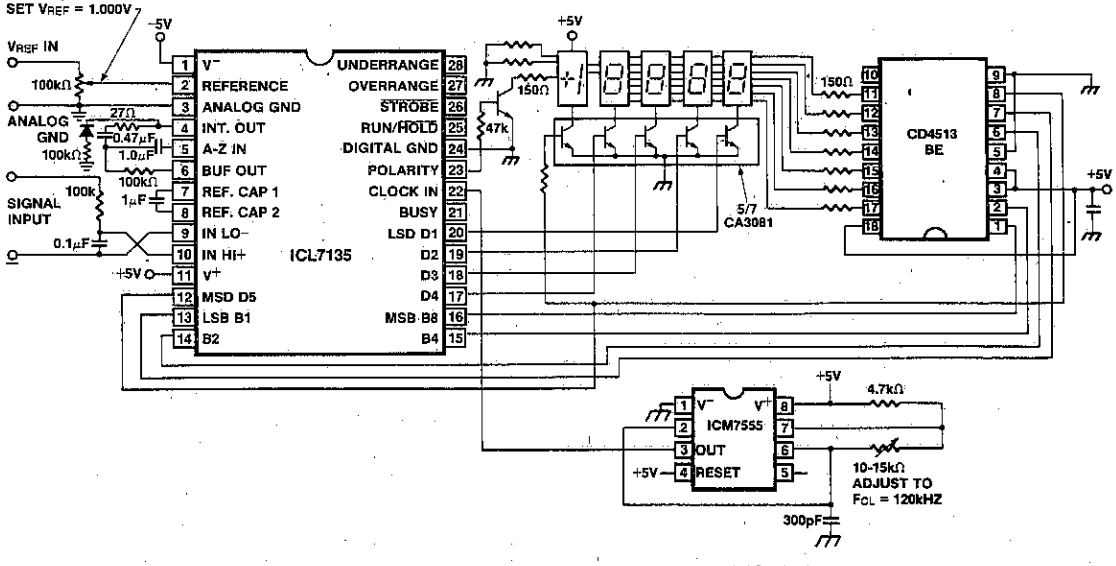


Figure 8: Driving multiplexed common cathode LED displays

A suitable circuit for driving a plasma-type display is shown in Fig. 9. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'BI' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2.5k & 3k resistors set the current levels in the display. A similar arrangement can be used with Nixie® tubes.

The popular LCD displays can be interfaced to the O/P of the ICL7135 with suitable display drivers, such as the ICM7211A as shown in Figure 11. A standard CMOS 4000 series LCD driver circuit is used for displaying the 1/2 digit, the polarity, and an 'overrange' flag. A similar circuit can be used with the ICL7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-1/2 digit (±2.000V) A/D.

Figure 10 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the $\overline{\text{STROBE}}$ signal and 'Overrange' is indicated by blanking the 4 full digits.

® Nixie is a registered trademark of Burroughs Corporation.

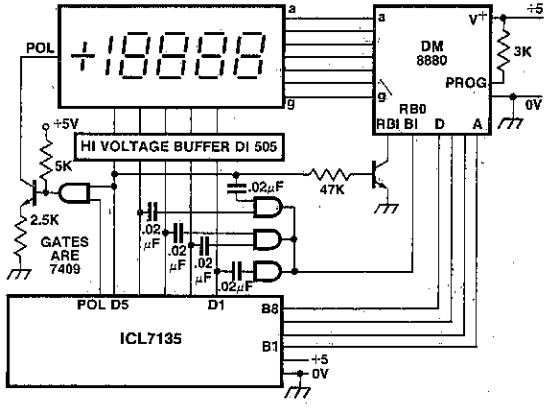


Figure 9: ICL7135 Plasma Display Circuit

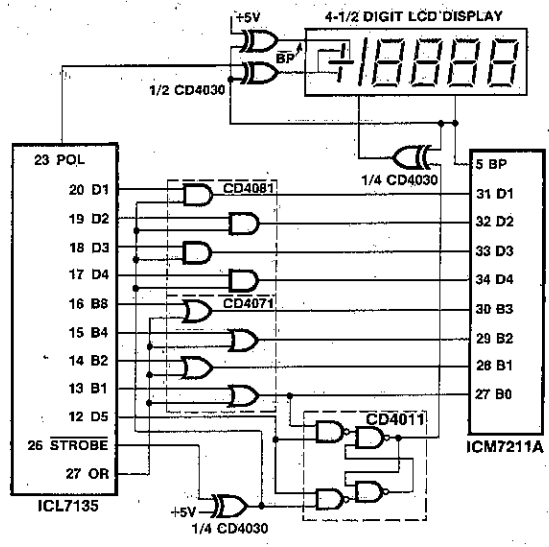


Figure 10: LCD Display with Digit Blanking on Overrange

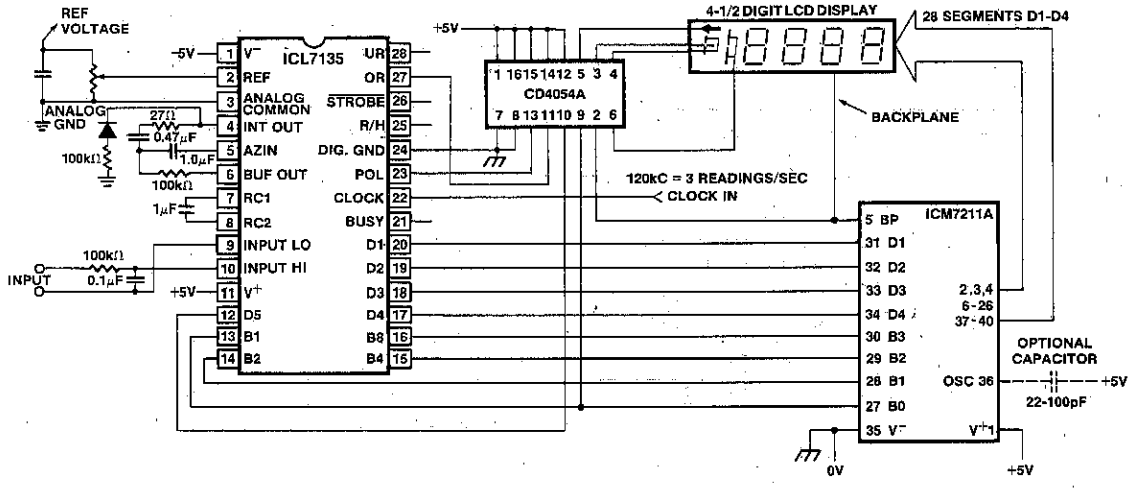


Figure 11: Driving LCD Displays

TYPICAL APPLICATIONS (Contd.)

A problem sometimes encountered with both LED & plasma-type display driving is that of clock source supply line variations. Since the supply is shared with the display, any variation in voltage due to the display reading may cause clock supply voltage modulation. When in overrange the display alternates between a blank display and the 0000 overrange indication. This shift occurs during the reference integrate phase of conversion causing a low display reading just after overrange recovery. Both of the above circuits have considerable current flowing in the digital supply from drivers, etc. A clock source using Intersil's LM311 voltage comparator in positive feedback mode (Figure 12) could minimize any clock frequency shift problem.

The 7135 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from 2 capacitors, and an inexpensive I.C. (Figure 13).

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 14 shows a very simple interface between a free-running ICL7135 and a UART. The five $\overline{\text{STROBE}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 15. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The BUSY signal resets the Data Ready Reset (DRR). Again $\overline{\text{STROBE}}$ starts the

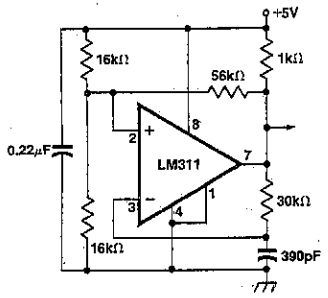


Figure 12: LM311 Clock Source

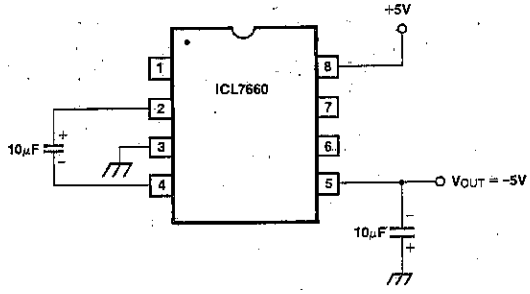


Figure 13: Generating Negative Supply from +5V

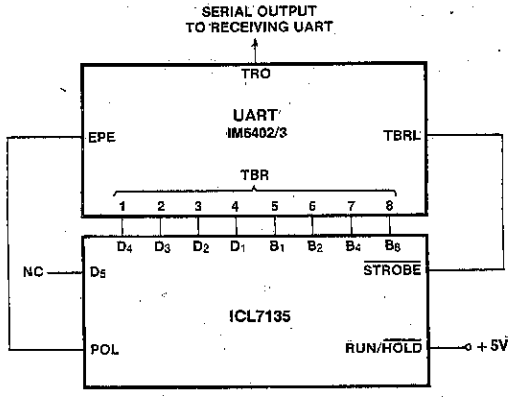


Figure 14: ICL7135 to UART Interface

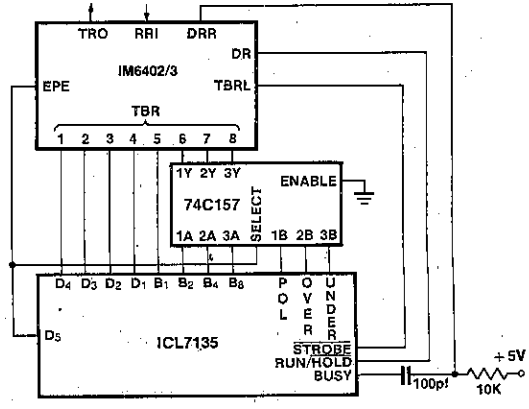


Figure 15: Complex ICL7135 to UART Interface

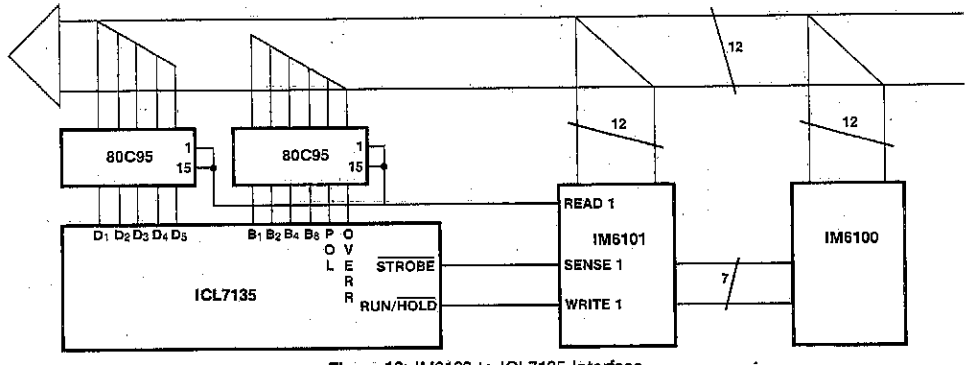


Figure 16: IM6100 to ICL7135 Interface

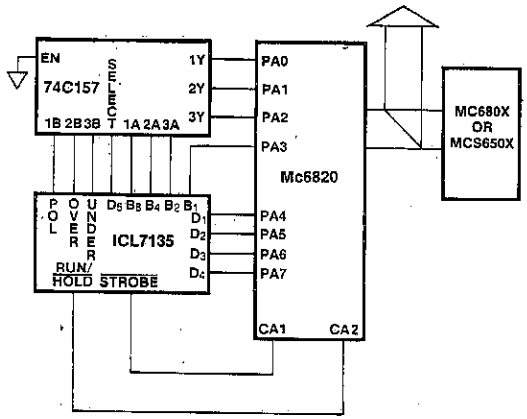


Figure 17: ICL7135 to MC6800, MCS650X Interface

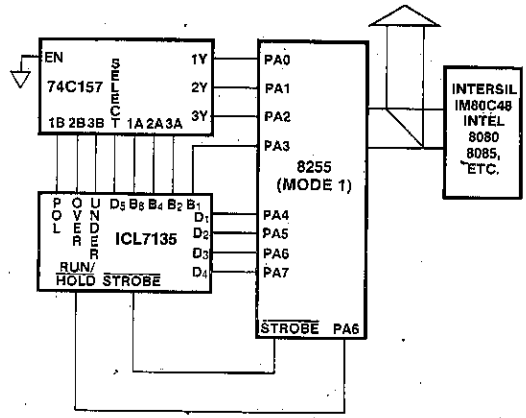


Figure 18: ICL7135 to MCS-48, -80, 85 Interface

transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next $\overline{\text{STROBE}}$ pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the ICL7135 directly with three popular microprocessors are shown in Figures 16, 17 and 18. The main differences in the circuits are that the IM6100 with its 12 bit word capability can accept polarity, over-range, under-range, 4 bits of BCD and 5 digits simultaneously where the 8080/8048 and the MC6800 groups with 8 bit words need to have polarity, over-range and under-range multiplexed onto the Digit 5 word - as in the UART circuit. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

4

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converters," by Lee Evans
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A019 "4-1/2 Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort
A028 "Building an Auto-Ranging DMM Using the 8052A/7103A A/D Converter Pair," by Larry Goff
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family", by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

ICL7136

3½-Digit

Low Power A/D Converter

FEATURES

- First-reading recovery from overrange gives immediate "OHMS" measurement
- Guaranteed zero reading for 0V input
- True polarity at zero for precise null detection
- 1pA typical input current
- True differential input and reference
- Direct LCD display drive — no external components required
- Pin compatible with the ICL7106, ICL7126
- Low noise — 15μVp-p without hysteresis or overrange hangover
- On-chip clock and reference
- Low power dissipation, guaranteed less than 1mW — gives 8,000 hours typical 9V battery life
- No additional active circuits required
- Evaluation Kit available (ICL7136EV/Kit)

4

GENERAL DESCRIPTION

The Intersil ICL7136 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7136 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is under 100μA, ideally suited for 9V battery operation.

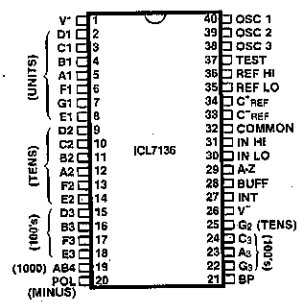
The 7136 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

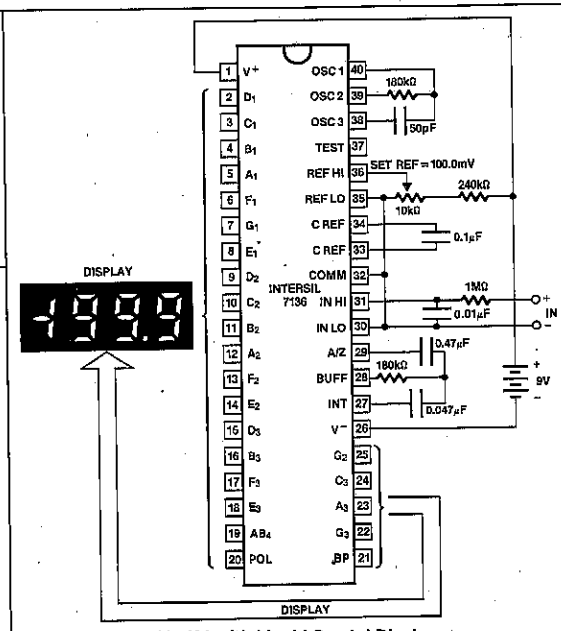
The ICL7136 is an improved version of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

ORDERING INFORMATION

PART	PACKAGE	TEMPERATURE RANGE	ORDER PART NUMBER
7136	40-pin CERDIP	0°C to +70°C	ICL7136CJL
7136	40-pin Ceramic DIP	0°C to +70°C	ICL7136CDL
7136	40-pin Plastic DIP	0°C to +70°C	ICL7136CPL
7136 Kit	Evaluation Kits		ICL7136EV/KIT

PIN CONFIGURATION (Outline dwgs. DL, JL PL)





ICL7136 with Liquid Crystal Display

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		70	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion.
Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).
Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

TEST CIRCUITS

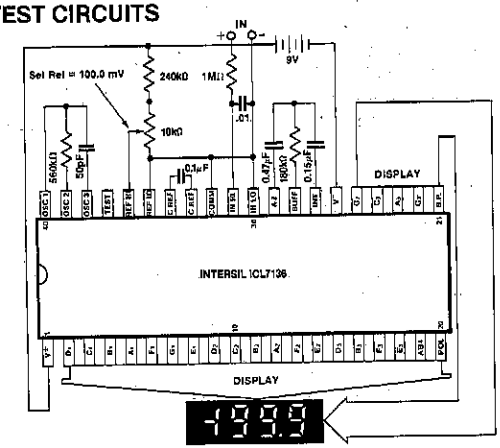


Figure 1. 7136 Clock Frequency 16kHz (1 reading/sec)

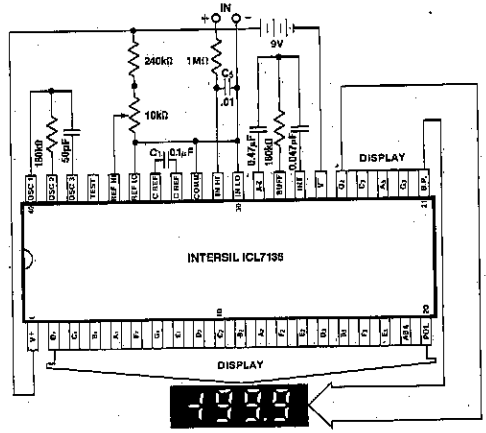


Figure 2. Clock Frequency 48kHz (3 readings/sec)

DETAILED DESCRIPTION—Analog Section

4

CONVERSION CYCLE

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

1. Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-Integrate Phase

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is 1000 (V_{IN}/V_{REF}).

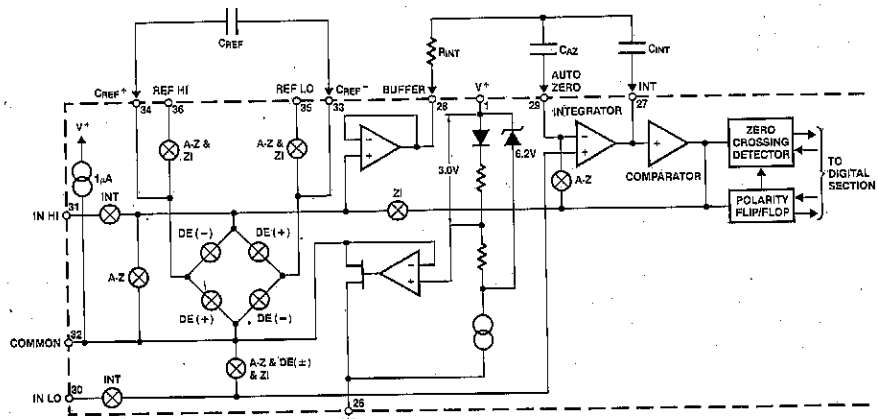


Figure 3. Analog Section of 7136

4. Zero Integrator Phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

DIFFERENTIAL INPUT

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

DIFFERENTIAL REFERENCE

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection).

ANALOG COMMON

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance (≃ 35Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 4.

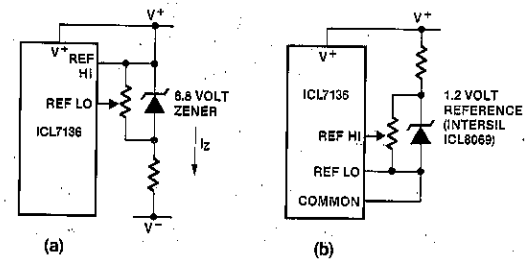


Figure 4. Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 100μA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus, it can be used as the negative supply for external segment drivers such as for decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

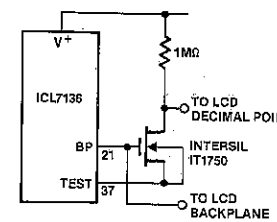


Figure 5. Simple Inverter for Fixed Decimal Point

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read −1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

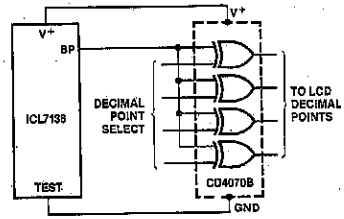


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

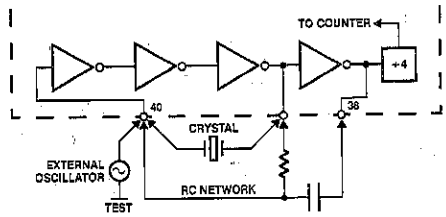


Figure 8. Clock Circuits

DETAILED DESCRIPTION—Digital Section

Figure 7 shows the digital section for the 7136. An internal digital ground is generated from a 6V Zener diode and a large P channel source follower. This supply is made stiff to absorb the relatively large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

SYSTEM TIMING

Figure 8 shows the clock oscillator provided in the 7136. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

DISPLAY FONT

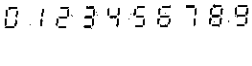


Figure 7. Digital Section

and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz). See also A052.

COMPONENT VALUE SELECTION (See also A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply −1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7126 or ICL7106 (see A032).

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7136 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

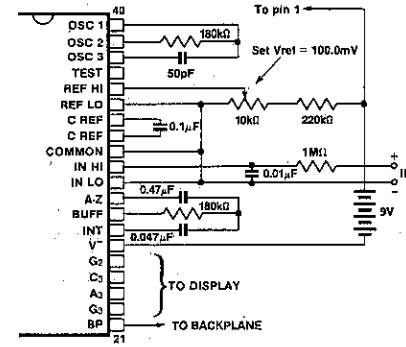


Figure 9. 7136 Using the Internal Reference. Values shown are for 200.0mV full-scale, 3 readings/sec, floating supply voltage (9V battery).

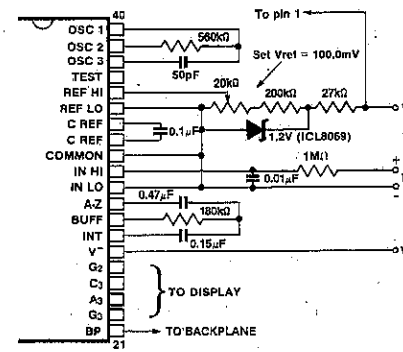


Figure 10. 7136 with an External Band-Gap Reference (1.2V Type). IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

TYPICAL APPLICATIONS (Continued)

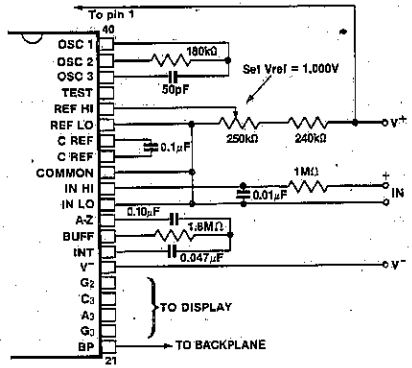


Figure 11. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 10.

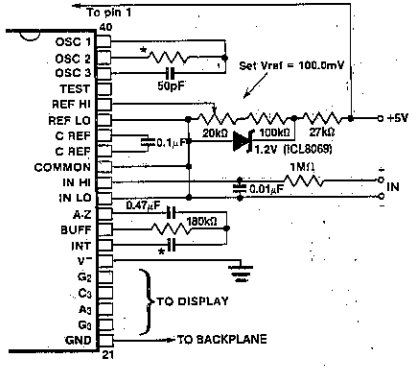


Figure 13. 7136 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

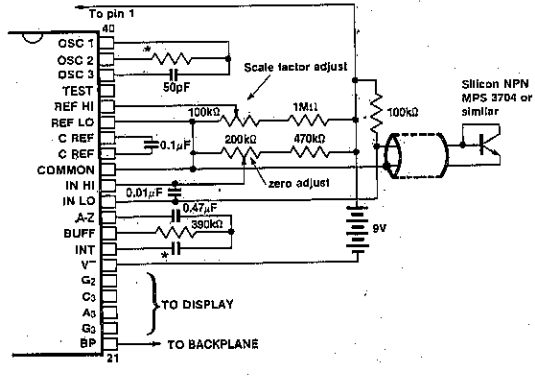


Figure 15. 7136 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See ICL8073/4 and AD590 data sheets for alternative circuits.

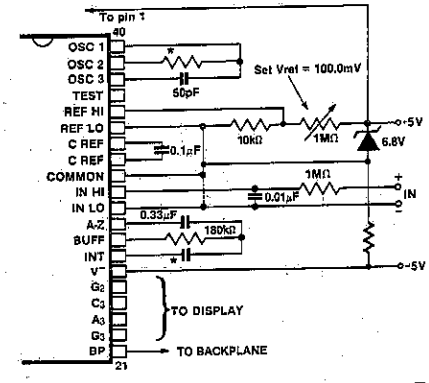


Figure 12. 7136 with Zener Diode Reference. Since low TC zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

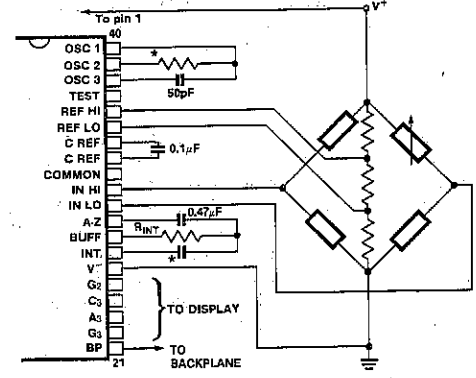


Figure 14. 7136 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

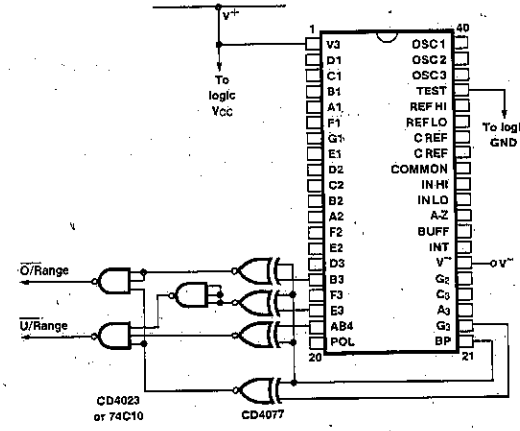


Figure 16. Circuit for Developing Underrange and Overrange Signals from 7136 Outputs.

*Values depend on clock frequency. See Figures 9, 10, 11.

TYPICAL APPLICATIONS (Continued)

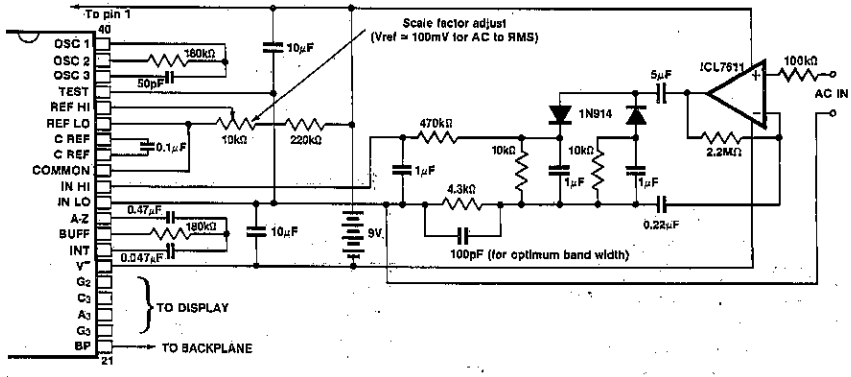


Figure 17. AC to DC Converter with 7136. Test is used as a common-mode reference level to ensure compatibility with most op amps.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort.

A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.

A047 "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

7136 EVALUATION KITS

After purchasing a sample of the 7136, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7136EV/Kit and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

4

ICL7137

3½-Digit Low Power A/D Converter

FEATURES

- First-reading recovery from overrange gives immediate "OHMS" measurement
- Guaranteed zero reading for 0V input
- True polarity at zero for precise null detection
- 1pA typical input current
- True differential input and reference
- Direct LED display drive — no external components required
- Pin compatible with the ICL7107
- Low noise — 15μVp-p without hysteresis or overrange hangover
- On-chip clock and reference
- Improved rejection of voltage on COMMON pin
- No additional active circuits required
- Evaluation Kit available (ICL7137EV/Kit)

4

GENERAL DESCRIPTION

The Intersil ICL7137 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7137 is designed to interface with a light emitting diode (LED) display. The supply current (exclusive of display) is under 200μA, ideally suited for battery operation.

The 7137 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of the ICL7137 allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

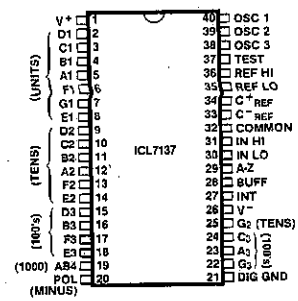
The ICL7137 is an improved version of the ICL7107, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications, changing only the passive component values.

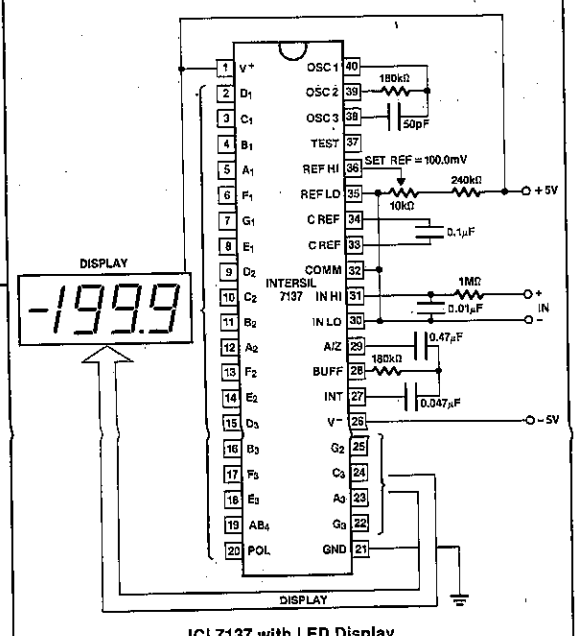
ORDERING INFORMATION*

PART	PACKAGE	TEMPERATURE RANGE	ORDER PART NUMBER
7137	40-pin CERDIP	0°C to +70°C	ICL7137CJL
7137	40-pin Ceramic DIP	0°C to +70°C	ICL7137CDL
7137*	40-pin Plastic DIP	0°C to +70°C	ICL7137CPL
7137 Kit	Evaluation Kit		ICL7137EV/KIT

*Plastic package device is available with reverse-bent leads. Order ICL7137RCPL.

PIN CONFIGURATION* (outline dwgs PL, JL, DL)





ICL7137 with LED Display

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} \simeq +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	$V_{CM} = \pm 1V$, V_{IN} = 0V Full-Scale = 200.0mV		30		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current)	V_{IN} = 0V (Note 5)		70	200	μA
V^- Supply Current			40		
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion.
Note 5: 48kHz oscillator, Figure 2, increases current by 35μA (typ).
Note 6: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

TEST CIRCUITS

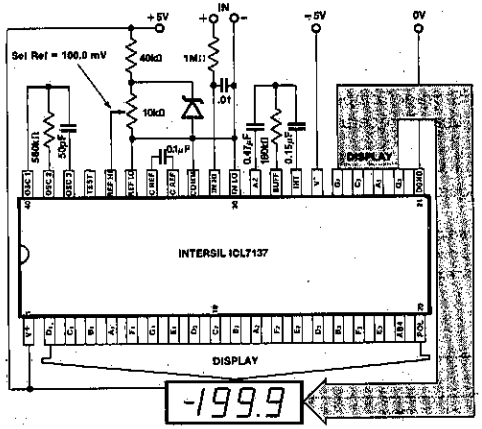


Figure 1. 7137 Clock Frequency 16kHz (1 reading/sec)

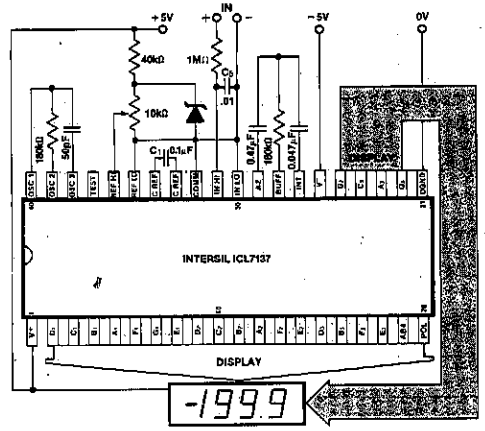


Figure 2. Clock Frequency 48kHz (3 readings/sec)

4

DETAILED DESCRIPTION—Analog Section

CONVERSION CYCLE

Figure 3 shows the Block Diagram of the Analog Section for the ICL7137. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

1. Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-Integrate Phase

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is 1000 (V_{IN}/V_{REF}).

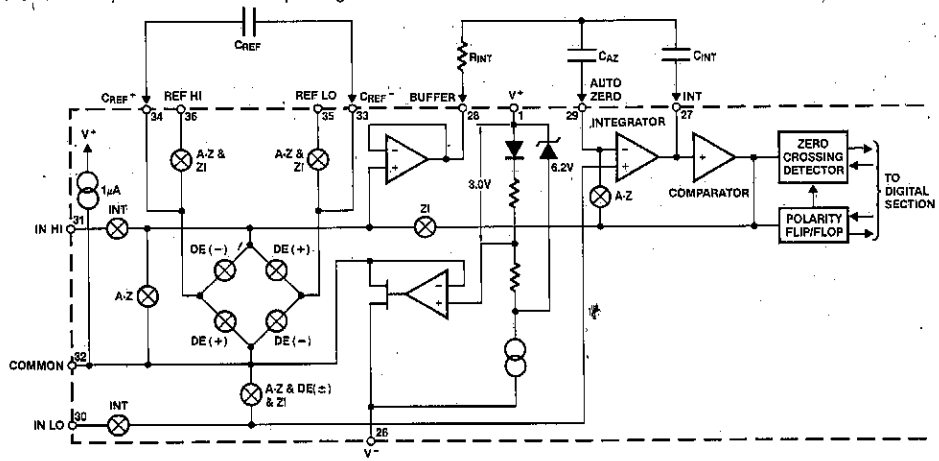


Figure 3. Analog Section of 7137

4. Zero Integrator Phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

DIFFERENTIAL INPUT

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 90dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

DIFFERENTIAL REFERENCE

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Value Selection).

ANALOG COMMON

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance (≃ 35Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 4.

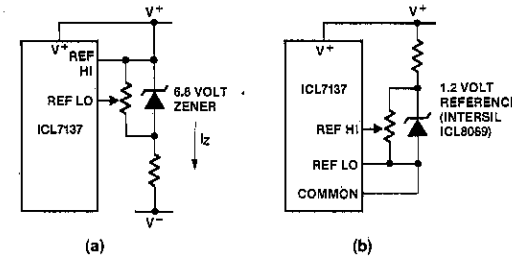


Figure 4. Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 100μA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

TEST

The TEST pin is coupled to the internal digital supply through a 500Ω resistor, and functions as a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read −1888. The TEST pin will sink about 10mA under these conditions.

DETAILED DESCRIPTION—Digital Section

Figure 5 shows the digital section for the 7137. The segments are driven at 8mA, suitable for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16 mA. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

Figure 6 shows a method of increasing the output drive current, using four DM7407 Hex Buffers. Each buffer is capable of sinking 40mA.

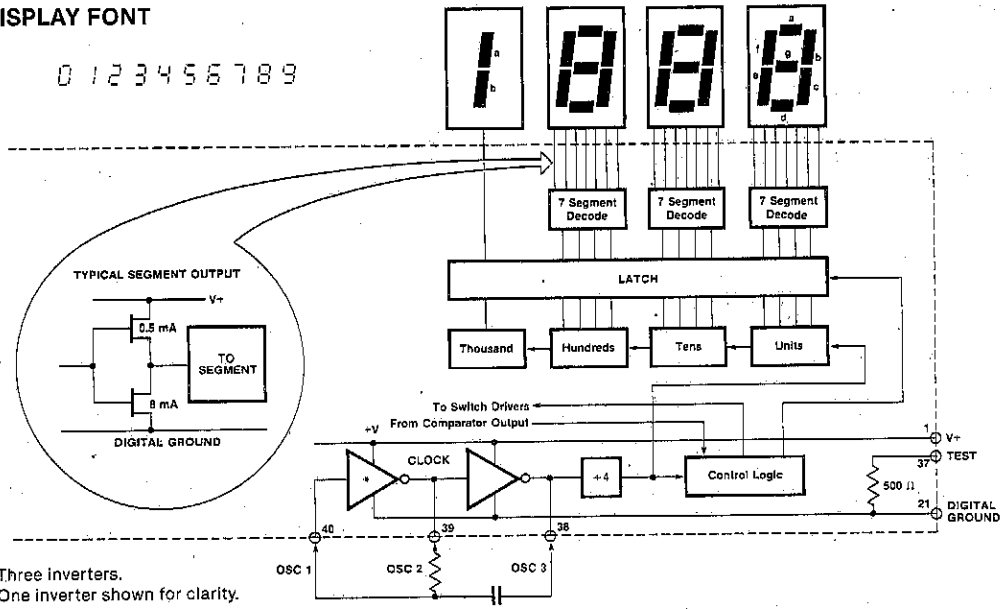
SYSTEM TIMING

Figure 7 shows the clock oscillator provided in the 7137. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

DISPLAY FONT

0 1 2 3 4 5 6 7 8 9



*Three inverters.
One inverter shown for clarity.

Figure 5. Digital Section

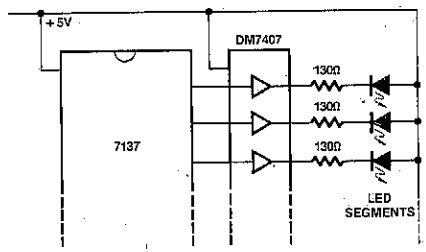


Figure 6. Display Buffering for Increased Drive Current

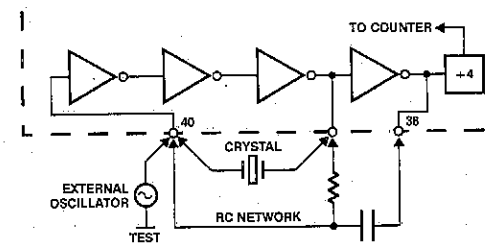


Figure 7. Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33⅓ kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz). See also A052.

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

COMPONENT VALUE SELECTION (See also A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7107 or ICL7117 (see A032).

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation f ~ 0.45/RC. For 48kHz clock (3 readings/second), R = 180kΩ, while for 16kHz (1 reading/sec), R = 560kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7137 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

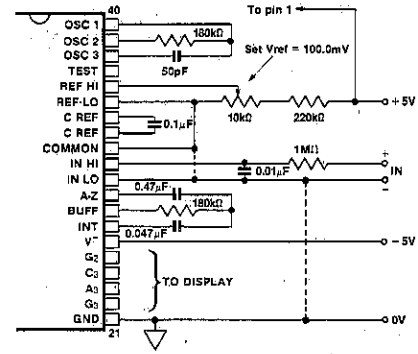


Figure 8. 7137 Using the Internal Reference. Values shown are for 200.0mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

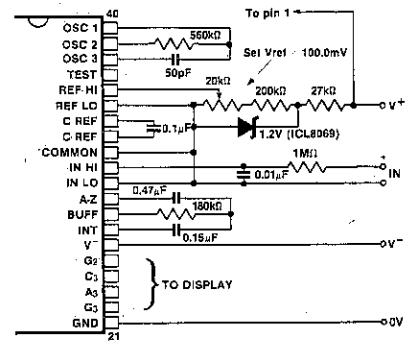


Figure 9. 7137 with an External Band-Gap Reference (1.2V Type). IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

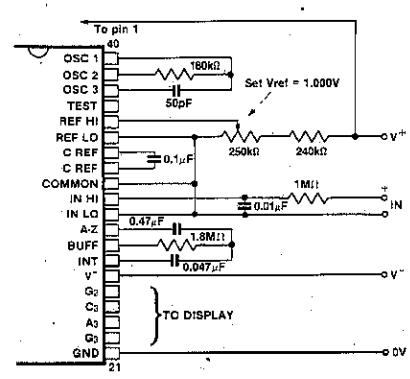


Figure 10. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 9.

TYPICAL APPLICATIONS (Continued)

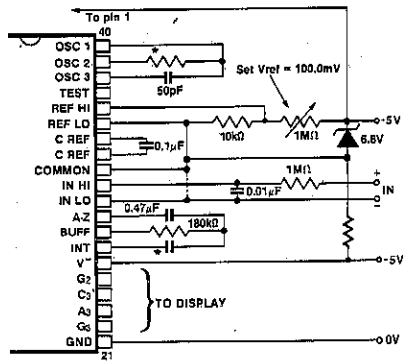


Figure 11. 7137 with Zener Diode Reference. Since low TC zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 9, IN LO may be tied to COMMON.

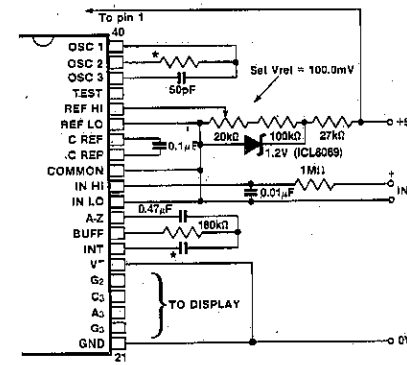


Figure 12. 7137 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

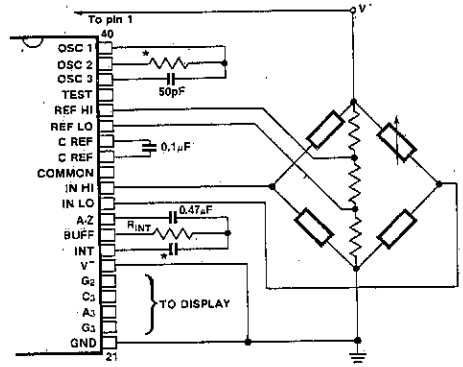


Figure 13. Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

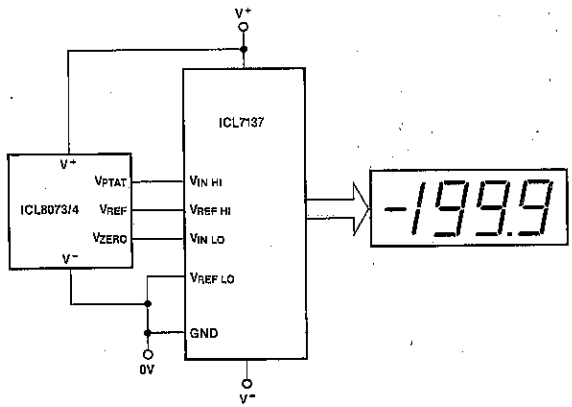


Figure 14. Basic Digital Thermometer. Both the ICL8073 (°C) and ICL8074 (°F) contain all necessary offset and reference (scale-factor) voltages to allow a direct-reading thermometer to be constructed without the need for external adjustments. Component values for 200mV full-scale should be used with the ICL8073, and (ideally) 170mV full-scale for the ICL8074.

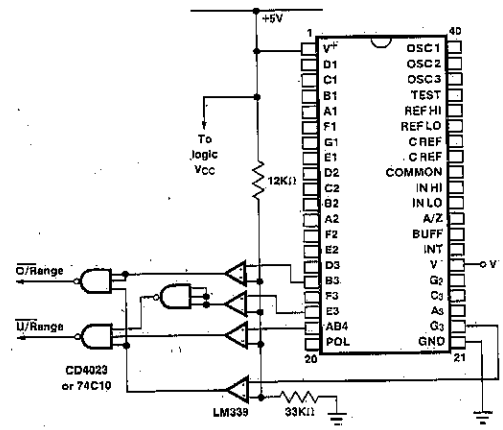


Figure 15. Circuit for developing Underrange and Overrange signals from outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

*Values depend on clock frequency. See Figures 8, 9 and 10.

TYPICAL APPLICATIONS (Continued)

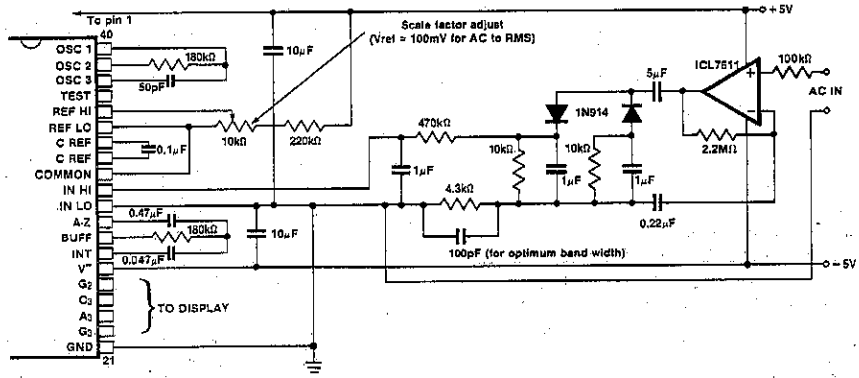


Figure 16. AC to DC Converter with 7137

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A019 "4½-Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort.

A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.

A047 "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

7137 EVALUATION KITS

After purchasing a sample of the 7137, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7137EV/Kit, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, LED display, passive components, and miscellaneous hardware.

4

ICL7145

16-Bit μP-Compatible Multiplying D/A Converter

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

- 16-bit resolution
- High linearity—0.003% FSR
- Microprocessor compatible with buffered inputs
- Bipolar application requires no external resistors
- Output current settling time 3μs max (1.0μs typ)
- Low linearity and gain temperature coefficients (1ppm/°C typ)
- Low power dissipation
- Full four-quadrant multiplication
- Full temperature range operation

4

GENERAL DESCRIPTION

The ICL7145 combines a four-quadrant multiplying DAC using thin film resistors and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve 0.003% linearity without laser trimming.

Microprocessor bus interfacing is eased by standard memory $\overline{WR}$ite cycle timing and control signal use. The input buffer register is loaded with the 16-bit input, and directly controls the output switches. The register is transparent if $\overline{WR}$ and $\overline{CS}$ are held low.

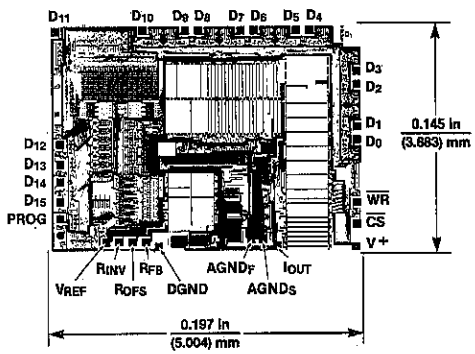
The ICL7145 is designed and programmed for bipolar operation. There is an offset resistor to the output with a reference input which should be connected to $-V_{REF}$, giving the DAC a true 2's complement input transfer function. Two extra resistors to facilitate the reference inversion are included on the chip, so that only an external op amp is needed.

ORDERING INFORMATION

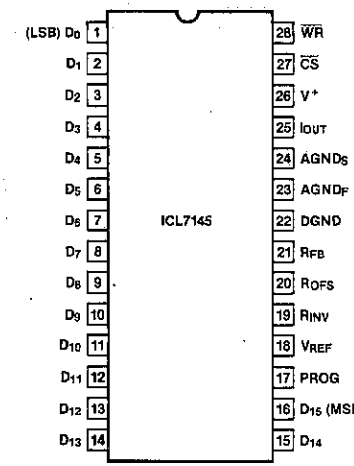
NON-LINEARITY	TEMPERATURE RANGE	
	0°C TO +70°C	−25°C TO +85°C
0.006%	ICL7145JCJI	ICL7145JIJI
0.003%	ICL7145KCJI	ICL7145KIJI

Package: 28-pin CERDIP only

CHIP TOPOGRAPHY



PIN CONFIGURATION (outline dwg JI)



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND ..... −0.3V to 7.5V
V_{REF}, R_{OFS}, R_{INV}, R_{FB} to DGND ..... ±25V
Current in $AGND_F$, $AGND_S$ 25mA
D_N, $\overline{WR}$, $\overline{CS}$, PROG, I_{OUT}, $AGND_F$, $AGND_S$ ..... −0.3V to V^+ +0.3V
Operating Temperature
ICL7145C ..... 0°C to +70°C
ICL7145I ..... −25°C to +85°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation (Note 2) 500mW
derate above 70°C @ 10mW/°C
Lead Temperature (soldering, 10 seconds) ..... 300°C

Note 1: All voltages with respect to DGND.
Note 2: Assumes all leads soldered or welded to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS $V^+ = +5V$, $V_{REF} = +5V$, $T_A = +25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Resolution			16			Bits
Non-Linearity J		(Notes 3 and 4)			0.006	% FSR
Non-Linearity K		(Notes 3 and 4)			0.003	% FSR
Differential Non-Linearity		(Notes 3 and 4)		0.003		% FSR
Non-Linearity Temperature Coefficient		Operating Temperature Range		1		ppm/°C
Gain Error J		(Notes 3 and 4)			0.04	% FSR
Gain Error K		(Notes 3 and 4)			0.02	% FSR
Gain Error Temperature Coefficient		Operating Temperature Range		1		ppm/°C
Zero Output Offset	V_{OZ}	$T_A = +25°C$			10	mV
Zero Output Offset	V_{OZ}	Operating Temperature Range		10		mV
Power Supply Rejection Ratio	PSRR	$T_A = +25°C$, $V^+ = 5V \pm 10\%$		1	20	ppm/V
Output Current Settling Time				1	3	µs
Reference Input Resistance	Z_{REF}	V_{REF}	3		6	kΩ
Output Capacitance	C_{OUT}	D_N = All 0s		110		pF
Output Capacitance	C_{OUT}	D_N = All 1s		260		pF
Output Noise		Equivalent Johnson Resistance		7		kΩ
Low State Input	V_{INl}	Operating Temperature Range			0.8	V
High State Input	V_{INh}	Operating Temperature Range	2.4			V
Logic Input Current	I_{LIN}	$0 \le V_{IN} \le V^+$	−1.0		1.0	µA
Logic Input Capacitance	C_{LIN}			15		pF
Supply Voltage Range	V^+	Functional Operation	4.5		5.5	V
Supply Current	I^+	Excluding Ladder		0.5	1.2	mA

Note 3: Full-Scale Range (FSR) is 10V (±5V).
Note 4: Using internal feedback and reference inverting resistors.

AC ELECTRICAL CHARACTERISTICS $V^+ = +5V$, $T_A = +25°C$, see Timing Diagram.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Chip Select-Write Set-Up Time	t_{CWs}				0	ns
Chip Select-Write Hold Time	t_{CWh}				0	ns
Write Pulse Width Low	$t_{\overline{WR}}$				200	ns
Data-Write Set-Up Time	t_{DWs}				200	ns
Data-Write Hold Time	t_{DWh}				0	ns

Timing Diagram

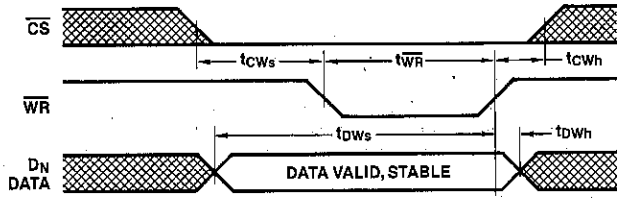


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Table 1. Pin Assignment and Function Description

PIN	NAME	DESCRIPTION	
1	D_0	Bit 0	Least Significant Bit
2	D_1	Bit 1	
3	D_2	Bit 2	
4	D_3	Bit 3	
5	D_4	Bit 4	
6	D_5	Bit 5	
7	D_6	Bit 6	
8	D_7	Bit 7	Input Data Bits (High = True)
9	D_8	Bit 8	
10	D_9	Bit 9	
11	D_{10}	Bit 10	
12	D_{11}	Bit 11	
13	D_{12}	Bit 12	
14	D_{13}	Bit 13	
15	D_{14}	Bit 14	
16	D_{15}	Bit 15	Most Significant Bit
17	PROG	Used for programming only. Tie to +5V for normal operation.	
18	V_{REF}	V_{REF} input to ladder.	
19	R_{INV}	Summing node for inverting amplifier.	
20	R_{OFS}	Bipolar offset resistor, to $-V_{REF}$.	
21	R_{FB}	Feedback resistor for voltage output applications.	
22	DGND	Digital GrouND return.	
23	$AGND_F$	Analog GrouND force line. Use to carry current from internal Analog GrouND connections. Tiedlinternally to $AGND_S$.	
24	$AGND_S$	Analog GrouND sense line. Reference point for external circuitry. Pin should carry minimal current. Tied internally to $AGND_F$.	
25	I_{OUT}	Current output pin.	
26	V^+	Positive supply voltage.	
27	$\overline{CS}$	Chip Select (active low). Enables writing to register.	
28	$\overline{WR}$	WRite (active low). Writes into register. Equivalent to $\overline{CS}$.	

DEFINITION OF TERMS

NON-LINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full-scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to full-scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

DETAILED DESCRIPTION

The ICL7145 consists of a 16-bit primary DAC, PROM controlled correction DACs, the input buffer registers, and the microprocessor interface logic. The 16-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistors in the ladder, results in excellent temperature stability.

The high linearity is achieved by programming a floating polysilicon gate PROM array which controls the correction DAC. The most significant bits of the DAC register address the PROM array, whose outputs control a 12-bit linearity correction DAC. Thus for every combination of the primary DAC's most significant bits a different C-DAC code is selected, allowing correction of superposition errors caused by bit interaction on the primary ladder's current bus and by voltage non-linearity in the feedback resistor. Superposition errors cannot be corrected by any method that corrects individual bits only, such as laser trimming. Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging, unlike wafer-level trimming methods. Since the thin film resistors do not suffer laser trimming stresses, no degradation of time-stability results.

Also controlled by the onboard PROM, the 6-bit G-DAC reduces gain error to less than 0.02% FSR by diverting to analog ground up to 2% of the current flowing in R_{FB}.

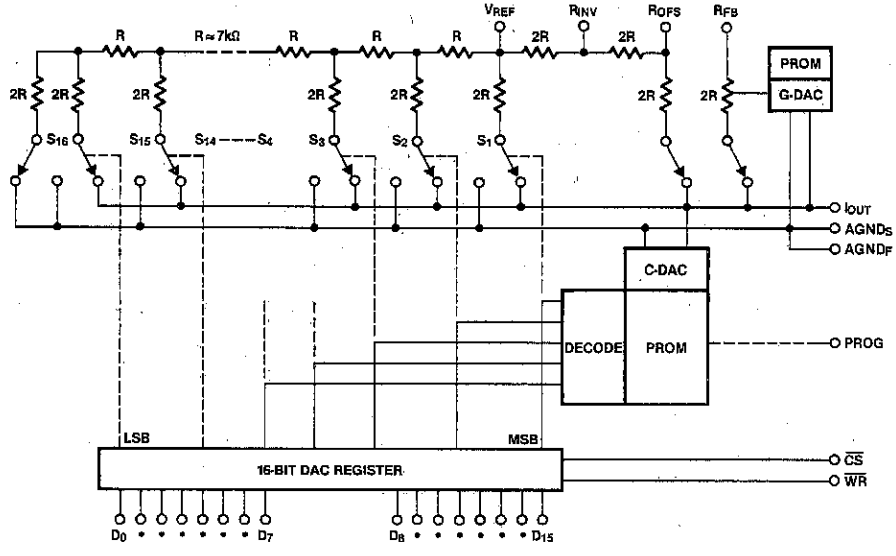


Figure 1. ICL7145 Functional Diagram

APPLICATIONS

Bipolar Operation

The circuit configuration for the normal bipolar mode operation of the ICL7145 is shown in Figure 2. The 2's complement input and positive and negative reference voltage values allow full four-quadrant multiplication. Amplifier A_3, together with the internal resistors R_{INV1} and R_{INV2}, forms a simple voltage inverter circuit to generate $-V_{REF}$ for the R_{OFS} offset input pin. This will give the nominal "digital input code/analog output value" relationship of Table 2.

Table 2. Code Table—Bipolar Operation

DIGITAL INPUT	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-1/2^{15})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2^{15})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$V_{REF}(1/2^{15})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	$V_{REF}(1-1/2^{15})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	V_{REF}

Amplifier A_1 is the output amplifier. An additional amplifier A_2 may be used to force $AGND_F$ if the ground reference point is established elsewhere than at the DAC, as in Figure 3.

A feedback compensation capacitor, C_F, improves the settling time by reducing ringing. This capacitor is normally in the 10pF-40pF range, depending on layout and the output amplifier selected. If C_F is too small, ringing or oscillation can occur when using an op amp with a high gain-bandwidth. If C_F is too large, the response of the output amplifier will be overdamped and will settle slowly. Figure 6 shows the effect of C_F.

The input circuits of some high speed op amps will sink large currents to their negative supply during power up and power down. The Schottky diode at I_{OUT} limits any negative going transients to less than −0.4V, avoiding the SCR latch-up which could result if significant current was injected into the parasitic diode between I_{OUT} and V^- of the ICL7145. This diode is not needed when using the ICL7650 ultra low V_{OS} op amp.

Offset Adjustment

1. Connect all data inputs and $\overline{WR}$ and $\overline{CS}$ to DGND.
2. Adjust the offset zero-adjust of the operational amplifier A_2, if used, for $< \pm 50\mu V$ at $AGND_S$.
3. Set data to 0000....000 (all low). Adjust the offset zero-adjust of output operational amplifier A_1 for $< \pm 50\mu V$ at I_{OUT}. V_{OUT} will be offset from 0V by the bipolar zero error of ±10mV.

The bipolar zero error may be trimmed out by adjusting the offset of A_3. The bipolar zero error can be as large as 10mV, but has a typical tempco of only $10\mu V/°C$.

Gain Adjustment

In many systems, gain adjustment will not be needed since the gain of the ICL7145 is accurate to within 0.02% FSR. When system gain must be adjusted, the low gain error limits the required adjustment range to only slightly more than the initial accuracy error of the reference. This is desirable since external gain trims degrade the gain temperature coefficient of a monolithic DAC. This degradation in the gain tempco comes about because, although the internal resistors track each other closely, they have a temperature coefficient of resistance of approximately −250ppm/°C.

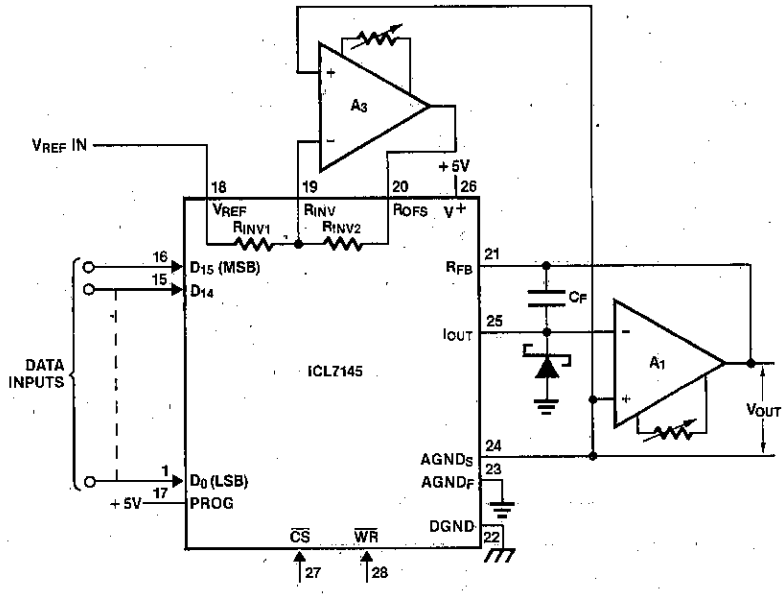


Figure 2. Bipolar Operation, Four-Quadrant

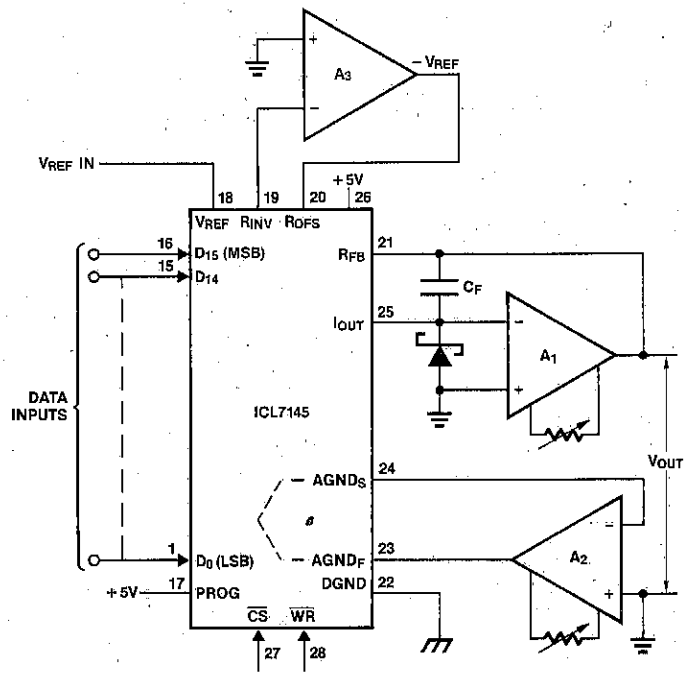


Figure 3. Operation with Forced Ground

To increase V_{OUT}, connect a series resistor of 200Ω or less between the A_1 output and the R_{FB} terminal (pin 21). To decrease V_{OUT}, connect a resistor of 100Ω or less between the reference voltage and the V_{REF} terminal (pin 18). These resistor values result in a minimum of 1% FSR gain trim and add about 3ppm/°C gain tempco. If only a small gain trim range is needed, the resistor values should be reduced in order to preserve the excellent 1ppm/°C gain tempco.

Digital Interface

The ICL7145 has a 16-bit latch onboard and can interface directly to a 16-bit data bus. Use external latches or peripheral ICs to interface to an 8-bit data bus, as shown in Figure 4. To ensure that the data is written into the onboard latch, the data must be valid 200ns before the rising edge of $\overline{WR}$. The onboard latch is transparent, meaning that if $\overline{WR}$ and $\overline{CS}$ are tied low, the input data is directly applied to the internal R-2R ladder switches. While this simplifies interfacing in non-microprocessor systems it may cause additional glitches in some microprocessor systems. These small glitches will occur if $\overline{WR}$ goes low before data is valid. Data must be valid at the time $\overline{WR}$ goes low to avoid these additional glitches.

All digital interfaces can suffer from capacitive coupling between the digital lines and the analog section. There are two general precautions that will reduce the capacitive coupling problem: 1) reduce stray capacitance between digital lines and analog lines; and 2) reduce the number of transitions on the digital inputs. Careful board layout and shielding can minimize the capacitive coupling (see Figure 5, PCB layout). The activity on the digital input lines can be reduced by using external latches or peripheral interface ICs between the microprocessor bus and the ICL7145. This will reduce the number of transitions on the digital data and control lines of the ICL7145, and thereby reduce the amount of digital noise coupled into the sensitive analog sections.

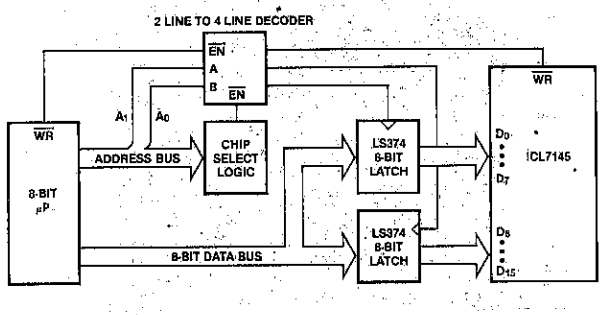
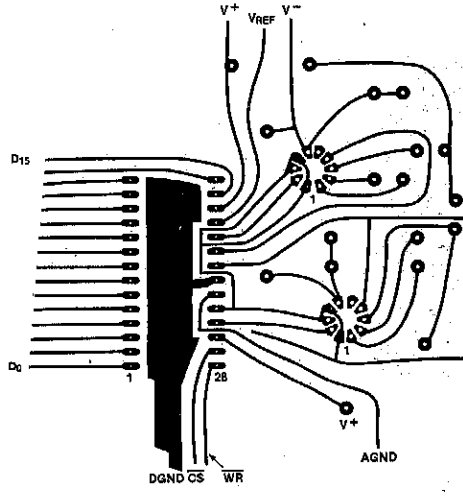


Figure 4. Interface to 8-Bit Microprocessor



Printed Circuit Side of Card (Single Sided Board)

Figure 5a. Printed Circuit Board Layout

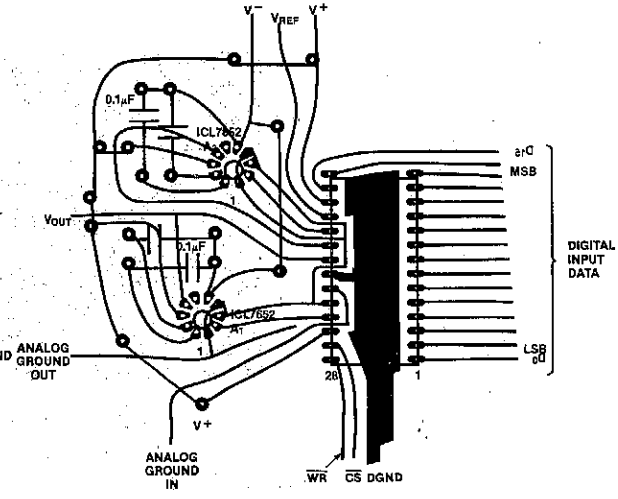


Figure 5b. Top Side with Component Placement

Operational Amplifier Selection

The input offset voltage, input current, gain, and bandwidth of the op amps used affect the circuit performance. Since the output impedance of I_{OUT} varies with the digital input code, A_1's input current will cause a code-dependent error at V_{OUT}, degrading the linearity. The input bias current should be significantly less than 1 LSB current, which is about 10nA. In a similar manner, any offset voltage in A_1 will also cause linearity errors. The offset voltage of the output amplifier should be significantly less than 1 LSB, which is 153μV.

The voltage output settling time is highly dependent on the slew rate and gain-bandwidth of A_1, so for high speed operation a high speed op amp such as the HA2600 is recommended. For applications where high speed is not required, the ICL7650 or ICL7652 can be used for A_1. Since the ICL7650/52 offset voltage is less than 5μV, no offset trimming is needed. To get a full 5V swing, ±7.5V supplies should be used for the ICL7650/52. Figures 6 and 7 show typical performance.

Amplifier A_3, which is used to generate the inverted reference, needs only to have a stable offset and to be able to drive a 3kΩ load. Since this is strictly a DC amplifier, the low noise ICL7652 is an ideal choice. Any variation in the offset voltage of A_3 will result in a drift in the bipolar zero, but will not affect the linearity of the ICL7145.

Amplifier A_2, used to generate a high quality ground, also needs a low offset and the ability to sink about 2mA.

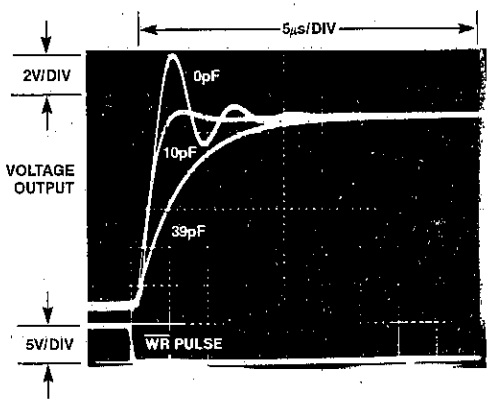
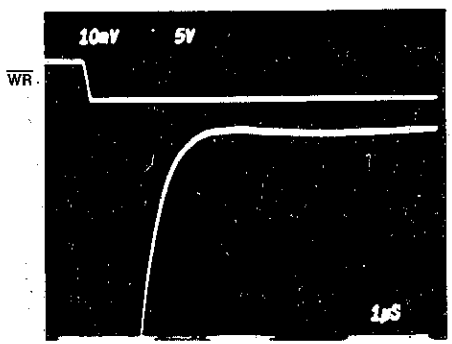


Figure 6. Voltage Output Settling with HA2525-5 Output Amplifier



Upper 50mV of a 10V Step

Figure 7. Voltage Output Settling with LF356 Output Amplifier

Ground Loops

Careful consideration must be given to ground loops in any high accuracy system. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, $AGND_S$ and $AGND_F$. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 8. Output signals should ideally be referenced to the sense pin $AGND_S$, as shown in the application circuits.

Multiplying Mode Performance

While the ICL7145 can perform full four-quadrant multiplication, full 0.003% linearity is guaranteed only at $V_{REF} = +5V$. This is because the voltage coefficient of resistance of the R-2R ladder and the feedback resistor are significant at the 14- or 16-bit level. This effect is most significant at higher voltages, and adds errors on the order of 0.01% for a ±10V full-scale. While the ICL7145 is tested and specified for $V_{REF} = +5V$, the R-2R ladder has the same voltage across it when $V_{REF} = -5V$. Therefore, voltage coefficients do not add any error with a $-5V$ V_{REF}.

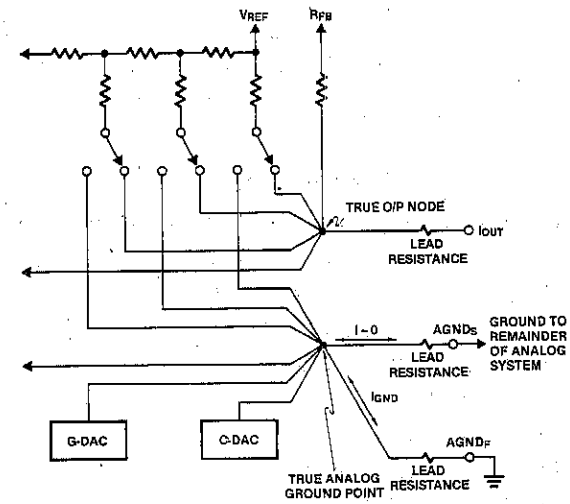


Figure 8. Eliminating Ground Loops

ICL7146 Complete 12-Bit Processor Compatible CMOS DAC

PRELIMINARY
Specifications Subject To Change Without Notice

FEATURES

- Low Impedance Voltage Output
- Double-Buffered Processor Interface
- Easy-To-Use Bipolar Offset
- Multiplying Capability
- On-Chip Trimmed Reference
- 7μSec Settling Time
- No External Gain or Offset Adjustment Required
- Low Power Dissipation 50mW
- No Critical External Components

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ORDERING INFORMATION

Part Number	Linearity	Temperature Range	Package
ICL7146LCJI	0.01%	0 to +70°C	CERDIP
ICL7146LIJI		−40°C to +85°C	
ICL7146KCJI	0.02%	0 to +70°C	
ICL7146KIJI		−40°C to +85°C	
ICL7146JCJI	0.05%	0 to +70°C	
ICL7146JIJI		−40°C to +85°C	

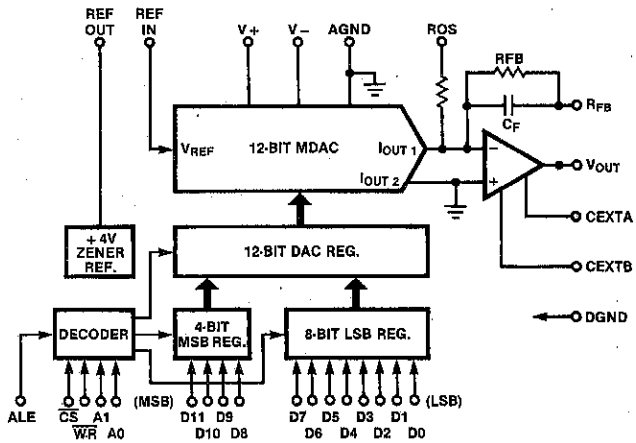
GENERAL DESCRIPTION

The ICL7146 is the first of a series of complete 12-Bit CMOS DAC's. These DAC's feature all of the needed support circuitry to interface to processors and give a voltage output. Contained on the chip are two levels of latches for double buffers, a trimmed reference, a latch controller, and an output buffer amplifier. All devices are accurately trimmed for both gain and offset so that no external trimming is required.

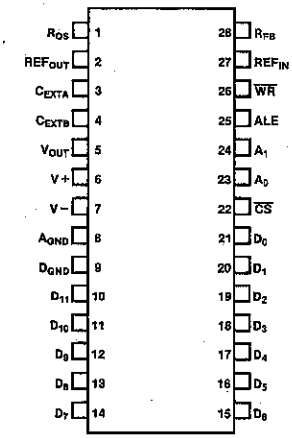
CMOS circuitry is used to keep the power dissipation low, and with all devices contained on a single chip, significant board size reductions are possible. As an alternative to this, many more analog channels could be added to a board and still decrease power consumption. Intersil's patented autostabilized op amp construction eliminates drifts in the zero offset and provides a fast (7 μsec) settling time.

Processor interface is double-buffered with all 12-bits being brought out. The first level of latches is divided into 4 and 8 bit bytes with a 12 bit wide second buffer. Data can be directly entered into any of the three buffers or the buffers can be operated separately.

BLOCK DIAGRAM



PIN CONFIGURATION



Absolute Maximum Ratings (Note 1)

REF_{IN}, R_{FB}, R_{OS} ..... ±25V
V^+ 6.2V
V^- ..... −9.0V
REF_{OUT}, V_{OUT}, C_{EXT},
A_{GND} ..... V^- − 0.3V to V^+ + 0.3V
Digital Inputs ..... V^+ + 0.3V to D_{GND} − 0.3V
Storage Temperature Range..... −65°C to +150°C

Streses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: All Voltages with Respect to D_{GND}

Operating Characteristics

$V+ = 5V$, $V- = -5V$, $V_{ref} = 4.00V$, $T_A = 25°C$, $R_L = 20K$, $C_L = 50pF$

Parameter	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
Resolution			12			Bits
Non Linearity J K L					.05 .02 .01	% FSR % FSR % FSR
Differential Linearity J K L		 Guaranteed Monotonic		 ±3/4 ±1/2 ±1/2	 ±2 ±1 ±1	LSB
Gain Error				0.1	0.2	% FSR
Unipolar Zero Error				60	120	μV
Bipolar Zero Code Error		R_{FB} Connected to V_{OUT} R_{OS} Connected to $-V_{REF}$		0.025	0.05	% FSR
Positive Power Supply Rejection Ratio		$V+ = 4.5$ to 5.5V External Reference		±0.001	0.005	% FSR/ % V+
Negative Power Supply Rejection Ratio		$V- = -4.5$ to −5.5V External Reference		0	±0.001	% FSR/ % V+
Voltage Setting Time (Note 1)		To 1/2 LSB		7	10	μs
Feedthrough Error		V_{REF} = 8V P-P, 10 KHz Sine Wave			1	mV P-P
Reference Input Resistance		−55°C to 125°C	5	10	20	KΩ
Internal Reference Voltage			−4.04	−4.00	−3.96	V
Internal Reference Tempco				25	50	PPM of FSR per °C
Positive Supply Voltage Range	V+	Functional Operation, Internal or External Reference	4.5	5.0	5.5	V
Negative Supply Voltage Range	V−	Functional Operation, External Reference	−4.5	−5.0	−7.5	V
		Functional Operation, Internal Reference	−4.75	−5.0	−7.5	V
Output Voltage Range		R_{FB} connected to V_{OUT}		±4		V
Output Drive Current			±2			mA

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Operating Characteristics (continued)

$V+ = 5V, V- = -5V, V_{ref} = 4.00V, T_A = 25°C, R_L = 20K, C_L = 50pF$

Parameter	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
Output Amp Bandwidth				2		MHz
Slew Rate				2.5		V/μs
Output Impedance		@D.C.		.02		Ω
Reference Input Range (Note 2)		For design use. Linearity Guar. @4.0V	±2.0		±10	V
Logic Low	V_{INL}				0.8	V
Logic High	V_{INH}		2.4			V
Logic Input Current					1	μA
Logic Input Capacitance (Note 1)					8	pF
Positive Supply Current		Inputs = 0V or 5V		4.0	5.0	mA
Negative Supply Current				4.0	5.0	mA
Power Dissipation		Input Code = 5.0V V+ = 5.0V, V− = −5.0V			50	mW
Gain Error Tempco		Internal Ref External Ref		±30 −12		PPM of FSR °C
DIGITAL SWITCHING CHARACTERISTICS						
Address $\overline{WR}$ Set-up Time	TAWS		100			nS
Address $\overline{WR}$ Hold Time	TAWH		0			nS
$\overline{CS}$ $\overline{WR}$ Set-up Time	TCWS		0			nS
$\overline{CS}$ $\overline{WR}$ Hold Time	TCWH		0			nS
Write Pulse Width	TWR		200			nS
Data Set-up Time	TDS		200			nS
Data Hold Time	TDH		0			nS
ALE Pulse Width	TLL		200			nS
Address-ALE Set-up Time	TAL		60			nS
Address-ALE Hold Time	TLA		40			nS
$\overline{CS}$-ALE Set-up Time	TCL		30			nS
$\overline{CS}$-ALE Hold Time	TLC		50			nS
$\overline{WR}$ Trailing Edge to ALE	TWL		0			nS

NOTE 1: Guaranteed by design, not 100% tested in production.
NOTE 2: External Op Amp Required for $V_{out} > \pm 4.0V$

DETAILED DESCRIPTION

The ICL7146 is a monolithic 12-bit processor compatible CMOS DAC. It is a complete DAC containing a DAC, a group of latches, a reference, digital control circuitry and an op amp.

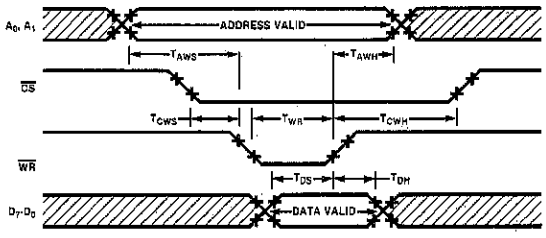
A wide range of applications can be implemented with the ICL7146 laser trimmed 12-bit multiplying DAC. CMOS switches and low tempco thin film resistors provide a stable output current proportional to the input digital code. Two matched and trimmed resistors are provided at the output for current to voltage conversion and for offset generation in bipolar operation.

An on-chip precision auto-stabilized operational amplifier is provided for current to voltage conver-

TIMING DIAGRAMS AND TRUTH TABLES

Non-Multiplexed Bus

TIMING DIAGRAM



TIMING FOR NON-MULTIPLEXED ADDRESS BUS

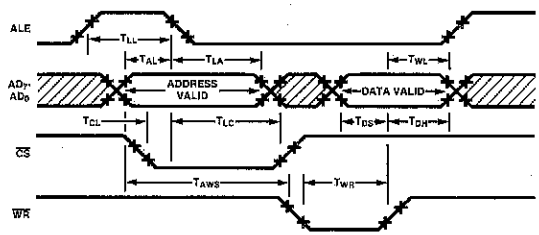
TRUTH TABLE (ALE tied to V+)

CONTROL INPUTS				OPERATION
A1	A0	$\overline{CS}$	$\overline{WR}$	
X X	X X	X 1	1 X	No Operation Device Not Selected
0	0	0	0	Load All Registers From Data Bus
0	1	0	0	Load LSB Register From Data Bus*
1	0	0	0	Load MSB Register From Data Bus*
1	1	0	0	Load DAC Register From LSB & MSB Register

*Data is latched on low to high transition of $\overline{WR}$ or $\overline{CS}$.

Multiplexed Bus

TIMING DIAGRAM



TIMING FOR MULTIPLEXED ADDRESS BUS

TRUTH TABLE (ALE is latch control input; $\overline{CS}$, A0 & A1 are latched outputs)

CONTROL INPUTS				OPERATION
A1	A0	$\overline{CS}$	$\overline{WR}$	
X X	X X	X 1	1 X	No Operation Device Not Selected
0	0	0	0	Load All Registers From Data Bus
0	1	0	0	Load LSB Register From Data Bus
1	0	0	0	Load MSB Register From Data Bus
1	1	0	0	Load DAC Register From LSB & MSB Register

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sion. The auto zeroing technique utilized guarantees extremely low offset and low gain drift over temperature. Two inexpensive capacitors are required for the internal auto zero circuitry. Th op amp has been left open loop for flexibility. The loop can be closed by connecting R_{OS} and R_{fb} to V_{OUT} for full scale voltages less than ±4 volts. An external amplifier can be closed in the loop for applications requiring larger output swing or current. An inexpensive buffer amplifier with no special input characteristics can be used without any system degradation. No external offset trimming is required due to the auto zeroing circuitry.

A zener reference that can be trimmed for both output voltage and temperature drift is provided. This reference is capable of driving an extra load of 200μA above the current required for the DAC ladder. This allows the reference to be used for other devices in the system when required.

Latches on the chip are set up in two levels, the first level connects to the data bus and is internally arranged as three groups of four latches each. The decoding circuitry is designed so that the user may address either the lower eight bits or the upper four bits. This allows the user to hard wire the 4 MSB's directly to the 4LSB's for easy interface to eight bit processors. Or the DAC can be wired directly to a 12 bit or larger data bus. Following the two input latches is another latch that is 12 bits wide. This makes the ICL7146 double-buffered. By double buffering the input of the DAC it is possible to interface the DAC to an eight bit data bus and prevent the DAC from having a major output glitch as the digital code changes. With a single level of latches, say a 4 bit latch and an 8 bit latch connected to an 8 bit data bus the following would occur if an attempt was made to generate a ramp. As the input code was incremented from 000_{HEX} to OFF_{HEX} an even stair case output would occur. But to change the code to 100_{HEX} the processor would either have to change to code to 000 and then to 100, or first to 1FF and then to 100. In the first case the output would go to zero for a full processor cycle. And in the second case it would double

its output value. Neither of these conditions are acceptable in a wide variety of applications. Hence the need for double buffering.

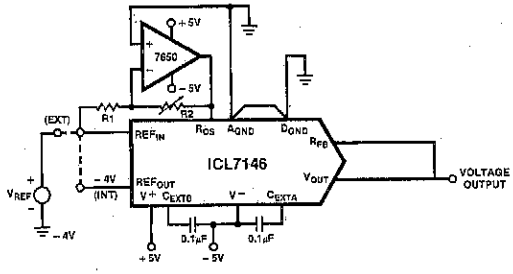
Buffer control is handled by a decoder to ease processor interface requirements. Operation of the decoder is shown in the truth table.

TYPICAL APPLICATIONS
Bipolar Output

Offset Binary Code Table

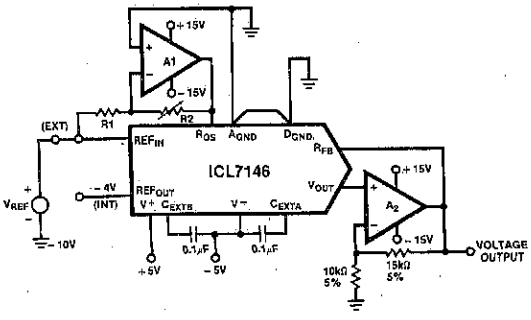
Binary Number In DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

±4V BIPOLAR OUTPUT:



NOTE 1: A1 should be selected or trimmed for low offset voltage; R1 & R2 are 10KΩ resistors trimmed to a matching of 0.1% or better.

±10V BIPOLAR OUTPUT:



NOTE 1: A1 should be selected or trimmed for low offset voltage; R1 & R2 are 10KΩ resistors trimmed to a matching of 0.1% or better.

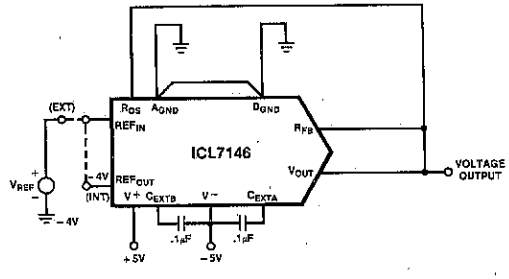
NOTE 2: A2 needs not to have a low offset voltage but it must be fast (>8MHz) to insure stability.

TYPICAL APPLICATIONS
Unipolar Output

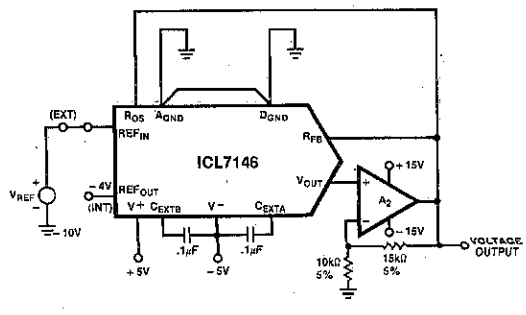
Code Table

Binary Number In DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0001	0V

+4V UNIPOLAR OUTPUT:

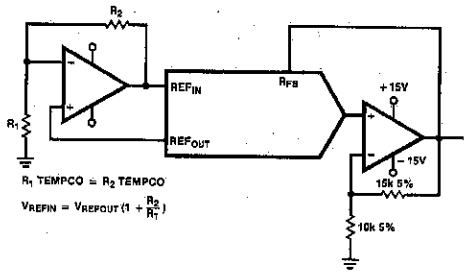


+10V UNIPOLAR OUTPUT:



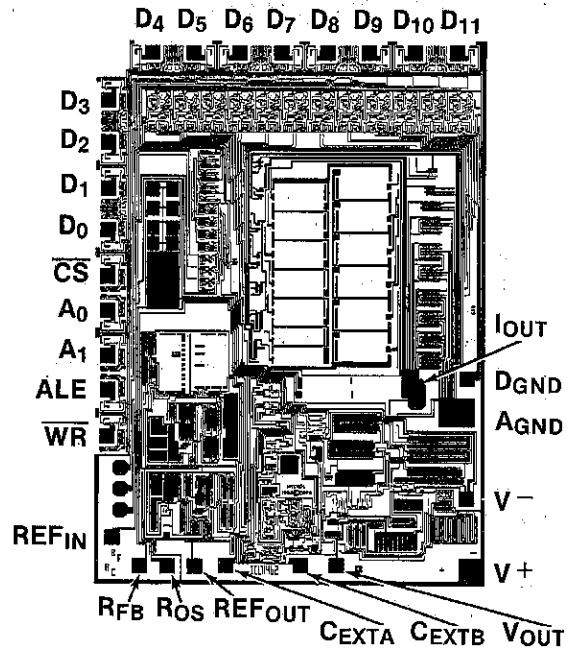
NOTE 1: A2 needs not to have a low offset voltage but it must be fast (>8MHz) to insure stability.

TYPICAL APPLICATIONS (Continued)



USING INTERNAL REF FOR V_{REF} >4V

CHIP TOPOGRAPHY



4

AD7520/7530
AD7521/7531
10 & 12 Bit Monolithic Multiplying D/A Converters

FEATURES

- **AD7520/AD7530: 10 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **AD7521/AD7531: 12 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **Low Power Dissipation: 20 mW (Max)**
- **Low Nonlinearity Tempco: 2 PPM of FSR/° C (Max)**
- **Current Settling Time: 500 ns to 0.05% of FSR**
- **Supply Voltage Range: +5V to +15V**
- **DTL/TTL/CMOS Compatible**
- **Full Input Static Protection**
- **883B Processed Versions Available**

GENERAL DESCRIPTION

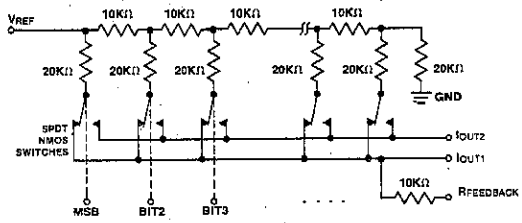
The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). INTERSIL thin-film on CMOS processing gives up to 10-bit accuracy with DTL/TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

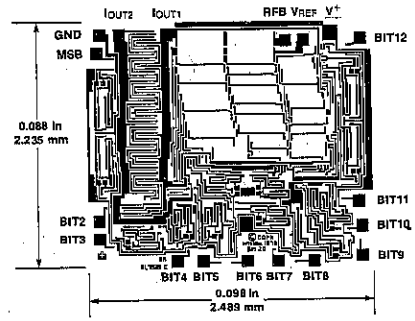
4

FUNCTIONAL DIAGRAM



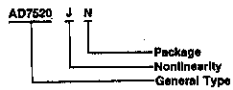
(Switches shown for Digital Inputs "High")
(Resistor values are nominal)

CHIP TOPOGRAPHY

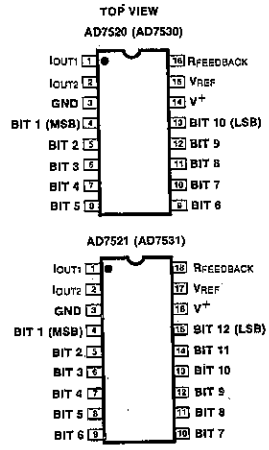


PACKAGE IDENTIFICATION

Suffix D: Cerdip package
Suffix N: Plastic DIP package



PIN CONFIGURATION (Outline dwgs DE, PE)



ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	−25°C to +85°C	−55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7530JN AD7521JN AD7531JN	AD7520JD AD7530JD AD7521JD AD7531JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KN	AD7520KD AD7530KD AD7521KD AD7531KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	AD7520LD AD7530LD AD7521LD AD7531LD	AD7520UD AD7521UD

ABSOLUTE MAXIMUM RATINGS (T_A = 25° C unless otherwise noted)

V^+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −100mV to V^+
Power Dissipation (package)
up to +75° C ..... 450 mW
derate above +75° C @ ..... 6 mW/° C

Operating Temperatures
JN, KN, LN Versions ..... 0° C to +70° C
JD, KD, LD Versions ..... −25° C to 85° C
SD, TD, UD Versions ..... −55° C to +125° C
Storage Temperature ..... −65° C to +150° C

CAUTION: 1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{fb}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, TA = 25 °C unless otherwise specified)

PARAMETER		AD7520 (AD7530)	AD7521 (AD7531)	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1) Resolution		10	12	Bits			
Nonlinearity	J S	0.2 (8-Bit)		% of FSR	Max	S, T, U: over −55° C to =125° C	1
	K T	0.1 (9-Bit)		% of FSR	Max		1
	L U	0.05 (10-Bit)		% of FSR	Max	$-10V \le V_{REF} \le +10V$	1
Nonlinearity Tempco		2		PPM of FSR/° C	Max	$-10V \le V_{REF} \le +10V$	
Gain Error (Note 2)		0.3		% of FSR	Typ		
Gain Error Tempco (Note 2)		10		PPM of FSR/° C	Max		
Output Leakage Current (either output)		200 (300)		nA	Max	Over the specified temperature range	
Power Supply Rejection		±0.005		% of FSR/%	Typ		2
AC ACCURACY Output Current Settling Time		500		nS	Typ	To 0.05% of FSR (All digital inputs low to high and high to low)	6
Feedthrough Error		10		mV pp	Max	V_{REF} = 20V pp, 100kHz (50kHz) All digital inputs low	5
REFERENCE INPUT Input Resistance (Note 3)		5k 10k 20k		Ω	Min Typ Max	All digital inputs high. I_{OUT1} at ground.	
ANALOG OUTPUT Voltage Compliance (both outputs)		See absolute max. ratings					
Output Capacitance		I_{OUT1} 120 I_{OUT2} 37		pF pF	Typ Typ	All digital inputs high	4
		I_{OUT1} 37 I_{OUT2} 120		pF pF	Typ Typ	All digital inputs low	4
Output Noise (both outputs)		Equivalent to 10kΩ Johnson noise			Typ		3
DIGITAL INPUTS Low State Threshold		0.8		V	Max	Over the specified temp range	
High State Threshold		2.4		V	Min		
Input Current (low to high state)		1		μA	Typ		
Input Coding		Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5	
POWER REQUIREMENTS Power Supply Voltage Range		+5 to +15		V			
I^+		5		nA	Typ	All digital inputs at GND	
		2		mA	Max	All digital inputs high or low	
Total Power Dissipation (including the ladder)		20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Ladder and feedback resistor Tempco is approximately −150ppm/° C.

TEST CIRCUITS

NOTE: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7530, AD7521 and AD7531.

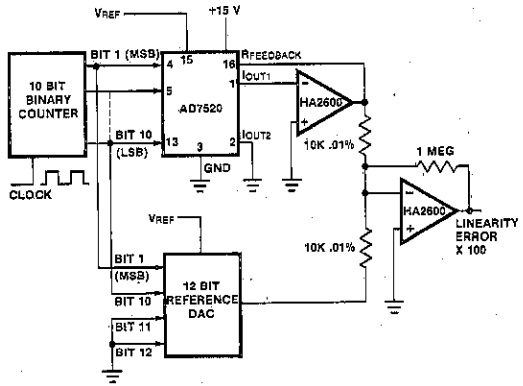


Figure 1. Nonlinearity

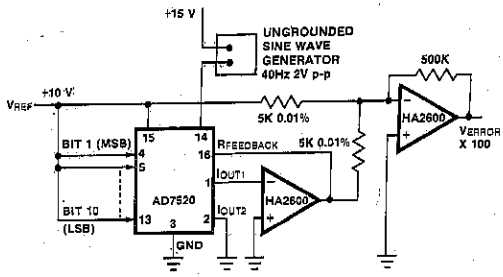


Figure 2. Power Supply Rejection

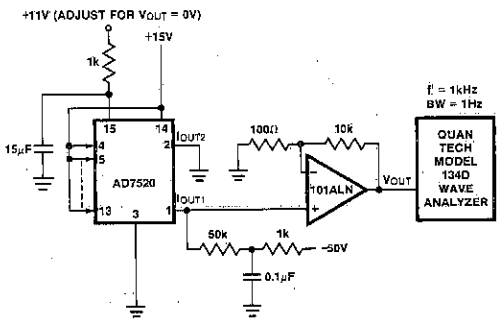


Figure 3. Noise

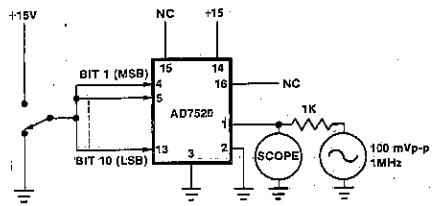


Figure 4. Output Capacitance

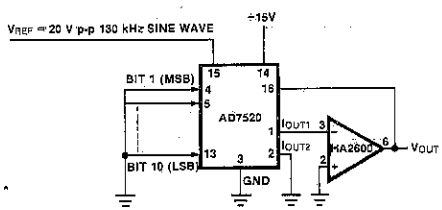


Figure 5. Feedthrough Error

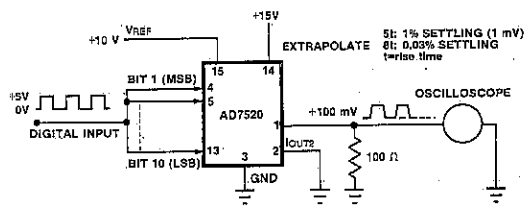


Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

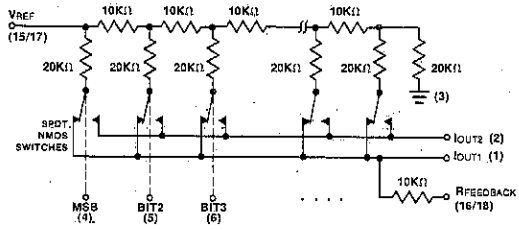
OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7530) and AD7521 (AD7531) are monolithic, multiplying D/A converters. Highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} busses which must be held either at ground or virtual ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 7. 7520/7521 Functional Diagram

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

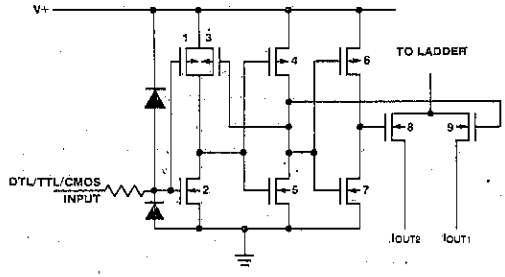


Figure 8. CMOS Switch

APPLICATIONS

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7520 (AD7530) and AD7521 (AD7531) in unipolar mode is shown in Figure 9. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

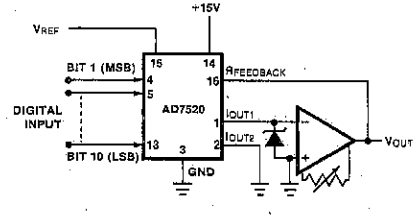


Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1 mV at V_{OUT}.

Gain Adjustment

1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}(1-2^{-n})$ reading. (n = 10 for AD7520 (AD7530) and n = 12 for AD7521 (AD7531)).
3. To decrease V_{OUT}, connect a series resistor (0 to 500 ohms) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT}, connect a series resistor (0 to 500) ohms) in the I_{OUT_1} amplifier feedback loop.

TABLE 1

CODE TABLE — UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-n})$
1000000001	$-V_{REF}(1/2+2^{-n})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}(1/2-2^{-n})$
0000000001	$-V_{REF}(2^{-n})$
0000000000	0

NOTE: 1. LSB = 2^{-n} V_{REF} 2. n = 10 for 7520, 7530; n = 12 for 7521, 7531

(APPLICATIONS, Cont'd.)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7520 (AD7530) or AD7521 (AD7531) in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

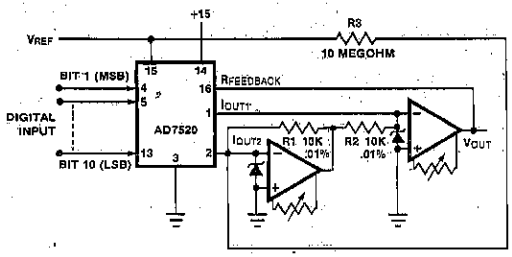


Figure 10. Bipolar Operation
(4-Quadant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 Megohm), from V_{REF} to I_{OUT2}.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset zero adjust trimpot for 0V ±1 mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V*.
2. Monitor V_{OUT} for a $-V_{REF}(1-2^{-(n-1)})$ volts reading. (n = 10 for AD7520 and AD7530, and n = 12 for AD7521 and AD7531).
3. To increase V_{OUT}, connect a series resistor of up to 500Ω between V_{OUT} and R_{fb}.
4. To decrease V_{OUT}, connect a series resistor of up to 500Ω between the reference voltage and the V_{REF} terminal.

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-(n-1)})$
1000000001	$-V_{REF}(2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF}(2^{-(n-1)})$
0000000001	$V_{REF}(1-2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. LSB = $2^{-(n-1)}$ V_{REF} 2. n = 10 for 7520 and 7521; n = 12 for 7530 and 7531

POWER DAC DESIGN USING AD7520

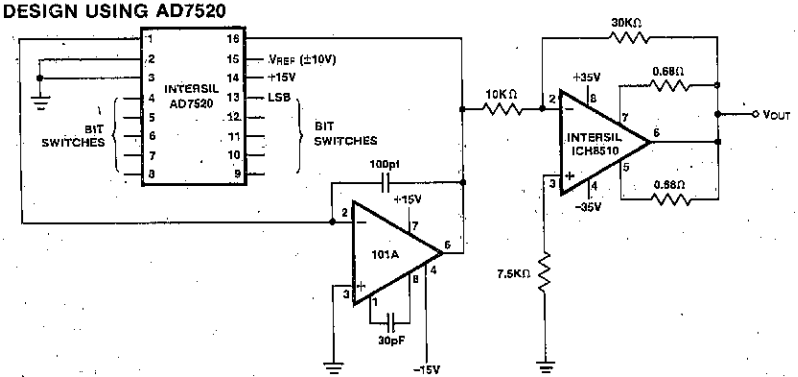


Figure 11. The Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 11. An INTERSIL IH8510 power amplifier (1 Amp continuous output at up to ±25 V) is driven by the AD7520.

A summing amplifier between the AD7520 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7520 can be directly connected to the IH8510, by using a 25 V reference for the DAC.

An important note on the AD7520/101A interface concerns the connection of pin 1 of the DAC and pin 2 of the 101A. Since this point is the summing junction of an amplifier with an AC gain of 50,000 or better, stray capacitance should be minimized; otherwise instabilities and poor noise performance will result. Note that the output of the 101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration. (For more information see: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

(APPLICATIONS, Cont'd.)

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 12, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).

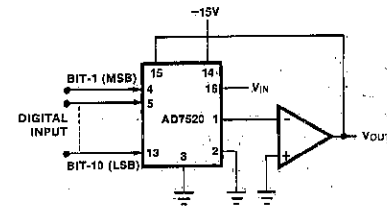


Figure 12. Analog/Digital Divider

For further information on the use of this device, see the following Application Bulletins:

A016 "Selecting A/D Converters," by David Fullagar
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A020 "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger
A021 "Power D/A Converters Using the IH8510," by Dick Wilenken
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al., Electronics, Dec. 9, 1976

4

AD7523
8 Bit Monolithic Multiplying D/A Converters

FEATURES

- 8, 9 and 10 bit linearity
- Low gain and linearity Tempcos
- Full temperature range operation
- Full input static protection
- DTL/TTL/CMOS compatible
- +5 to +15 volts supply range
- Fast settling time: 100 nS
- Four quadrant multiplication
- 883B Processed versions available

GENERAL DESCRIPTION

The Intersil AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

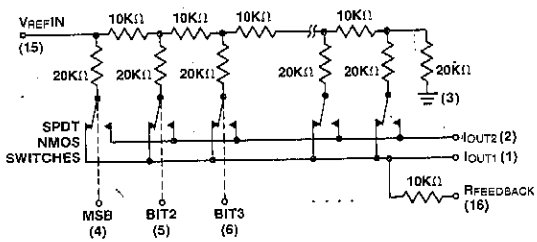
Intersil's thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with DTL/TTL/CMOS compatible operation.

Intersil AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND and very low power dissipation make it a very versatile converter.

Low noise audio gain control, motor speed control, digitally controlled gain and attenuators are a few of the wide number of applications of the 7523.

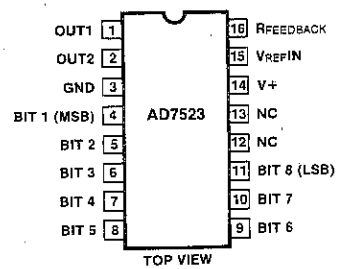
4

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION



TOP VIEW

OUTLINE DRAWINGS
DE,PE

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	−20°C to +85°C	−55°C to +125°C
0.2% (8 Bit)	AD7523JN	AD7523AD	AD7523SD
0.1% (9 Bit)	AD7523KN	AD7523BD	AD7523TD
0.05% (10 Bit)	AD7523LN	AD7523CD	AD7523UD

AD7523 -T D

- D — Package: 16-Pin CERDIP DIP; N — 16-Pin Plastic DIP
- T — Nonlinearity and Temperature Range: J, K, L — Commercial 0°C to +70°C; A,B,C — Industrial −20°C to +85°C; S,T,U — Military −55°C to +125°C
- AD7523 — Basic Part Number

INTERSIL

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... −0.3 to VDD
Output Voltage Compliance ..... −0.3 to VDD
Power Dissipation (package)
Plastic
up to +70°C 670mW
derates above +70°C by ..... 8.3mW/°C
Ceramic
up to 75°C 450mW
derates above 75°C by ..... 6mW/°C
Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD, CD Versions ..... −25°C to +85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than VDD and lower than GND to any terminal except V_{REF} + R_{FB}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

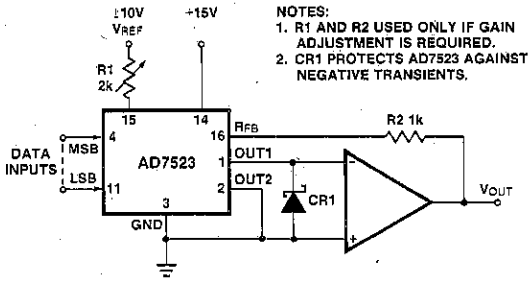
SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V unless otherwise specified)

PARAMETER		TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)						
Resolution		8	8	Bits	Min	
Nonlinearity (Note 2)	(±1/2 LSB)	±0.2	±0.2	% of FSR	Max	−10V ≤ V_{REF} ≤ +10V
	(±1/4 LSB)	±0.1	±0.1	% of FSR	Max	
	(±1/8 LSB)	±0.05	±0.05	% of FSR	Max	V_{OUT1} = V_{OUT2} = 0V
Monotonicity		Guaranteed				
Gain Error (Note 2)		±1.5	±1.8	% of FSR	Max	Digital inputs high.
Nonlinearity Tempco (Note 2 and 3)		2		PPM of FSR/°C	Max	−10V V_{REF} +10V
Gain Error Tempco (Note 2 and 3)		10		PPM of FSR/°C	Max	
Output Leakage Current (either output)		±50	±200	nA	Max	V_{OUT1} = V_{OUT2} = 0
AC ACCURACY (Note 3)						
Power Supply Rejection (Note 2)		0.02	0.03	% of FSR/%	Max	V^+ = 14.0 to 15.0V
Output Current Settling Time		150	200	nS	Max	To 0.2% of FSR, R_L = 100Ω
Feedthrough Error		±1/2	±1	LSB	Max	V_{REF} = 20V pp, 200KHz sine wave; All digital inputs low.
REFERENCE INPUT		5K		Ω	Min	All digital inputs high, I_{OUT1} at ground.
Input Resistance (Pin 15)		20K		Ω	Max	
Temperature Coefficient (Note 3)		−500		ppm/°C	Max	
ANALOG OUTPUT (Note 3)						Both outputs.
Voltage Compliance (Note 4)		−100mV to V^+				See maximum ratings.
Output Capacitance	C_{OUT1}	100		pF	Max	All digital inputs high (VINH)
	C_{OUT2}	30		pF	Max	
	C_{OUT1}	30		pF	Max	All digital inputs low (VINL)
	C_{OUT2}	100		pF	Max	
DIGITAL INPUTS						
Low State Threshold (V_{INL})		0.8		V	Max	Guarantees DTL/TTL and CMOS (0.5 max, 14.5 min) levels
High State Threshold (V_{INH})		2.4		V	Min	
Input Current (per input)		±1		μA	Max	V_{IN} = 0V or +15V
Input Coding		Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)		4		pF	Max	
POWER REQUIREMENTS						Accuracy is tested and guaranteed at
Power Supply Voltage Range		+5 to +16		V		V^+ = +15V, only.
I^+		100		μA	Max	All digital inputs low or high.

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

APPLICATIONS
UNIPOLAR OPERATION



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. CR1 PROTECTS AD7523 AGAINST NEGATIVE TRANSIENTS.

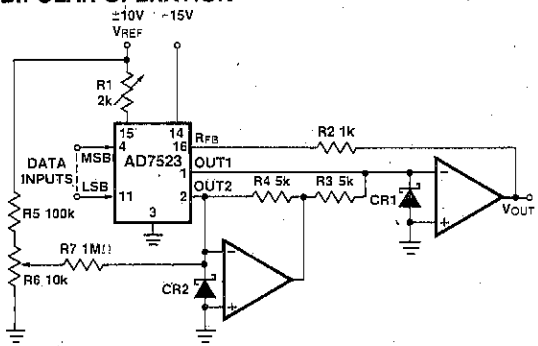
Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT	
11111111	$-V_{REF}\left(\frac{255}{256}\right)$	
10000001	$-V_{REF}\left(\frac{129}{256}\right)$	
10000000	$-V_{REF}\left(\frac{128}{256}\right)$	$= -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$	
00000001	$-V_{REF}\left(\frac{1}{256}\right)$	
00000000	$-V_{REF}\left(\frac{0}{256}\right)$	$= 0$

Note: 1 LSB = (2^{-8}) $(V_{REF}) = \left(\frac{1}{256}\right)$ (V_{REF})

Table 1. Unipolar Binary Code Table

BIPOLAR OPERATION



NOTES:
1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. R5-R7 USED TO ADJUST V_{OUT} = 0V AT INPUT CODE 10000000.
4. CR1 & CR2 PROTECT AD7523 AGAINST NEGATIVE TRANSIENTS.

Figure 2. Bipolar (4-Quadrant) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT	
11111111	$-V_{REF}\left(\frac{127}{128}\right)$	
10000001	$-V_{REF}\left(\frac{1}{128}\right)$	
10000000	0	
01111111	$+V_{REF}\left(\frac{1}{128}\right)$	
00000001	$+V_{REF}\left(\frac{127}{128}\right)$	
00000000	$+V_{REF}\left(\frac{128}{128}\right)$	

Note: 1LSB = (2^{-7}) $(V_{REF}) = \left(\frac{1}{128}\right)$ (V_{REF})

Table 2. Bipolar (Offset Binary) Code Table

POWER DAC DESIGN USING AD7523

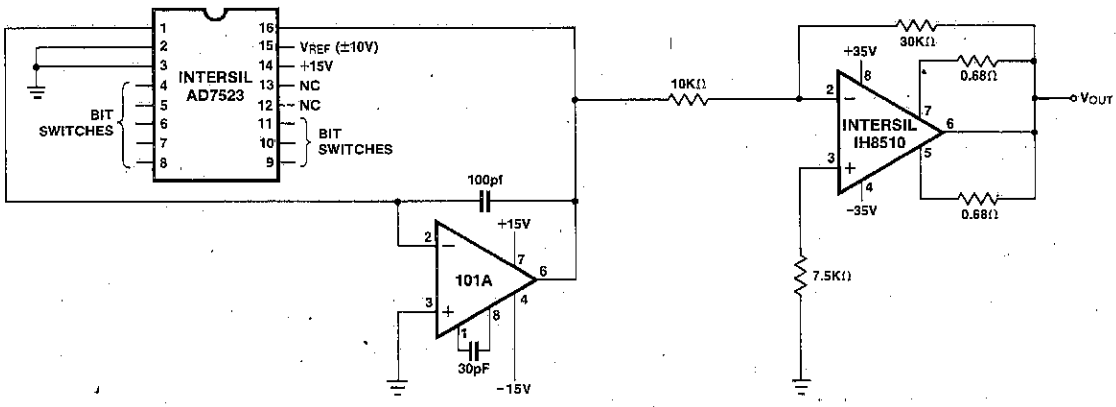


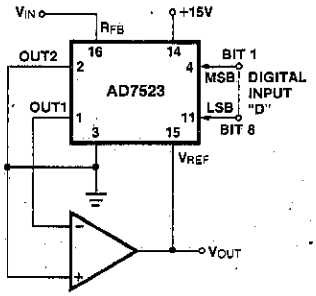
Figure 3. The Basic Power DAC

A typical power DAC designed for 10 bit accuracy and 8 bit resolution is shown in Figure 3. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the AD7523.

A summing amplifier between the AD7523 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7523 can be directly connected to the IH8510, by using a 25 volts reference for the DAC.

APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



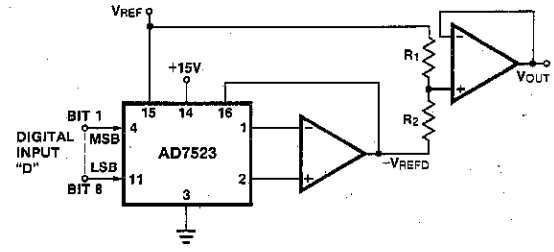
$V_{OUT} = -V_{IN}/D$

WHERE:

$$D = \frac{BIT1}{2^1} + \frac{BIT2}{2^2} + \ldots \frac{BIT8}{2^8}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

MODIFIED SCALE FACTOR AND OFFSET



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1+R_2}\right) - \left(\frac{R_1 D}{R_1+R_2}\right)\right] \quad \text{WHERE:} \quad D = \frac{\text{BIT 1}}{2^1} + \frac{\text{BIT 2}}{2^2} + \ldots \frac{\text{BIT 8}}{2^8}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

4

For further information on the use of this device, see the following Application Bulletins:

A016 "Selecting A/D Converters," by David Fullagar
A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A020 "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger
A021 "Power D/A Converters Using the IH8510," by Dick Wilenken
R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al., Electronics, Dec. 9, 1976

AD7533
10 Bit Monolithic Multiplying D/A Converters

FEATURES

- Lowest cost 10-bit DAC
- 8, 9 and 10 bit linearity
- Low gain and linearity Tempcos
- Full temperature range operation
- Full input static protection
- DTL/TTL/CMOS direct interface
- +5 to +15 volts supply range
- Low power dissipation
- Fast settling time
- Four quadrant multiplication
- Direct AD7520 equivalent
- 883B Processed versions available

GENERAL DESCRIPTION

The Intersil AD7533 is a low cost, monolithic 10-bit, four-quadrant multiplying digital-to-analog converter (DAC).

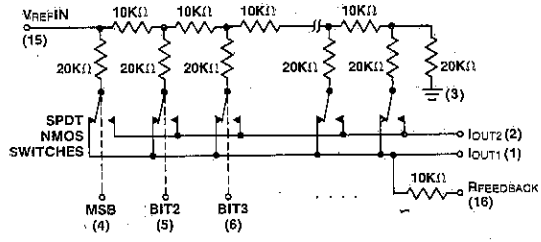
Intersil's thin-film resistors on CMOS circuitry provide 10, 9 and 8 bit accuracy, full temperature range operation, +5V to +15V power range, full input protection from damage due to static discharge by clamps to V+ and ground and very low power dissipation.

Pin and function equivalent to Industry Standard AD7520, the AD7533 is recommended as a lower cost alternative for old or new 10-bit DAC designs.

Application of AD7533 includes programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

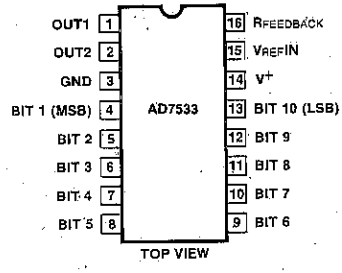
4

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION

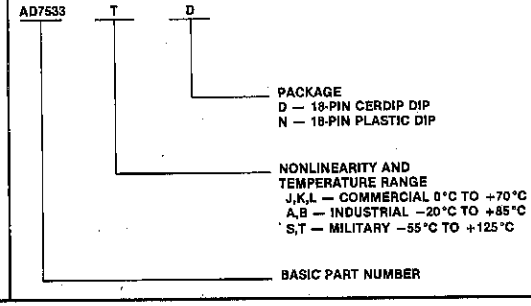


(Outline dwg DE, PE)

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	−20°C to +85°C	−55°C to +125°C
±0.2% (8-bit)	AD7533JN	AD7533AD	AD7533SD
±0.1% (9-bit)	AD7533KN	AD7533BD	AD7533TD
±0.05% (10-bit)	AD7533LN	AD7533CD	AD7533UD

PACKAGE IDENTIFICATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+ ..... −0.3V, +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... −0.3V to V^+
Output Voltage Compliance ..... −0.3 to V^+
Power Dissipation (package)
Ceramic
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C
Plastic
up to 70°C 670mW
derates above 70°C by ..... 8.3mW/°C
Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD, CD Versions ..... −25°C to +85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages lower than ground or higher than V^+ to any pin except V_{REF} and R_{FB}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2} = 0$ unless otherwise specified.)

PARAMETER		T_A +25°C	T_A MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)						
Resolution		10	10	Bits	Min	
Nonlinearity (Note 2)		±0.2	±0.2	% of FSR	Max	
		±0.1	±0.1	% of FSR	Max	$-10V \le V_{REF} \le +10V$
		±0.05	±0.05	% of FSR	Max	$V_{OUT1} = V_{OUT2} = 0V$
Gain Error (Note 2 and 5)		±1.4	±1.5	% of FS	Max	Digital Inputs = V_{INH}
Output Leakage Current (either output)		±50	±200	nA	Max	V_{REF} = ±10V
AC ACCURACY						
Power Supply Rejection (Note 2 and 3)		0.005	0.008	% of FSR/%	Max	V^+ = 14.0 to 17.0V
Output Current Settling Time		600 (Note 6)	800 (Note 3)	nS	Max	To 0.05% of FSR, R_L = 100Ω
Feedthrough Error (Note 3)		±0.05	±0.1	% FSR	Max	V_{REF} = ±10V, 100kHz sine wave. Digital inputs low.
REFERENCE INPUT		5K			Min	
Input Resistance (Pin 15)		20K		Ω	Max	All digital inputs high.
Temperature Coefficient		−300		ppm/°C	Typ	
ANALOG OUTPUT						Both outputs.
Voltage Compliance (Note 4)		−100mV to V^+				See maximum ratings.
Output Capacitance (Note 3)	C_{OUT1}	100		pF	Max	All digital inputs high (V_{INH})
	C_{OUT2}	35		pF	Max	
	C_{OUT1}	35		pF	Max	All digital inputs low (V_{INL})
	C_{OUT2}	100		pF	Max	
DIGITAL INPUTS						
Low State Threshold (VINL)		0.8		V	Max	
High State Threshold (VINH)		2.4		V	Min	
Input Current (I_{IN})		±1		μA	Max	V_{IN} = 0V and V^+
Input Coding		Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)		5		pF	Max	
POWER REQUIREMENTS						
V_{DD}		+15 ±10%		V		Rated Accuracy
Power Supply Voltage Range		+5 to +16		V		
I^+		2		mA	Max	Digital Inputs = V_{INL} to V_{INH}
		100	150	μA	Max	Digital Inputs = 0V or V^+

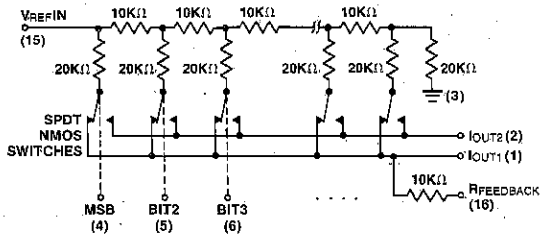
NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.
5. Full scale (FS) = − (V_{REF}) • (1023/1024)
6. Sample tested to ensure specification compliance.
7. 100% screened to MIL-STD-883, method 5004, para. 3.1.1. through 3.1.12 for class B device. Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I^+ @ +25°C and +125°C (SD, TD, UD) or +25°C and +85°C (AD, BD, CD).

Specifications subject to change without notice.

GENERAL CIRCUIT INFORMATION

The Intersil AD7533 is a 10 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 1. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 1

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 2). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

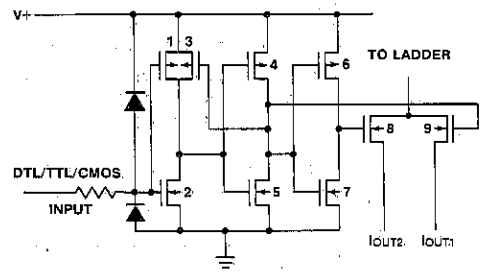
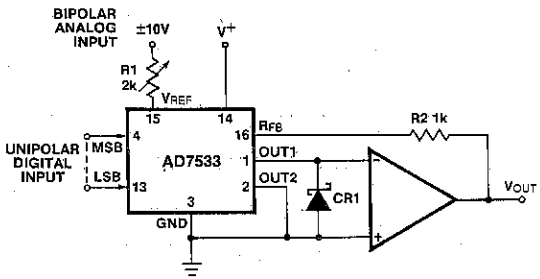


Figure 2

4

APPLICATIONS

UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. SCHOTTKY DIODE CR1 (HP5082-2811 OR EQUIV) PROTECTS OUT1 TERMINAL AGAINST NEGATIVE TRANSIENTS.

Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (VOUT as shown in Figure 3)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:

1. Nominal Full Scale for the circuit of Figure 3 is given by

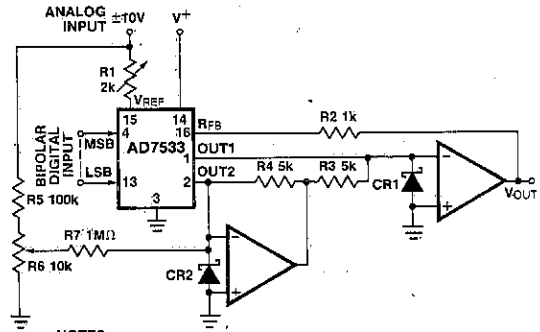
$$FS = -V_{REF}\left(\frac{1023}{1024}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 3 is given by

$$LSB = V_{REF}\left(\frac{1}{1024}\right)$$

Table 1. Unipolar Binary Code

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. SCHOTTKY DIODES CR1 AND CR2 (HP5082-2811 OR EQUIV) PROTECT OUT1 AND OUT2 TERMINALS FROM NEGATIVE TRANSIENTS

Figure 4. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (VOUT as shown in Figure 4)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES:

1. Nominal Full Scale Range for the circuit of Figure 4 is given by

$$FSR = V_{REF}\left(\frac{1023}{512}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 4 is given by

$$LSB = V_{REF}\left(\frac{1}{512}\right)$$

Table 2. Bipolar (Offset Binary) Code Table

POWER DAC DESIGN USING AD7533

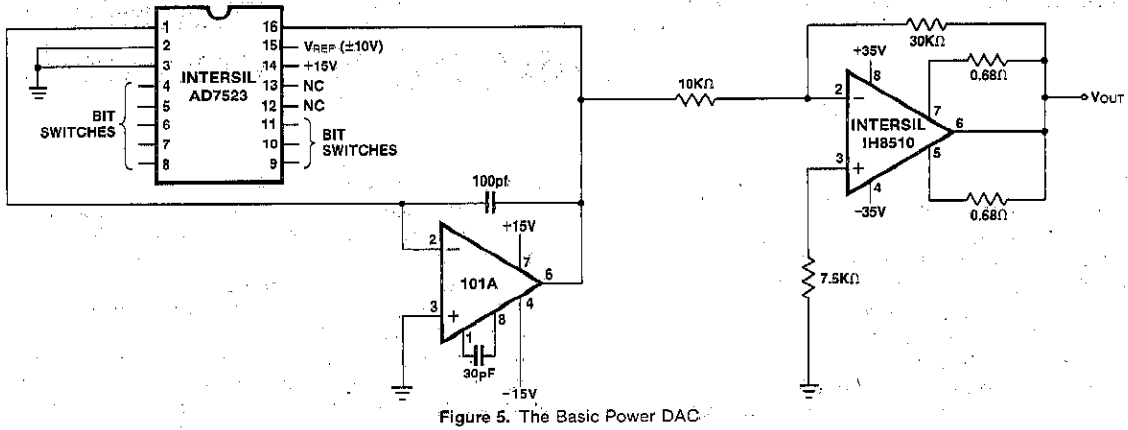
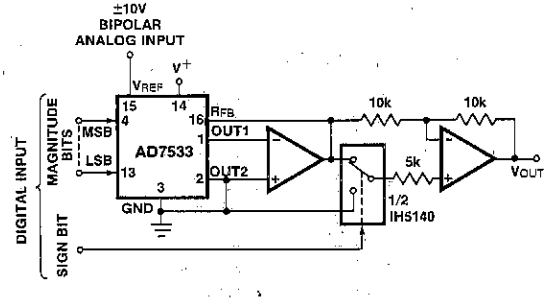


Figure 5. The Basic Power DAC

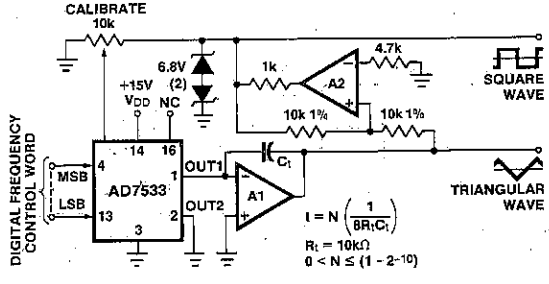
A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 5. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the AD7533.

A summing amplifier between the AD7533 and the IH8510 is used to separate the gain block containing the AD7533 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7533 can be directly connected to the IH8510, by using a 25 volts reference for the DAC. Notice that the output of the 101A is fed into an inverting amplifier with a gain of −3, which can be easily changed to a non-inverting configuration. (For more information write for: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

10-BIT AND SIGN MULTIPLYING DAC



PROGRAMMABLE FUNCTION GENERATOR



INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.

AD7541
12 Bit Monolithic Multiplying D/A Converters

FEATURES

- 12 bit linearity (0.01%)
- Pretrimmed gain
- Low gain and linearity Tempcos
- Full temperature range operation
- Full input static protection
- DTL/TTL/CMOS compatible
- +5 to +15 volts supply range
- Low power dissipation (20mW)
- Current settling time: 1μs to 0.01% of FSR
- Four quadrant multiplication
- 883B Processed versions available

GENERAL DESCRIPTION

The Intersil AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Intersil's wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with DTL/TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil AD7541.

Pin compatible with AD7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

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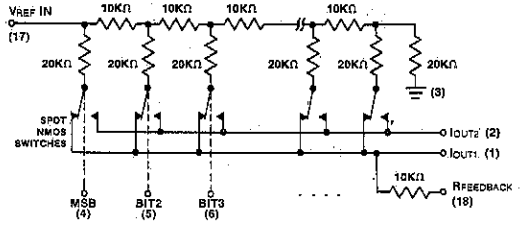
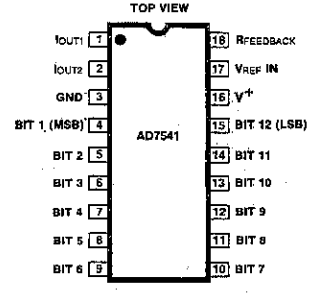
FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

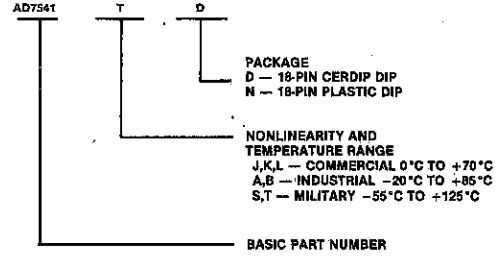
PIN CONFIGURATION



(Outline dwg DN, PN)

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	−20°C to +85°C	−55°C to +125°C
0.02% (11-bit)	AD7541JN	AD7541AD	AD7541SD
0.01% (12-bit)	AD7541KN	AD7541BD	AD7541TD
0.01% (12-bit) Guaranteed Monotonic	AD7541LN	—	—



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −100mV to V^+
Power Dissipation (package)
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C

Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD Versions ..... −20°C to +85°C
SD, TD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C

CAUTION 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{fb}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, T_A = 25°C unless otherwise specified)

PARAMETER			TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1) Resolution			12	12	Bits	Min		
Nonlinearity (Note 2)	S	J	±0.020	±0.024	% of FSR	Max	−10V ≤ V_{REF} ≤ +10V V_{OUT1} = V_{OUT2} = 0V	1
	T	K	±0.010	±0.012	% of FSR	Max		
		L	±0.010	±0.012	% of FSR	Max		
			Guaranteed Monotonic					
Gain Error (Note 2)			±0.3	±0.4	% of FSR	Max	−10V ≤ V_{REF} ≤ +10V	
Output Leakage Current (either output)			±50	±200	nA	Max	V_{OUT1} = V_{OUT2} = 0	
AC ACCURACY (Note 3) Power Supply Rejection (Note 2)			±0.01	±0.02	% of FSR/%	Max	V^+ = 14.5 to 15.5V	2
Output Current Settling Time			1		µS	Max	To 0.01% of FSR	6
Feedthrough Error			1		mV pp	Max	V_{REF} = 20V pp, 10 kHz. All digital inputs low.	5
REFERENCE INPUT Input Resistance			5K		Ω	Min	All digital inputs high. I_{OUT1} at ground.	
			10K			Typ		
			20K			Max		
ANALOG OUTPUT Voltage Compliance (Note 4)			−100mV to V^+				Both outputs. See maximum ratings.	
Output Capacitance (Note 3)	C_{OUT1}		200		pF	Max	All digital inputs high (V_{INH})	4
	C_{OUT2}		60		pF	Max		
	C_{OUT1}		60		pF	Max	All digital inputs low (V_{INL})	4
	C_{OUT2}		200		pF	Max		
Output Noise (both outputs)			Equivalent to 10KΩ Johnson noise			Typ		3
DIGITAL INPUTS Low State Threshold (VINL)			0.8		V	Max		
High State Threshold (VINH)			2.4		V	Min		
Input Current			±1		µA	Max	V_{IN} = 0 or V^+	
Input Coding			Binary/Offset Binary				See Tables 1&2 on pages 4 and 5.	
Input Capacitance (Note 3)			8		pF	Max		
POWER REQUIREMENTS Power Supply Voltage Range			+5 to +16		V		Accuracy is not guaranteed over this range	
I^+			2		mA	Max	All digital inputs high or low	
Total Power Dissipation (including the ladder)			20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

TEST CIRCUITS

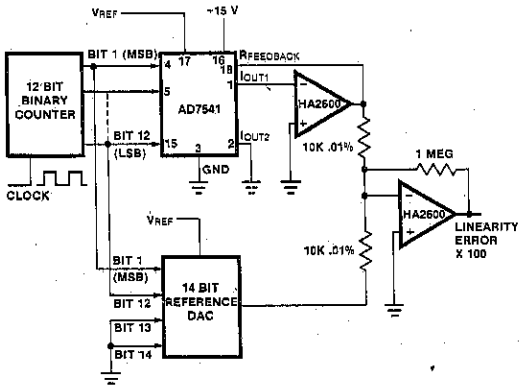


Figure 1. Nonlinearity

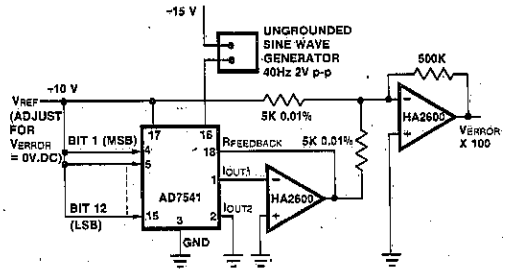


Figure 2. Power Supply Rejection

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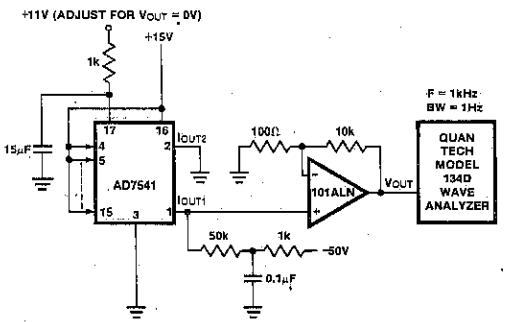


Figure 3. Noise

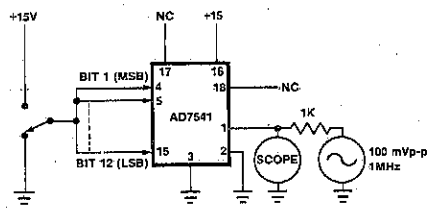


Figure 4. Output Capacitance

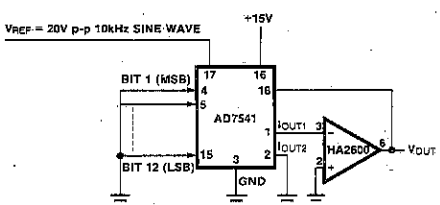


Figure 5. Feedthrough Error

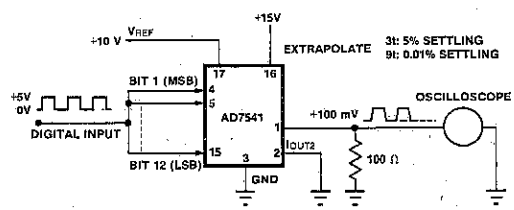


Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

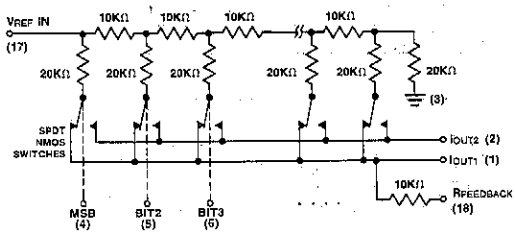
The Intersil AD7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.



(Switches shown for Digital Inputs "High")

Figure 7. AD7541 Functional Diagram

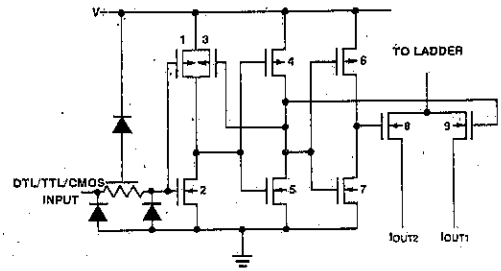


Figure 8. CMOS Switch

APPLICATIONS

General Recommendations

Static performance of the AD7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than $\pm 200\mu V$).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V^+ (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor (~1MΩ) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

APPLICATIONS, Continued

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 9. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. Schottky diode (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

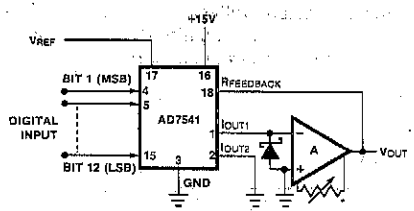


Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}(1 - 1/2^{12})$ reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

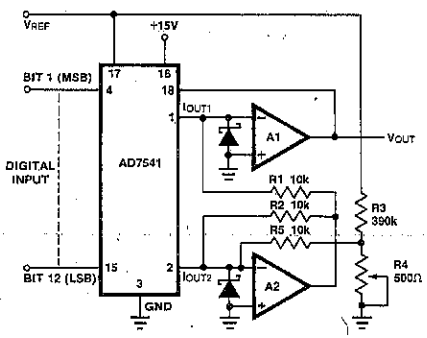
TABLE 1

Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}(1 - 1/2^{12})$
100000000001	$-V_{REF}(1/2 + 1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}(1/2 - 1/2^{12})$
000000000001	$-V_{REF}(1/2^{12})$
000000000000	0

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.



Note: R1 and R2 should be 0.01%, low-TCR resistors.

Figure 10. Bipolar Operation (4-Quadrant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Set R4 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT2} amplifier output.
5. Connect a short circuit across R2.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT1} amplifier output.
8. Remove short circuit across R2.
9. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R4 for 0V ±0.2mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}(1 - 1/2^{11})$ volts reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 2

Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}(1 - 1/2^{11})$
100000000001	$-V_{REF}(1/2^{11})$
100000000000	0
011111111111	$V_{REF}(1/2^{11})$
000000000001	$V_{REF}(1 - 1/2^{11})$
000000000000	V_{REF}

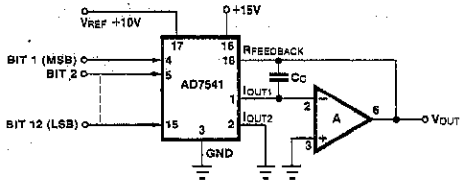


Figure 11. General DAC Circuit with Compensation Capacitor, C_C.

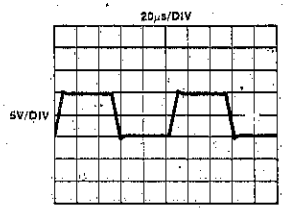


Figure 12. AD7541 Response with: A = Intersil 741HS

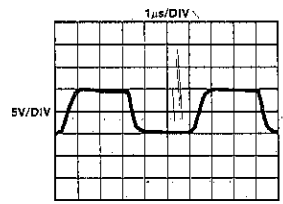


Figure 13. AD7541 Response with: A = Intersil 2515
C_C = 15pF

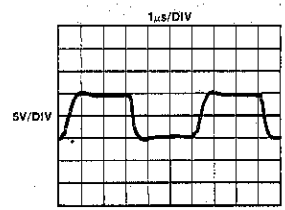


Figure 14. AD7541 Response with: A = Intersil 2520

DYNAMIC PERFORMANCE

The dynamic performance of the DAC, alsodepends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, open-loop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between 10kΩ ($R_{Feedback}$ alone) and 5kΩ ($R_{Feedback}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

Three typical circuits and the resultant waveforms are shown in Figures 11 to 14. A low-cost general purpose (Intersil 741HS), a low-cost high-speed (Intersil 2515) and a high-speed fast-settling (Intersil 2520) amplifier cover the principal application areas.

4

INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.

ICL8018A/8019A/8020A
Quad Current Switch for D/A Conversion

FEATURES
- **TTL Compatible: LOW—0.8V HIGH—2.0V**
- **12 Bit Accuracy**
- **40 nsec, Switching Speed**
- **Wide Power Supply Range**
- **Low Temperature Coefficient**

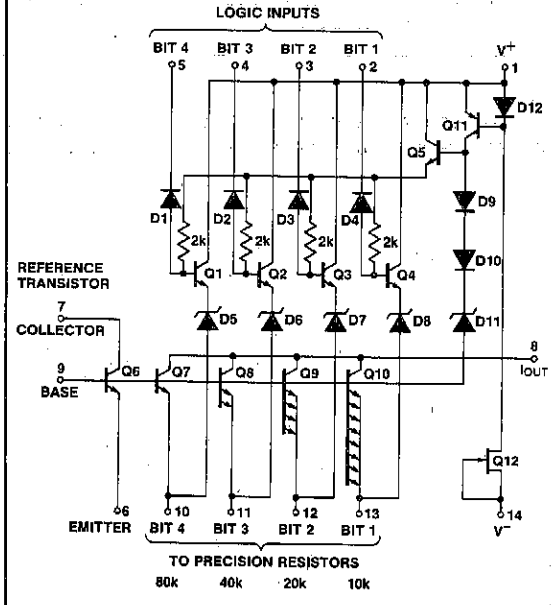
APPLICATIONS:
- D/A-A/D Converters
- Digital Threshold Control
- Programmable Voltage Source
- Meter Drive
- X-Y Plotters

4

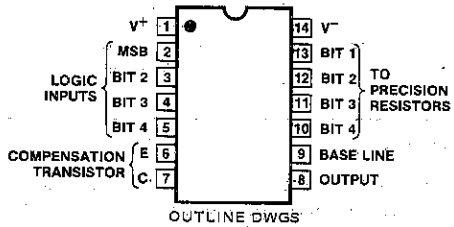
GENERAL DESCRIPTION
The Intersil ICL8018A family are high speed precision current switches for use in current summing digital-to-analog converters. They consist of four logically controlled current switches and a reference device on a single monolithic silicon chip. The reference transistor, combined with precision resistors and an external source, determines the magnitude of the currents to be summed. By weighting the currents in proportion to the binary bit which controls them, the total output current will be proportional to the binary number represented by the input logic levels.

The performance and economy of this family make them ideal for use in digital-to-analog converters for industrial process control and instrumentation systems.

SCHEMATIC DIAGRAM
EQUIVALENT CIRCUIT



PIN DIAGRAM



OUTLINE DWGS
JD, PD

ORDERING INFORMATION

ACCURACY	MILITARY TEMP RANGE CERDIP	COMMERCIAL TEMP RANGE PLASTIC DIP
Individual Devices		
.01%	ICL8018AMJD	ICL8018ACPD
0.1%	ICL8019AMJD	ICL8019ACPD
1.0%	ICL8020AMJD	ICL8020ACPD
Matched Sets*		
.01%	ICL8018AMXJD	ICL8018ACXPD
0.1%	ICL8019AMXJD	ICL8019ACXPD
1.0%	ICL8020AMXJD	ICL8020ACXPD

***NOTE:** Units ordered in equal quantities will be matched such that the V_{be}'s of the 8019 will be within ±10mV of the 8018 compensating transistor, and the V_{be}'s of the 8020 will be within ±50mV. The ICL8018 - X matched sets consist of one 8018, one 8019, and one 8020. The 8019 - X contains one 8019 and one 8020, while the 8020 - X contains two 8020's. Units shipped as matched sets will be marked with a unique set number.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Logic Input Voltage ..... −2V to V^+
Output Voltage ..... $V_{BASELINE}$ to +20V
$V_{BASELINE}$ ..... V^- to +5V
Storage Temperature ..... −65°C to +150°C
Operating Temperature ICL8018AM
ICL8019AM ..... −55°C to +125°C
ICL8020AM
ICL8018AC
ICL8019AC ..... 0°C to +70°C
ICL8010AC
Lead Temperature (soldering 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($4.5V \le V^+ \le 20V$, $V^- = -15V$, $T_A = 25°C$, V @ pin 6 = −5V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Error					
ICL8018A	V_{INHI} = 5.0V			±.01	
ICL8019A	V_{INLO} = 0.0V			±0.1	%
ICL8020A				±1	
Error Temperature Coefficient					
ICL8018A			±2	±5	ppm/°C
ICL8019A			±2	±25	
ICL8020A			±2	±50	
Settling Time To ±1/2 LSB, R_L = 1kΩ					
8 BIT			100		
12 BIT			200		ns
Switching Time To Turn On LSB			40		ns
Output Current (Nominal)					
BIT 1 (MSB)			1.0		mA
BIT 2			0.5		
BIT 3			0.25		
BIT 4 (LSB)			0.125		
Zero Output Current	V_{IN} = 5.0V		10	50	nA
Output Voltage Range		$V_{BASELINE}$ +1V		+10	V
Input Coding-Complimentary Binary (See Truth Table)					
Logic Input Voltage	ΔI_{OUT} <400nA				
"0" (Switch ON)				0.8	V
"1" (Switch OFF)		2.0			
Logic Input Current					
"0"	V_{IN} = 0V		−1.0	−2	mA
"1" (into device)	V_{IN} = 5V		0.01	0.1	μA
Power Supply Rejection					
V^+			.005		%/V
V^-			.0005		
Supply Voltage Range					
V^+		4.5	5	20	V
V^-		−10	−15	−20	
Supply Current (V_{SUPP} = ±20V)					
I^+			7	10	mA
I^-			1	3	

BASIC D/A THEORY

The majority of digital to analog converters contain the elements shown in Figure 1. The heart of the D/A converter is the logic controlled switching network, whose output is an analog current or voltage proportional to the digital number on the logic inputs. The magnitude of the analog output is determined by the reference supply and the array of precision resistors, see fig. 2. If the switching network has a current output, often a transconductance amplifier is used to provide a voltage output.

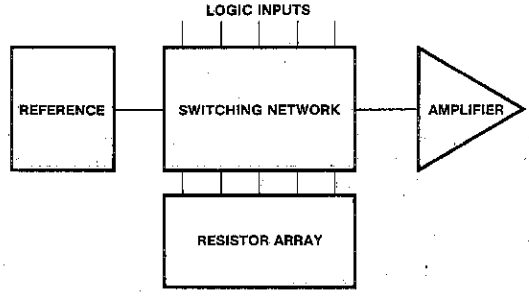


Figure 1: Elements of a D/A Converter

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Logic Input	Nominal Output Current (mA)
0 0 0 0	1.875
0 0 0 1	1.750
0 0 1 0	1.625
0 0 1 1	1.500
0 1 0 0	1.375
0 1 0 1	1.250
0 1 1 0	1.125
0 1 1 1	1.000
1 0 0 0	0.825
1 0 0 1	0.750
1 0 1 0	0.625
1 0 1 1	0.500
1 1 0 0	0.375
1 1 0 1	0.250
1 1 1 0	0.125
1 1 1 1	0.000

Figure 2: Truth Table

DEFINITION OF TERMS

The **resolution** of a D/A converter refers to the number of logic inputs used to control the analog output. For example, a D/A converter using two quad current sources would be an 8 bit converter. If three quads were used, a 12 bit converter would be formed. Resolution is often stated in terms of one part in, e.g., 256 since the number of controlling bits is related to total number of identifiable levels by the power of 2. The four bit quad has sixteen different levels (see Truth Table) each output corresponding to a particular logic input word.

Note that **maximum output** of the quad switch is $1+1/2+1/4+1/8=1-7/8=1.875$ mA. If this series of bits were continued as $1/16+1/32+1/64\ldots\ldots 1/2^{(n-1)}$, the maximum output limit would approach 2.0 mA. This limiting value is called **full scale output**. The maximum output is always less than the full scale output by one least significant bit, LSB. For a twelve bit system (resolution 1 part in 4096) with a full scale output of 10.0 volts the maximum output would be $\frac{4095}{4096}$ X 10V. Since the numbers are extremely close for high resolution systems, the terms are often used interchangeably.

The **accuracy** of a D/A converter is generally taken to mean the largest error of any output level from its nominal value. The accuracy or **absolute error** is often expressed as a **percentage of the full scale output.**

Linearity relates the maximum error in terms of the deviation from the best straight line drawn through all the possible output levels. Linearity is related to accuracy by the scale factor and output offset. If the scale factor is exactly the nominal value and offset is adjusted to zero, then accuracy and linearity are identical. Linearity is usually specified as being within ±1/2 LSB of the best straight line.

Another desirable property of D/A converter is that it be **monotonic**. This simply implies that each successive output level is greater than the preceding one. A possible worst case condition would be when the output changes from most significant bit (MSB) OFF, all other bits ON to the next level which has the MSB ON and all other bits OFF, e.g., 10000 . . . to 01111.

In applications where a quad current switch drives a transconductance amplifier (current to voltage converter), transient response is almost exclusively determined by the output amplifier itself. Where the quad output current drives a resistor to ground, switching time and settling time are useful parameters.

Switching time is the familiar 10% to 90% rise time type of measurement. Low capacitance scope probes must be used to avoid masking the high speeds that current source switching affords. The **settling time** is the elapsed time between the application of a fast input pulse and the time at which the output voltage has settled to or approached its final value within a specified limit of accuracy. This limit of accuracy should be commensurate with the resolution of the DAC to be used.

Typically, the settling time specification describes how soon after an input pulse the output can be relied upon as accurate to within ±1/2 LSB of an N bit converter. Since the 8018A family has been desiged with all the collectors of the current switching transistors tied together, the output capacitance is constant. The transient response is, therefore, a simple exponential relationship, and from this the settling time can be calculated and related to the measured rise time as shown in Figure 3.

Bits of Resolution	±1/2 LSB Error % Full Scale	Number of Time Constants	Number of Rise Times
8	.2 %	6.2	2.8
10	.05%	7.6	3.4
12	.01%	9.2	4.2
Rise Time (10%-90%) = 2.2 R_L C_{eff}			

Figure 3: Settling Time vs. Rise Time Resistor Load

CIRCUIT OPERATION

An example of a practical circuit for the ICL8018A quad current switch is shown in Figure 4. The circuit can be analyzed in two sections; the first generates very accurate currents and the second causes these currents to be switched according to input logic signals. A reference current of 125μA is generated by a stable reference supply and a precision resistor. An op-amp with low offset voltage

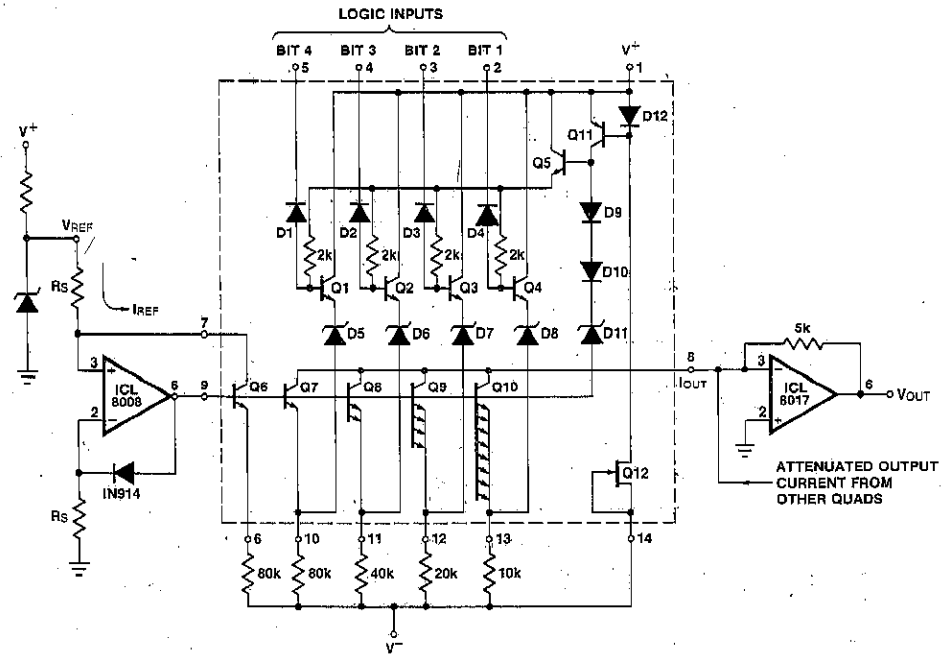


Figure 4: Typical Circuit

and low input bias current, such as the ICL8008, is used in conjunction with the internal reference transistor, Q_6, to force the voltage on the common base line, so that the collector current of Q_6 is equal to the reference current. The emitter current of Q_6 will be the sum of the reference current and a small base current causing a drop of slightly greater than 10 volts across the 80k resistor in the emitter of Q_6. Since this resistor is connected to –15V, this puts the emitter of Q_6 at nearly –5V and the common base line at one V_{BE} more positive at –4.35V typically.

Also connected to the common base line are the switched current source transistors Q_7 through Q_{10}. The emitters of these transistors are also connected through weighted precision resistors to –15V and their collector currents summed at pin 8. Since all these transistors, Q_6 through Q_{10}, are designed to have equal emitter-base voltages, it follows that all the emitter resistors will have equal voltage drops across them. It is this constant voltage and the precision resistors at the emitter that determine the exact value of switched output current. The emitter resistor of Q_7 is equal to that of Q_6, therefore, Q_7's collector current will be I_{REF} or 125μA. Q_8 has 40k in the emitter so that its collector current will be twice I_{REF} or 250μA. In the same way, the 20k and 10k in the emitters of Q_9 and Q_{10} contribute .5 mA and 1 mA to the total collector current.

The reference transistor and four current switching transistors are designed for equal emitter current density by making the number of emitters proportional to the current switched.

The remaining circuitry provides switching signals from the logic inputs. In the switch ON mode, zener diodes D_5 through D_8, connected to the emitter of each current switch transistor Q_7 thru Q_{10}, are reverse biased allowing the transistors to operate, producing precision currents summed in the collectors. The transistors are turned off by raising the voltage on the zeners high enough to turn on the zeners and raise the emitters of the switching transistor. This reverse biases the emitter base diode thereby shutting off that transistor's collector current.

The analog output current can be used to drive one load directly, (1kΩ to ground for FS = 1.875V for example) or can be used to drive a transconductance amplifier to give larger output voltages.

EXPANDING THE QUAD SWITCH

While there are few requirements for only 4 bit D to A converters, the 8018A is readily expanded to 8 and 12 bits with the addition of other quads and resistor dividers as shown in Figure 5.

To maintain the progression of binary weighted bit currents, the current output of the first quad drives the input of the transconductance amplifier directly, while a resistor divider network divides the output current of the second quad by 16 and the output current of the third by 256.

e.g., $I_{Total} = 1 \times (1 + 1/2 + 1/4 + 1/8) + 1/16\,(1 + 1/2 + 1/4 + 1/8) + 1/256\,(1 + 1/2 + 1/4 + 1/8) = 1 + 1/2 + 1/4 + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256 + 1/512 + 1/1024 + 1/2048.$

Note that each current switch is operating at the same high speed current levels so that standard 10k, 20k, 40k and 80k resistor networks can be used. Another advantage of this technique is that since the current outputs of the second and third quad are attenuated, so are the errors they contribute. This allows the use of less accurate switches and resistor networks in these positions; hence, the three accuracy grades of .01%, 0.1%, and 1% for the 8018A, 8019A and 8020A, respectively. It should be noted that only the reference transistor on the most significant quad is required to set up the voltage on the common base line joining the three sets of switching transistors (Pin 9).

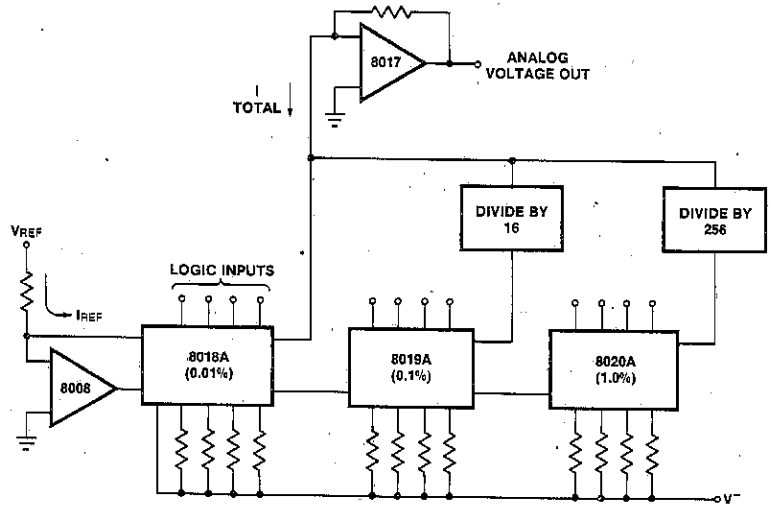


Figure 5: Expanding the Quad Switch

4 GENERATING REFERENCE CURRENTS — ZENER REFERENCE

As mentioned above, the 8018A switches currents determined by a constant voltage across the external precision resistors in the emitter of each switch. There are several ways of generating this constant voltage. One of the simplest is shown in Figure 6. Here an external zener diode is driven by the same current source line used to bias internal Zener D_{11}.

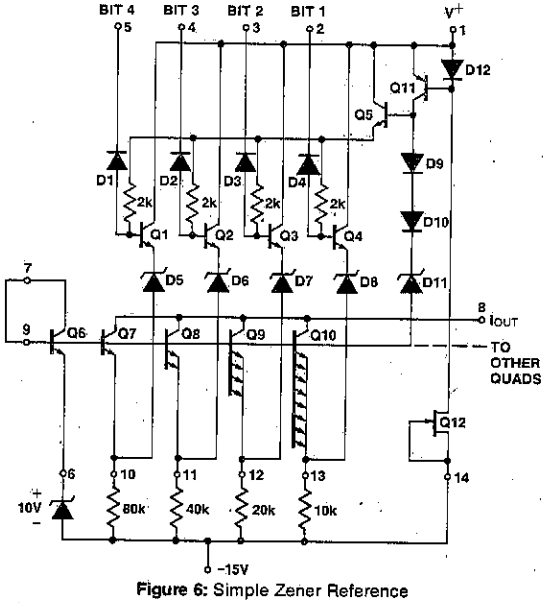


Figure 6: Simple Zener Reference

The zener current will be typically 1 mA per quad. The compensation transistor Q_6 is connected as a diode in series with the external zener. The V_{BE} of this transistor will approximately match the V_{BE}'s of the current switching transistors, thereby forcing the external zener voltage across each of the external resistors. The temperature coefficient of the external zener will dominate the temperature dependence of this scheme, however using a temperature compensated zener minimizes this problem. Since Q_6 is operating at a higher current density than the other switching transistors, the temperature matching of V_{BE}'s is not optimum, but should be adequate for a simple 8 or 10 bit converter.

The 8018A series is tested for accuracy with 10V reference voltage across the precision resistors, implying use of a 10 volt zener. Using a different external zener voltage will only slightly degrade accuracy if the zener voltage is above 5 or 6 volts.

When using other than 10 volt reference, the effects on logic thresholds should also be noted (see logic levels below). Full scale adjustment can be made at the output amplifier.

PNP REFERENCE

Another simple reference scheme is shown in Figure 7. Here an external PNP transistor is used to buffer a resistor divider. In this case, the −15 volt supply is used as a reference. Holding the V^- supply constant is not too difficult since the 8018A is essentially a constant current load. In this scheme, the internal compensation transistor is not necessary, since the V_{BE} matching is provided by the emitter-base junction of the external transistor. A small pot in series with the divider facilitates full scale output adjustment. A capacitor from base to collector of the external PNP will lower output impedance and minimize transient effects.

FULL COMPENSATION REFERENCE

For high accuracy, low drift applications, the reference scheme of Figure 4, offers excellent performance. In this circuit, a high gain op-amp compares two currents. The first is a reference current generated in R_S by the temperature compensated zener and the virtual ground at the non-inverting op-amp input. The second is the collector current of the reference transistor Q_6, provided on the quad switch. The output of the op-amp drives the base of Q_6 keeping its collector current exactly equal to the reference current. Since the switching transistor's emitter current densities are equal and since the precision resistors are proportional, all of the switched collector currents will have the proper value.

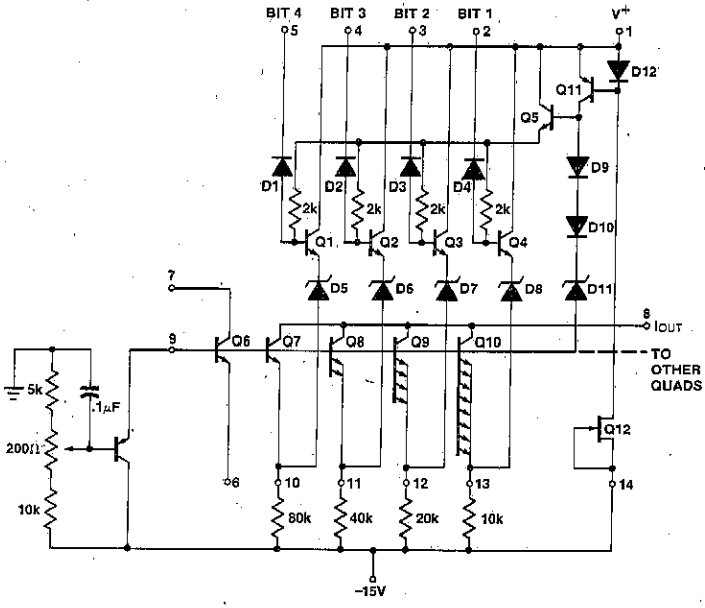
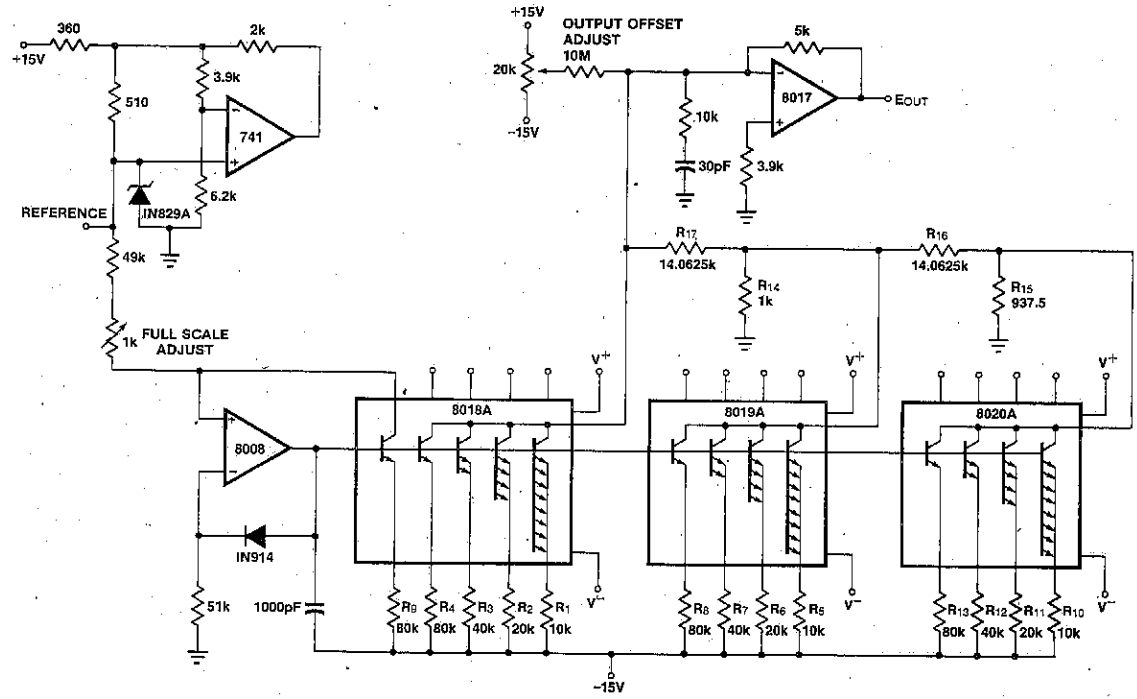


Figure 7: PNP Reference



NOTE: ALL RESISTORS RATIO TO R_1 UNLESS OTHERWISE NOTED.

TOLERANCE TABLE

R_1	10k	0.1% ABS
R_2	20k	0.0122%
R_3	40k	0.0244%
R_4	80k	0.0488%
R_5	10k	0.096%
R_6	20k	0.195%
R_7	40k	0.391%
R_8	80k	0.781%
R_9	80k	0.1%
R_{10}	10k	0.5% ABS
R_{11}	20k	RATIO TO R_{10} 1%
R_{12}	40k	RATIO TO R_{10} 1%
R_{13}	80k	RATIO TO R_{10} 1%
R_{14}	1k	1% ABS
R_{15}	937.5Ω	1% ABS
R_{16}	14.0625k	RATIO TO R_{15} 1%
R_{17}	14.0625k	RATIO TO R_{14} 0.1%

Figure 8

The op-amp feedback loop using the internal reference transistor will maintain proper currents in spite of V_{BE} drift, beta drift, resistor drift and changes in V^-. Using this circuit, temperature drifts of 2 ppm/°C are typical. A discrete diode connected as shown will keep Q_6 from saturating and prevent latch up if V^- is disconnected.

In any reference scheme, it is advisable to capacitively decouple the common base line to minimize transient effects. A capacitor, .001μF to .1μF from Pin 9 to analog ground is usually sufficient.

IMPROVED ACCURACY

As a final note on the subject of setting up reference levels, it should be pointed out that the largest contributor of error is the mismatch of V_{BE}'s of the current switching transistors. That is, if all the V_{BE}'s were identical, then all precision resistors would have exactly the same reference voltage across them. A one millivolt mismatch compared with ten volt reference across the precision resistors will cause a .01% error. While decreasing the reference voltage will decrease the accuracy, the voltage can be increased to achieve better than .01% accuracies. The voltage across the emitter resistors can be doubled or tripled with a proportional increase in resistor values resulting in improved absolute accuracy as well as improved temperature drift performance. This technique has been used successfully to implement up to 16 bit D/A converters.

4

PRACTICAL D/A CONVERTERS

The complete circuit for a high performance 12 bit D/A converter is shown in Figure 8. This circuit uses the "full compensation reference" described above to set the base line drive at the proper level, the temperature compensated zener is stabilized using an op-amp as a regulated supply, and the circuit provides a very stable, precise voltage reference for the D/A converter. The 16:1 and 256:1 resistor divider values are shown for a straight binary system; for a binary coded decimal system the dividers would be 10:1 and 100:1 (BCD is frequently encountered in building programmable voltage sources).

The analog output current of the 8018A current switches is converted to an output voltage using the 8017 as shown. The output amplifier must have low input bias current (small compared with the LSB current), low offset voltage and offset voltage drift, high slew rate and fast settling time. The input compensation shown helps improve pulse response by providing a finite impedance at high frequencies for a point that is virtual ground at DC.

An alternative bias scheme is shown in Figure 9. In this case, the bias at the common base line is fixed by inverting op-amp A_4, the gain of which is adjusted to give −5.0 volts at the emitter of the reference transistor. With the bias at the common base line fixed, the regular circuit of A_1 uses the internal reference transistor and drives the bus connecting all the precision resistors. This isolates the precision resistors from V^- fluctuations. Zener D_3 and constant current source Q_1 keep the regulating 8008 op-amp in mid-range. There are several alternative bias schemes depending on power supplies available. If −20 volts is used for V^-, the bottom of the precision resistor will be at −15 and operation will be the same as the standard circuit. If only −15V is available for V^- the gain of the output transconductance amplifier can be increased by 30% to allow use of a smaller switching currents with 7 volts across the precision resistors.

MULTIPLYING DAC

The circuit of Figure 9 is also convenient to use as a one quadrant multiplying D/A converter. In a multiplying DAC, the analog output is proportional to the product of a digital number and an analog signal. The digital number drives the logic inputs, while the analog signal replaces the constant reference voltage, and produces a current to set up the regulating 8008 op-amp. To vary the magnitude of currents being switched, the voltage across all the 10k, 20k, 40k and 80k resistors must be modulated according to the analog input. An analog input of 0 to +10 volts and an 80k resistor at the input to the 8008 will fulfill this requirement.

CALIBRATING THE 12 BIT D/A CONVERTER

1. With all logic inputs high (ones) adjust the output amplifier offset for zero volts out.
2. Put in the word 0000 1111 1111 (Quad 1 maximum output Quad 2 and 3 off) and adjust full scale pot for V_O of 15/16 (10V) where full scale output is to be 10 volts.
3. Put in the word 1111 0000 1111 and trim the Quad 2 divider for V_O of 15/256 (10V). This adjustment compensates for V_{BE} mismatches between quads although matched sets are available (see data sheet).
4. Put in the word 1111 1111 0000 and trim the Quad 3 divider for V_O of 15/4096 (10V).
5. Finally, with all bits ON (all 0's) readjust the full scale factor pot for

$$V_O = 4095/4096\ (10V)$$

SYSTEM INTERFACE REQUIREMENTS

Using the 8018A series in practical circuits requires consideration of the following interface requirements.

Logic Levels: The 8018A is designed to be compatible with TTL, DTL and RTL logic drive systems. The one constraint imposed on the external voltage levels is that the emitters of the conducting current switch transistors be in the vicinity of −5V; this will be the same as the voltage on Pin 6 if the reference transistor is used. When using other than −5V at Pin 6, the direct bearing on logic threshold should be considered.

Power Supplies: One advantage of the ICL8018A is its tolerance of a wide range of supply voltage. The positive supply voltage need only be large enough (greater than +4.5V) to keep Q_{11} out of saturation, and the negative supply needs to be more negative than −10V to ensure constant current operation of Q_{12}. The maximum supply voltage of ±20V is dictated by transistor breakdown voltages. It is often convenient to use ±15V supplies in systems with op-amps and other I.C.'s. These supplies tend to be better regulated and free from high current transients found on supplies used to power TTL Logic. As with any high speed circuit, attention to layout and adequate power supply decoupling will minimize switching effects.

Ground: High resolution D/A, e.g., 12 bits require fairly large logic drive currents. The change from all bits ON to all bits OFF is a considerable change in supply current being returned to ground. Because of this, it is usually advisable to maintain separate ground points for the analog and digital sections.

Resistors: Each quad current switch requires a set of matched resistors scaled proportional to their binary currents as R, 2R, 4R and 8R. For a 10V resistor voltage drop and "2 mA" full scale output current, resistor values of 10k, 20k, 40k and 80k are convenient. Other resistor values can be used, for example, to increase total output current. The

individual switched currents can be increased up to 100% of their nominal values. The overall accuracy of the complete D/A converter depends on the accuracy of the reference, the accuracy of the quad current switch and tolerance of resistor matching. Because of the binary progression of switched currents, the tolerance of 80k/10k match can be twice that of the 40k/10k which, in turn, can be twice the tolerance of the 20k/10k ratio and still have equal output current errors. The current dividers between quads allows use of less well matched sets of resistors further along in the D/A just as it allows use of .01%, 0.1%, and 1% accurate quad current switches. There are several manufacturers producing the complete precision resistor networks required to implement up to 12 bit D/A converters. Contact Intersil for additional information.*

*Resistor Ladder Networks are manufactured by the following companies:

Micro Networks Corporation
5 Barbara Lane
Worcester, Massachusetts 01604
Tel. (617) 756-4635

Allen-Bradley Company
1201 S. Second Street
Milwaukee, Wisconsin 53204
Tel. (414) 671-2000

Hycomp, Inc.
146 Main Street
Maynard, Massachusetts 01754
Tel. (617) 897-4578

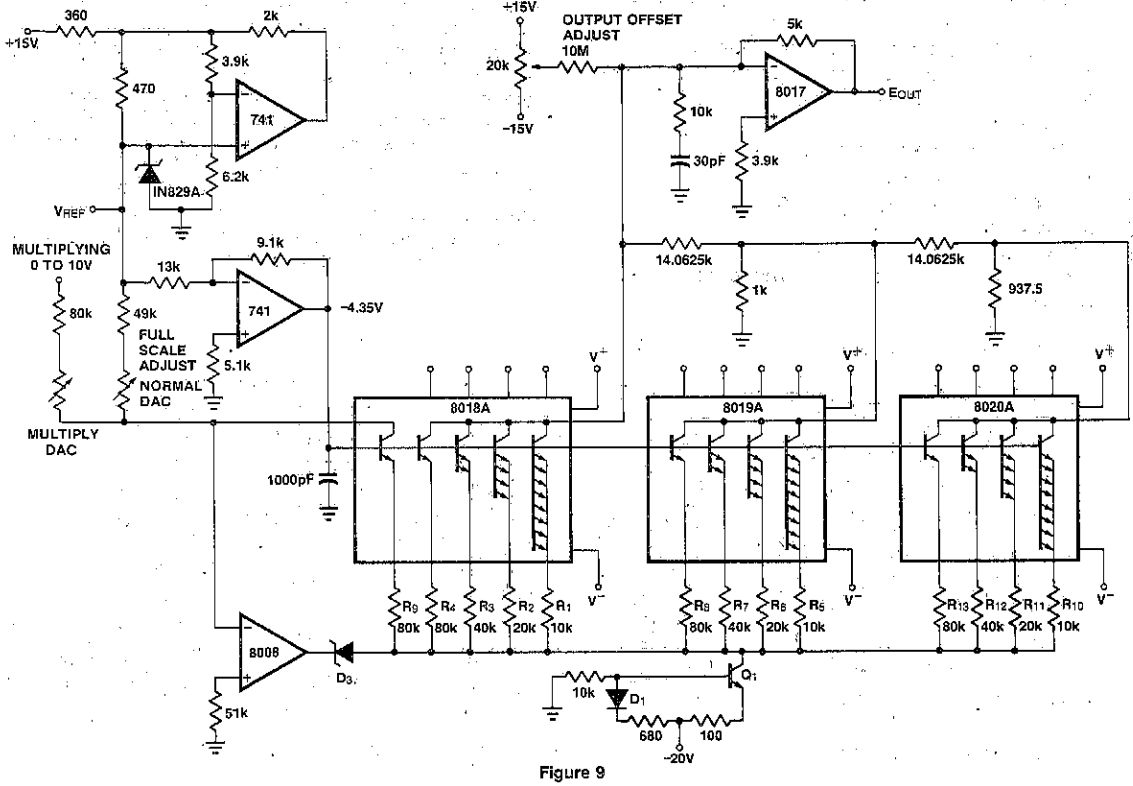


Figure 9

For further information see the following Applications Bulletins.

A016 "Selecting A/D Converters" by Dave Fullagar.
A018 "Do's and Don'ts of Applying A/D Converters" by Peter Bradshaw and Skip Osgood.
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger.

ICL8052/ICL7104 and ICL8068/ICL7104

16/14/12 Bit Binary A/D Converter Pairs for μProcessors

FEATURES

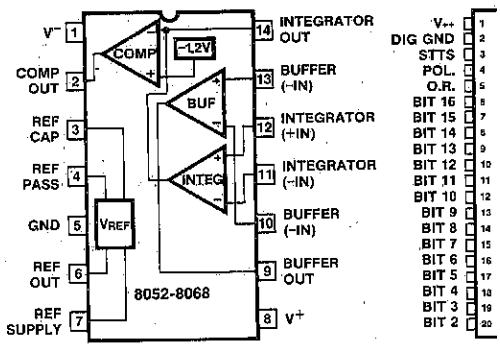
- 16 bit binary three-state latched outputs plus polarity and overrange. Also 14 and 12 bit versions.
- Ideally suited for interface to UARTs, microprocessors, or other complex circuitry.
- Conversion on demand or continuously.
- Handshake byte-serial transmission synchronously or on demand.
- Guaranteed zero reading for zero volts input.
- True polarity at zero count for precise null detection.
- Single reference voltage for true ratiometric operation.
- Onboard clock and reference.
- Auto-Zero; Auto-Polarity
- Accuracy guaranteed to 1 count.
- All outputs TTL compatible.
- ±10V analog input range
- Status signal available for external sync, A/Z in preamp, etc.

4

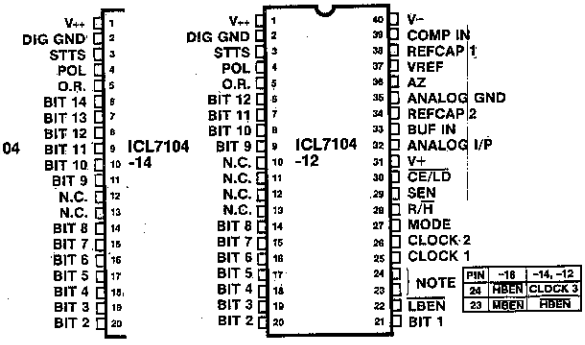
GENERAL DESCRIPTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Intersil's high performance A/D converter family. The 16-bit version, the ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for a wide range of output interfacing. The ICL7014-14 and ICL7104-12 are 14 and 12-bit versions. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc.

PIN CONFIGURATIONS



(OUTLINE DWGS DD,JD,PD)



(OUTLINE DWGS DL,JL,PL)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14-Pin Plastic DIP	ICL8052CPD
8052	0°C to 70°C	14-Pin Ceramic DIP	ICL8052CDD
8052A	0°C to 70°C	14-Pin Plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14-Pin Ceramic DIP	ICL8052ACDD
8068	0°C to 70°C	14-Pin CERDIP	ICL8068CJD
8068A	0°C to 70°C	14-Pin CERDIP	ICL8068ACJD

Part	Temp. Range	Package	Order Number
7104 12-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-12CJL
7104 12-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-12CPL
7104 12-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-12CDL
7104 14-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-14CJL
7104 14-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-14CPL
7104 14-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-14CDL
7104 16-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-16CJL
7104 16-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-16CPL
7104 16-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-16CDL

SYSTEM ELECTRICAL CHARACTERISTICS: 8068/7104

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency = 200KHz

CHARACTERISTICS	CONDITIONS	8068A/7104-12			8068A/7104-14			8068A/7104-16			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{In} = 0.0V Full Scale = 4.000V	-.000	±.000	+.000	-0.0000	±0.0000	+0.0000	-0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (1)	V_{In} = $V_{Ref.}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	−4V ≤ V_{In} ≤ +4V		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step	−4V ≤ V_{in} ≤ +4V		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{In} \cong +V_{in} \approx$ 4V		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{In} = 0V Full scale = 4.000V		3			2			2		μV
Leakage Current at Input (2)	V_{In} = 0V		200	265		100	165		100	165	pA
Zero Reading Drift	V_{in} = 0V 0° C ≤ T_A ≤ 70° C		1	5		0.5	2		0.5	2	μV/° C
Scale Factor Temperature Coefficient (3)	V_{in} = +4V 0 ≤ T_A ≤ 50° C (ext. ref. 0 ppm/° C)		2	5		2	5		2	5	ppm/° C

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SYSTEM ELECTRICAL CHARACTERISTICS: 8052/7104

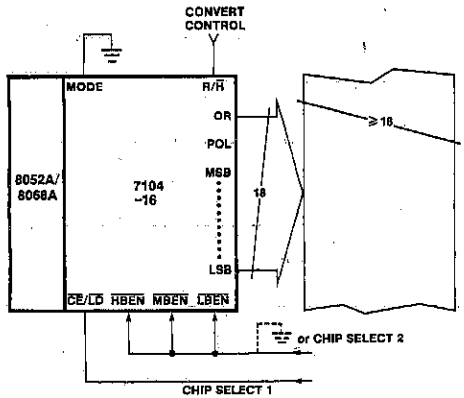
(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency = 200KHz

CHARACTERISTICS	CONDITIONS	8052/7104-12			8052A/7104-14			8052A/7104-16			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{In} = 0.0V Full Scale = 4.000V	-.000	±.000	+.000	-0.0000	±0.0000	+0.0000	-0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (3)	V_{In} = $V_{Ref.}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	−4V ≤ V_{In} ≤ +4V		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step)	−4V ≤ V_{In} ≤ +4V		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{In} \cong +V_{in} \approx$ 4V		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{In} = 0V Full scale = 4.000V		20 50			30			30		μV
Leakage Current at Input (2)	V_{In} = 0V		30	80		20	30		20	30	pA
Zero Reading Drift	V_{In} = 0V 0° ≤ T_A ≤ 70° C		1	5		0.5	2		0.5	2	μV/° C
Scale Factor Temperature Coefficient	V_{In} = +4V 0 ≤ T_A ≤ 70° C (ext. ref. 0 ppm/° C)		3	15		2	5		2	5	ppm/° C

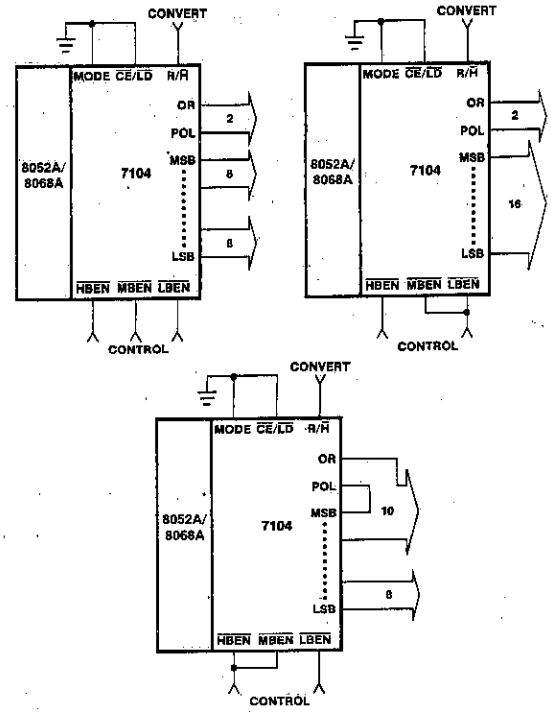
Note 1: Tested with low dielectric absorption integrating capacitor.

Note 2: The input bias currents are junction leakage currents which approximately double for every 10° C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\ Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 3: The temperature range can be extended to 70° C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.



Full 18 Bit Three State Output



Various Combinations of Byte Disables

AC CHARACTERISTICS (V++ = +15V, V+ = +5V, V− = −15V)

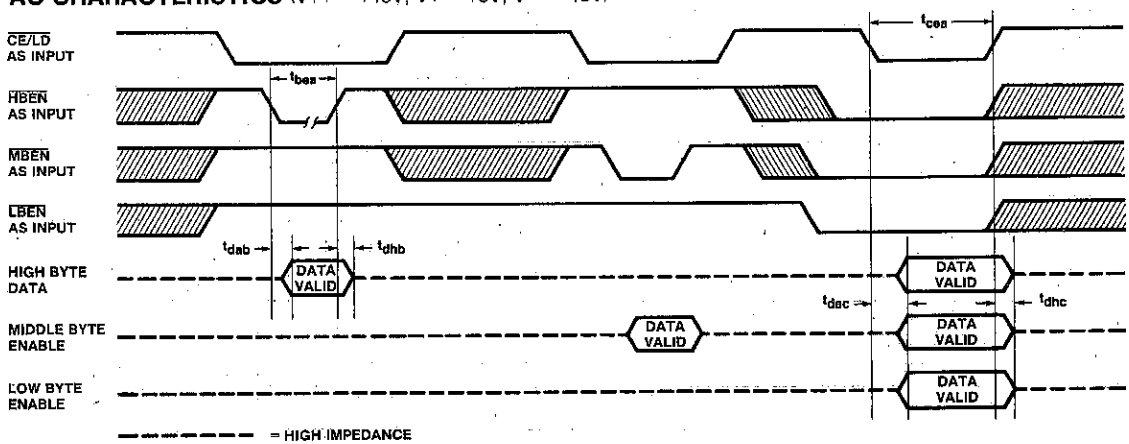


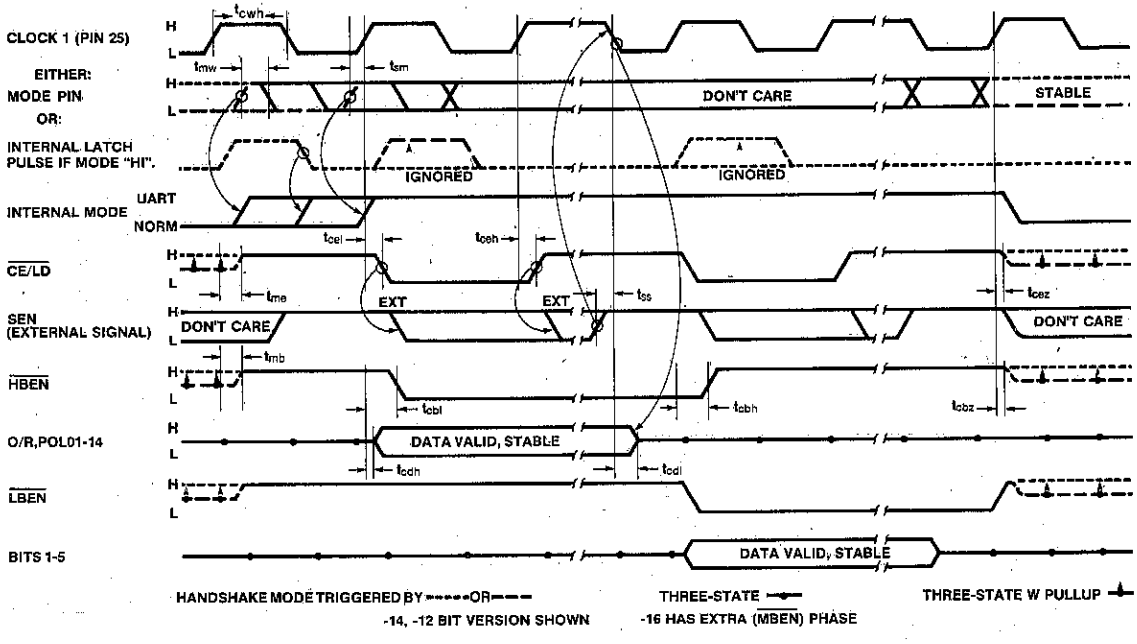
TABLE 1: Direct Mode Timing Requirements (Note: Not tested in production)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{bea}	$\overline{XBEN}$ Min. Pulse Width	400	300		ns
t_{dab}	Data Access Time from $\overline{XBEN}$		300	400	
t_{dhb}	Data Hold Time from $\overline{XBEN}$		200	250	
t_{cea}	$\overline{CE/LD}$ Min. Pulse Width	450	350		
t_{dac}	Data Access Time from $\overline{CE/LD}$		350	450	
t_{dhc}	Data Hold Time from $\overline{CE/LD}$		280	350	
t_{cwh}	CLOCK 1 High Time	1250	1000		

TABLE 2: Handshake Timing Requirements

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{mw}	MODE Pulse (minimum)		20		ns
t_{sm}	MODE pin set-up time		−150		
t_{me}	MODE pin high to low Z $\overline{CE/LD}$ high delay		200		
t_{mb}	MODE pin high to $\overline{XBEN}$ low Z (high) delay		200		
t_{cel}	CLOCK 1 high to $\overline{CE/LD}$ low delay		700		
t_{ceh}	CLOCK 1 high to $\overline{CE/LD}$ high delay		600		
t_{cbl}	CLOCK 1 high to $\overline{XBEN}$ low delay		900		
t_{cbh}	CLOCK 1 high to $\overline{XBEN}$ high delay		700		
t_{cdh}	CLOCK 1 high to data enabled delay		1100		
t_{cdl}	CLOCK 1 low to data disabled delay		1100		
t_{ss}	Send ENable set-up time		−350		
t_{cbz}	CLOCK 1 high to $\overline{XBEN}$ disabled delay		2000		
t_{cez}	CLOCK 1 high to $\overline{CE/LD}$ disabled delay		2000		
t_{cwh}	CLOCK 1 High Time	1250	1000		

4



Timing Relationships In Handshake Mode

TABLE 3: Pin Assignment and Function Description

PIN	SYMBOL	OPTION	DESCRIPTION
1	V(+)		Positive Supply Voltage Nominally +15V
2	GND		Digital Ground .0V, ground return
3	STTS		STaTuS output .HI during Integrate and Deintegrate until data is latched .LO when analog section is in Auto-Zero configuration.
4	POL		POLarity. Three-state output. HI for positive input.
5	OR		OverRange. Three-state output.
6	BIT 16 BIT 14 BIT 12	–16 –14 –12	(Most significant bit)
7	BIT 15 BIT 13 BIT 11	–16 –14 –12	Data Bits, Three-state outputs. See Table 4 for format of $\overline{\text{EN}}$ables and bytes. HIGH = true.
8	BIT 14 BIT 12 BIT 10	–16 –14 –12	
9	BIT 13 BIT 11 BIT 9	–16 –14 –12	
10	BIT 12 BIT 10 nc	–16 –14 –12	
11	BIT 11 BIT 9 nc	–16 –14 –12	
12	BIT 10 nc nc	–16 –14 –12	
13	BIT 9 nc nc	–16 –14 –12	
14	BIT 8		
15	BIT 7		
16	BIT 6		
17	BIT 5		
18	BIT 4		
19	BIT 3		
20	BIT 2		
21	BIT 1		Least significant bit
22	$\overline{\text{LBEN}}$		Low Byte $\overline{\text{EN}}$able. If not in handshake mode (see pin 27) when LO (with $\overline{\text{CE/LD}}$, pin 30) activates low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 8, 9 and 10.
23	$\overline{\text{MBEN}}$	–16	Mid Byte $\overline{\text{EN}}$able. Activates BITS 9-16, see $\overline{\text{LBEN}}$ (pin 22)
	$\overline{\text{HBEN}}$	–14 –12	High Byte $\overline{\text{EN}}$able. Activates BITS 9-14, POL, OR, see $\overline{\text{LBEN}}$ (pin 22)
24	$\overline{\text{HBEN}}$	–16	High Byte $\overline{\text{EN}}$able. Activates POL, OR, see $\overline{\text{LBEN}}$ (pin 22).
	CLOCK3	–14 –12	RC oscillator pin. Can be used as clock output.

PIN	SYMBOL	DESCRIPTION
25	CLOCK1	Clock input. External clock or oscillator.
26	CLOCK2	Clock output. Crystal or RC oscillator.
27	MODE	Input LO;Direct output mode where $\overline{\text{CE/LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ act as inputs directly controlling byte outputs. If pulsed HI causes immediate entry into handshake mode (see Figure 9). If HI, enables $\overline{\text{CE/LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ as outputs. Handshake mode will be entered and data output as in Figures 7 & 8 at conversion completion.
28	R/$\overline{\text{H}}$	Run/$\overline{\text{Hold}}$; Input HI-conversions continuously performed every 2^{17} (–16) 2^{15} (–14) or 2^{13} (–12) clock pulses. Input LO-conversion in progress completed, converter will stop in Auto-Zero 7 counts before input integrate.
29	SEN	Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates 'send'.
30	$\overline{\text{CE/LD}}$	$\overline{\text{C}}$hip-$\overline{\text{E}}$nable/$\overline{\text{L}}$oa$\overline{\text{D}}$. With MODE (pin 27) LO, $\overline{\text{CE/LD}}$ serves as a master output enable; when HI, the bit outputs and POL, OR are disabled. With MODE HI, pin serves as a $\overline{\text{L}}$oa$\overline{\text{D}}$ strobe (-ve going) used in handshake mode. See Figures 7 & 8.
31	V(+)	Positive Logic Supply Voltage. Nominally +5V.
32	AN.IN	ANalog INput. High side.
33	BUF IN	BUFfer INput to analog chip (ICL8052 or ICL8068)
34	REFCAP2	REFerence CAPacitor (negative side)
35	AN.GND.	ANalog GrouND. Input low side and reference low side.
36	A-Z	Auto-Zero node.
37	VREF	Voltage REFerence input (positive side)
38	REFCAP1	REFerence CAPacitor (positive side)
39	COMP-IN	COMParator INput from 8052/8068
40	V(–)	Negative Supply Voltage. Nominally –15V.

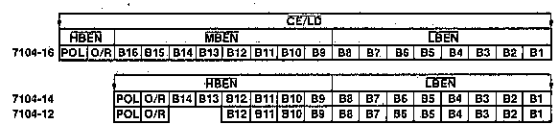


TABLE 4: Three-State Byte Formats and $\overline{\text{EN}}$able Pins.

Fig. 1 shows the functional block diagram of the operating system. For a detailed explanation, refer to fig. 2 below.

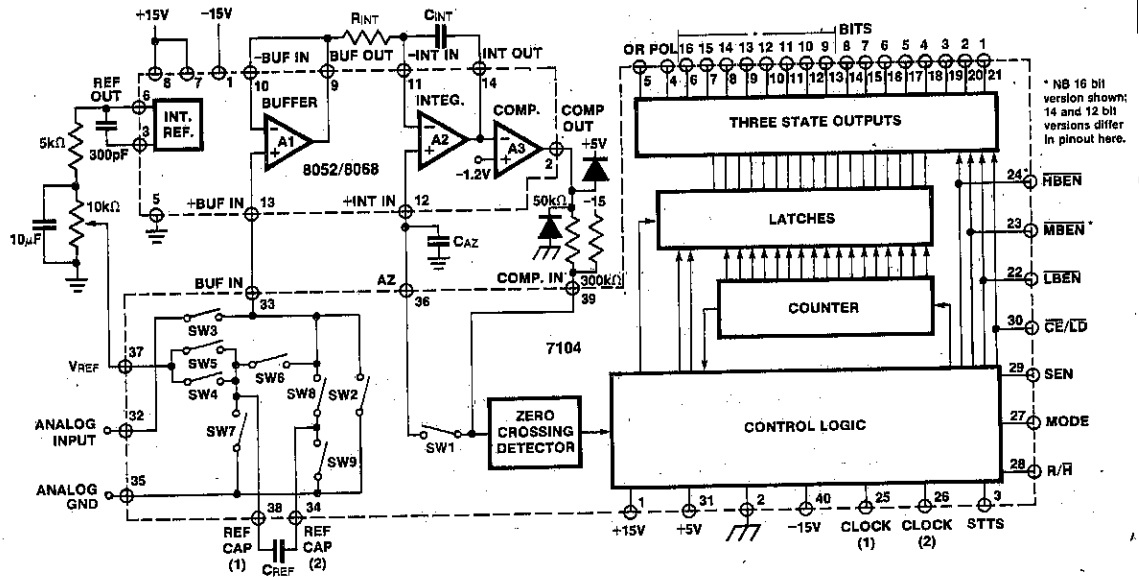


Figure 1: 8052A (8068A)/7104 16/14/12 Bit A/D Converter Functional Block Diagram

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent Circuit of the Analog Section of both the ICL7104/8052 and the ICL7104/8068 in the 3 different phases of operation. If the Run/Hold pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 131,072 for −16; 32,368 for −14; and 8092 for −12 clock periods per cycle (see Figure conversion timing).

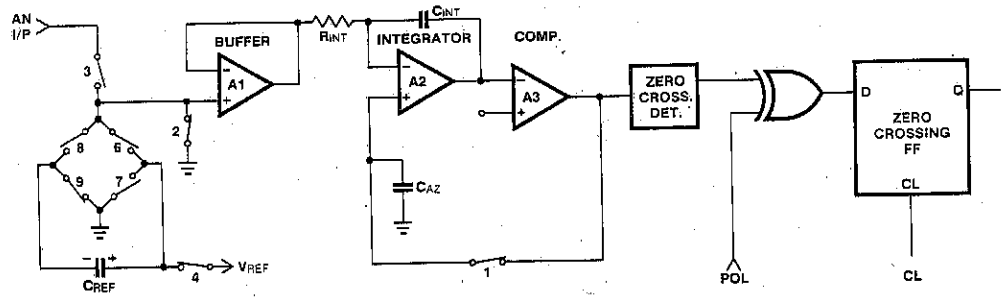


Figure 2A: Phase I Auto-Zero

1. Auto-Zero Phase I Fig. 2A

During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output no longer changes with time. Also, switches 4 and 9 recharge the reference capacitor to V_{REF}.

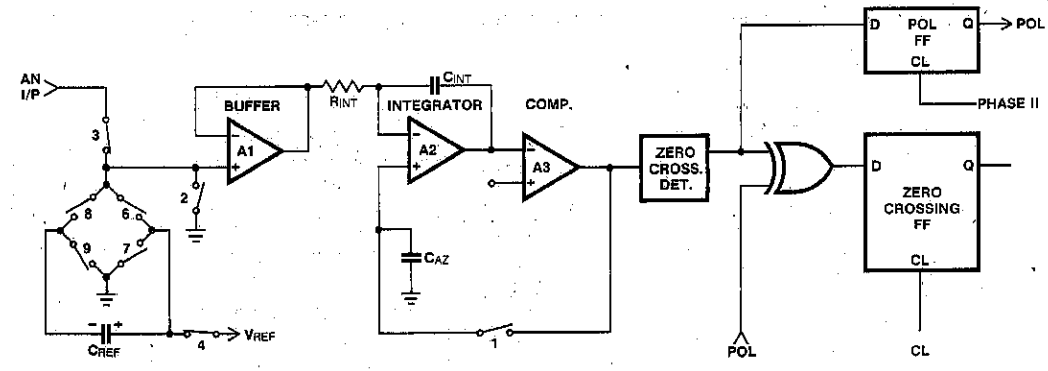


Figure 2B: Phase II Integrate Input

2. Input Integrate Phase II Fig. 2B

During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to V_{REF} during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

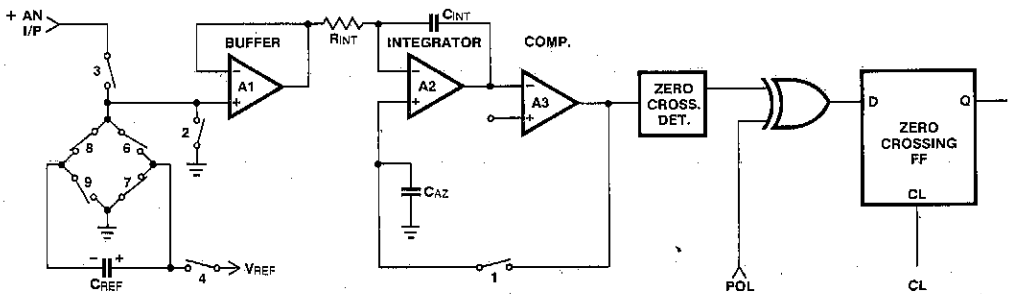


Figure 2C: Phase III + Deintegrate

Deintegrate Phase III Fig. 2C & D

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause $+V_{REF}$ to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate phase, the input voltage required to give a full scale reading = $2V_{REF}$.

Note: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/$\overline{\text{Hold}}$ is manipulated, see Run/$\overline{\text{Hold}}$ Input in detailed description, digital section).

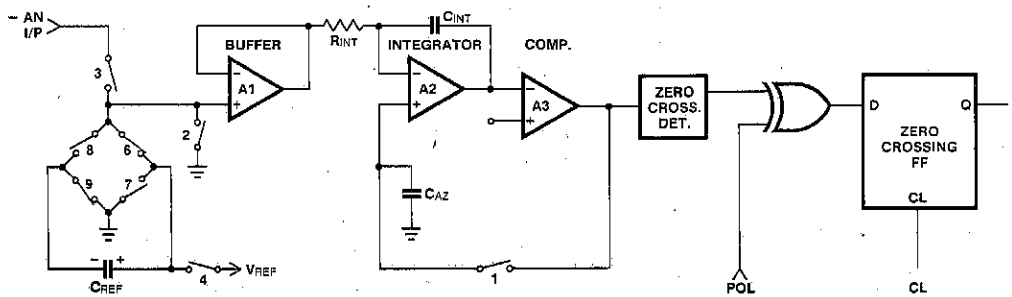


Figure 2D: Phase III - Deintegrate

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 4. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1-2μV, allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermo-electric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. For further discussion, see App. Note A030.

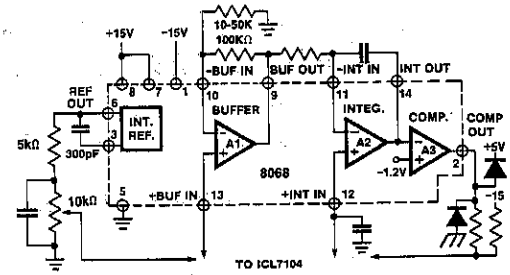


Figure 4: Adding Buffer Gain to ICL8068

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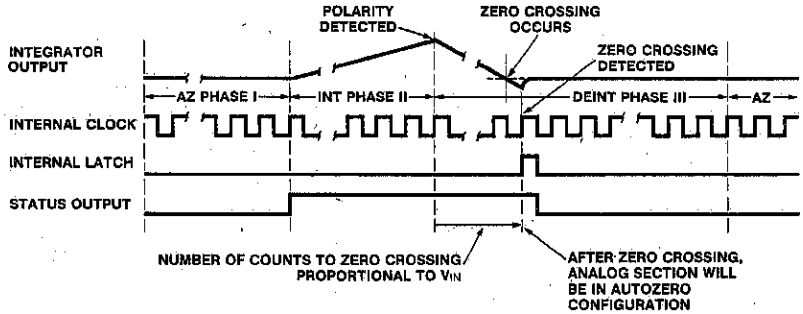
Table 5: Typical Component Values

V++ = +15V, V+ = 5V, V− = −15V, Clock Freq = 200 kHz

ICL8052/8068 with	ICL7104-16			ICL7104-14		ICL7104-12		UNITS
Full scale V_{IN}	200	800	4000	100	4000	50	4000	mV
Buffer Gain	10	1	1	10	1	10	1	
R_{INT}	100	43	200	47	180	27	200	kΩ
C_{INT}	.33	.33	.33	0.1	0.1	.022	.022	μF
C_{AZ}	1.0	1.0	1.0	1.0	1.0	.47	.47	μF
C_{ref}	10	1.0	1.0	10	1.0	4.7	4.7	μF
V_{REF}	100	400	2000	50	2000	25	200	mV
Resolution	3.1	12	61	6.1	244	12	980	μV

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and for systems where system noise is a limiting factor, particularly in low signal level conditions, will give better performance.



COUNTS			
	Phase I	Phase II	Phase III
-16	32768	32768	65536
-14	8192	8192	16384
-12	2048	2048	4096

Figure 3: Conversion Timing

4

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40 μA give good results with a nominal of 20 μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then -

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is give by

$$C_{INT} = \frac{\begin{bmatrix}\text{(32768 for -16}\\ \text{(8192 for -14 X clock period)}\\ \text{(2048 for -12}\end{bmatrix} \text{ X } (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale (100...000) and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of 1/3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator circuit, a 16, 14 or 12 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 5 (16 bit version shown).

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ICL7104 Electrical Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14 and 7104-12, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.

Run/Hold Input

When the Run/Hold input is connected to V+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16, 32768 for 7104-14 and 8192 for 7104-2 clock periods, regardless of the resulting value.

If Run/Hold goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/Hold stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/Hold input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/Hold. See Figure 6 for details.

Using the Run/Hold input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in Auto-Zero with Run/Hold low. When Run/Hold goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). Run/Hold may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/Hold can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/Hold input can be provided by connecting it to the CLOCK3 (-12, -14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

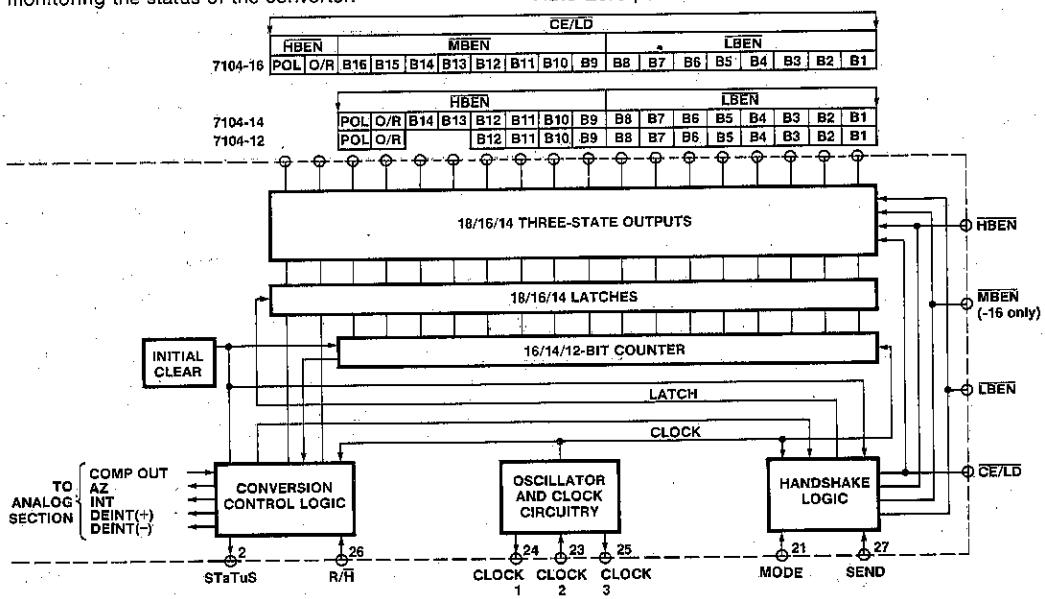


Figure 5: Digital Section

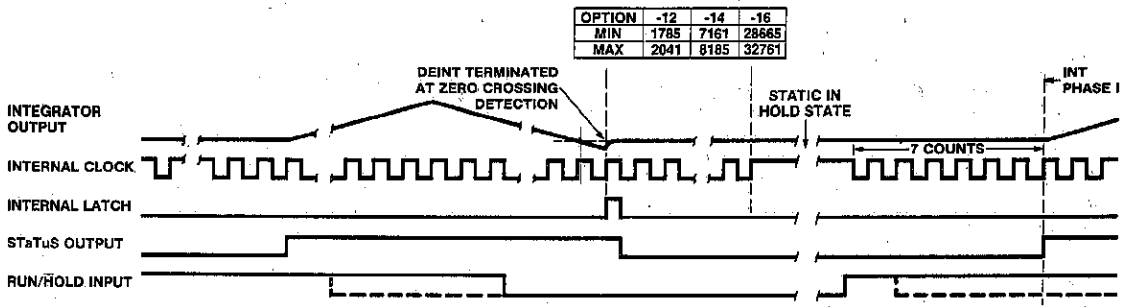


Figure 6: Run/Hold Operation

If the Run/Hold input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/Hold to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs[bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes]are accessible under control of the byte and chip ENable terminals as inputs. These $\overline{\text{EN}}$able inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip $\overline{\text{EN}}$able input is low, taking a byte $\overline{\text{EN}}$able input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used. The timing requirements for these outputs are shown under AC Characteristics and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

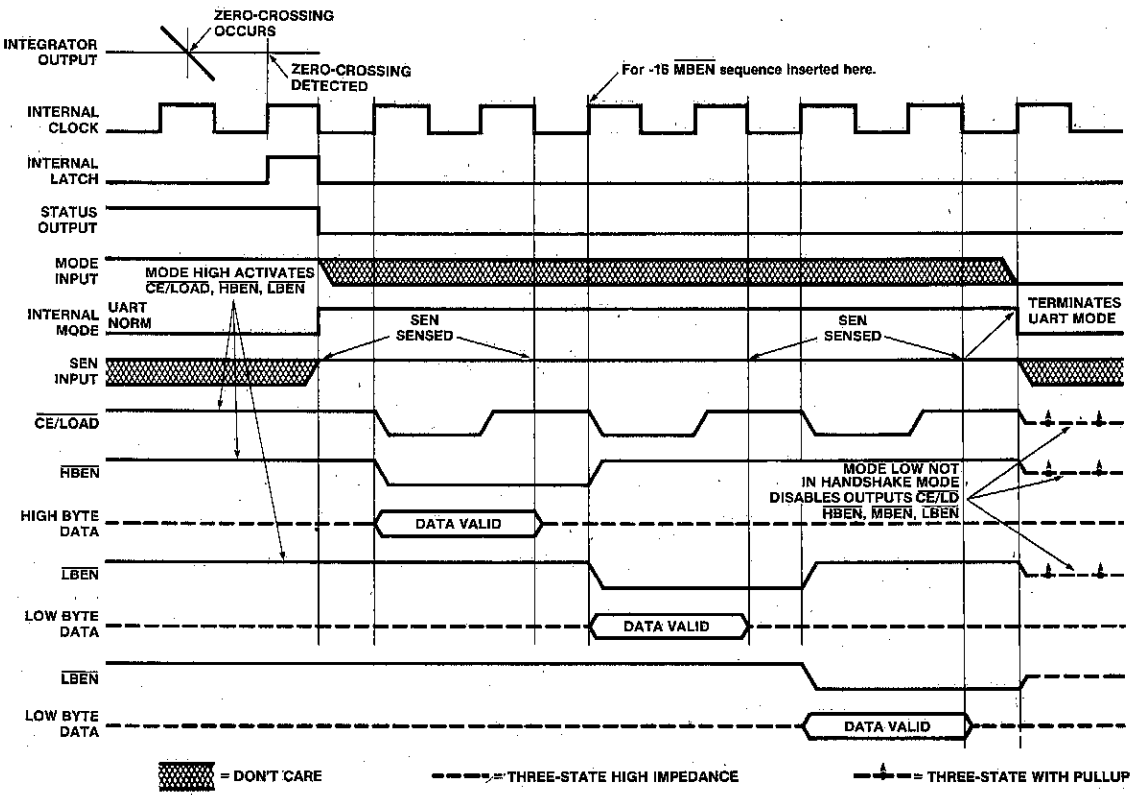


Figure 7: Handshake With SEN Held Positive

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte ENable inputs. This mode is specifically designed to allow a direct interface between the ICL7104 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7104 provides all the control and flag signals necessary to sequence the three (ICL7106-16) or two (ICL7104-14, -12) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte ENable terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send ENable pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte ENable line goes low, and the Chip ENable/LoaD line (pin 30) (CE/LD) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte ENable pin will be cleared high, and (unless finished) the CE/LD and the next byte ENable pin will go low. This will continue until all three (2 in the case of 12 and 14 bit devices) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte ENable pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip ENable will be three-stated off, if MODE is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 7, 8, and 9, and Table 2.

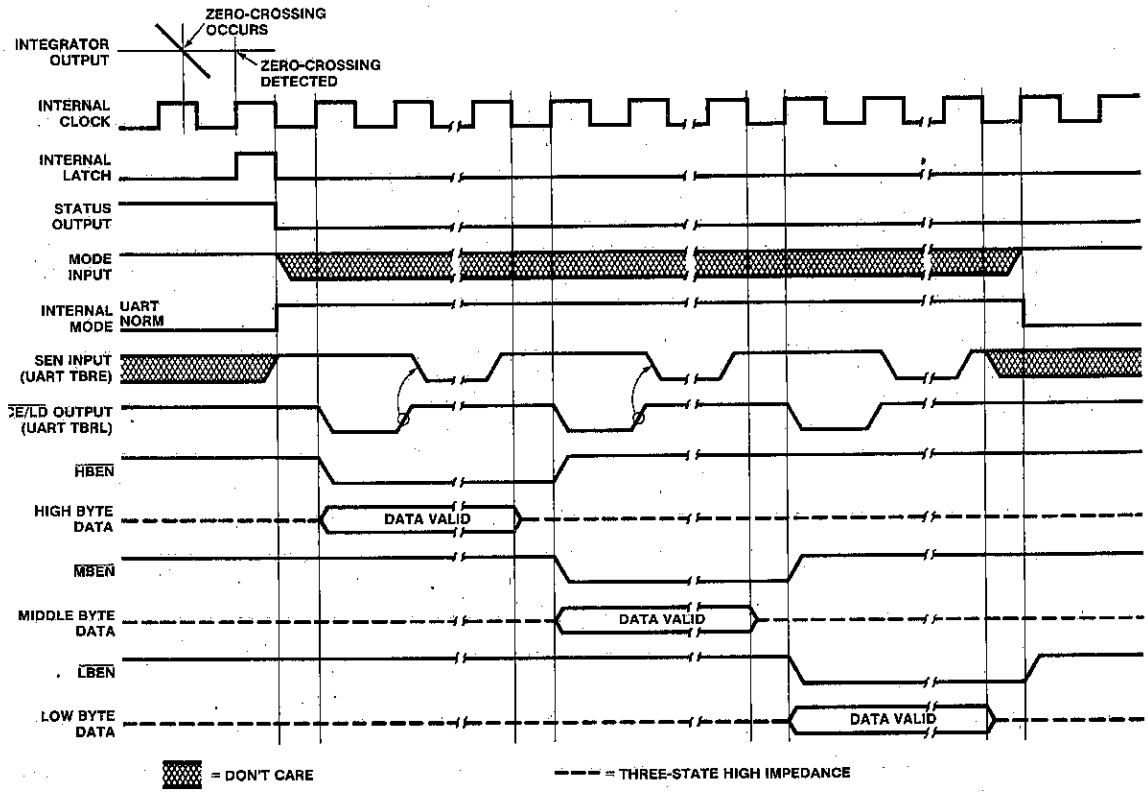


Figure 8: Handshake - Typical UART Interface Timing

Figure 7 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{CE}/\overline{LD}$, $\overline{LBEN}$, $\overline{MBEN}$ and $\overline{HBEN}$ terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{CE}/\overline{LD}$ and the $\overline{HBEN}$ outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bis 9-14) outputs are enabled. The $\overline{CE}/\overline{LD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte $\overline{EN}$able remains low for two clock periods. Thus the $\overline{CE}/\overline{LD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte $\overline{EN}$able as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using $\overline{CE}/\overline{LD}$, $\overline{MBEN}$ and $\overline{LBEN}$ while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14, -12).

Figure 8 shows an output sequence where the SENinput is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}/\overline{LD}$ terminal of the ICL7104 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The $\overline{CE}/\overline{LD}$ and $\overline{HBEN}$ terminals will go low after SEN is sensed, and the high order byte outputs become active. When $\overline{CE}/\overline{LD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE}/\overline{LD}$ and $\overline{MBEN}$ (-16) or $\overline{LBEN}$ outputs go low, and the corresponding byte outputs become active. Similarly, when the $\overline{CE}/\overline{LD}$ returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for $\overline{LBEN}$. One-half internal clock later, the handshake mode will be cleared, and the chip and byte $\overline{EN}$able terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion

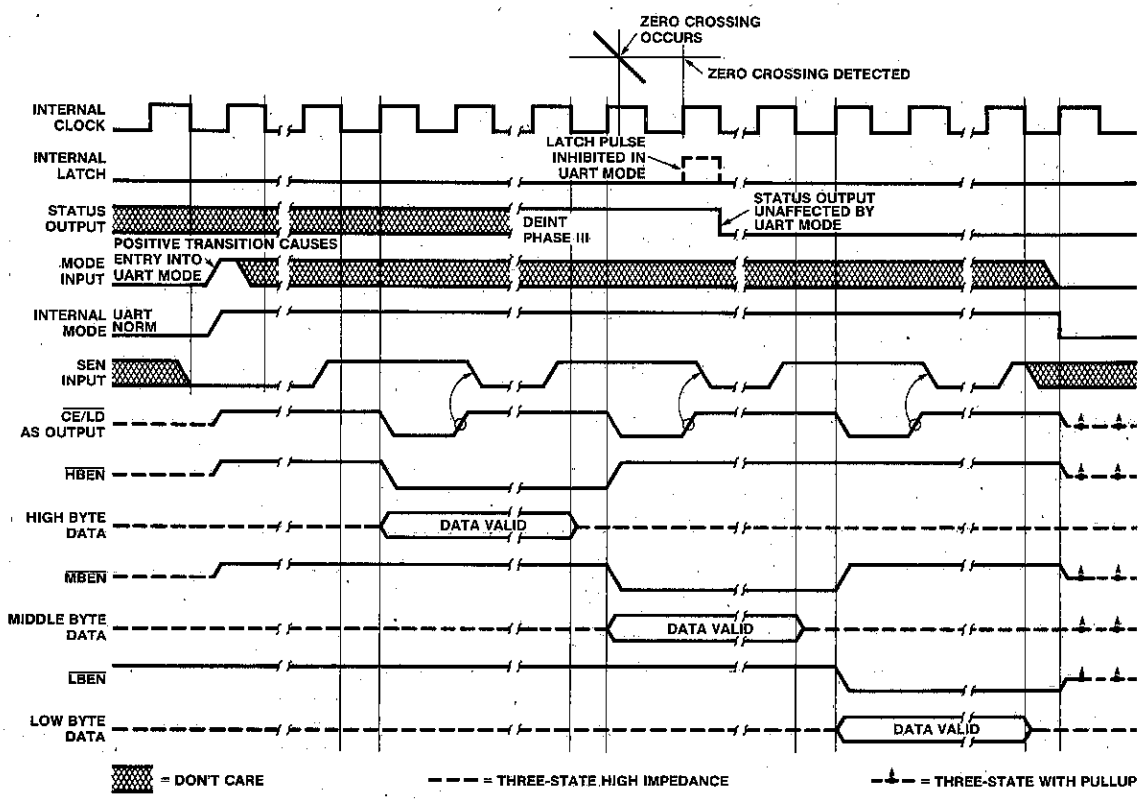


Figure 9: Handshake Triggered By Mode

except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 11 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/Hold input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Initial Clear Circuitry

The internal logic of the 7104 is supplied by an internal regulator between V++ and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" FF cleared (i.e. in "direct" mode). This, however, will also clear these registers if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" FF should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to buss conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE FF will be cleared as fast as possible (see Fig. 7 for timing). For these and other reasons, adequate supply bypass is recommended.

Oscillator

The ICL7104-14 and -12 are provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator.

Figure 10 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by f = .45/RC. A 50-100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 32768 (-16), 8192 (-14), 2048 (-12) clock periods is close to an integral multiple of the 60Hz period.

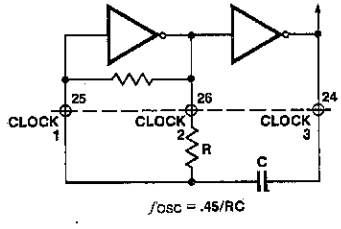


Figure 10: RC Oscillator

Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 11 shows a crystal oscillator circuit, which can be used with all 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.

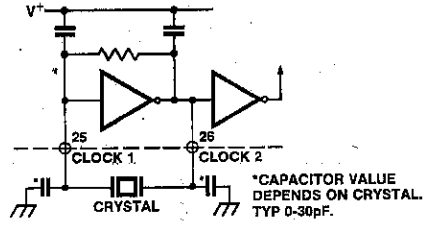


Figure 11: Crystal Oscillator

POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the ICL7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V+ supply (nom. +5V) being more positive than the V++ supply. If there is any possibility of this occuring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V+ and V++ to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of 8068 or 8052/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 12.

APPLICATIONS INFORMATION

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar
A017 "The Integrating A/D Converter", by Lee Evans
A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood
A025 "Building a Remote Data Logging Station", by Peter Bradshaw
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

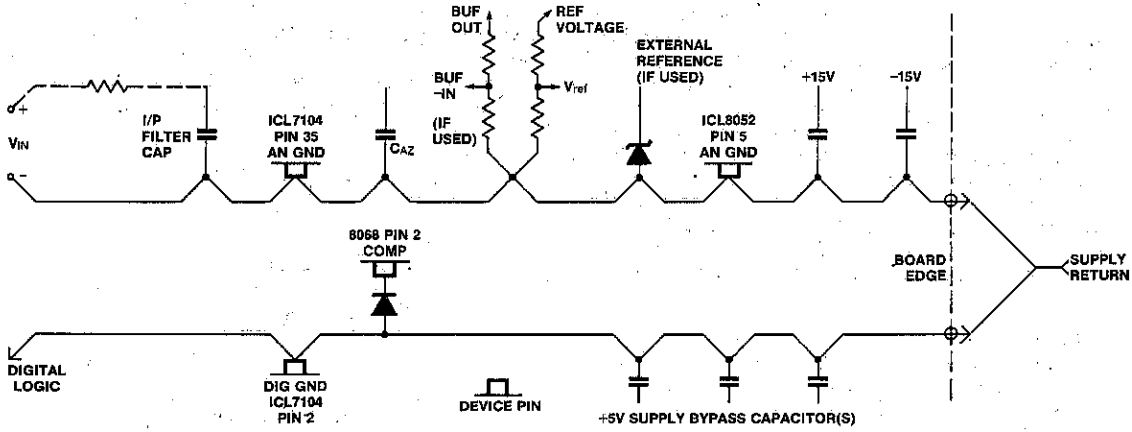


Figure 12: Grounding Sequence

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