HMC701LP6CE

8 GHz 16-Bit Fractional-N Synthesizer

Features

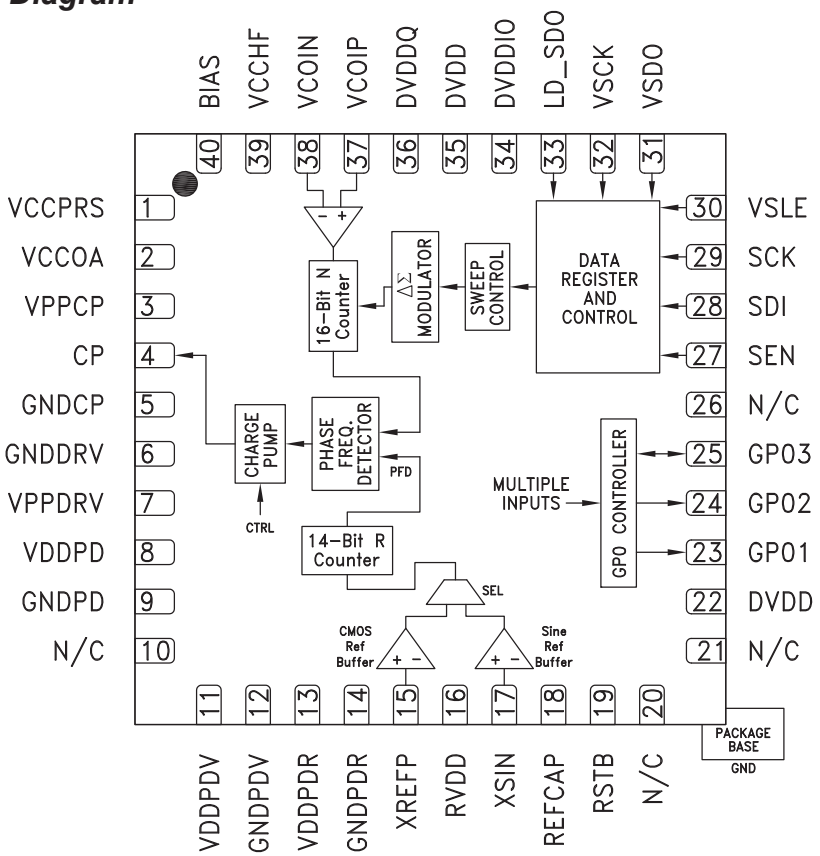
- Fractional or Integer Modes
- 8 GHz, 16-Bit RF N-Counter
- 24-Bit Step Size Resolution, 3 Hz typ
- Ultra Low Phase Noise 6 GHz, 50 MHz Ref. -103 / -110 dBc/Hz @ 20 kHz (Frac / Integer)
- Reference Path Input: 200 MHz
- 14-Bit Reference Path Divider
- Low Fractional Spurious
- Reference spurs: -90 dBc typ
- Auto and Triggered Sweeper Functions
- Cycle Slip Prevention (CSP) for fast settling
- Autotune support for external step tuned VCOs
- Multi-VCO Support
- Auxiliary Clock Source
- 40 Lead 6x6mm SMT Package: 36mm²

Typical Applications

- Base Stations for Mobile Radio (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANs, WiMax
- Communications Test Equipment
- CATV Equipment
- FMCW Sensors
- Automotive Radar
- Phased-Array Systems

Functional Diagram

(Figure 1.)



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8 GHz 16-Bit Fractional-N Synthesizer

General Description

The HMC701LP6CE is a SiGe BiCMOS fractional-N frequency synthesizer. The synthesizer includes a 8GHz 16-bit RF N-Divider, a 24-bit delta-sigma modulator, a very low noise digital phase frequency detector (PFD), and a precision controlled charge pump. In addition the synthesizer supports an external step tuned VCO.

The fractional synthesizer features an advanced delta-sigma modulator design that allows ultra-fine frequency step sizes. The synthesizer features the ability to alter both the phase-frequency detector (PFD) gain and the cycle slipping characteristics of the PFD. This feature can reduce the time to arrive at the new frequency by 50% vs. conventional PFDs. Ultra low in-close phase noise also allows wider loop bandwidths for faster frequency hopping.

The synthesizer contains a built-in linear sweeper function, which allows it to perform frequency chirps with a wide variety of sweep times, polarities and dwells, all with an external or automatic sweep trigger.

A General Purpose Output (GPO) bus supports the use of multiple VCOs. In addition the synthesizer has a number of auxiliary clock generation modes that can be accessed via the GPO.

Electrical Specifications, T_A = +25°C

VCCHF = VCCPRS = RVDD = +3.3V
VPPCP = VCCOA = VDDPDR = VPPDRV = VDDPD = VDDPDV = +5V
DVDD = DVDDIO = DVDDQ = +3.3V
GNDDRV = GNDCP = GNDPD = GNDPDV = GNDPDR = 0V

Table 1. Electrical Specifications

Parameter	Conditions / Notes	Min	Typ	Max	Units
Prescaler Characteristics					
Max RF Input Frequency (3.3V)		8	9		GHz
Max RF Input Frequency (2.7 - 3.3V)		7	8		GHz
Min RF Input Frequency				0.1	MHz
RF Input Power		-10	-6	10	dBm
16-bit N-Divider Range (Integer)		32		65,535	
16-bit N-Divider Range (Fractional)	Fraction Nominal Divide ratio varies (-3 / +4) dynamically max	35		65,531	
REF Input Characteristics					
Max Ref Input Frequency (pin XREFP)		180	200		MHz
Max Ref Input Frequency (pin XSIN)		200	220		MHz
Max Ref Frequency with AutoCal			60		MHz
Min Ref Input Frequency			100		kHz
Ref Input Voltage Range (pin XREFP)	AC Coupled	750	1000	3300	mVpp
Ref Input Power Range (pin XSIN)	50 Ω Source	-6	0	12	dBm
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	

Table 1. Electrical Specifications (Continued)

Parameter	Conditions / Notes	Min	Typ	Max	Units
Phase Detector					
Fractional Mode					
Max Phase Detector Frequency		70	75		MHz
Min Phase Detector Frequency				100	kHz
Integer Mode					
Max Phase Detector Frequency		110	150		MHz
Min Phase Detector Frequency				100	kHz
Charge Pump					
Max Output Current			4		mA
Min Output Current			125		µA
Charge Pump Gain Step Size (5-bits)			125		µA
Charge Pump Trim Step Size (3-bits)			14		µA
Charge Pump Offset Step Size (4-bits)			29		µA
PFD / Charge Pump Noise (Integer)	6 GHz, 50 MHz Ref, Input referred				
1 kHz			-141		dBc/Hz
10 kHz			-149		dBc/Hz
100 kHz			-155		dBc/Hz
Compliance Voltage	Less than 3 dB degradation typ. at these limits				
	-406 µA Offset	0.4		VPPCP-0.8	V
	-406 µA Offset	0.8		VPPCP-0.4	V
Logic Inputs					
VIH Input High Voltage		VDDIO-0.4			V
VIL Input Low Voltage				0.4	V
Logic Outputs					
VIH Output High Voltage		VDDIO-0.1			V
VIL Output Low Voltage				0.1	V
Power Supply Voltages					
VCC - Analog 3V Supplies	VCCPRS, RVDD, VCCHF	3	3.3	3.45	V
DVDD - Digital Internal Supply	DVDD, DVDDQ	3	3.3	3.45	V
DVDDIO - Digital I/o Supply	DVDDIO	1.8	3.3	5.5	V
Analog 5V Supplies	VCCOA, VPPCP, VPPDRV, VDDPD, VDDPDV, VDDPDR	4.5	5.0	5.5	V
Power Supply Current (6 GHz Fractional Mode, 50 MHz PFD)					
Analog +5V	VCCOA, VPPCP, VPPDRV, VDDPD, VDDPDV, VDDPDR		37		mA
Analog +3.3V	VCCPRS, RVDD, VCCHF		71		mA
Digital +3.3V	DVDD, DVDDIO, DVDDQ		19		mA
Power Down - Crystal Off	Reg 01h = 0 Crystal not clocked		6		µA
Power Down - Crystal On, 100 MHz	Reg 01h = 0 Crystal clocked 100 MHz		20	200	µA

Table 1. Electrical Specifications (Continued)

Parameter	Conditions / Notes	Min	Typ	Max	Units
Temperature Sensor (3-bit)					
Min Temperature	Readout: 000		-32		°C
Max Temperature	Readout: 111		+82		°C
Temp Change / LSB			17.5		°C/LSB
Worst Case Absolute Temp Error			±10		°C
Current Consumption (when Enabled)			2		mA
Power on Reset					
Typical Reset Voltage on DVDD			700		mV
Min DVDD Voltage for No Reset		1.5			V
Closed Loop Phase Noise					
6 GHz VCO, Integer, 50 MHz PFD	1 kHz offset		-98		dBc/Hz
6 GHz VCO, Integer, 50 MHz PFD	10 kHz offset		-108		dBc/Hz
6 GHz VCO, Integer, 50 MHz PFD	100 kHz offset		-110		dBc/Hz
6 GHz VCO, Fractional, 50 MHz PFD	1 kHz offset		-93		dBc/Hz
6 GHz VCO, Fractional, 50 MHz PFD	10 kHz offset		-103		dBc/Hz
6 GHz VCO, Fractional, 50 MHz PFD	100 kHz offset		-105		dBc/Hz
Closed Loop Phase Noise	Normalized to 1 Hz				
Integer Mode	Measured with 50 MHz PFD		-227		dBc/Hz
Fractional Mode	Measured with 50 MHz PFD		-221		dBc/Hz

Table 2. Absolute Maximum Ratings

Parameter	Rating
RVDD, VCCHF, DVDD, DVDDQ, VCCPRS	-0.3 to +3.6V
VCCOA, VPPCP, VPPDRV, VDDPD, VDDPDV, VDDPDR, DVDDIO	-0.3 to +6V
Operating Temperature	-40 to +85 °C
Storage Temperature	-65 to +120 °C
Maximum Junction Temperature	+150 °C
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Pin Description

Pin No.	Pin Name	PIn Type	Description
1	VCCPRS	Supply	RF Prescaler Power Supply. Nominally +3.3V
2	VCCOA	Supply	ChargePump OpAmp Power Supply. Nominally +5V
3	VPPCP	Supply	Power Supply for Charge Pump. Nominally +5V
4	CP	Analog O/P	Charge Pump output
5	GNDCP	GND	Power Supply GND for Charge Pump
6	GNDDRV	GND	Charge Pump GND
7	VPPDRV	Supply	Power supply for Charge Pump, Nominally +5V
8	VDDPD	Supply	Power Supply for Phase Detectors, Nominally +5V
9	GNDPD	GND	Power Supply GND for Phase Detector
10, 20, 21, 26	N/C	N/C	No Connection
11	VDDPDV	Supply	Power Supply for Phase Detector VCO Path, Nominally +5V
12	GNDPDV	GND	Power Supply GND for Phase Detector VCO Path
13	VDDPDR	Supply	Power Supply for Phase Detector Ref Path, Nominally +5V
14	GNDPDR	GND	Power Supply GND for Phase Detector Ref Path
15	XREFP	Analog I/P	Square Wave Crystal Ref Input
16	RVDD	Supply	Power Supply for Ref Path, Nominally +3.3V
17	XSIN	Analog I/P	Sinusoidal Crystal reference input
18	REFCAP	Analog I/O	Reference Path bypass
19	RSTB	CMOS I/P	Reset Input (active low)
22	DVDD	Supply	Digital Power Supply, Nominally +3.3V
23	GPO1	DO	General Purpose Output 1 with Tristate
24	GPO2	DO	General Purpose Output 2 with Tristate
25	GPO3	DIO	General Purpose Input/Output with Tristate may be configured for External Ramp trigger Input. See register REG 14h[5]
27	SEN	CMOS I/P	Main Serial port enable input
28	SDI	CMOS I/P	Main Serial port data input
29	SCK	CMOS I/P	Main Serial port clock input
30	VSLE	CMOS O/P	VCO Serial port enable output
31	VSDO	CMOS O/P	VCO Serial port data output
32	VSCK	CMOS O/P	VCO Serial port clock output
33	LD_SDO	CMOS O/P	Lock Detect or Main Serial Port Data Output
34	DVDDIO	Supply	Power Supply for digital I/O, matches external Digital Supply in 1.8V to 5.5V range
35	DVDD	Supply	Internal Digital Power Supply. Nominally 3.3V
36	DVDDQ	Supply	Power Supply Isolation pin. Nominally 3.3V, bypassed to GND, zero current.
37	VCOIP	RF I/P	Complementary Input to the RF Prescaler. If single ended input, this point must be decoupled to the ground plane with a ceramic bypass capacitor, typically 100 pF
38	VCOIN	RF I/P	Input to the RF Prescaler. This signal input is ac-coupled to the external VCO
39	VCCHF	Supply	RF Section Power Supply. Nominally 3.3V
40	BIAS	Analog I/P	Decoupling Pin for RF section, nominally external 1nF bypassed to VCCHF

Figure 2.

Typical Phase Noise - Integer Mode

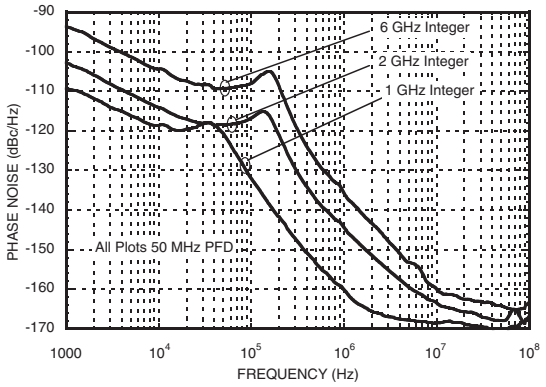


Figure 3.

Typical Phase Noise - Fractional Mode

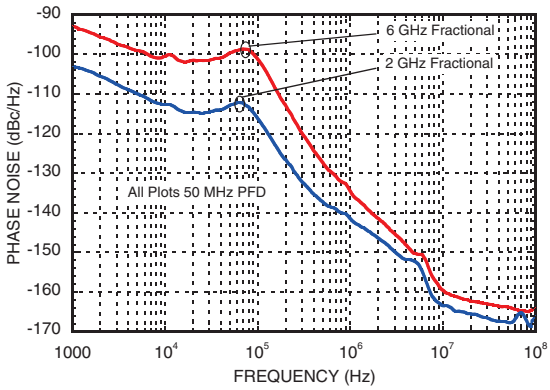


Figure 4.

RF Divider Sensitivity

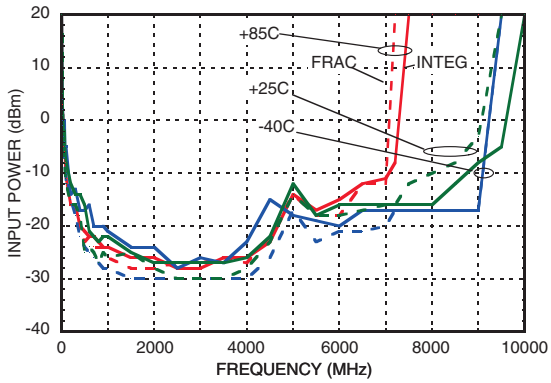


Figure 5.

Frequency Sweep

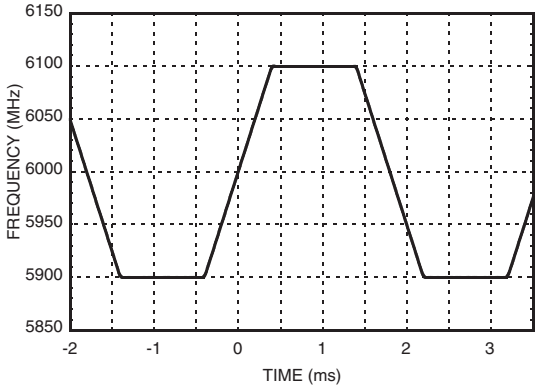
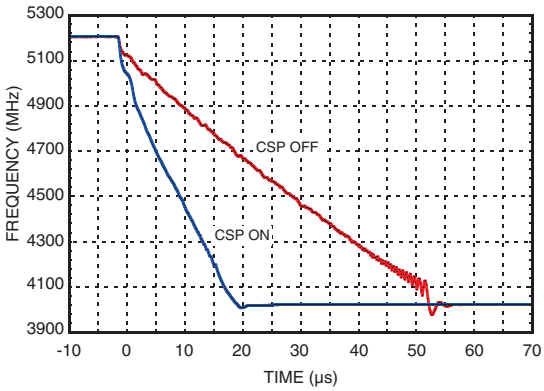


Figure 6.

Cycle Slip Prevention: Frequency Hop from 5200 MHz to 3950 MHz



Theory of Operation

The HMC701LP6CE synthesizer consists of the following functional blocks

1. Reference Path Input Buffers
2. Reference Path Divider
3. VCO Path Input Buffer
4. VCO Path Multi-Modulus Prescaler/Divider
5. ΔΣ Fractional Modulator
6. Phase Frequency Detector
7. Charge Pump
8. Main Serial Port
9. VCO Serial Port for Stepped VCO Support
10. Temperature Sensor
11. Power On Reset Circuit
12. VCO Autocalibration Subsystem
13. CW Sweeper Subsystem
14. Auxiliary Clock Generator
15. General Purpose Output (GPO) Bus
16. Multiple VCO Controller

Each of these blocks is described briefly in the following section.

Reference Path

The full Reference Path block diagram is shown in Figure 7. The ultra low noise phase detector requires the best possible reference signal. Since a given application may desire to use a square wave or a 50 Ohm sinusoidal crystal source, HMC701LP6CE offers two input ports, each one optimized for the lowest possible noise for the source type being used.

For absolute best low noise performance, the sine wave path should be used.

The user should use only one Ref path input, that is the input that matches their reference source type. Note the input is defaulted to the square wave input on power up. Should the sine reference path be used, it is necessary to enable the sine input, shut down the square wave input and set the mux (*rfp_buf_sin_en=1, rfp_buf_sq_en=0, rfp_buf_sin_sel=1*, Table 12). The unused port should be left open.

The reference path supports input frequencies of up to 200 MHz typical, however the maximum frequency at the phase detector (PFD) depends upon the mode of operation, worst case at +85°C, 70 MHz in fractional mode and 110 MHz in integer mode. Hence reference inputs of greater than the PFD maximum frequency must use the appropriate R divider setting. A further restriction exists. If the VCO auto calibration feature is used, the reference input must not exceed 60 MHz.

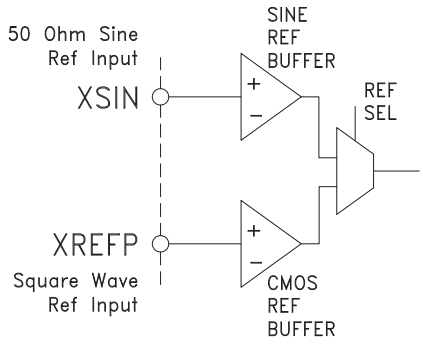


Figure 7. Reference Sine Input Stages

The unused reference port is normally not connected.

Sine Reference Input

The crystal reference sine input stage is shown in Figure 8. This is the lowest noise reference path. This is a common emitter single ended bipolar buffer. The XSIN input pin is DC coupled and has about 950 mV bias on it. Expected input is a 0 dBm sinusoid from a 50 Ohm source. Normally the input should be AC coupled externally. The sine buffer input impedance is dominated by a 25 Ohm shunt resistor in series with a 50 pF on chip cap. Should a lower input impedance be needed, an external 50 Ohm shunt resistor can be used, DC isolated by an external bypass cap. The sine input reference path phase noise floor is approximately equivalent to -159 dBc/Hz. For best performance care should be taken to provide a crystal reference source with equivalent or better phase noise floor.

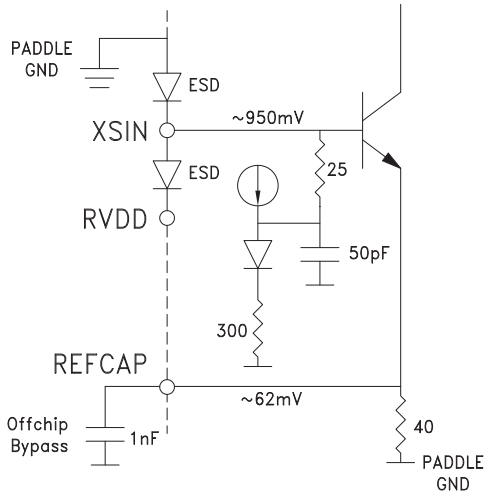


Figure 8. Ref Sine Input

Square Wave Reference Input

The square wave Ref Input stage is shown in Figure 9. The stage is designed to accept square wave inputs from CML to CMOS levels. Slightly degraded phase noise performance may be obtained with quasi sine 1 Vpp inputs. It may be necessary to attenuate very large CMOS levels if absolute best in close phase noise performance is required. Input reference should have a noise floor better than -160 dBc/Hz to avoid degradation of the input reference path.

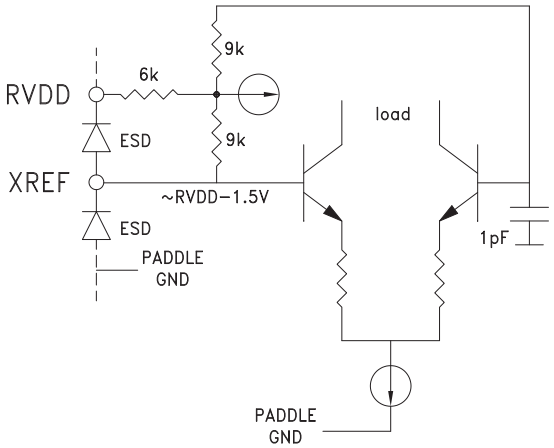


Figure 9. Square Wave Ref Input Stage

Reference Path 'R' Divider

The referenced path features a 14-bit divider (*rfp_div_ratio, Reg03h<13:0>* Table 14) and can divide input signals at up to 200 MHz by numbers from 1 to 16,383. The selected input reference source may be divided or bypassed (*rfp_div_select*), and applied to the phase detector reference input.

VCO Auto Tuning and Serial Port Clocks

The optional VCO Auto Tuning state machine and the VCO Serial Port clocks use the undivided selected external reference signal, as determined by *rfp_xref_sin_select Reg12h<6>* (Table 29), and as shown in Figure 10.

Reference Path Test Features

A fractional synthesizer is a complex combination of a low phase noise analog oscillator running in close proximity with a nearly randomly modulated delta-sigma digital modulator.

Clean spur free operation of the synthesizer requires proper board layout of power and grounds. Spurious sources are often difficult to identify and may be related to harmonics of the digital modulation which land near the operating frequency of the VCO, or they may arise from repeating patterns in the digital modulation itself . The loop filter and the fractional modulator are designed to suppress these fractional spurs, but it is sometimes the case that the isolation of the spurious products comes from layout issues. The problem is how to identify the sources of spurious products if they occur?

The reference path of the HMC701LP6CE features some interesting test options for clocking the digital portion of the synthesizer which may provide for a better understanding of the source of reference spurs should they occur. See Figure 10, Table 12 and Table 29 for more register details.

It is possible for example to set the synthesizer to integer mode of operation, where the digital harmonics normally fall directly on the VCO frequency. We might chose for example to use the sine source (*rfp_buf_sine_sel=1, div_todig_en=0*) to drive the reference divider. In such a case the delta sigma modulator is not normally used, however if we wish to test the effects of the digital power supply isolation, we could input a 2nd reference source on the square wave input, enable its buffer (*rfp_buf_sq_en=1*), and enable the 2nd crystal to clock the unused delta sigma modulator (*sqr_todig_en=1* and *dsm_xref_sin_select=0*). This would allow the square wave clock to be set independently of the locked integer mode VCO, and hence measure the coupling of the digital to the sidebands of the VCO at various frequencies. Such a test can help in identifying and debugging grounding and layout issues in the application circuit related to the digital portion of the PCB should they occur. In general it is recommended to follow the suggested layout closely to avoid any such problems.

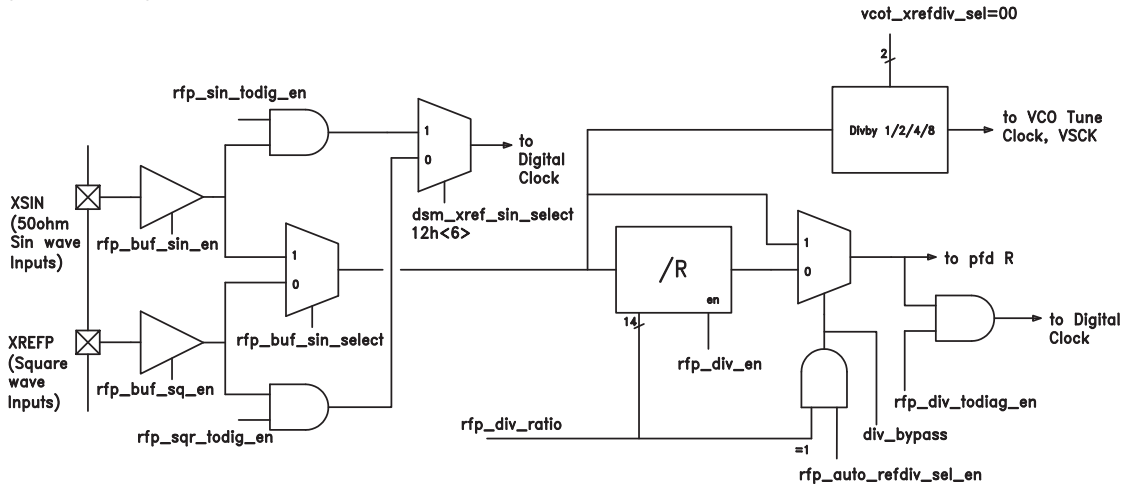


Figure 10. Reference Path Block Diagram

VCO Path

The RF path from the VCO to the phase detector, is referred to as the VCO path. The VCO path consists of an input isolation buffer and a multi-modulus prescaler, or simply the N divider. The N divider is controlled by the fractional modulator. This path operates with inputs directly from the external VCO.

RF Input Stage

The synthesizer RF input stage routes the external VCO to the phase detector via a 16-bit fractional divider. The RF input path is rated to operate nominally from 100 kHz to 8 GHz in fractional and 9 GHz in integer modes. The RF input stage also provides isolation between the VCO and the prescaler. The RF input stage is a differential common emitter stage, DC coupled for maximum flexibility. The input is protected by ESD diodes as shown in Figure 11. Normally the RF input is AC coupled to a single ended external source. The RFINP buffer is well matched from a single ended 50 Ohm source above about 3.5 GHz, with the complimentary input grounded. If a better match is required at low frequency a simple shunt 50 Ohm resistor can be used external to the package. If a differential external source is used then the two input pins may be used for best performance.

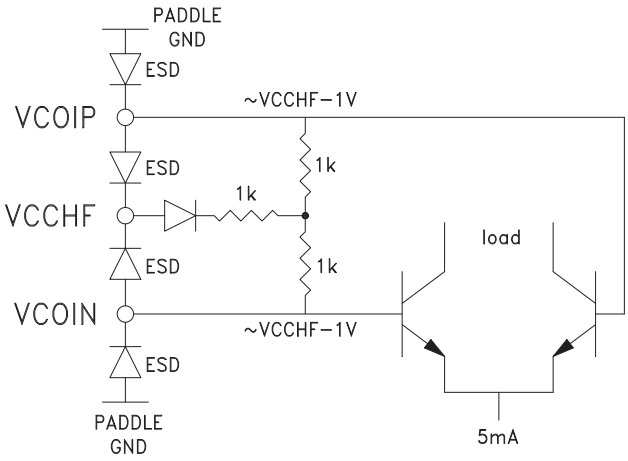


Figure 11. RF Input Stage

RF Path 'N' Divider

The main RF path divider is capable of average divide ratios between 65,531 and 36 in fractional mode, and 65,535 to 32 in integer mode. The reason for the difference between integer and fractional modes is that the fractional divider actually divides by up to ±4 from the average divide number. Actual division ratios when used with a given VCO will depend upon the reference frequency used and the desired output band.

General Purpose Output (GPO) Interface

The HMC701LP6CE features a 3-wire General Purpose Output (GPO) interface. GPO registers are described in *Reg1Bh* Table 37. The GPO is a flexible interface that supports a number of different functions and real time waveform access including:

a. General Data Output from SPI register gpo_sel_0_ data *(gpo_sel=0)*

b. Prescaler & reference path outputs *(gpo_sel=1)*

c. Lock Detect Windows *(gpo_sel=2)*

d. Anti-cycle Slip waveforms *(gpo_sel=3)*

e. Internal synchronized frac strobe with clocks *(gposel=4)*

f. Mirror of VCO Serial Port Data, Clock, Latch Enable *(gposel=5)*

g. ΔΣ Modulator Phase Accumulator *(gposel=6)*

h. Auxiliary oscillators *(gposel=7)*

i. Auto Calibration Busy Flag *(gposel=8)*

j. Multiple VCO Control, Latch Enables *(gposel=9)*

k. ΔΣ Modulator Outputs *(gposel=10)*

General Data to GPO *(gpo_sel=0)*

Setting register *gpo_sel=0 in* Table 37 assigns the 3-bit data from register *gpo_sel_0_data Reg1B<6:4>* to the GPO bus.

Prescaler and Reference Path Outputs *(gpo_sel = 1)*

Setting register *gpo_sel=1* (*Reg1B<3:0>* Table 37) results in the input crystal being buffered out to GPO3 as shown in Figure 12. This is useful for example to generate a copy of the input crystal signal to drive other circuits in the application, while at the same time isolating the noisy circuits from the sensitive crystal output. Often only the synthesizer requires very low phase noise from the crystal, hence it is desirable to isolate other circuits from the crystal itself and allow the synthesizer sole use of the low phase noise crystal.

gpo_sel=1 also routes the 200 MHz 14-bit reference path divider to GP02 and the 16-bit 7 GHz VCO path prescaler output to GP01. This option allows the synthesizer to function as a stand alone fractional or integer prescaler and provides visibility into the prescaler and reference path timing for sensitive applications.

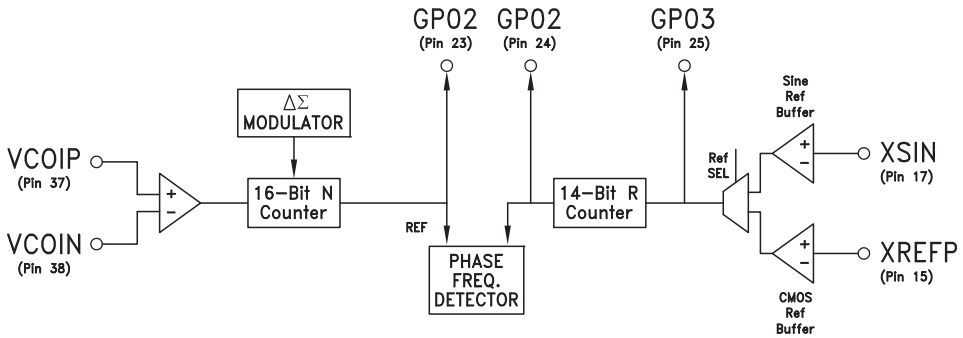


Figure 12. gpo_01 Outputs

Lock Detect Windows (gpo_sel=2)

Setting register *gpo_sel = 2* (*Reg1Bh<3:0>* Table 37) results in the lock detect window (Figure 21) and the phase frequency detector UP and DN output control signals (Figure 24) to be routed to pins GPO1, GPO3 and GPO2 respectively. This option gives insight into the Lock Detection Process and could allow the synthesizer to be used with an external charge pump.

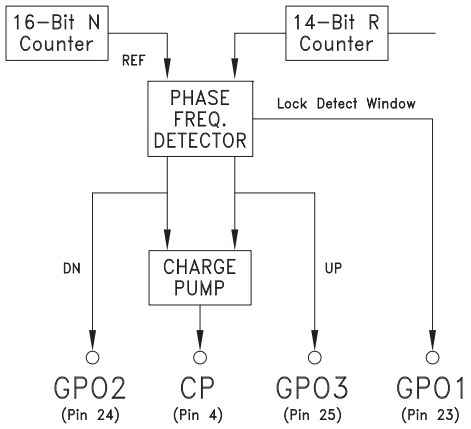


Figure 13. gpo_02 Outputs

Anti-cycle Slip Waveforms (gpo_sel = 3)

Setting register *gpo_sel=3* (*Reg1Bh<3:0>* Table 37) gives visibility into the anti-cycle slipping function of the PFD as described in section *Cycle Slip Prevention* (CSP). Three waveforms, reference path freq > VCO path freq, vco path freq > ref path freq, and a PFD strobe which holds the PFD at maximum gain, are routed to GPO3, GPO2, and GPO1 respectively. These lines will be active during frequency pull-in and will indicate instantaneously which signal, reference or vco path is greater in frequency. The PFD strobe gives insight into when the PFD is near maximum gain at 2π. The PFD strobe will be active until the VCO pulls into lock.

Internal Synchronized Frac strobe with clocks (gpo_sel= 4)

Setting register *gpo_sel=4* in (*Reg1Bh<3:0>* Table 37) gives visibility into the internally synchronized strobe that is generated when commanding a frequency change by writing to the frac register. The internal strobe initiates the update to the fractional modulator, and the VCO SPI transfer if applicable. The internal frac strobe, the ref path divider output and the sine reference input are buffered out to GPO1,GPO2 and GPO3 respectively as shown in Figure 14. In this mode, GPO1 may be used to trigger an external instrument = when doing frequency hopping tests for example.

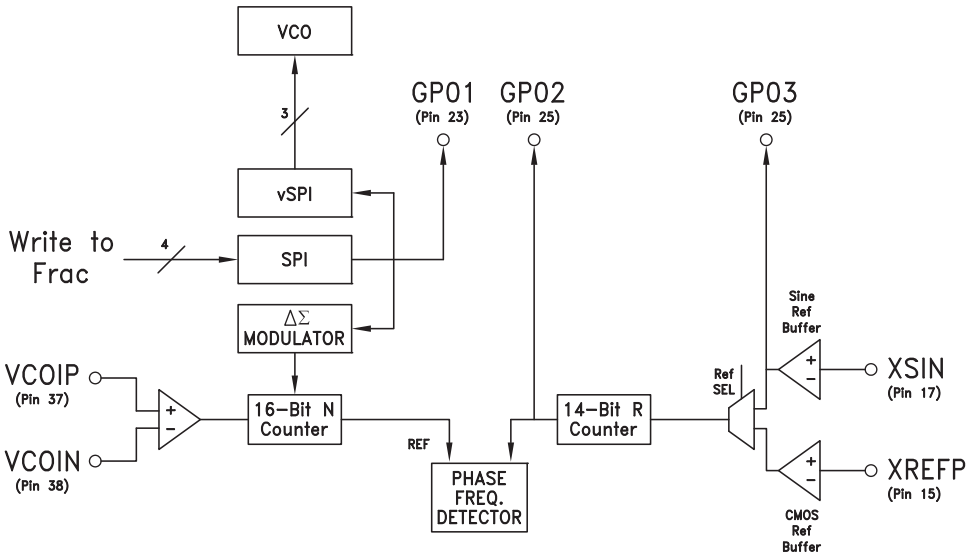


Figure 14. gpo_04 Outputs

Mirror of VCO Port Data, Clock, Latch Enable *(gpo_sel=5)*

Setting register gpo_sel=5 (Reg1Bh <3:0> Table 37) mirrors the output of the VCO SP on the gpo pins.

ΔΣ Modulator Phase Accumulator *(gpo_sel=6)*

Setting register *gpo_sel=6* (*Reg1Bh<3:0>* Table 37) assigns the three msb's of the delta sigma modulator first accumulator to GPO<3:1> , where GPO3 is the msb. This feature provides insight into the phase of the VCO.

Auxiliary Oscillators *(gpo_sel=7)*

Setting register *gpo_sel=7* (*Reg1Bh<3:0>* Table 37) assigns an auxiliary clock, an internal ring oscillator, and the internal sigma delta clock to GPO3, 2, 1 respectively. The control of the auxiliary clock is determined by Reg18h Table 34 and *Reg19h* Table 35. In general terms, this highly flexible clock source allows the selection of one of the various VCO or crystal related clocks inside the synthesizer or the selection of a flexible unstabilized auxiliary ring oscillator clock. Any of the sources may be routed out via gpo_sel=7. Additional *Reg18h* Table 34 clock controls allow the aux clock to be delayed by a variable amount *(auxclk_modesel Reg18h<3:2>)*, or to be divided down by even values from 2 to 14 *(auxclk_divsel Reg18h<6:4>)*.

Auto Calibration Busy Flag *(gpo_sel=8)*

Setting register *gpo_sel=8* (*Reg1B<3:0>* Table 37) assigns a "*vco calibration busy flag*" to GPO1. This output will be high while the auto calibration is running.

ΔΣ *Modulator Outputs (gpo_sel=10)*

Setting register *gpo_sel=10* (*Reg1B<3:0>* Table 37) assigns the three lsb's of the delta sigma modulator output to GPO<3:1> , where GPO1 is the lsb. This feature allows the possibility of using the HMC701LP6CE as a general purpose digital delta sigma modulator for many possible applications.

External VCO

The HMC701LP6CE is targeted for ultra low phase noise applications with an external VCO. The synthesizer has been designed to work with VCOs that can be tuned nominally over 0.5 to 4.5 Volts on the varactor tuning port with a +5V charge pump supply voltage. Slightly wider ranges are possible with a +5.5V charge pump supply or with slightly degraded performance. An external opamp active filter is required to support VCOs with tuning voltages above 5V.

External VCO with Active Inverting OpAmp Loop Filter

An external opamp active filter is required to support external VCOs with tuning voltages above 5V. If an inverting opamp is used with a positive slope VCO, phase_sel Reg05h <0> = 1 Table 16 must be set to invert the PFD phase polarity and obtain correct closed loop operation.

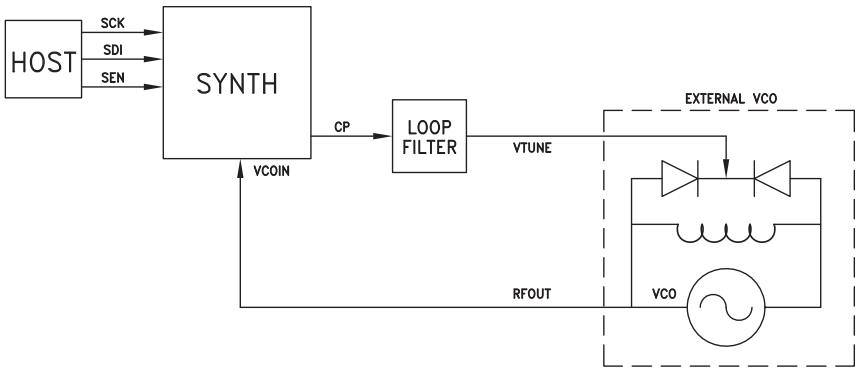


Figure 15. Conventional Synthesizer with VCO

Step Tuned VCO Support

In addition to conventional varactor tuned VCOs, the HMC701LP6CE also supports step tuned type VCOs, as shown Figure 16. A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the mid-voltage tuning point of the synthesizer charge pump. This helps to keep the tuning sensitivity more linear and reduces variations in kvco, which in turn minimizes variations in the closed loop bandwidth of the locked oscillator. VCOs with up to 6-bits of discrete digital tuning, and up to 10-bits of total control bits, are supported via a simple 3-wire VCO Serial Port.

If a step tuned VCO is used, the VCO switches are normally controlled automatically by the synthesizer using the auto tune feature. The VCO switches may also be controlled directly from register bits *Reg0B<4:0>* of *spivco_direct_data*, (*Reg0Bh* Table 22) via direct serial port access for testing or for other special purpose operation. Other control bits specific to the VCO may be output from *Reg0B<9:5>*.

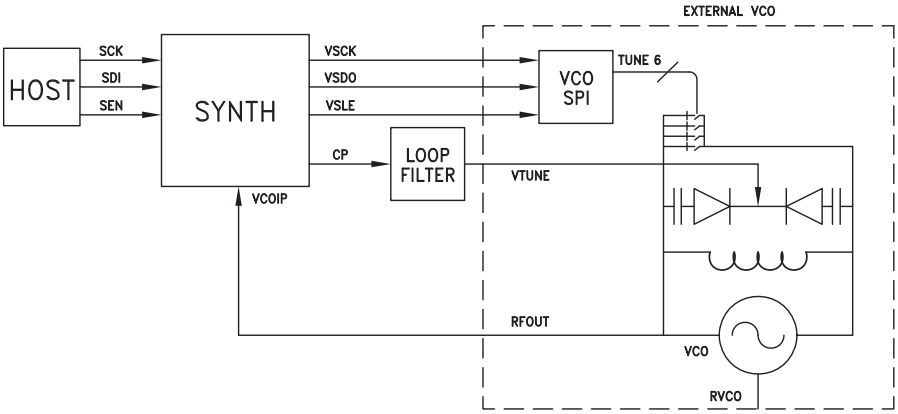


Figure 16. Step Tuned VCO

External VCO Control

The HMC701LP6CE is capable of controlling external VCOs that support additional features on the VCO serial port interface. Up to 10 data control bits may be written to an external VCO via *Reg0Bh* in Table 22. For example such features as band selection or VCO power down may be supported in some VCOs.

Multiple VCO Control

Hittite step tuned VCOs are directly addressable (see Figure 31) and also supports the possibility of controlling multiple HMC step tuned VCOs by sharing the VCO Serial Port lines as shown in Figure 17.

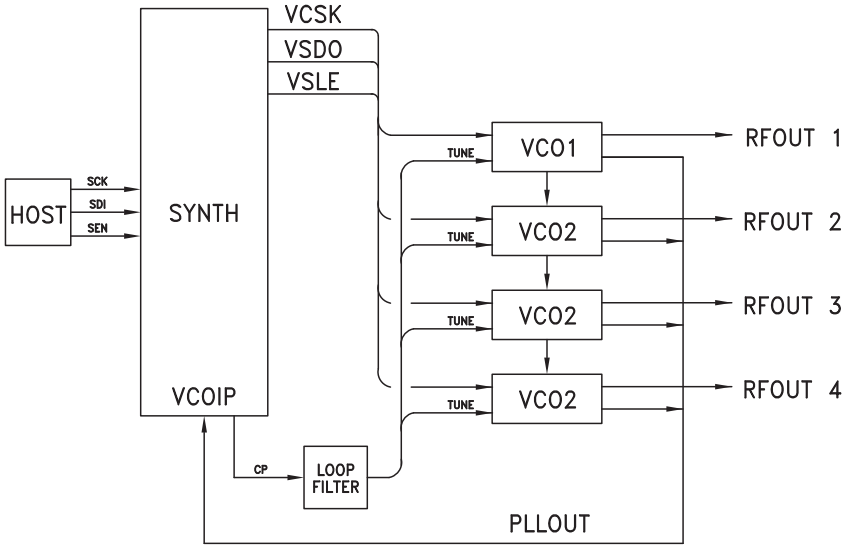


Figure 17. Multiple VCO Control

VCO Tuning, Calibration & Temperature Correction

The HMC701LP6CE supports the use of an optional external step tuned VCO. A step tuned VCO allows the advantages of low phase noise associated with a low kvco, a consistent loop voltage on the tuning varactor from part to part, and lower charge pump voltages for a given range of VCO operation than would be possible with a conventional VCO with only varactor tuning. This feature also helps to reduce synthesizer charge pump non-linearity by keeping the output voltage of the charge pump as close as possible to the mid-rail condition.

Stepped Resonator VCO Calibration & Auto Tuning

In order to use a step tuned VCO in a closed loop, the VCO must be calibrated such that the synthesizer knows which switch position on the VCO is optimum for the desired output frequency. The HMC701LP6CE supports the automatic calibration of the step tuned VCO. The calibration fixes the VCO tuning voltage at the optimum mid-point of the charge pump output, then measures the free running VCO frequency on each switch setting and selects the setting which results in the free running output frequency that is closest to the desired phase locked frequency. This procedure results in a phase locked oscillator that locks over a very narrow voltage range on the varactor.

The calibration can be run automatically every time that a change of frequency is desired. This ensures optimum selection of resonator settings vs. time and temperature. The accuracy desired in the calibration affects the amount of time required to calibrate the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency, while at a varactor voltage that is closest to mid-rail.

If it is desirable to switch frequencies very quickly it is possible to eliminate the calibration time by calibrating the VCO in advance and storing the calibration information in the host. It will then be necessary for the host to run a routine that interrogates the VCO over the desired range of operation and records the optimum resonator switch settings for the desired frequency range. The calibration is then only run once on power up, and the settings stored in the host. The host must then program the switch settings directly when changing frequencies.

Frequency programming of the synthesizer by the host, including switch selection, can be done in the background, while the VCO is locked to the current frequency. The synthesizer normally writes the frequency control information to the VCO, via the VCO Serial Port, upon receipt of a command that changes the PLL frequency, hence eliminating calibration delay from the locking time.

A large change of frequency may require Main Serial Port writes to:

1. The *dsm_seed* register *(Reg 11h* Table 28*)*,
2. VCO switch register *spivco_direct_data (Reg0Bh* Table 22*),*
3. Integer register *dsm_intg (Reg0Fh* Table 26*)* and
4. The fractional register *dsm_frac (Reg10h* Table 27*)*.
   This last register triggers the frequency change in fractional mode.

Smaller steps in frequency may require fewer register writes. Hence a maximum of 4 Main Serial Port transfers to the synthesizer could be required to change frequencies. If the start phase of the fractional modulator is not of concern, then it is not necessary to write the *dsm_seed* register. Similarly if the frequency step is small and the integer or the vco switch settings do not change, then these registers may also be left constant. In all cases, in fractional mode, it is necessary to write to the fractional register for frequency changes.

Frequency Change & VCO AutoCal

The HMC701LP6CE will update the active registers described above only when a frequency change is requested.

a. When in fractional mode (*dsm_integer-mode Reg12h<3>=0*) frequency change happens when the fractional register is written (*Reg10h* Table 27). Integer register may be written first and is buffered until the frac register is written.

b. When in Integer mode *(dsm_integer-mode Reg12h<3>=1)* frequency change happens when the integer register is written (*Reg0Fh* Table 26). Frac register is not used.

c. If *dsm_autoseed* is enabled *(Reg12h(7)=1)*, a frequency change updates the seed value of the fractional modulator digital phase accumulator (DPA) with the value from the seed register *Reg11h* Table 28.

d. If a step tuned VCO is used and Auto tuning is enabled *(Reg 0Ah(1)=1)*, then the frequency change will also initiate the VCO autotuning calibration. Serial Port transfer to the VCO will happen automatically at the end of the autotuning procedure. The VCO will update its registers on the last clock tick of the VSCK (see VCO Serial Port WRITE Operation).

e. If a step tuned VCO is used and Auto tuning is disabled *(Reg 0Ah(1)=1)*, then the frequency change will also initiate the VCO Serial Port transfer to the VCO. The VCO will update its registers with the value from *spivco_direct_data* (*Reg0Bh* Table 22) on the last clock tick of the VSCK (see *VCO Serial Port WRITE Operation*).

Buffering of the integer frequency value, seed value and vco tuning value allows the synthesizer and VCO to hold the current frequency while new values are written. The synthesizer prescaler will only change when a valid frequency change is written. If a step tuned VCO is used, and autotune is disabled, the VCO will be updated after the end of the VCO Serial Port write cycle, about 16 clock cycles after the frequency change command.

Step Tuned VCO AutoCal on Frequency Change

Setting *vcot_auto_start* (*Reg0Ah<0>* Table 21) will cause the switched resonator VCO calibration to start automatically whenever a frequency change is requested.

Step Tuned VCO Manual Calibration

Setting *vcot_man_start* (*Reg0Ah<1>=1* Table 21) starts a switched resonator VCO calibration cycle for the current programmed frequency. *dsm_auto_start (Reg0Ah<0>=0)* must be cleared. The value of the current VCO switch setting determined by the calibration cycle is readable in the *spivco_direct_data* (*Reg0Bh* Table 22) register.

Step Tuned VCO Calibration Time & Accuracy

If a switched resonator VCO, is used, it may be calibrated by searching for the nearest resonator switch position that yields the closest free running VCO frequency to the programmed frequency of the synthesizer. The measurement is done with the VCO open loop and the varactor tuning port forced to VPPCP/2.

The VCO frequency is divided by 32 and counted for T_{mmt}. T_{mmt} is equal to 2vcot_ncyc_rdiv periods of the reference crystal times *vcot_xrefdiv_sel Reg0A<11:10>* Table 21. The frequency result is the value in the vco counter, VCTR, as shown in Figure 18. Currently only *vcot_xrefdiv_sel = 1* is supported.

The nominal VCO frequency measured, f_{vcom}, is given by

$$f_{vcom} = 32\frac{VCTR}{T_{mmt}} \pm f_{erro} \quad \text{(EQ 1)}$$

Where the worst case measurement error, f_{erro}, is:

$$f_{erro} = \pm\frac{32}{T_{mmt}} \quad \text{(EQ 2)}$$

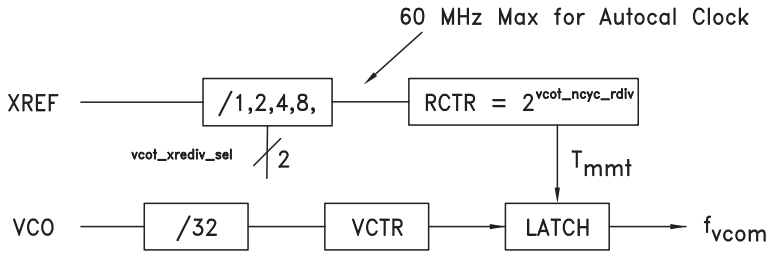


Figure 18. VCO Calibration

The period of a single VCO calibration measurement, T_{mmt}, is given by:

$$T_{mmt} = \frac{1}{f_{xtal}} \cdot 2^{ncyc} \cdot 2^{vcot} \quad \text{(EQ 3)}$$

Where

ncyc = *vcot_ncyc_rdiv Reg0A<5:2>* Table 21

vcot = Ref tune clock division ratio, vcot_xrediv_sel *Reg0Ah<11:10>,* Table 21
Note: Only vcot = 0 is supported currently

A 5-bit switched resonator VCO, for example, nominally requires 5 measurements for calibration, worst case 6, hence total calibration time, worst case, is given by:

$$T_{cal} = 6T_{mmt} \quad \text{(EQ 4)}$$

Normally we wish the absolute value of f_{erro} to be less than one half of the VCO switched resonator step size specified for the switched resonator VCO.

VCO Auto Tuning Example

Suppose our target frequency is to operate at 2.3 GHz with a nominal 1.5V on the charge pump. Our example crystal is 50 MHz and *vcot_xrefdiv_sel* divider is 1, hence the auto calibration clock = 50 MHz. Note, when using autocal, the maximum input crystal cannot exceed 60 MHz.

We must decide how long, and how accurate we need to make the tuning. Suppose the switched resonator lsb steps are 6.5 MHz nominal, 6 MHz worst case.

A reasonable calibration target would be to set the calibration frequency error to one half the VCO lsb steps, i.e. f_{erro} <= 3 MHz. With some reasonable margin, lets target 2 MHz f_{erro} worst case. Using (EQ 1) we see that the minimum calibration measurement time for a single measurement must be

$$T_{mmtmin} = \frac{32}{f_{erro}} = \frac{32}{2e6} = 16us \quad \text{(EQ 5)}$$

Hence we must choose ncyc such that $T_{mmt} > T_{mmtmin}$

Solving for (EQ 3)

$$ncyc \geq \frac{\log\frac{T_{mmt}f_{xtal}}{R}}{\log 2} = 9.64 = 10 \quad \text{(EQ 6)}$$

We arrive at a value of 10 for ncyc, and hence a single measurement period is T_{mmt} = 20.48 usec, the worst case frequency error of the measurement is ±1.56 MHz and the total time to run the full calibration for a 5 bit switched VCO is six measurements worst case, hence T_{cal} = 6 T_{mmt} = 122.9 usec, plus time for six VCO serial port transfers and state machine housekeeping, typically about $90*R/f_{xtal}$, about 1.8 usec more.

Example Calibration Procedure with an Example External VCO

Using the above example calculation for calibration time and accuracy, the procedure to run the calibration is as follows using an example VCO at 2.3 GHz:

The example VCO must first be set up to operate in the desired band, with, in this example, a 50 MHz crystal and a 50 MHz PFD frequency.

a. Setup the VCO register as required by the VCO (*Reg0Bh* Table 22)
b. Input a reference signal at 50 MHz
c. Set the Ref divider to divide by 1 , rfp_div_ratio = 00 0000 0000 0001, *(Reg03h<13:0>* Table 14*)*
d. Set the integer division, *intg* = 46d = 002Eh *(Reg0Fh* Table 26*)*

Then set up the auto calibration features as follows:

e. Set the auto calibration time by setting *vcot_ncyc_rdiv* = 1010 *(Reg0Ah<5:2>* Table 21*)*
f. Enable the auto calibration feature by setting *vcot_auto_start (Reg0Ah<0>* Table 21*)*

Then program the fractional frequency to start the calibration and change frequencies.

g. Set the fractional register to zero in this example, *frac* = 000000h (*Reg10h* Table 27)

The last step of programming the frequency register initiates the calibration which will run in about 124 usec, as per our calculation. The state machine will write the autotune result into *Reg20h* Table 42. The synthesizer will then be tuned to the commanded output frequency with the optimized switch setting on the VCO. The normal locking time will apply after the calibration is run.

The optimum tuning setting for this frequency may be read by the host from read only register *vcot_caps Reg20h<7:0>* (Table 42) and stored for later use for faster tuning to this frequency.

Manual VCO Control for Fast Frequency Changes

If the auto calibration reading is run first for a given frequency and the calibration settings are read and stored for later use in the host, then a frequency change can be run without re-running the autocal routine.

Assume that the VCO band and reference are all programmed correctly in advance. Further that we disable the auto calibration feature by clearing *vcot_auto_start* (*Reg0Ah<0>* Table 21).

Then a frequency change is executed as follows:

a. Write the calibration switch setting for the desired frequency to *spivco_direct_data* (*Reg0Bh* Table 22). (VCO specific)
b. If necessary set the integer frequency register *dsm_intg* (*Reg0Fh* Table 26)
c. Write the fractional register to trigger the frequency change frac (*Reg10h* Table 27)
d. The synthesizer then automatically updates the fractional divider and initiates the VCO Serial Port transfer for the new frequency

Calibration Polarity, Tune Word Inversion & Active Opamp Loop Filters

vcot_invert_outdata (*Reg0Ah<6>* Table 21) inverts the VCO tuning cap polarity. The polarity must be set to match the VCO polarity in question or the autotune search algorithm will not work. This bit is normally set if an active loop filter is used with an inverting opamp with a positive tuning slope VCO

vcot_swap_outdata (*Reg0Ah<7>* Table 21) swaps the cap data left to right. This makes it easy to match the VCO in use. Binary weighted caps are expected.

Temperature Sensor

The HMC701LP6CE features a built in temperature sensor which may be used as a general purpose temperature sensor.

The temperature sensor is enabled via *tsens_spi_enable* (*Reg1Eh=1* Table 40) and when enabled draws 2 mA. The temperature sensor features a built in 3-bit quantizer that allows the temperature to be read in register *tsens_temperature* (*Reg21h* Table 43). The temperature sensor data converter is not clocked. Updates to the temperature sensor register are made by strobbing register *tsens_spi_strobe* (Reg00h<3> Table 11). The 3-bit quantizer operates over a -40°C to +100°C range as follows:

Tn = floor {(Temperature +40) / 17.5 where T_n is the decimal value of register *tsens_temperature}* (EQ 7)

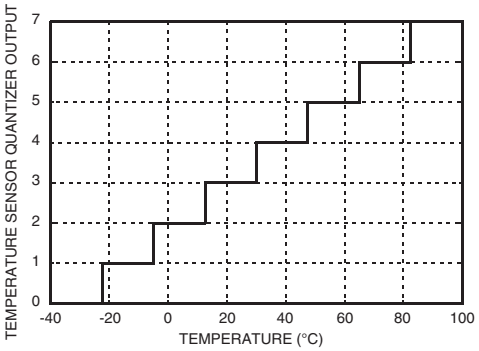


Figure 19. Typical Temperature Sensor Quantizer output

Temperature sensor slope is 17.5 mV/lsb. Absolute tolerances on the temperature sensor thresholds may vary by up to ±10°C worst case.

Nominal temperature is given by:

$$Temperature = 17.5T_n - 31.25 \pm 8.75 \quad (^oC) \qquad \text{(EQ 8)}$$

Charge Pump & Phase Frequency Detector (PFD)

The Phase Frequency Detector or PFD has two inputs, one from the reference path divider and one from the VCO path divider. The PFD compares the phase of the VCO path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians input phase difference.

PFD Functions

phase_sel (*Reg05h<0>* Table 16) inverts the phase detector, polarity for use with an inverting opamp or negative slope VCO.

upout_en in *Reg05h<1>* Table 16 allows masking of the PFD up output, which effectively prevents the charge pump from pumping up.

dnout_en in *Reg05h<2>* Table 16 allows masking of the PFD down output, which effectively prevents the charge pump from pumping down.

Charge Pump Tri-State

De-asserting both *upout_en* and *dnout_en* effectively tri-states the charge pump while leaving all other functions operating internally.

PFD Jitter & Lock Detect Background

In normal phase locked operation the divided VCO signal arrives at the phase detector in phase with the divided crystal signal, known as the reference signal. Despite the fact that the device is in lock, the phase of the VCO signal and the reference signal vary in time due to the phase noise of the crystal and VCO oscillators, the loop bandwidth used and the presence of fractional modulation or not. The total integrated noise on the VCO path normally dominates the variations in the two arrival times at the phase detector if fractional modulation is turned off.

If we wish to detect if the VCO is in lock or not we need to distinguish between normal phase jitter when in lock and phase jitter when not in lock.

First, we need to understand what is the jitter of the synthesizer, measured at the phase detector in integer or fractional modes.

The standard deviation of the arrival time of the VCO signal, or the jitter, in integer mode may be estimated with a simple approximation if we assume that the locked VCO has a constant phase noise, $\Phi^2(f_0)$, at offsets less than the loop 3 dB bandwidth and a 20 dB per decade roll off at greater offsets. The simple locked VCO phase noise approximation is shown on the left of Figure 20.

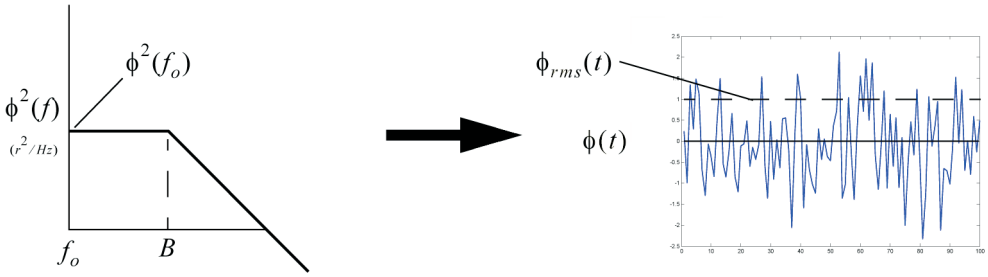


Figure 20. Synthesizer Phase Noise & Jitter

With this simplification the single sideband integrated VCO phase noise, Φ^2 , in rads^2 at the phase detector is given by

$$\phi_{SSB}{}^2 = \left(\phi^2(f_o)B\frac{\pi}{2}\right)/N^2 \qquad \text{(EQ 9)}$$

where

$\Phi^2{}_{SSB}(f_0)$ is the single sideband phase noise in rads^2/Hz inside the loop bandwidth, B is the 3 dB corner frequency of the closed loop PLL and N is the division ratio of the prescaler

The rms phase jitter of the VCO in rads, Φ , results from the power sum of the two sidebands:

$$\Phi = \sqrt{2\Phi^2_{SSB}} \qquad \text{(EQ 10)}$$

$$\pm 3\sqrt{2}T_{jpn} = 0.756\,ps$$

Since the simple integral of (EQ 9) is just a product of constants, we can easily do the integral in the log domain. For example if the VCO phase noise inside the loop is -100 dBc/Hz at 10 kHz offset and the loop bandwidth is 100 kHz, and the division ratio N=100, then the integrated single sideband phase noise at the phase detector in dB is given by $\Phi^2{}_{dB}$ = 10log ($\Phi^2(f_0)B\pi / N^2$) = -100 + 50 + 5 - 40 = -85 dBrads, or equivalently $\Phi = 10^{-82/20}$ = 56 urads rms or 3.2 milli-degrees rms.

While the phase noise reduces by a factor of 20logN after division to the reference, the jitter is a constant.

The rms jitter from the phase noise is then given by $T_{jnp} = T_{ref}\,\Phi / 2\pi$

In this example if the reference was 50 MHz, T_{ref} = 20 nsec, and hence T_{jpn} = 178 femto-sec.

A normal 3 sigma peak-to-peak variation in the arrival time therefore would be

If the synthesizer was in fractional mode, the fractional modulation of the VCO divider will dominate the jitter. The exact standard deviation of the divided VCO signal will vary based upon the modulator chosen, however a typical modulator will vary by about ±3 VCO periods, ±4 VCO periods, worst case.

If, for example, a nominal VCO at 5 GHz is divided by 100 to equal the reference at 50 MHz, then the worst case division ratios will vary by 100±4. Hence the peak variation in the arrival times caused by ΔΣ modulation of the fractional synthesizer at the reference will be

$$T_{j\Delta\Sigma pk} = \pm T_{vco} \cdot (N_{max} - N_{min})/2 \quad \text{(EQ 11)}$$

In this example, $T_{j\Delta\Sigma pk}$ = ±200 ps(104-96)/2 = ±800 psec. If we note that the distribution of the delta sigma modulation is approximately gaussian, we could approximate $T_{j\Delta\Sigma pk}$ as a 3 sigma jitter, and hence we could estimate the rms jitter of the ΔΣ modulator as about 1/3 of $T_{j\Delta\Sigma pk}$ or about 266 psec in this example.

Hence the total rms jitter T_j, expected from the delta sigma modulation plus the phase noise of the VCO would be given by the rms sum , where

$$T_j = \sqrt{T_{jpn}^2 + \left(\frac{T_{j\Delta\Sigma pk}}{3}\right)^2} \quad \text{(EQ 12)}$$

In this example the jitter contribution of the phase noise calculated previously would add only 0.764psec more jitter at the reference, hence we see that the jitter at the phase detector is dominated by the fractional modulation.

Bottom line, we have to expect about ±0.8 nsec of normal variation in the phase detector arrival times when in fractional mode. In addition, lower VCO frequencies with high reference frequencies will have much larger variations., for example, a 1 GHz VCO operating at near the minimum nominal divider ratio of 36, would, according to (EQ 11), exhibit about ±4 nsec of peak variation at the phase detector, under normal operation. The lock detect circuit must not confuse this modulation as being out of lock.

PFD Lock Detect

lkd_en (*Reg01h<11>* Table 12) enables the lock detect functions of the HMC701LP6CE.

The Lock Detect circuit in the HMC701LP6CE places a one shot window around the reference. The one shot window may be generated by either an analog one shot circuit or a digital one shot based upon an internal ring oscillator timer. Clearing *lkd_ringosc_mono_select* (*Reg1Ah<14>* Table 36) will result in a nominal ±10nsec 'analog' window of fixed length, as shown in Figure 21. Setting *lkd_ringosc_mono_select* will result in a variable length 'digital' widow. The digital one shot window is controlled by *lkd_ringosc_cfg (Reg1Ah<16:15>)*. The resulting lock detect window period is then generated by the number of ring oscillator periods defined in *lkd_monost_duration Reg1Ah<18:17>* (Table 36). The lock detect ring oscillator may be observed on the GPO2 port by setting *ringosc_testmode* (*Reg1Ah<19>* Table 36) and configuring the *gpo_sel<3:0>* = 0111 in (*Reg1Bh* Table 37). Lock detect does not function when this test mode is enabled.

lkd_wincnt_max (*Reg1Ah<9:0>* Table 36) defines the number of consecutive counts of the VCO that must land inside the lock detect window to declare lock. If for example we set *lkd_wincnt_max* = 1000 , then the VCO arrival would have to occur inside the selected lock widow 1000 times in a row to be declared locked. When locked the Lock Detect flag *ro_lock_detect* (*Reg1Fh<0>* Table 41) will be set. A single occurrence outside of the window will result in clearing the Lock Detect flag, *ro_lock_detect*.

The Lock Detect flag *ro_lock_detect* (*Reg1Fh<0>* Table 41) is a read only register, readable from the serial port. The Lock Detect flag is also output to the *LD_SDO* pin according to *lkd_to_sdo_always (Reg1Ah<13>)* and *lkd_to_sdo_automux_en (Reg1Ah<12>)*, both in Table 36. Setting *lkd_to_sdo_always* will always display the Lock Detect flag on *LD_DSO*. Clearing *lkd_to_sdo_always* and setting *lkd_to_sdo_automux_en* will display the Lock Detect flag on *LD_SDO* except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin, and returns to the lock detect function after the read is completed.

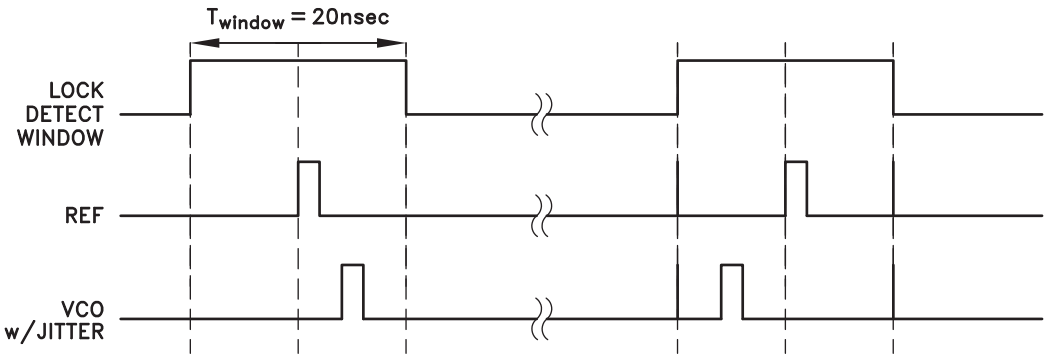


Figure 21. Normal Lock Detect Window

Lock Detect with Phase Offset

When operating in fractional mode the linearity of the charge pump and phase detector are more critical than in integer mode. The phase detector linearity is worse when operated with zero phase offset. Hence in fractional mode it is necessary to offset the phase of the reference and the VCO at the phase detector. In such a case, for example with an offset delay, as shown in Figure 22, the mean phase of the VCO will always occur after the reference. The lock detect circuit window can be made more selective with a fixed offset delay by setting *win_asym_enable* and *win_asym_up_select* (*Reg1Ah<11>* Table 36). Similarly the offset can be in advance of the reference by clearing *win_asym_up_select* while leaving *win_asym_enable Reg1Ah<10>* set both in Table 36.

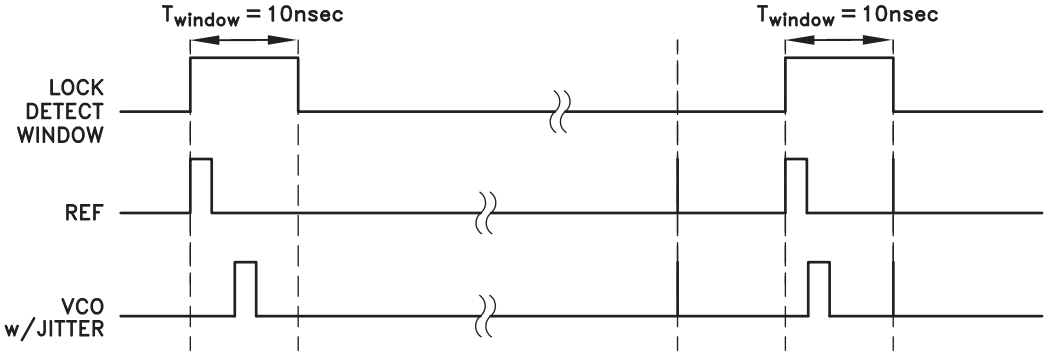


Figure 22. Delayed Lock Detect Window

Cycle Slip Prevention (CSP)

When changing frequencies the VCO is not yet locked to the reference and the phase difference at the PFD varies rapidly over a range much greater than ±2π radians. Since the gain of the PFD varies linearly with phase up to ±2π, the gain of conventional PFDs will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. This phenomena is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically as shown in the red curve in Figure 23. Cycle slipping increases the time to lock to a value far greater than that predicted by normal small signal Laplace analysis.

The HMC701LP6CE PFD features Cycle Slip Prevention (CSP), an ability to virtually eliminate cycle slipping during acquisition. When enabled, the CSP feature essentially holds the PFD gain at maximum until such time as the frequency difference is near zero. CSP allows significantly faster lock times as shown in Figure 23. The use of the CSP feature is enabled with *pfds_rstb* (*Reg01<15>* Table 12). The CSP feature may be optimized for a given set of PLL dynamics by adjusting the PFD sensitivity to cycle slipping. This is achieved by adjusting *pfds_sat_deltaN* (*Reg1C<3:0>* Table 38).

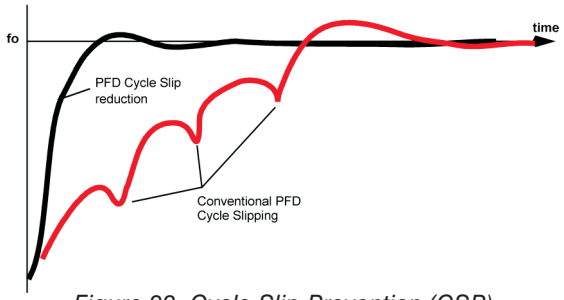


Figure 23. Cycle Slip Prevention (CSP)

Charge Pump Gain

A simplified diagram of the charge pump is shown in Figure 24. Charge pump up and down gains are set by *cp_UPcurrent_sel* and *cp_DNcurrent_sel* respectively (*Reg07* Table 18). Normally the registers are set to the same value. Each of the UP and DN charge pumps consist of 5-bit charge pumps with lsb of 125 µA. The current gain of the pump, in Amps/radian, is equal to the gain setting of this register divided by 2π.

For example if both *cp_UPcurrent_sel* and *cp_DNcurrent_sel* are set to '01000' the output current of each pump will be 1mA and the gain *Kp* = 1mA/2π radians, or 159 uA/rad.

Charge Pump Gain Trim

In most applications Gain Trim is not used. However it is available for special applications.

Each of the UP and DN pumps may be trimmed separately to more precise values to improve current source matching of the UP and DN values, or to allow finer control of pump gain.

The pump trim controls are 3-bits, binary weighted for UP and DN, in *cp_UPtrim_sel* and *cp_DNtrim_sel* respectively (Reg 08h Table 19). LSB weight is 14.7 uA, x000 = 0 trim, x001 = 14.7 ua added trim, x111 = 100uA.

Charge Pump Phase Offset

Either of the UP or DN charge pumps may have a DC leakage or "offset" added. The leakage forces the phase detector to operate with a phase offset between the reference and the divided VCO inputs. It is recommended to operate with a phase offset when using fractional mode to reduce non-linear effects from the UP and DN pump mismatch. Phase noise in fractional mode is strongly affected by charge pump offset.

DC leakage or "offset" may be added to the UP or DN pumps using *cp_UPoffset_sel* and *cp_DNoffset_sel* (*Reg08* Table 19). These are 4 bit registers with 28.7uA LSB. Maximum offset is 430uA.

As an example, if the main pump gain was set at 1mA, an offset of 373uA would represent a phase offset of about (392/1000)*360 = 133degrees.

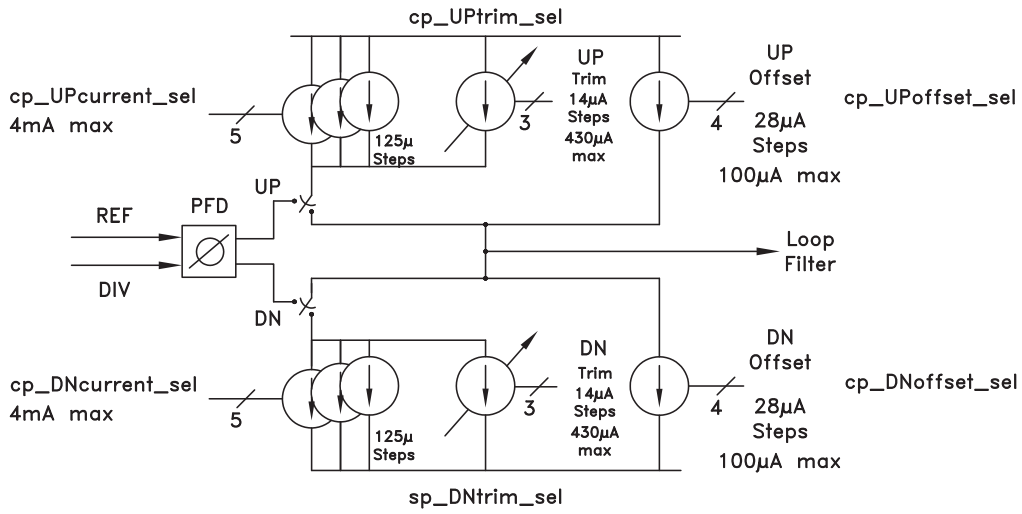


Figure 24. Charge Pump Gain, Trim and Phase Offset Control

Frequency Programming

The HMC701LP6CE can operate in either fractional mode or integer mode. In integer mode of operation the delta sigma modulator is disabled. Frequency programming and mode control is described below.

Fractional Frequency

The fractional frequency synthesizer, when operating in fractional mode, can lock to frequencies which are fractional multiples of the reference frequency.

Fractional mode is the default mode. To run in fractional mode ensure that *dsm_integer_mode* Reg12h<5> Table 29 is clear and *dsm_rstb* Reg01<13> Table 12). Then program the frequency as explained below:

The output frequency of the synthesizer is given by, f_{vco}, where

Fractional Frequency of VCO

$$f_{vco} = \frac{f_{xtal}}{R} N_{int} + \frac{f_{xtal} \cdot N_{frac}}{R \cdot 2^{24}} = f_{int} + f_{frac} \quad \text{(EQ 13)}$$

where

N_{int}	is the integer division ratio, an integer number between 36 and 65,533 (*dsm_intg* (*Reg0Fh* Table 26))
N_{frac}	is the fractional part, a number from 1 to 2^{24} (*dsm_frac Reg10h* Table 27)
R	is the reference path division ratio, (*rfp_div_ratio Reg03h<13:0>* Table 14)
f_{xtal}	is the frequency of the crystal oscillator input (XSIN or XREF Figure 10)

As an Example:

f_{xtal}	= 50 MHz
R	= 1
f_{ref}	= 50 MHz
N_{int}	= 46
N_{frac}	= 1

$$f_{vco} = \frac{50e6}{1}46 + \frac{50e6 \cdot 1}{1 \cdot 2^{24}} = 2.3GHz + 2.98Hz \quad \text{(EQ 14)}$$

In this example the output frequency of 2,300,000,002.98 Hz is achieved by programming the 16-bit binary value of 46d = 2Eh = 0000 0000 0010 1110 into *dsm_intg*.

Similarly the 24-bit binary value of the fractional word is written into *dsm_frac*,

1d = 000 001h = 0000 0000 0000 0000 0000 0001

Example 2: Set the output to 4.600 025 GHz using a 100 MHz reference, R=2.

Find the nearest integer value, N_{int}, N_{int} = 92, f_{int} = 4.600 000 GHz

This leaves the fractional part to be f_{frac} =25 kHz

$$N_{frac} = \frac{2^{24} \cdot R \cdot f_{frac}}{f_{xtal}} = \frac{2^{24} \cdot 2 \cdot 25e3}{100e6} = 8389 \quad \text{(EQ 15)}$$

Since N_{frac} must be an integer number, the actual fractional frequency will be 25,001.17 Hz, an error of 1.17 Hz.

Here we program the 16-bit N_{int} = 92d = 5Ch = 0000 0000 0101 1100 and

the 24-bit N_{frac} = 8389d = 20C5h = 0000 0010 0000 1100 0101

In addition to the above frequency programming words, the fractional mode must be enabled using the frac register. Other DSM configuration registers should be set to the recommended values. Register setup files are available on request.

Integer Frequency

The synthesizer is capable of operating in integer mode. In integer mode the digital ΔΣ modulator is normally shut off and the division ratio of the VCO divider is set at a fixed value. To run in integer mode set *dsm_integer_mode* (*Reg12h<3>* Table 29) and clear *dsm_rstb* (*Reg01h<13>* Table 12). Then program the integer portion of the frequency, N_{INT}, as explained by (EQ 13), ignoring the fractional part.

Frequency Hopping Trigger

If the synthesizer is in fractional mode, a write to the fractional frequency register, *Reg10h* Table 27, will initiate the frequency hop on the falling edge of the 31st clock edge of the serial port write (see Figure 29).

If the integer frequency register, *Reg0Fh* Table 26, is written when in fractional mode the information will be buffered and only executed when the fractional frequency register is written.

If the synthesizer is in integer mode, a write to the integer frequency register, *Reg0Fh* Table 26, will initiate the frequency hop on the falling edge of the 31st clock edge of the serial port write (see Figure 29).

Power On Reset (POR)

Normally all logic cells in the HMC701LP6CE are reset when the device digital power supply, DVDD, is applied. This is referred to as Power On Reset, or just POR. POR normally takes about 500us after the DVDD supply exceeds 1.5V, guaranteed to be reset in 1msec. Once the DVDD supply exceeds 1.5V, the POR will not reset the digital again unless the supply drops below 100mV.

Soft Reset

The SPI registers may also be soft reset by an SPI write to strobe *global_swrst_regs* (*Reg00h<0>* Table 11).

All other digital, including the fractional modulator, may be reset with an SPI write to strobe *global_swrst_dig (Reg00h<1>* Table 11).

Hardware Reset

The SPI registers may also be hardware reset by holding RSTB, pin 19, low.

Power Down

The HMC701LP6CE may be powered down by writing a zero to *Reg01h* Table 12. In power down state the HMC701LP6CE should draw less than 10uA. It should be noted that *Reg01h* is the Enable and Reset Register which controls 16 separate functions in the chip. Depending upon the desired mode of operation of the chip, not all of the functions may be enabled when in operation. Hence power up of the chip requires a selective write to *Reg01* bits. An easy way to return the chip to its prior state after a power down is to first read *Reg01h* and save the state, then write a zero to *Reg01h* for reset and then simply rewrite the previous value to restore the chip to the desired operating mode.

CW Sweeper Mode

The HMC701LP6CE features a built in frequency sweeper function. This function supports external or automatic triggered sweeps.

Sweeper Modes include:

a. 2-Way Sweep Mode: alternating positive and negative frequency ramps.

b. 1-Way Sweep Mode

c. Single Step Ramp Mode

Applications include test instrumentation, FMCW sensors, automotive radars and others. The parameters of the sweep function are illustrated in Figure 26.

The sweep generator is enabled with *ramp_enable* in (*Reg14h<1>* Table 30). The sweep function cycles through a series of discrete frequency values, which may be

a. Stepped by an automatic sequencer, or

b. Single stepped by individual triggers in Single Step Mode.

Triggering of each sweep, or step, may be configured to operate:

a. Via a serial port write to *Reg14h<2> ramp_trigg* (if Reg 14h<2> = 0)

b. Automatically generated internally,

c. Triggered via TTL input on GPO3 Reg14h<5> = 1.

Sweep parameters are set as follows:

Initial Frequency, f_o = Current frequency value of the synthesizer, (EQ 15)

Final Frequency, f_f = Frequency of the synthesizer at the end of the ramp

The frequency step size while ramping is controlled by *rampstep*, (*Reg15h* Table 31).

Frequency Step Size Δf_{step} = *rampstep* • *fatal* / 2^{24} • *R*

where R is the value of the reference divider (*rfp_div_ratio in* Table 14)

CW Sweeper Mode *(Continued)*

Clearing or setting *ramp_startdir_dn*, (*Reg14h<4>* Table 30), sets the initial ramp direction to be increasing or decreasing in frequency respectively. Setting *ramp_singledir* (*Reg14h<7>* Table 30), restricts the direction of the sweep to the initial sweep direction only.

The sweeper timebase T_{ref} is the period of the divided reference, f_{PFD}, at the phase detector T_{ref}

The total number of ramp steps taken in a single sweep is given by ramp_steps_number in Reg16h Table 32.

The total time to ramp from f_o to f_f is given by $T_{ramp} = T_{ref} \bullet ramp\_steps\_number$

The final ramp frequency, f_f, is given by $f_f = f_i + \Delta f_{step} \bullet ramp\_steps\_number$

Sweeper action at the end of sweep depends upon the mode of the sweep:

a. With both *ramp_singledir* and *ramp_repeat_en* disabled, at the end of the ramp time, T_{ramp}, the sweeper will dwell at the final frequency f_f, until a new trigger is received. The next trigger will reverse the current sequence, starting from f_f, and stepping back to f_o. Odd triggers will ramp in the same direction as the initial ramp, even triggers will ramp in the opposite direction.

b. with *ramp_singledir* enabled and *ramp_repeat_en* disabled, at the end of the ramp time, T_{ramp}, the sweeper will dwell at the final frequency f_f, until a new trigger is received. The second trigger will hop the synthesizer back to the initial frequency, f_o. The third trigger will restart the sweep from f_o. Hence all odd numbered triggers will start a new ramp in the same direction as the initial ramp, even numbered triggers will hop the synthesizer from the current frequency to f_o , where it will wait for a trigger to start a sweep.

Ramp Busy

In all types of sweeps *ramp_busy* will indicate an active sweep and will stay high between the 1st and nth ramp step. *ramp_busy* may be monitored one of two ways. *ramp_busy* is readable via read only register *Reg1Fh<5>* Table 41.

ramp_busy may also be monitored on GPO2, hardware pin 24, by setting *Reg1Bh<3:0> =8h* Table 37.

Autosweep Mode

The Autosweep mode is similar to Figure 26 except that once started, triggers are not required. Once enabled, (*ramp_repeat_en=1 Reg14h<3>* Table 30) the Autosweep mode initiates the first trigger, steps n times, one step per ref clock cycle, and then waits for the programmed dwell period and automatically triggers the ramp in the opposite direction. The sweep process continues alternating sweep directions until disabled. *dwell_time* (*Reg17h* Table 33) controls the number of T_{ref} periods to wait at the end of the ramp before automatically retriggering a new sweep.

2-Way Sweeps

If *ramp_repeat_en* (*Reg14h<3>* Table 30) is cleared, then the ramps are triggered by

a. Writing to *ramp_trigg* (*Reg14h<2>* Table 30), if bit <2> = 0, or

b. by rising edge TTL signal input on GPO3, if *ramp_trig_ext_en* is set, and GPO3 is enabled.

All functions are the same in Figure 26 for Autosweep or 2-Way Triggered sweeps, the only difference is the trigger source is generated internally for autosweep, and is input via serial port or GPO3 for triggered sweeps. *Sweep_busy* will go high at the start of every ramp and stay high until the nth step in the ramp.

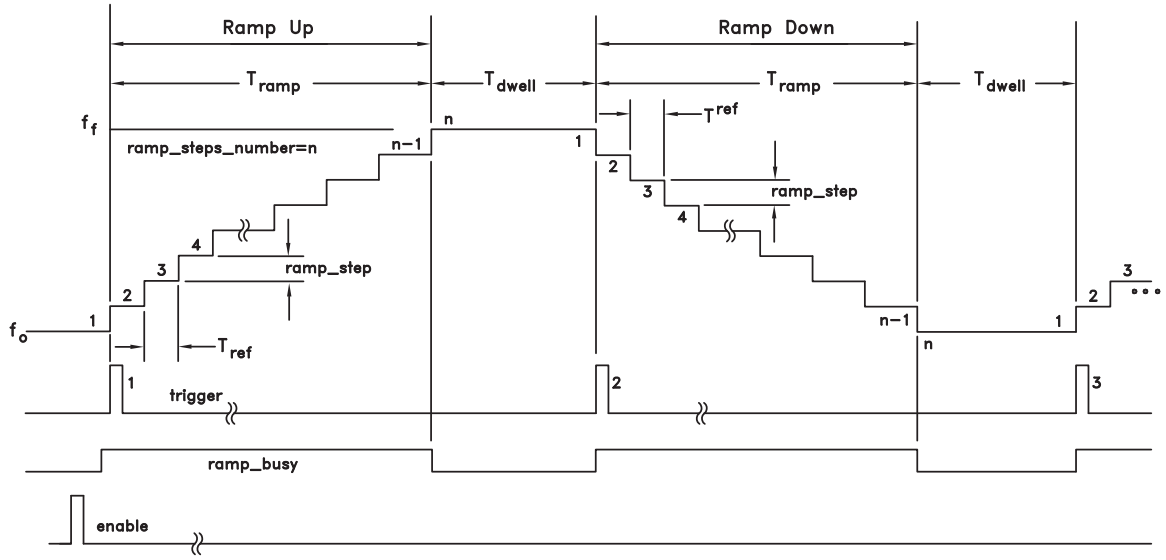


Figure 26. 2-Way Sweep Control via Trigger

Triggered 1-Way Sweeps

1-Way sweeps are shown in Figure 27.

Unlike 2-Way sweeps, 1-Way sweeps require that the VCO hop back to the start frequency after the dwell period. Triggered 1-Way sweeps also require a 3rd trigger to start the new sweep. The 3rd trigger must be timed appropriately to allow the VCO to settle after the large frequency hop back to the start frequency. Subsequent odd numbered triggers will start the 1-Way sweep and repeat the process.

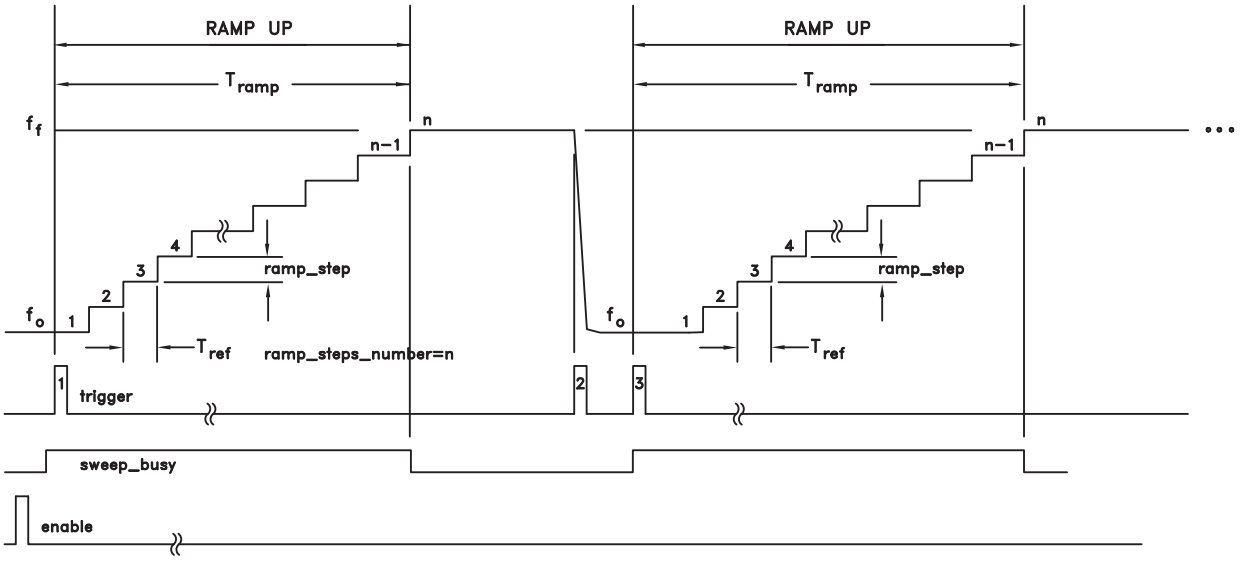


Figure 27. 1-Way Sweep Control

Single Step Ramp Mode

A Single Step 1-Way Ramp is shown in Figure 28. In this mode, a trigger is required for each step of the ramp. Single step will function in either 1-Way or 2-Way ramps. Similar to autosweep, the ramp_busy flag will go high on the first trigger, and will stay high until the nth trigger. The n+1 trigger will cause the ramp to jump to the start frequency in 1-way ramp mode. The n+2 trigger will restart the 1-way ramp.

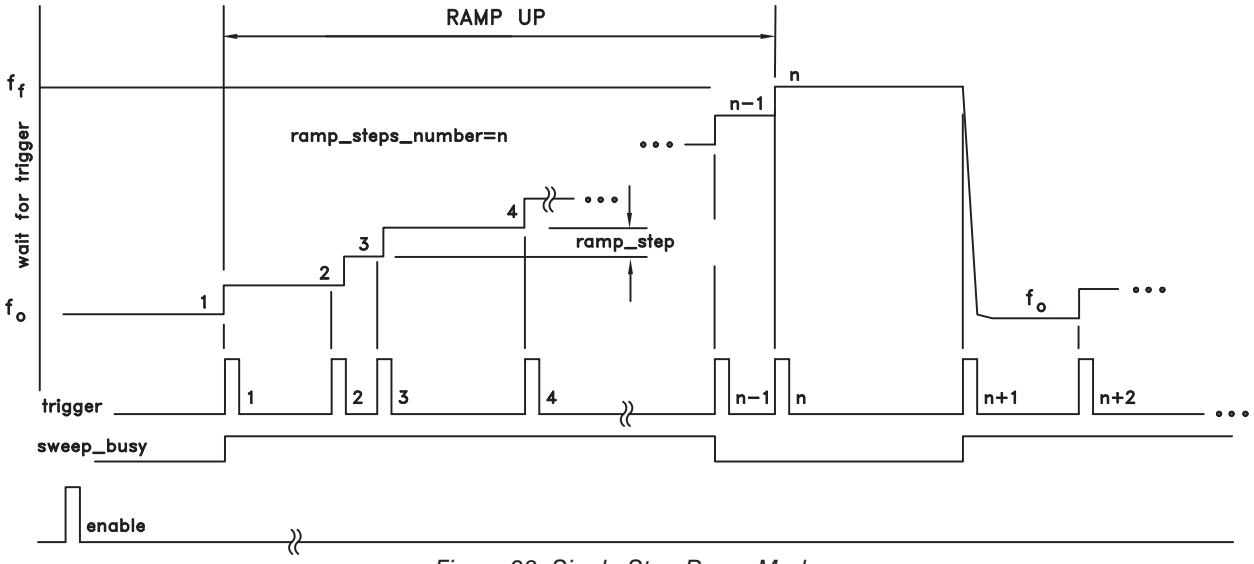


Figure 28. Single Step Ramp Mode

The user should be aware that the synthesized ramp is subject to normal phase locked loop dynamics. If the loop bandwidth in use is much wider than the rate of the steps then the locking will be very fast and the ramp will have a staircase shape. If the update rate is higher than the loop bandwidth, as is normally the case, then the loop will not fully settle before a new frequency step is received. Hence the swept output will have a small lag and will sweep in a near continuous fashion.

MAIN SERIAL PORT

The HMC701LP6CE features a four wire serial port for simple communication with the host controller. Register types may be Read Only, Write Only, Read/Write or Strobe, as described in the registers descriptions. The synthesizer also features an auxiliary 3-wire serial port, known as the VCO Serial Port. The VCO Serial Port is a write only interface from the synthesizer to an optional switched resonator VCO that supports 3-wire serial port control.

Typical main serial port operation can be run with SCLK at speeds up to 50 MHz. Serial port registers are described in the section REGISTER MAP.

[1] Phase-Error Measurement and Compensation in PLL Frequency Synthesizers for FMCW, Sensors—I: Context and Application, Pichler, Stelzer, Member, IEEE, Seisenberger, and Vossiek, IEEE Transactions on Circuits and Systems—I, VOL. 54, No. 5, May 2007

Serial Port WRITE Operation

AVDD = DVDD = 3V ±10%, AGND = DGND = 0V

Table 4. Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SEN to SCLK setup time	8			nsec
t_2	SDI to SCLK setup time	10			nsec
t_3	SDI to CLK hold time	10			nsec
t_4	SCLK high duration	8			nsec
t_5	SCLK low duration	8			nsec
t_6	SEN High duration	640			nsec
t_7	SEN low duration	20			nsec

A typical WRITE cycle is shown in Figure 29.

a. The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCLK.

b. The slave (synthesizer) reads SDI on the 1st rising edge of SCLK after SEN. SDI low initiates the WRITE cycle (/WR)

c. Host places the six address bits on the next six falling edges of SCLK, MSB first.

d. Slave registers the address bits in the next six rising edges of SCLK (2-7).

e. Host places the 24 data bits on the next 24 falling edges of SCK, MSB first .

f. Slave registers the data bits on the next 24 rising edges of SCK (8-31).

g. SEN is de-asserted on the 32nd falling edge of SCLK.

h. The 32nd rising edge of SCLK completes the cycle

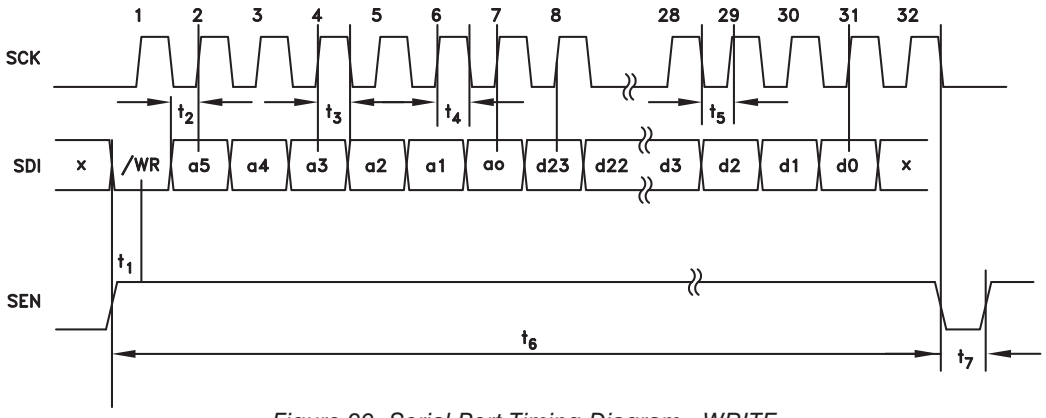


Figure 29. Serial Port Timing Diagram - WRITE

Main Serial Port READ Operation

The synthesizer uses the multi-purpose pin, *LD_SDO*, for both Lock Detect and Serial Data Out (SDO) functions. The registers *lkd_to_sdo_automux_en (Reg1A<12>)* and *lkd_to_sdo_always* (*Reg1A<13>* Table 36) determine how the Data Output pin is muxed with the Lock Detect function. If both of the registers are cleared, then the pin is exclusively SDO. If automux is enabled, the pin switches to SDO when the RD function is sensed on the 1st rising edge of SCLK. If *lkd_to_sdo_always* is set, then the pin *LD_SDO* is dedicated for Lock Detect only, and it is not possible to read from the synthesizer.

A typical READ cycle is shown in Figure 30.

a. The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCLK

b. The slave (synthesizer) reads SDI on the 1st rising edge of SCLK after SEN. SDI high initiates the READ cycle (RD)

c. Host places the six address bits on the next six falling edges of SCLK, MSB first.

d. Slave registers the address bits on the next six rising edges of SCLK (2-7).

e. Slave places the 24 data bits on the next 24 rising edges of SCK (8-31), MSB first .

f. Host registers the data bits on the next 24 falling edges of SCK (8-31).

g. SEN is de-asserted on the 32nd falling edge of SCLK.

h. The 32nd falling edge of SCLK completes the cycle

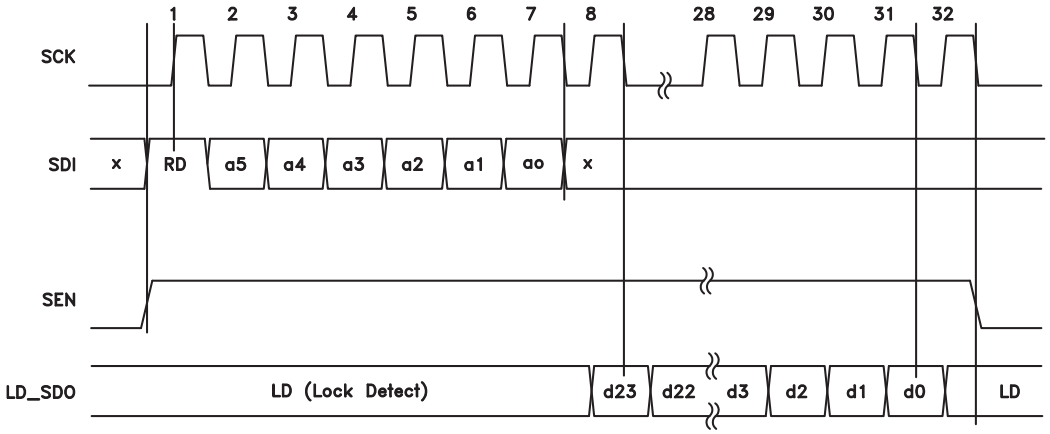


Figure 30. Serial Port Timing Diagram - READ

VCO SERIAL PORT

The VCO Serial Port is a 3-wire serial port that may be used to control external step tuned VCOs that support serial port control. Visit the Hittite website or contact Hittite Sales for a full list of compatible VCOs. The VCO Serial Port is a 3-wire serial port that may be used to control external step tuned VCOs that support serial port control. The 3-wire VCO serial port uses the following pins, as shown in Figure 31:

VSDO: VCO Serial Port Data Out
VSCK: VCO Serial Port Clock
VSLE: VCO Serial Port Latch Enable

The VCO Serial Port transfers the contents of the 16-bit register *spivco_direct_data* (*Reg0Bh* Table 22) to the VCO upon receipt of a frequency change command. The lsbs of *spivco_direct_data* are the switch settings for the VCO and may be set directly or by the autotune routine described in the section Step Tuned VCO Support. Multiple VCO formats are supported for autotuning. VCO tuning bits are configured with *sar_bits_number* (*Reg0Dh<5:4>* Table 24). Multiple VCO SPI formats are also supported and are configured by *spivco_mode* (*Reg0Dh<1:0>* Table 24).

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

The msbs of *Reg0Bh*, are VCO control bits and are also VCO specific. The VCO should be designed to only register the data upon receipt of the latch signal, VSLE.

Multiple VCO control can be implemented by addressing the individual VCOs.

VCO Serial Port WRITE Operation

DVDD = 3V ±10%, DGND = 0V

Table 5. Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	VSLE to VSDO setup time	8			nsec
t_2	VSDO to VSCK setup time	10			nsec
t_3	VSDO to VSCK hold time	10			nsec
t_4	VSCK high duration	8			nsec
t_5	VSCK low duration	8			nsec
t_6	VSLE high duration	8			nsec

VCO Serial port status is flagged in Read Only register *spi_vco_busy* (*Reg1Fh<4>* Table 41).

Individual step tuned VCOs may have different capabilities, such as power down, or divide by two outputs, and may also have different number of switches in the resonator. The HMC701LP6CE can adapt its control format and number of tuning bits used in the autotuning routine as described in *Reg0Dh* Table 24.

16-Bit VCO Write Cycle

HMC VCOs that support the 16-bit write cycle described here are fully addressable via the VSPI control.

A typical 16-bit VCO WRITE cycle is shown in Figure 31.

a. The Synthesizer (Master) both clears VSLE (VCO Serial Port Latch) and places data bit d8 (msb) on VSDO.
b. the synthesizer places a rising edge on VSCK to shift d8 into the VCO
c. Synthesizer places the next eight data bits, d7:d0, on the next eight falling edges of VSCLK, LSB last.
d. The synthesizer clocks each data bit on the next eight rising edges of VSCLK .
e. Synthesizer places the next four VCO Register bits, r3:r0, on the next four falling edges of VSCLK, LSB last.
f. Synthesizer places the next three VCO address bits, a2:a0, on the next three falling edges of VSCLK, LSB last.
g. The synthesizer asserts VSLE after the falling edge of the 16th VSCK, which latches the data into the VCO
h. the synthesizer clears VSLE to complete the cycle

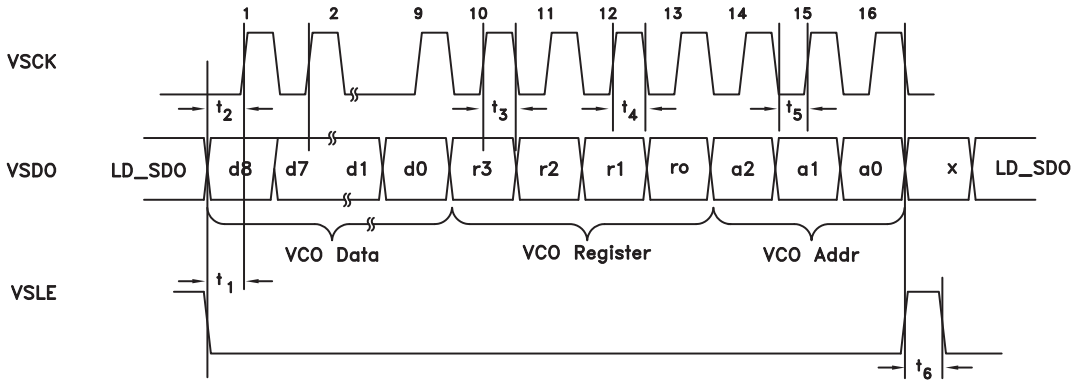


Figure 31. VCO Serial Port Timing Diagram - WRITE ONLY

Typical Step Tuned VCO Register Map

Step Tuned VCO Registers Example

Note: HMC step tuned VCOs come in different configurations. The following four registers give examples of typical control registers in HMC step tuned VCOs. Consult the VCO data sheet to confirm available VCO features.

Table 6. VSPI Format

Bit	Name	Width	Default	Description
[2:0]	VCO ID	3	n/a	VCO Address, MSB First
[6:3]	VCO Register Address	4	n/a	VCO Register Address
[15:7]	VCO Data	9	n/a	VCO Data Bits

Table 7. VCO R00 *(Switch Controller Register)*

Bit	Name	Width	Default	Description
[0]	Enable Calibration	1	0	Reserved for Calibration mode, forces a locally generated temperature compensated voltage on the VCO tuning port
[6:1]	Tune control	6	100000 b	6 bit tuning control 000000 minimum tuning capacitance 000001 next to minimum ... 111111 maximum tuning capacitance
[8:7]	Not Used	2		Not Used

Table 8. VCO R01 *(Enable Register)*

Bit	Name	Width	Default	Description
[3:0]	Reserved	4	x	Reserved
[4]	PLL Buffer En	1	1	PLL Buffer Enable (Low power output to PLL)
[5]	Divider En	1	1	Divider Enable (if present)
[6]	Buffer En	1	1	Buffer Enable (High power RF output to application)
[7]	VCO En	1	1	VCO Enable
[8]	Global En	1	1	Global Enable 0: Forces all cells to power down state 1: Enables individual Cell state control via bits 4 thru 7.

Table 9. VCO R02 *(Bias Control Register)*

Bit	Name	Width	Default	Description
[1:0]	PLL Buffer Bias Bits (MSB:LSB)	2	1	0: Min Bias 1: Next to min bias 2: Next to max bias 3: Max Bias
[3:2]	Divider or Doubler Bias Bits (MSB:LSB), if present in VCO	2	00	0: Min Bias 1: Next to min bias 2: Next to max bias 3: Max Bias
[5:4]	Mixer Buffer Bias Bits (MSB:LSB)	2	00	0: Min Bias 1: Next to min bias 2: Next to max bias 3: Max Bias
[8:6]	Reserved	3		

Table 10. VCO R03 *(Temperature & Gain Control Register)*

Bit	Name		Default	Description
[4:0]	Reserved	5	x	Reserved
[6:5]	Temp Compensation Offset Control (MSB: LSB)	2	1	0: Reduce Tuning voltage 50mV 1: Use default Tuning voltage 2: Increase Tuning voltage 50mV 3: Increase Tuning voltage 100mV
[8:7]	PLL Buffer Gain Control (MSB: LSB)	2	1	0: Min Gain 1: Next to Min Gain 2: Next to Max Gain 3: Max Gain

REGISTER MAP

Reg 00h Chip ID (Read Only) Register

Bit	Type	Name	Width	Default	Description
[23:0]	Ro	Chip ID	24	581502	Chip ID

Table 11. Reg 00h Strobe (Write Only) Register

Bit	Type	Name	Width	Default	Description
0	STR	global_swrst_regs	1	0	Strobe to soft reset the SPI registers
1	STR	global_swrst_dig	1	0	Strobe to soft reset the rest of digital
2	STR	mcnt_resynch	1	0	Reserved
3	STR	tsens_spi_strobe	1	0	Strobe to clock the temp measurement on demand

Table 12. Reg 01h Enable & Reset Register

Bit	Type	Name		Default	Description
0	R/W	malg_vcobug_en	1	1	VCO Buffer Enable
1	R/W	mag_bias_en	1	1	Bias enable
2	R/W	rfp_div_en	1	0	Enables / Holds refdiv in reset Holding Ref divider in reset is equivalent to bypassing the divider, see Figure 10
3	R/W	xrefmux_todig_en	1	1	Enables clock gate for xtal muxed (sq or sin) reference to digital
4	R/W	rfp_div_todig_en	1	0	Enables divided reference clock to the digital see Figure 10
5	R/W	rfp_sqr_todig_en	1	0	Enables square wave xtal clock to main digital see Figure 10
6	R/W	rfp_sin_todig_en	1	0	Enables sine wave xtal clock to main digital see Figure 10
7	R/W	rfp_bug_sq_en	1	1	Enables Square wave Ref Buffer, see Figure 10
8	R/W	rfp_bug_sin_en	1	0	Enables Sine wave Ref Buffer, see Figure 10
9	R/W	vcop_todig_en	1	0	1= divided VCO as digital, ΔΣ modulator clock 0= Divided Ref path as the
10	R/W	vcop_presc_en	1	1	Enables the prescaler bias
11	R/W	pfd_lkd_en	1	0	Enable / Resetb to digital lockdetect circuit and PFD's lockdetect output gates
12	R/W	cp_en	1	1	Charge Pump Enable, disable is tri-stated output
13	R/W	dsm_rstb	1	0	1 - Enables fractional modulator see also *dsm_integer_mode Reg12h<3>*
14	R/W	lkd_rstb	1	0	1 - enables lock detect circuit
15	R/W	pfds_rstb	1	1	CSP PFD FF rstb 1 - Enables the Cycle Slip Prevention (CSP) feature of the PFD

Table 13. Reg 02h Serial Data Out Force Register

Bit	Type	Name	Default	Description
0	R/W	malg_sdo_driver_force_val	1	Serial Data Out Force value This value may be forced onto LD_SDO by setting malg_sdo_driver_force_en
1	R/W	malg_sdo_driver_force_en	1	Serial Data Out EN Force enable Places value from malg_sdo_driver_force_val on SDO

Table 14. Reg 03h Reference Path Register

Bit	Type	Name	Default	Description
13:0	R/W	rfp_div_ratio also referred to as 'R'	0	Divides the crystal input by this number 'R' if rfp_div_en=1 and rfp_div_select = 1 rfp_div_ratio = 0 not allowed 2<=div_ratio<=2^14 see Figure 10
14	R/W	rfp_div_select	0	1 = reference divider enabled 0 = bypass ref divider see Figure 10
15	R/W	rfp_auto_refdiv_sel_en	0	1 = auto ref divider enable or bypass is automatic if rfp_div_ratio = 1, bypass divider if rfp_div_bypass ~=1 use divider see Figure 10
16	R/W	rfp_buf_sin_sel	0	Selects sine wave reference for normal operation see Figure 10

Table 15. Reg 04h Prescaler Duty Cycle Register

Bit	Type	Name	Default	Description
0	R/W	vcop_dutycycmode	0	Extends the low time from 15 to 47 VCO cycles for large divide ratios

Table 16. Reg 05h Phase Freq Detector Register (pfd)

Bit	Type	Name	Default	Description
0	R/W	pfd_phase_sel	0	Inverts PFD Polarity 0 = Passive Filter +ve slope VCO 1 = Passive Filter -ve slope VCO 1 = Active inverting filter, +ve slope VCO 0 = Active inverting filter, -ve slope VCO
1	R/W	pfd_upout_en	1	Allows masking of the up outputs between PFD and CP
2	R/W	pfd_dnout_en	1	Allows masking of the dn outputs between PFD and CP

Table 17. Reg 06h Phase Freq Detector Delay Register

Bit	Type	Name	Default	Description
2:0	R/W	pfd_del_sel	2	Delay line setpoint to PFD

Table 18. Reg 07h Charge Pump UP/DN Control Register

Bit	Type	Name	Default	Description
4:0	R/W	cp_UPcurrent_sel	16	Sets Charge-Pump Up gain, 125uA lsb, binary, 4mA max
9:5	R/W	cp_DNcurrent_sel	16	Sets Charge-Pump Dn gain, 125uA lsb, binary, 4mA max

Table 19. Reg 08h Charge Pump Trim & Offset Register

Bit	Type	Name	Default	Description
3:0	R/W	cp_UPtrim_sel	0	Trim Up gain, 14.3uA lsb, binary, 100uA max
7:4	R/W	cp_DNtrim_sel	0	Trim Dn gain, 14.3uA lsb, binary, 100uA max
11:8	R/W	cp_UPoffset_sel	4	Up Offset leakage current, 28.7uA lsb, binary, 430uA max
15:12	R/W	cp_DNoffset_sel	0	Dn Offset leakage current, 28.7uA , binary, 430uAmax
17:16	R/W	cp_amp_bias_sel	2	Charge Pump Dummy Branch Op amp bias selection, 100uA

Table 20. Reg 09h Charge Pump EN Register

Bit	Type	Name	Default	Description
0	R/W	cp_pull_updn_en	0	Enables CP UP/Down Control Reg09 [1]
1	R/W	cp_pull_dn_upb	0	0 - Forces Charge Pump Up when Reg09[0]=1 1 - Forces Charge Pump DN when Reg09[0]=1

Table 21. Reg 0Ah VCO Auto Tune & Control Register

Bit	Type	Name	Default	Description
0	R/W	vcot_auto_start	0	Enables Auto start of VCO cap tuning when frac word is written to spi
1	R/W	vcot_man_start	0	Starts manual vco tuning when auto_start=0 (must be cleared to 0 before another tune)
5:2	R/W	vcot_ncyc_rdiv	2	Exponent selection for number of rdiv cycles to wait during measurement (effects time to perform the measurement and hence the accuracy)
6	R/W	vcot_invert_outdata	0	Inverts the vco tuning cap polarity
7	R/W	vcot_swap_outdata	0	Swaps the cap tuning data (left-to-right)
8	R/W	vcot_force_data_en	0	Force enable for the VCO tuning cap word - Obsolete
9	R/W	vcot_force_dblbuff_mode	0	Enables double buffer for vco caps. Caps will go to the vco when dsm_frac reg is written
11:10	R/W	vcot_xrefdiv_sel	0	xref divider generate vco tuning calibration clock, and VCO Serial Port Clock VSCK from the crystal input (see Figure 10) . This divider affects calibration time and accuracy, currently only divby1 is supported 00-->div by 1 01-->div by 2 not supported 10-->div by 4 not supported 11-->div by 8 not supported

Table 22. Reg 0Bh VCO Tuning & Control Register

Bit	Type	Name	Default	Description
15:0	R/W	spivco_direct_data	0	Used to set VCO control settings VCO Specific, see VCO SERIAL PORT description

Table 23. Reg 0Ch VCO Auto Tune Wait Register

Bit	Type	Name	Default	Description
13:0	R/W	vcot_initial_wait	256	Initial wait time (xtal cycles) after tri-stating charge-pump to start VCO tuning

Table 24. Reg 0Dh VCO Control Register

Bit	Type	Name	Default	Description
1:0	R/W	spivco_mode	0	Support for different VCO SPI formats 0: 16-bit VSPI 1: 10-bit VSPI with 5-bit SAR 2: 10-bit VSPI with 6-bit SAR 3: blank VCOSPI data
3:2	R/W	f1_modesel	0	CSP Speedup Function Increases CSP current when Lock Detect window exceeds threshold 0: disabled 1: 1nsec threshold 2: 3nsec threshold 3: 5nsec threshold
5:4	R/W	sar_bits_number	0	Autotune Successive Approximation Register (SAR) Autotune Algorithm supports VCOs with 5, 6, 7 or 8-bit step tuning 8-n = SAR bits 0: 8 bit SAR 1: 7 bit SAR 2: 6 bit SAR 3: 5 bit SAR
6	R/W	autocal_when_unlocked	0	0 : disabled 1: automatically runs the autotuning routine to relock the VCO if loss of lock is detected

Table 25. Reg 0Eh Reserved

Bit	Type	Name	Default	Description
23:0	R/W	Reserved	0	Reserved

Table 26. Reg 0Fh Integer Division Register

Bit	Type	Name	Default	Description
15:0	R/W	dsm_intg	200d	unsigned integer portion of VCO divider value, also known as N_{INT}, see (EQ 12)

Table 27. Reg 10h Fractional Division Register

Bit	Type	Name	Default	Description
23:0	R/W	dsm_frac	0	unsigned fractional portion of VCO divider also known as N_{FRAC}, see (EQ 12)

Table 28. Reg 11h Seed Register

Bit	Type	Name	Default	Description
23:0	R/W	dsm_seed	0	unsigned seed value for ΔΣ modulator sets the start phase of the modulator

Table 29. Reg 12h Delta Sigma Modulator Register

Bit	Type	Name	Default	Description
0	R/W	dsm_ref_clk_select	0	use reference instead of divider
1	R/W	dsm_invert_clk_sd3	1	invert ΔΣ clk
2	R/W	dsm_invert_clk_rph	0	inverts the ref clock phase
3	R/W	dsm_integer_mode	0	1- enables Integer Mode, bypasses the ΔΣ modulator, leaves it running see also dsm_rstb Reg01h<13> to disable the modulator
4	R/W	Reserved	0	
5	R/W	Reserved	0	
6	R/W	dsm_xref_sin_select	0	when xref is selected specifies that the sine source is used
7	R/W	dsm_autoseed	1	automatic seed load when changing the frac part, uses value in seed
9:8	R/W	dsm_order	2	00-first order 01-second 10-third fb 11-third ff
13:10	R/W	dsm_quant_max	4'b0111	max value allowed out of ΔΣ modulator quantizer limits are +7 to -8, typ ±3 or ±4
17:14	R/W	dsm_quant_min	4'b1000	min value allowed out of ΔΣ modulator quantizer limits are +7 to -8, typ ±3 or ±4

Table 30. Reg 14h CW Sweep Control Register

Bit	Type	Name	Default	Description
0	R/W	clear_ovf_undf	0	asynchronous clear for ovf/undf flags
1	R/W	ramp_enable	0	Ramp En/rstb 1= enables the CW Ramp Function
2	R/W	ramp_trigg	0	Write always triggers ramps if bit <2> = 0, if bit <2> = 1, Ramp will not trigger, bit <2> must be reset to 0 first
3	R/W	ramp_repeat_en	0	Ramp Repeat Seq enable 1= enables autotrigger of ramps 0 = ramp_trigg starts each ramp
4	R/W	ramp_startdir_dn	0	Ramp start direction 1= Start with Ramp Down 0= Start with Ramp Up
5	R/W	ramp_trig_ext_en	0	Enable hardware trigger on GPO3 pin
6	R/W	ramp_singlestep	0	Ramp single step, advances the ramp to the next step, and holds frequency
7	R/W	ramp_singledir	0	Ramps in one direction only with hop to start at end of ramp

Table 31. Reg 15h CW Sweep Ramp Step Register

Bit	Type	Name	Default	Description
23:0	R/W	ramp_step	2048	Ramp Step size

Table 32. Reg 16h CW Sweep Ramp Step Number Register

Bit	Type	Name	Default	Description
23:0	R/W	ramp_steps_number	2048	Ramp Number of steps in ramp

Table 33. Reg 17h CW Sweep Dwell Time Register

Bit	Type	Name	Default	Description
23:0	R/W	ramp_dwell_time	2048	Ramp Number of cycles to hold at top/bottom in repeat mode

Table 34. Reg 18h Auxiliary Oscillator Register 1

Bit	Type	Name	Default	Description
1:0	R/W	dsmclk_auxclk_insel	0	Selects the input clk for auxclk 0:vcodiv 1:xrefsq or sin 2:refdiv 3:ring oscillator from mono, est 300 MHz to 1 GHz
3:2	R/W	dsmclk_auxclk_modesel	0	0: bypass-no delay 1: pass through w/ delay 2: ring-out constant 3: ring-out seeded/gated
6:4	R/W	dsmclk_auxclk_divsel	2	divider selection auxclk value divby 000 1 001 2 010 4 011 6 100 8 101 10 110 12 111 14
7	R/W	dsmclk_auxclk_sel	0	selects auxclk (if=1) as natural reference clk input of sigma delta
8	R/W	dsmclk_auxmod_lfsr_en	0	enables 10-bit lfsr inside the delay modulator (clocked by auxclk or auxclkb)
9	R/W	dsmclk_auxmod_accum_en	0	enables 8-bit accumulator inside the delay modulator (clocked by auxclk or auxclkb)
11:10	R/W	dsmclk_auxmod_mode	0	delay modulation mode 0: auxmod_lodly_in passthrough 1: accumulator based square-wave 2: lfsr (lo-amp) 3: lfsr (hi-amp)
19:12	R/W	dsmclk_auxmod_fracstep	3	step-size of accumulator (changes square-wave value once it wraps through 256)
22:20	R/W	dsmclk_auxmod_lodly	0	value of delay-element (when auxmod_mode=0) or low value used during sq-wave modulation

Table 35. Reg 19h Auxiliary Oscillator Register 2

Bit	Type	Name	Default	Description
2:0	R/W	dsmclk_auxmod_hidly	7	hi value of delay element during sq-wave modulation
3	R/W	dsmclk_auxmod_clkinv	1	optionally inverts auxclk as used by the modulator
4	R/W	dsmclk_auxmod_clkwring	9	select LKD ringosc to clock the LFSR

Table 36. Reg 1Ah Lock Detect Register

Bit	Type	Name	Default	Description
9:0	R/W	lkd_wincnt_max	10'd40	threshold count in the timer window to declare lock (reference cycles)
10	R/W	lkd_win_asym_enable	0	Enables asymmetric lock detect window (nominal 10nsec)
11	R/W	lkd_win_asym_up_select	0	Sets polarity of the window
12	R/W	lkd_to_sdo_automux_en	0	Muxes the lkd output signal to SDO when SDO is not being used for Main Serial Port Data Outputs (Read Operation)
13	R/W	lkd_to_sdo_always	0	Muxes the lkd output signal to SDO always, not possible to do Main Serial Port Read in this state
14	R/W	lkd_ringosc_mono_select	0	1 select ringosc based oneshot for lock detect window 0 selects analog based oneshot
16:15	R/W	lkd_ringosc_cfg	0	"00" fastest "11" slowest
18:17	R/W	lkd_monost_duration	0	"00" shortest "11" longest
19	R/W	lkd_ringosc_testmode	0	enables the ring osc by itself for testing

Table 37. Reg 1Bh GPO Control Register

Bit	Type	Name	Default	Description
3:0	R/W	gpo_sel	0	Selects data to be driven on GPO ports
		gpo_sel<3:0> = 0000		GPO3 <=gposel_0_data<2> GPO2 <= gposel_0_data<1> GPO1 <= gposel_0_data<0>
		gpo_sel<3:0> = 0001		GPO3 <= xref_clk_in GPO2 <= ref_clk_in GPO1 <= vco_div_clkin
		gpo_sel<3:0> = 0010		GP03 <= pfd_up_in GP02 <= pfd_dn_in GP01 <= LKD_monost_window
		gpo_sel<3:0> = 0011		GP03 <= pfd_sat_ref_in GP02 <= pfd_sat_vco_div_in GP01 <= delta_integer_cycslip_sel, this strobe holds the gain of the PFD at max for anti-cycle slipping
		gpo_sel<3:0> = 0100		GP03 <= xref_clk_in GP02 <= xref_sin_in GP01 <= sd_frac_strobe_sync, internally synchronized frac strobe
		gpo_sel<3:0> = 0101		VCO Serial Port Mirror GPO3 - VSDO GPO2 = VSCK GPO1 = SVLE
		gpo_sel<3:0> = 0110		GP03 <= SD_Intz1<1> GP02 <=SD_Intz1<2> GP01 <= SD_Intz1<3> 3-bit quantized version of the VCO phase
		gpo_sel<3:0> = 0111		GP03 <= aux_clk GP02 <= ringosc_test GP01 <= clk_SD
		gpo_sel<3:0> = 1000		GP03 <= 00 GP02 <= ramp_busy GP01 <= vcot_busy
		gpo_sel<3:0> = 1001		Not used
		gpo_sel<3:0> = 1010		GP03 <= ΔΣ Quantizer Output 3rd lsb GP02 <= ΔΣ Quantizer Output 2nd lsb GP01 <= ΔΣ Quantizer Output lsb
6:4	R/W	gpo_sel_0_data		this data is driven on gpo if gpo_sel==0
7	R/W	gpo_dig_drive_en		enables Tri-state drivers on GPO output pads
10:8	R/W	Chip ID 478732 Reserved Chip ID 481502 gpo_ind_drive_dis	0 0	reserved must write 0 on Chip ID 478732 Chip ID 481502 Only 000 = all GPO pad drivers enabled xx1 = disable GPO1 pad driver x1x = disable GPO2 pad driver 1xx = disable GPO3 pad driver

Table 38. Reg 1Ch Phase Detector CSP Register

Bit	Type	Name	Default	Description
3:0	R/W	pfds_sat_deltaN	5'd4	0= Cycle Slip Prevention (CSP) disabled 4-bit value to advance or retard phase detector in VCO cycles if it reaches 2pi , i.e. cycle slip prevention. 1st bit is polarity, enabled by rstb
4	R/W	pfds_rstb_force	0	CSP PFD Flip-flops RSTB: 1 - controlled by the pfds_rstb bit: 0 - auto-controlled by the CSP logic Forces the PFD into reset, which tristates charge pump, freezes charge on the loop filter, and hence opens the loop
5	R/W	pfds_rstb	1	CSP PFD FF rstb 1 - Enables the Cycle Slip Prevention (CSP) feature of the PFD

Table 39. Reg 1Dh VCO Tune Port Control Register

Bit	Type	Name	Default	Description
0	R/W	voltage_force	0	Selects the source of control of the timing of the mid-rail voltage, voltage_force=0 selects Autotune state machine voltage_force=1 selects voltage_enable from SPI Used for mid-rail control of VCO during autotuning
1	R/W	voltage_enable	0	Forces mid-rail voltage on the charge pump output from the SPI when voltage_force=1 Used for mid-rail control of VCO during autotuning

Table 40. Reg 1Eh Temperature Sensor Register

Bit	Type	Name	Default	Description
0	R/W	tsens_spi_enable	0	Enable the temperature sensor, draws ~2mA current, must strobe tsens_spi_strobe Reg 00h <3>

Table 41. Reg 1Fh LD, VCO & Ramp Busy Read Only Register

Bit	Type	Name	Default	Description
0	RO	ro_lock_detect	0	1 = locked, 0 = unlocked
3:1	RO	ro_dsm_overflow	0	1 = modulator overflow
4	RO	ro_spi_vco_busy	0	Set when VCO autotuning is running
5	RO	ro_ramp_busy	0	Sweeper status flag, set when ramp is busy, cleared when at end of ramp or not used

Table 42. Reg 20h VCO Tune Caps Read Only Register (vcot)

Bit	Type	Name	Default	Description
5:0	RO	vcot_caps	0	Reads the values of the VCO switched resonator bank determined by the autotune routine (see) 0 = max VCO freq 63 = min VCO freq

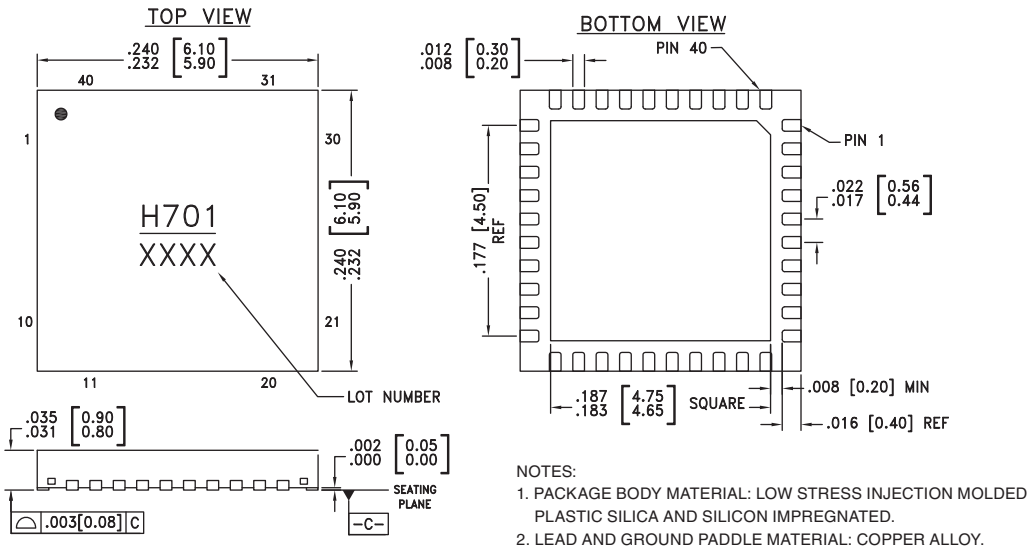
Table 43. Reg 21h Temperature Sensor Read Only Register

Bit	Type	Name	Default	Description
6:0	RO	tsens_temperature	0	Current Temperature from temp sensor lsb = 17.5°C 0000111 = Temp >= 82.5°C 0000110 = Temp 0000000 = Temp <=-22.5°C tsens_temperature = floor ((Temp+40)/17.5)

Table 44. Reg 22h Autotune Result Register

Bit	Type	Name	Default	Description
16:0	RO	vcot_cnt	0	Contains the results of the autotune counter Can be used to calculate the VCO frequency and optimum VCO setting selected by the autotune

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC701LP6CE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H701 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C