ELPIDA

1GB DDR2 SDRAM SO-DIMM

EBE10UE8AFSA (128M words × 64 bits, 1 Rank)

Specifications

- Density: 1GB
- Organization
— 128M words × 64 bits, 1 rank
- Mounting 8 pieces of 1G bits DDR2 SDRAM sealed in FBGA
- Package: 200-pin socket type small outline dual in line memory module (SO-DIMM)
— PCB height: 30.0mm
— Lead pitch: 0.6mm
— Lead-free (RoHS compliant) and Halogen-free
- Power supply: VDD = 1.8V ± 0.1V
- Data rate: 800Mbps/667Mbps (max.)
- Eight internal banks for concurrent operation (components)
- Interface: SSTL_18
- Burst lengths (BL): 4, 8
- /CAS Latency (CL): 3, 4, 5, 6
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/64ms
— Average refresh period
7.8μs at 0°C ≤ TC ≤ +85°C
3.9μs at +85°C < TC ≤ +95°C
- Operating case temperature range
— TC = 0°C to +95°C

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 4 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver Impedance Adjustment and On-Die-Termination for better signal quality
- /DQS can be disabled for single-ended Data Strobe operation

Ordering Information

Part number	Data rate Mbps (max.)	Component JEDEC speed bin (CL-tRCD-tRP)	Package	Contact pad	Mounted devices
EBE10UE8AFSA-8G-F	800	DDR2-800 (6-6-6)	200-pin SO-DIMM (lead-free and halogen-free)	Gold	EDE1108AFSE-8E-F EDE1108AFSE-8G-F
EBE10UE8AFSA-6E-F	667	DDR2-667 (5-5-5)			EDE1108AFSE-8E-F EDE1108AFSE-8G-F EDE1108AFSE-6E-F

Pin Configurations
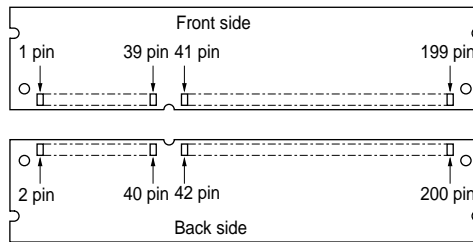
Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	51	DQS2	2	VSS	52	DM2
3	VSS	53	VSS	4	DQ4	54	VSS
5	DQ0	55	DQ18	6	DQ5	56	DQ22
7	DQ1	57	DQ19	8	VSS	58	DQ23
9	VSS	59	VSS	10	DM0	60	VSS
11	/DQS0	61	DQ24	12	VSS	62	DQ28
13	DQS0	63	DQ25	14	DQ6	64	DQ29
15	VSS	65	VSS	16	DQ7	66	VSS
17	DQ2	67	DM3	18	VSS	68	/DQS3
19	DQ3	69	NC	20	DQ12	70	DQS3
21	VSS	71	VSS	22	DQ13	72	VSS
23	DQ8	73	DQ26	24	VSS	74	DQ30
25	DQ9	75	DQ27	26	DM1	76	DQ31
27	VSS	77	VSS	28	VSS	78	VSS
29	/DQS1	79	CKE0	30	CK0	80	NC
31	DQS1	81	VDD	32	/CK0	82	VDD
33	VSS	83	NC	34	VSS	84	NC
35	DQ10	85	BA2	36	DQ14	86	NC
37	DQ11	87	VDD	38	DQ15	88	VDD
39	VSS	89	A12	40	VSS	90	A11
41	VSS	91	A9	42	VSS	92	A7
43	DQ16	93	A8	44	DQ20	94	A6
45	DQ17	95	VDD	46	DQ21	96	VDD
47	VSS	97	A5	48	VSS	98	A4
49	/DQS2	99	A3	50	NC	100	A2

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
101	A1	151	DQ42	102	A0	152	DQ46
103	VDD	153	DQ43	104	VDD	154	DQ47
105	A10/AP	155	VSS	106	BA1	156	VSS
107	BA0	157	DQ48	108	/RAS	158	DQ52
109	/WE	159	DQ49	110	/CS0	160	DQ53
111	VDD	161	VSS	112	VDD	162	VSS
113	/CAS	163	NC	114	ODT0	164	CK1
115	NC	165	VSS	116	A13	166	/CK1
117	VDD	167	/DQS6	118	VDD	168	VSS
119	NC	169	DQS6	120	NC	170	DM6
121	VSS	171	VSS	122	VSS	172	VSS
123	DQ32	173	DQ50	124	DQ36	174	DQ54
125	DQ33	175	DQ51	126	DQ37	176	DQ55
127	VSS	177	VSS	128	VSS	178	VSS
129	/DQS4	179	DQ56	130	DM4	180	DQ60
131	DQS4	181	DQ57	132	VSS	182	DQ61
133	VSS	183	VSS	134	DQ38	184	VSS
135	DQ34	185	DM7	136	DQ39	186	/DQS7
137	DQ35	187	VSS	138	VSS	188	DQS7
139	VSS	189	DQ58	140	DQ44	190	VSS
141	DQ40	191	DQ59	142	DQ45	192	DQ62
143	DQ41	193	VSS	144	VSS	194	DQ63
145	VSS	195	SDA	146	/DQS5	196	VSS
147	DM5	197	SCL	148	DQS5	198	SA0
149	VSS	199	VDDSPD	150	VSS	200	SA1

Pin Description

Pin name	Function
A0 to A13	Address input Row address A0 to A13 Column address A0 to A9
A10 (AP)	Auto precharge
BA0, BA1, BA2	Bank select address
DQ0 to DQ63	Data input/output
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0	Chip select
CKE0	Clock enable
CK0, CK1	Clock input
/CK0, /CK1	Differential clock input
DQS0 to DQS7, /DQS0 to /DQS7	Input and output data strobe
DM0 to DM7	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0, SA1	Serial address input
VDD	Power for internal circuit
VDDSPD	Power for serial EEPROM
VREF	Input reference voltage
VSS	Ground
ODT0	ODT control
NC	No connection

Serial PD Matrix

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80H	128 bytes
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08H	256 bytes
2	Memory type	0	0	0	0	1	0	0	0	08H	DDR2 SDRAM
3	Number of row address	0	0	0	0	1	1	1	0	0EH	14
4	Number of column address	0	0	0	0	1	0	1	0	0AH	10
5	Number of DIMM ranks	0	1	1	0	0	0	0	0	60H	1
6	Module data width	0	1	0	0	0	0	0	0	40H	64
7	Module data width continuation	0	0	0	0	0	0	0	0	00H	0
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	1	05H	SSTL 1.8V
9	DDR SDRAM cycle time, CL = X -8G (CL = 6)	0	0	1	0	0	1	0	1	25H	2.5ns*[1]
	-6E (CL = 5)	0	0	1	1	0	0	0	0	30H	3.0ns*[1]
10	SDRAM access from clock (tAC) -8G	0	1	0	0	0	0	0	0	40H	0.4ns*[1]
	-6E	0	1	0	0	0	1	0	1	45H	0.45ns*[1]
11	DIMM configuration type	0	0	0	0	0	0	0	0	00H	None
12	Refresh rate/type	1	0	0	0	0	0	1	0	82H	7.8μs
13	Primary SDRAM width	0	0	0	0	1	0	0	0	08H	× 8
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00H	None
15	Reserved	0	0	0	0	0	0	0	0	00H	0
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	0	0	0CH	4,8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	1	0	0	0	08H	8
18	SDRAM device attributes: /CAS latency -8G	0	1	1	1	0	0	0	0	70H	4, 5, 6
	-6E	0	0	1	1	1	0	0	0	38H	3, 4, 5
19	DIMM Mechanical Characteristics	0	0	0	0	0	0	0	1	01H	3.80mm max.
20	DIMM type information	0	0	0	0	0	1	0	0	04H	SO-DIMM
21	SDRAM module attributes	0	0	0	0	0	0	0	0	00H	Normal
22	SDRAM device attributes: General	0	0	0	0	0	0	1	1	03H	Weak Driver 50Ω ODT Support
23	Minimum clock cycle time at CL = X − 1 -8G (CL = 5)	0	0	1	1	0	0	0	0	30H	3.0ns*[1]
	-6E (CL = 4)	0	0	1	1	1	1	0	1	3DH	3.75ns*[1]
24	Maximum data access time (tAC) from clock at CL = X − 1 -8G (CL = 5)	0	1	0	0	0	1	0	1	45H	0.45ns*[1]
	-6E (CL = 4)	0	1	0	1	0	0	0	0	50H	0.5ns*[1]
25	Minimum clock cycle time at CL = X − 2 -8G (CL = 4)	0	0	1	1	1	1	0	1	3DH	3.75ns*[1]
	-6E (CL = 3)	0	1	0	1	0	0	0	0	50H	5.0ns*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
26	Maximum data access time (tAC) from clock at CL = X − 2 -8G (CL = 4)	0	1	0	1	0	0	0	0	50H	0.5ns[1]
	-6E (CL = 3)	0	1	1	0	0	0	0	0	60H	0.6ns[1]
27	Minimum row precharge time (tRP)	0	0	1	1	1	1	0	0	3CH	15ns
28	Minimum row active to row active delay (tRRD)	0	0	0	1	1	1	1	0	1EH	7.5ns
29	Minimum /RAS to /CAS delay (tRCD)	0	0	1	1	1	1	0	0	3CH	15ns
30	Minimum active to precharge time (tRAS)	0	0	1	0	1	1	0	1	2DH	45ns
31	Module rank density	0	0	0	0	0	0	0	1	01H	1G bytes
32	Address and command setup time before clock (tIS) -8G	0	0	0	1	0	1	1	1	17H	0.17ns[1]
	-6E	0	0	1	0	0	0	0	0	20H	0.20ns[1]
33	Address and command hold time after clock (tIH) -8G	0	0	1	0	0	1	0	1	25H	0.25ns[1]
	-6E	0	0	1	0	0	1	1	1	27H	0.27ns[1]
34	Data input setup time before clock (tDS) -8G	0	0	0	0	0	1	0	1	05H	0.05ns[1]
	-6E	0	0	0	1	0	0	0	0	10H	0.10ns[1]
35	Data input hold time after clock (tDH) -8G	0	0	0	1	0	0	1	0	12H	0.12ns[1]
	-6E	0	0	0	1	0	1	1	1	17H	0.17ns[1]
36	Write recovery time (tWR)	0	0	1	1	1	1	0	0	3CH	15ns[1]
37	Internal write to read command delay (tWTR)	0	0	0	1	1	1	1	0	1EH	7.5ns[1]
38	Internal read to precharge command delay (tRTP)	0	0	0	1	1	1	1	0	1EH	7.5ns[1]
39	Memory analysis probe characteristics	0	0	0	0	0	0	0	0	00H	TBD
40	Extension of Byte 41 and 42	0	0	0	0	0	1	1	0	06H	
41	Active command period (tRC)	0	0	1	1	1	1	0	0	3CH	60ns[1]
42	Auto refresh to active/ Auto refresh command cycle (tRFC)	0	1	1	1	1	1	1	1	7FH	127.5ns[1]
43	SDRAM tCK cycle max. (tCK max.)	1	0	0	0	0	0	0	0	80H	8ns[1]
44	Dout to DQS skew -8G	0	0	0	1	0	1	0	0	14H	0.20ns[1]
	-6E	0	0	0	1	1	0	0	0	18H	0.24ns[1]
45	Data hold skew (tQHS) -8G	0	0	0	1	1	1	1	0	1EH	0.30ns[1]
	-6E	0	0	1	0	0	0	1	0	22H	0.34ns[1]
46	PLL relock time	0	0	0	0	0	0	0	0	00H	Undefined

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
47 to 61		0	0	0	0	0	0	0	0	00H	
62	SPD Revision	0	0	0	1	0	0	1	0	12H	Rev. 1.2
63	Checksum for bytes 0 to 62 -8G	1	1	0	1	1	1	1	0	DEH	
	-6E	0	0	0	1	0	1	0	0	14H	
64 to 65	Manufacturer's JEDEC ID code	0	1	1	1	1	1	1	1	7FH	Continuation code
66	Manufacturer's JEDEC ID code	1	1	1	1	1	1	1	0	FEH	Elpida Memory
67 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00H	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	(ASCII-8bit code)
73	Module part number	0	1	0	0	0	1	0	1	45H	E
74	Module part number	0	1	0	0	0	0	1	0	42H	B
75	Module part number	0	1	0	0	0	1	0	1	45H	E
76	Module part number	0	0	1	1	0	0	0	1	31H	1
77	Module part number	0	0	1	1	0	0	0	0	30H	0
78	Module part number	0	1	0	1	0	1	0	1	55H	U
79	Module part number	0	1	0	0	0	1	0	1	45H	E
80	Module part number	0	0	1	1	1	0	0	0	38H	8
81	Module part number	0	1	0	0	0	0	0	1	41H	A
82	Module part number	0	1	0	0	0	1	1	0	46H	F
83	Module part number	0	1	0	1	0	0	1	1	53H	S
84	Module part number	0	1	0	0	0	0	0	1	41H	A
85	Module part number	0	0	1	0	1	1	0	1	2DH	—
86	Module part number -8G	0	0	1	1	1	0	0	0	38H	8
	-6E	0	0	1	1	0	1	1	0	36H	6
87	Module part number -8G	0	1	0	0	0	1	1	1	47H	G
	-6E	0	1	0	0	0	1	0	1	45H	E
88	Module part number	0	0	1	0	1	1	0	1	2DH	—
89	Module part number	0	1	0	0	0	1	1	0	46H	F
90	Module part number	0	0	1	0	0	0	0	0	20H	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30H	Initial
92	Revision code	0	0	1	0	0	0	0	0	20H	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
95 to 98	Module serial number										
99 to 127	Manufacture specific data										

Note: 1.These specifications are defined based on component specification, not module.

Block Diagram


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CKE0 ──RS2──/\/\──────────────────────────────────
ODT0 ──RS2──/\/\──────────────────────────────
/CS0 ──RS2──/\/\──────────────────────────
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/DQS0 ──RS1──/\/\── /DQS /CS ODT CKE
DQS0 ──RS1──/\/\── DQS
DM0 ──RS1──/\/\── DM   D0
DQ0 to DQ7 ──8──RS1──/\/\── DQ0 to DQ7

/DQS1 ──RS1──/\/\── /DQS /CS ODT CKE
DQS1 ──RS1──/\/\── DQS
DM1 ──RS1──/\/\── DM   D1
DQ8 to DQ15 ──8──RS1──/\/\── DQ0 to DQ7

/DQS2 ──RS1──/\/\── /DQS /CS ODT CKE
DQS2 ──RS1──/\/\── DQS
DM2 ──RS1──/\/\── DM   D2
DQ16 to DQ23 ──8──RS1──/\/\── DQ0 to DQ7

/DQS3 ──RS1──/\/\── /DQS /CS ODT CKE
DQS3 ──RS1──/\/\── DQS
DM3 ──RS1──/\/\── DM   D3
DQ24 to DQ31 ──8──RS1──/\/\── DQ0 to DQ7

/DQS4 ──RS1──/\/\── /DQS /CS ODT CKE
DQS4 ──RS1──/\/\── DQS
DM4 ──RS1──/\/\── DM   D4
DQ32 to DQ39 ──8──RS1──/\/\── DQ0 to DQ7

/DQS5 ──RS1──/\/\── /DQS /CS ODT CKE
DQS5 ──RS1──/\/\── DQS
DM5 ──RS1──/\/\── DM   D5
DQ40 to DQ47 ──8──RS1──/\/\── DQ0 to DQ7

/DQS6 ──RS1──/\/\── /DQS /CS ODT CKE
DQS6 ──RS1──/\/\── DQS
DM6 ──RS1──/\/\── DM   D6
DQ48 to DQ55 ──8──RS1──/\/\── DQ0 to DQ7

/DQS7 ──RS1──/\/\── /DQS /CS ODT CKE
DQS7 ──RS1──/\/\── DQS
DM7 ──RS1──/\/\── DM   D7
DQ56 to DQ63 ──8──RS1──/\/\── DQ0 to DQ7

BA0 to BA2 ──RS3──/\/\──▶ BA0 to BA2: SDRAMs (D0 to D7)
A0 to A13 ──RS3──/\/\──▶ A0 to A13: SDRAMs (D0 to D7)
/RAS ──RS3──/\/\──▶ /RAS: SDRAMs (D0 to D7)
/CAS ──RS3──/\/\──▶ /CAS: SDRAMs (D0 to D7)
/WE ──RS3──/\/\──▶ /WE: SDRAMs (D0 to D7)

CK0 ●────▶
                4 loads
/CK0 ●────▶

CK1 ●────▶
                4 loads
/CK1 ●────▶

VDDSPD ●────▶ SPD
VREF ●────▶ SDRAMs (D0 to D7)
VDD ●────▶ SDRAMs (D0 to D7, VDD and VDDQ)
VSS ●────▶ SDRAMs (D0 to D7, SPD)

Serial PD

SCL ──▶ SCL   SDA ──▶ SDA
SA0 ──▶ A0
SA1 ──▶ A1   U0
           A2   WP

Notes :
1. DQ wiring may be changed within a byte.
2. DQ, DQS, /DQS, ODT, DM, CKE, /CS relationships
   must be meintained as shown.

 * D0 to D7 : 1G bits DDR2 SDRAM
   U0 : 2k bits EEPROM
   Rs1 : 22Ω
   Rs2 : 3.0Ω
   Rs3 : 10.0Ω

Electrical Specifications

• All voltages are referenced to VSS (GND).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on any pin relative to VSS	VT	−0.5 to +2.3	V	1
Supply voltage relative to VSS	VDD	−0.5 to +2.3	V	
Short circuit output current	IOS	50	mA	1
Power dissipation	PD	8	W	
Operating case temperature	TC	0 to +95	°C	1, 2
Storage temperature	Tstg	−55 to +100	°C	1

Notes: 1. DDR2 SDRAM component specification.

2. Supporting 0°C to +85°C and being able to extend to +95°C with doubling auto-refresh commands in frequency to a 32ms period (tREFI = 3.9μs) and higher temperature self-refresh entry via the control of EMRS (2) bit A7 is required.

Caution   Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Operating Conditions (TC = 0°C to +85°C) (DDR2 SDRAM Component Specification)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD, VDDQ	1.7	1.8	1.9	V	4
	VSS	0	0	0	V	
	VDDSPD	1.7	—	3.6	V	
Input reference voltage	VREF	$0.49 \times$ VDDQ	$0.50 \times$ VDDQ	$0.51 \times$ VDDQ	V	1, 2
Termination voltage	VTT	VREF − 0.04	VREF	VREF + 0.04	V	3
DC input logic high	VIH (DC)	VREF + 0.125	—	VDDQ + 0.3	V	
DC input low	VIL (DC)	−0.3	—	VREF − 0.125	V	
AC input logic high	VIH (AC)	VREF + 0.200	—	—	V	
AC input low	VIL (AC)	—	—	VREF − 0.200	V	

Notes: 1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about $0.5 \times$ VDDQ of the transmitting device and VREF are expected to track variations in VDDQ.

2. Peak to peak AC noise on VREF may not exceed ±2% VREF (DC).

3. VTT of transmitting device must track VREF of receiving device.

4. VDDQ must be equal to VDD.

AC Overshoot/Undershoot Specification (DDR2 SDRAM Component Specification)

Parameter	Pins	Specification	Unit
Maximum peak amplitude allowed for overshoot	Command, Address, CKE, ODT	0.5	V
Maximum peak amplitude allowed for undershoot		0.5	V
Maximum overshoot area above VDD 　DDR2-800		0.66	V-ns
DDR2-667		0.8	V-ns
Maximum undershoot area below VSS 　DDR2-800		0.66	V-ns
DDR2-667		0.8	V-ns
Maximum peak amplitude allowed for overshoot	CK, /CK	0.5	V
Maximum peak amplitude allowed for undershoot		0.5	V
Maximum overshoot area above VDD		0.23	V-ns
Maximum undershoot area below VSS		0.23	V-ns
Maximum peak amplitude allowed for overshoot	DQ, DQS, /DQS,	0.5	V
Maximum peak amplitude allowed for undershoot	RDQS, /RDQS, DM	0.5	V
Maximum overshoot area above VDDQ		0.23	V-ns
Maximum undershoot area below VSSQ		0.23	V-ns
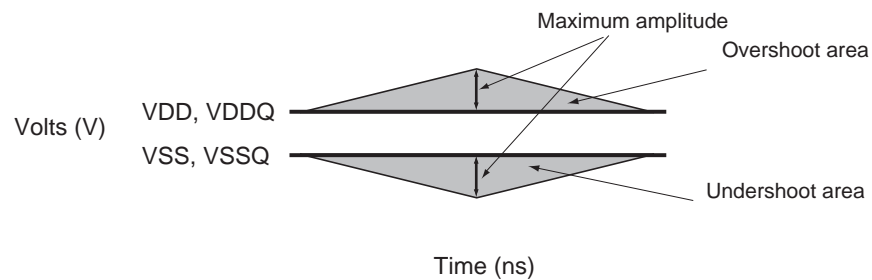
Overshoot/Undershoot Definition

DC Characteristics 1 (TC = 0°C to +85°C, VDD = 1.8V ± 0.1V, VSS = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition
Operating current (ACT-PRE)	IDD0	-8G -6E	680 640	mA	one bank; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS min.(IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING
Operating current (ACT-READ-PRE)	IDD1	-8G -6E	800 760	mA	one bank; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS min.(IDD); tRCD = tRCD (IDD); CKE is H, /CS is H between valid commands; Data pattern is same as IDD4W
Precharge power-down standby current	IDD2P		80	mA	all banks idle; tCK = tCK (IDD); CKE is L; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
Precharge quiet standby current	IDD2Q	-8G -6E	280 240	mA	all banks idle; tCK = tCK (IDD); CKE is H, /CS is H; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
Idle standby current	IDD2N	-8G -6E	320 280	mA	all banks idle; tCK = tCK (IDD); CKE is H, /CS is H; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
Active power-down standby current	IDD3P-F		280	mA	all banks open; tCK = tCK (IDD); CKE is L; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING — Fast PDN Exit MRS(12) = 0
	IDD3P-S		160	mA	Slow PDN Exit MRS(12) = 1
Active standby current	IDD3N	-8G -6E	720 640	mA	all banks open; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
Operating current (Burst read operating)	IDD4R	-8G -6E	1280 1120	mA	all banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W
Operating current (Burst write operating)	IDD4W	-8G -6E	1280 1120	mA	all banks open, continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING

Parameter	Symbol	Grade	max.	Unit	Test condition
Auto-refresh current	IDD5	-8G -6E	2320 2240	mA	tCK = tCK (IDD); Refresh command at every tRFC (IDD) interval; CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
Self-refresh current	IDD6		80	mA	Self Refresh Mode; CK and /CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING
Operating current (Bank interleaving)	IDD7	-8G -6E	2320 2200	mA	all bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD (IDD) −1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD(IDD), tFAW = tFAW (IDD), tRCD = 1 × tCK (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4W;

Notes: 1. IDD specifications are tested after the device is properly initialized.

2. Input slew rate is specified by AC Input Test Condition.

3. IDD parameters are specified with ODT disabled.

4. Data bus consists of DQ, DM, DQS, /DQS, RDQS and /RDQS. IDD values must be met with all combinations of EMRS bits 10 and 11.

5. Definitions for IDD

L is defined as VIN ≤ VIL (AC) (max.)

H is defined as VIN ≥ VIH (AC) (min.)

STABLE is defined as inputs stable at an H or L level

FLOATING is defined as inputs at VREF = VDDQ/2

SWITCHING is defined as:

inputs changing between H and L every other clock cycle (once per two clocks) for address and control signals, and inputs changing between H and L every other data transfer (once per clock) for DQ signals not including masks or strobes.

6. Refer to AC Timing for IDD Test Conditions.

AC Timing for IDD Test Conditions

For purposes of IDD testing, the following parameters are to be utilized.

Parameter	DDR2-800 6-6-6	DDR2-667 5-5-5	Unit
CL (IDD)	6	5	tCK
tRCD (IDD)	15	15	ns
tRC (IDD)	60	60	ns
tRRD (IDD)	7.5	7.5	ns
tFAW (IDD)	35	37.5	ns
tCK (IDD)	2.5	3	ns
tRAS (min.)(IDD)	45	45	ns
tRAS (max.)(IDD)	70000	70000	ns
tRP (IDD)	15	15	ns
tRFC (IDD)	127.5	127.5	ns

DC Characteristics 2 (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V)

(DDR2 SDRAM Component Specification)

Parameter	Symbol	Value	Unit	Notes
Input leakage current	|ILI|	2	μA	VDD ≥ VIN ≥ VSS
Output leakage current	|ILO|	5	μA	VDDQ ≥ VOUT ≥ VSS
Minimum required output pull-up under AC test load	VOH	VTT + 0.603	V	5
Maximum required output pull-down under AC test load	VOL	VTT − 0.603	V	5
Output timing measurement reference level	VOTR	0.5 × VDDQ	V	1
Output minimum sink DC current	IOL	+13.4	mA	3, 4, 5
Output minimum source DC current	IOH	−13.4	mA	2, 4, 5

Notes: 1. The VDDQ of the device under test is referenced.
2. VDDQ = 1.7V; VOUT = 1.42V.
3. VDDQ = 1.7V; VOUT = 0.28V.
4. The DC value of VREF applied to the receiving device is expected to be set to VTT.
5. After OCD calibration to 18Ω at TC = 25°C, VDD = VDDQ = 1.8V.

DC Characteristics 3 (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V)

(DDR2 SDRAM Component Specification)

Parameter	Symbol	min.	max.	Unit	Notes
AC differential input voltage	VID (AC)	0.5	VDDQ + 0.6	V	1, 2
AC differential cross point voltage	VIX (AC)	0.5 × VDDQ − 0.175	0.5 × VDDQ + 0.175	V	2
AC differential cross point voltage	VOX (AC)	0.5 × VDDQ − 0.125	0.5 × VDDQ + 0.125	V	3

Notes: 1. VID (AC) specifies the input differential voltage |VTR -VCP| required for switching, where VTR is the true input signal (such as CK, DQS, RDQS) and VCP is the complementary input signal (such as /CK, /DQS, /RDQS). The minimum value is equal to VIH (AC) − VIL (AC).
2. The typical value of VIX (AC) is expected to be about 0.5 × VDDQ of the transmitting device and VIX (AC) is expected to track variations in VDDQ. VIX (AC) indicates the voltage at which differential input signals must cross.
3. The typical value of VOX (AC) is expected to be about 0.5 × VDDQ of the transmitting device and VOX (AC) is expected to track variations in VDDQ. VOX (AC) indicates the voltage at which differential output signals must cross.

Differential Signal Levels*[1, 2]
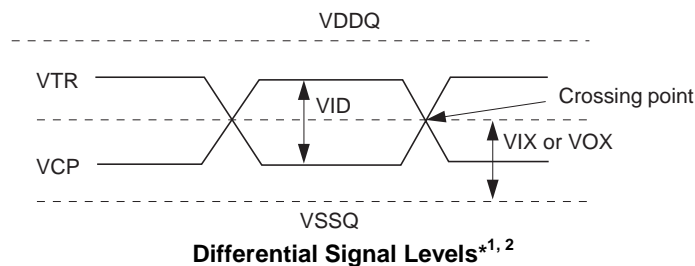
ODT DC Electrical Characteristics (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V)

(DDR2 SDRAM Component Specification)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Rtt effective impedance value for EMRS (A6, A2) = 0, 1; 75 Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS (A6, A2) = 1, 0; 150 Ω	Rtt2(eff)	120	150	180	Ω	1
Rtt effective impedance value for EMRS (A6, A2) = 1, 1; 50 Ω	Rtt3(eff)	40	50	60	Ω	1
Deviation of VM with respect to VDDQ/2	ΔVM	−6	—	+6	%	1

Note: 1. Test condition for Rtt measurements.

Measurement Definition for Rtt (eff)
Apply VIH (AC) and VIL (AC) to test pin separately, then measure current I(VIH (AC)) and I(VIL (AC)) respectively.
VIH (AC), and VDDQ values defined in SSTL_18.

$$Rtt(eff) = \frac{VIH(AC) - VIL(AC)}{I(VIH(AC)) - I(VIL(AC))}$$

Measurement Definition for ΔVM
Measure voltage (VM) at test pin (midpoint) with no load.

$$\Delta VM = \left(\frac{2 \times VM}{VDDQ} - 1\right) \times 100$$

OCD Default Characteristics (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V)

(DDR2 SDRAM Component Specification)

Parameter	min.	typ.	max.	Unit	Notes
Output impedance	12.6	18	23.4	Ω	1, 5
Pull-up and pull-down mismatch	0	—	4	Ω	1, 2
Output slew rate	1.5	—	5	V/ns	3, 4

Notes: 1. Impedance measurement condition for output source DC current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT−VDDQ)/IOH must be less than 23.4Ω for values of VOUT between VDDQ and VDDQ−280mV. Impedance measurement condition for output sink DC current: VDDQ = 1.7V; VOUT = 280mV; VOUT/IOL must be less than 23.4Ω for values of VOUT between 0V and 280mV.
   2. Mismatch is absolute value between pull up and pull down, both are measured at same temperature and voltage.
   3. Slew rate measured from VIL(AC) to VIH(AC).
   4. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
   5. DRAM I/O specifications for timing, voltage, and slew rate are no longer applicable if OCD is changed from default settings.

Pin Capacitance (TA = 25°C, VDD = 1.8V ± 0.1V)

(DDR2 SDRAM Component Specification)

Parameter	Symbol	Pins	min.	max.	Unit	Notes
CLK input pin capacitance	CCK	CK, /CK	1.0	2.0	pF	1
Input pin capacitance -8G	CIN	/RAS, /CAS, /WE, /CS, CKE, ODT, Address	1.0	1.75	pF	1
-6E			1.0	2.0	pF	1
Input/output pin capacitance	CI/O	DQ, DQS, /DQS, RDQS, /RDQS, DM	2.5	3.5	pF	2

Notes: 1   Matching within 0.25pF.

2.   Matching within 0.50pF.

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AC Characteristics (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V, VSS, VSSQ = 0V)

(DDR2 SDRAM Component Specification)

- New units tCK(avg) and nCK, are introduced in DDR2-800 and DDR2-667
  tCK(avg): actual tCK(avg) of the input clock under operation.
  nCK: one clock cycle of the input clock, counting the actual clock edges.

		-8G		-6E			
Speed bin		DDR2-800 (6-6-6)		DDR2-667 (5-5-5)			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Active to read or write command delay	tRCD	15	—	15	—	ns	
Precharge command period	tRP	15	—	15	—	ns	
Active to active/auto-refresh command time	tRC	60	—	60	—	ns	
DQ output access time from CK, /CK	tAC	−400	+400	−450	+450	ps	10
DQS output access time from CK, /CK	tDQSCK	−350	+350	−400	+400	ps	10
CK high-level width	tCH (avg)	0.48	0.52	0.48	0.52	tCK (avg)	13
CK low-level width	tCL(avg)	0.48	0.52	0.48	0.52	tCK (avg)	13
CK half period	tHP	Min. (tCL(abs), tCH(abs))	—	Min. (tCL(abs), tCH(abs))	—	ps	6, 13
Clock cycle time (CL = 6)	tCK (avg)	2500	8000	3000	8000	ps	13
(CL = 5)	tCK (avg)	3000	8000	3000	8000	ps	13
(CL = 4)	tCK (avg)	3750	8000	3750	8000	ps	13
(CL = 3)	tCK (avg)	5000	8000	5000	8000	ps	13
DQ and DM input hold time	tDH (base)	125	—	175	—	ps	5
DQ and DM input setup time	tDS (base)	50	—	100	—	ps	4
Control and Address input pulse width for each input	tIPW	0.6	—	0.6	—	tCK (avg)	
DQ and DM input pulse width for each input	tDIPW	0.35	—	0.35	—	tCK (avg)	
Data-out high-impedance time from CK,/CK	tHZ	—	tAC max.	—	tAC max.	ps	10
DQS, /DQS low-impedance time from CK,/CK	tLZ (DQS)	tAC min.	tAC max.	tAC min.	tAC max.	ps	10
DQ low-impedance time from CK,/CK	tLZ (DQ)	2 × tAC min	tAC max.	2 × tAC min	tAC max.	ps	10
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	—	200	—	240	ps	
DQ hold skew factor	tQHS	—	300	—	340	ps	7
DQ/DQS output hold time from DQS	tQH	tHP – tQHS	—	tHP – tQHS	—	ps	8
DQS latching rising transitions to associated clock edges	tDQSS	−0.25	+0.25	−0.25	+0.25	tCK (avg)	
DQS input high pulse width	tDQSH	0.35	—	0.35	—	tCK (avg)	
DQS input low pulse width	tDQSL	0.35	—	0.35	—	tCK (avg)	
DQS falling edge to CK setup time	tDSS	0.2	—	0.2	—	tCK (avg)	
DQS falling edge hold time from CK	tDSH	0.2	—	0.2	—	tCK (avg)	
Mode register set command cycle time	tMRD	2	—	2	—	nCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK (avg)	
Write preamble	tWPRE	0.35	—	0.35	—	tCK (avg)	
Address and control input hold time	tIH (base)	250	—	275	—	ps	5
Address and control input setup time	tIS (base)	175	—	200	—	ps	4
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK (avg)	11

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Speed bin		-8G		-6E			
		DDR2-800 (6-6-6)		DDR2-667 (5-5-5)			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK (avg)	12
Active to precharge command	tRAS	45	70000	45	70000	ns	
Active to auto-precharge delay	tRAP	tRCD min.	—	tRCD min.	—	ns	
Active bank A to active bank B command period	tRRD	7.5	—	7.5	—	ns	
Four active window period	tFAW	35	—	37.5	—	ns	
/CAS to /CAS command delay	tCCD	2	—	2	—	nCK	
Write recovery time	tWR	15	—	15	—	ns	
Auto precharge write recovery + precharge time	tDAL	WR + RU (tRP/ tCK (avg))	—	WR + RU (tRP/ tCK (avg))	—	nCK	1, 9
Internal write to read command delay	tWTR	7.5	—	7.5	—	ns	14
Internal read to precharge command delay	tRTP	7.5	—	7.5	—	ns	
Exit self-refresh to a non-read command	tXSNR	tRFC + 10	—	tRFC + 10	—	ns	
Exit self-refresh to a read command	tXSRD	200	—	200	—	nCK	
Exit precharge power down to any non-read command	tXP	2	—	2	—	nCK	
Exit active power down to read command	tXARD	2	—	2	—	nCK	3
Exit active power down to read command (slow exit/low power mode)	tXARDS	8 – AL	—	7 – AL	—	nCK	2, 3
CKE minimum pulse width (high and low pulse width)	tCKE	3	—	3	—	nCK	
Output impedance test driver delay	tOIT	0	12	0	12	ns	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	
Auto-refresh to active/auto-refresh command time	tRFC	127.5	—	127.5	—	ns	
Average periodic refresh interval (0°C ≤ TC ≤ +85°C)	tREFI	—	7.8	—	7.8	µs	
(+85°C < TC ≤ +95°C)	tREFI	—	3.9	—	3.9	µs	
Minimum time clocks remains ON after CKE asynchronously drops low	tDELAY	tIS + tCK(avg) + tIH	—	tIS + tCK(avg) + tIH	—	ns	

Notes: 1. For each of the terms above, if not already an integer, round to the next higher integer.

2. AL: Additive Latency.

3. MRS A12 bit defines which active power down exit timing to be applied.

4. The figures of Input Waveform Timing 1 and 2 are referenced from the input signal crossing at the VIH(AC) level for a rising signal and VIL(AC) for a falling signal applied to the device under test.

5. The figures of Input Waveform Timing 1 and 2 are referenced from the input signal crossing at the VIL(DC) level for a rising signal and VIH(DC) for a falling signal applied to the device under test.
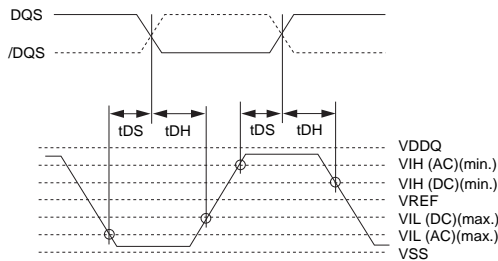
Input Waveform Timing 1 (tDS, tDH)   **Input Waveform Timing 2 (tIS, tIH)**
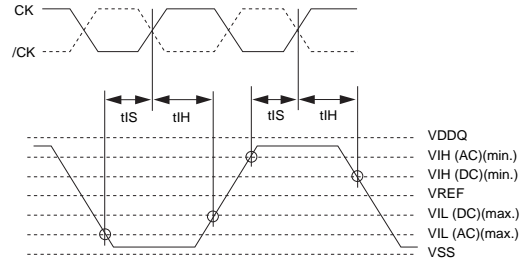
6. tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH.

The value to be used for tQH calculation is determined by the following equation;

$$tHP = min (tCH(abs), tCL(abs)),$$

where,

tCH(abs) is the minimum of the actual instantaneous clock high time;

tCL(abs) is the minimum of the actual instantaneous clock low time;

7. tQHS accounts for:

a. The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and

b. The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers.

8. tQH = tHP – tQHS, where:

tHP is the minimum of the absolute half period of the actual input clock; and tQHS is the specification value under the max column.

{The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}

Examples:

a. If the system provides tHP of 1315ps into a DDR2-667 SDRAM, the DRAM provides tQH of 975ps (min.)

b. If the system provides tHP of 1420ps into a DDR2-667 SDRAM, the DRAM provides tQH of 1080ps (min.)

9. RU stands for round up. WR refers to the tWR parameter stored in the MRS.

10. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per) min. = −272ps and tERR(6-10per) max. = +293ps, then tDQSCK min.(derated) = tDQSCK min. − tERR(6-10per) max. = −400ps − 293ps = −693ps and tDQSCK max.(derated) = tDQSCK max. − tERR(6-10per) min. = 400ps + 272ps = +672ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ) min.(derated) = −900ps − 293ps = −1193ps and tLZ(DQ) max.(derated)= 450ps + 272ps = +722ps.

11. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(per) min. = -72ps and tJIT(per) max. = +93ps, then tRPRE min.(derated) = tRPRE min. + tJIT(per) min. = $0.9 \times$ tCK(avg) $- 72$ps = +2178ps and tRPRE max.(derated) = tRPRE max. + tJIT(per) max. = $1.1 \times$ tCK(avg) + 93ps = +2843ps.

12. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(duty) min. = -72ps and tJIT(duty) max. = +93ps, then tRPST min.(derated) = tRPST min. + tJIT(duty) min. = $0.4 \times$ tCK(avg) $-$ 72ps = +928ps and tRPST max.(derated) = tRPST max. + tJIT(duty) max. = $0.6 \times$ tCK(avg) + 93ps = +1592ps.

13. Refer to the Clock Jitter table.

14. tWTR is at least two clocks ($2 \times$ tCK or $2 \times$ nCK) independent of operation frequency.

ODT AC Electrical Characteristics (DDR2 SDRAM Component Specification)

Parameter	Symbol	min.	max.	Unit	Notes
ODT turn-on delay	tAOND	2	2	tCK	
ODT turn-on	tAON	tAC (min)	tAC (max) + 700	ps	1, 3
ODT turn-on (power down mode)	tAONPD	tAC(min) + 2000	2tCK + tAC(max) + 1000	ps	
ODT turn-off delay	tAOFD	2.5	2.5	tCK	5
ODT turn-off	tAOF	tAC(min)	tAC(max) + 600	ps	2, 4, 5
ODT turn-off (power down mode)	tAOFPD	tAC(min) + 2000	2.5tCK + tAC(max) + 1000	ps	
ODT to power down entry latency	tANPD	3	3	tCK	
ODT power down exit latency	tAXPD	8	8	tCK	

Notes: 1. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

2. ODT turn off time min is when the device starts to turn off ODT resistance.
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

3. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)

4. When the device is operated with input clock jitter, this parameter needs to be derated by $\{-\text{tJIT(duty) max.} - \text{tERR(6-10per) max.}\}$ and $\{-\text{tJIT(duty) min.} - \text{tERR(6-10per) min.}\}$ of the actual input clock.(output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per) min. = -272ps, tERR(6-10per) max. = $+293$ps, tJIT(duty) min. = -106ps and tJIT(duty) max. = $+94$ps, then tAOF min.(derated) = tAOF min. + $\{-\text{tJIT(duty) max.} - \text{tERR(6-10per) max.}\}$ = -450ps + $\{-94\text{ps} - 293\text{ps}\}$ = -837ps and tAOF max.(derated) = tAOF max. + $\{-\text{tJIT(duty) min.} - \text{tERR(6-10per) min.}\}$ = 1050ps + $\{106\text{ps} + 272\text{ps}\}$ = $+1428$ps.

5. For tAOFD of DDR2-667/800, the 1/2 clock of nCK in the 2.5 × nCK assumes a tCH(avg), average input clock high pulse width of 0.5 relative to tCK(avg). tAOF min. and tAOF max. should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH(avg) of 0.48, the tAOF min. should be derated by subtracting 0.02 × tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.52, the tAOF max. should be derated by adding 0.02 × tCK(avg) to it. Therefore, we have;

tAOF min.(derated) = tAC min. − [0.5 − Min.(0.5, tCH(avg) min.)] × tCK(avg)

tAOF max.(derated) = tAC max. + 0.6 + [Max.(0.5, tCH(avg) max.) − 0.5] × tCK(avg)

or

tAOF min.(derated) = Min.(tAC min., tAC min. − [0.5 − tCH(avg) min.] × tCK(avg))

tAOF max.(derated) = 0.6 + Max.(tAC max., tAC max. + [tCH(avg) max. − 0.5] × tCK(avg))

where tCH(avg) min. and tCH(avg) max. are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls.

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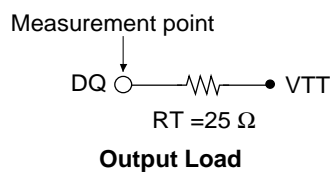**AC Input Test Conditions (DDR2 SDRAM Component Specification)**

Parameter	Symbol	Value	Unit	Notes
Input reference voltage	VREF	$0.5 \times$ VDDQ	V	1
Input signal maximum peak to peak swing	VSWING (max.)	1.0	V	1
Input signal minimum slew rate	SLEW	1.0	V/ns	2, 3

Notes: 1. Input waveform timing is referenced to the input signal crossing through the VIH/IL (AC) level applied to the device under test.

2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH (AC) (min.) for rising edges and the range from VREF to VIL (AC) (max.) for falling edges as shown in the below figure.

3. AC timings are referenced with input waveforms switching from VIL (AC) to VIH (AC) on the positive transitions and VIH (AC) to VIL (AC) on the negative transitions.

Falling slew = $\dfrac{\text{VREF} - \text{VIL (AC)(max.)}}{\Delta \text{TF}}$ Rising slew = $\dfrac{\text{VIH (AC) min.} - \text{VREF}}{\Delta \text{TR}}$
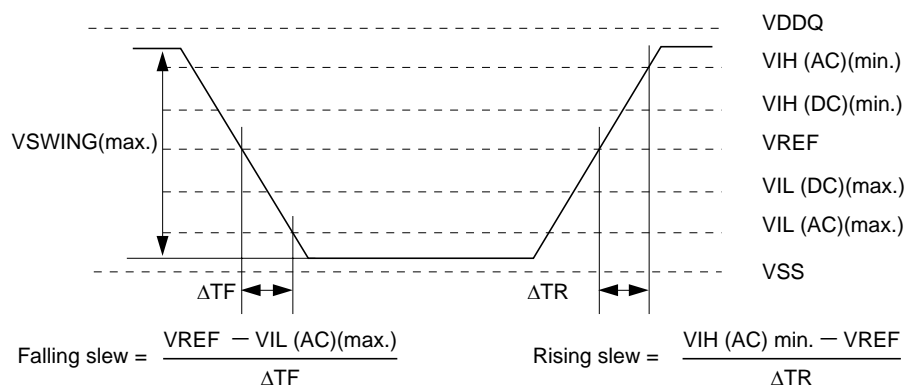
AC Input Test Signal Wave forms

Measurement point

DQ ○———∧∧∧——• VTT

RT =25 Ω

Output Load

Clock Jitter

Parameter	Symbol	-8G		-6E		Unit	Notes
Frequency (Mbps)		800		667			
		min.	max.	min.	max.		
Average clock period	tCK (avg)	2500	8000	3000	8000	ps	1
Clock period jitter	tJIT (per)	−100	100	−125	125	ps	5
Clock period jitter during DLL locking period	tJIT (per, lck)	−80	80	−100	100	ps	5
Cycle to cycle period jitter	tJIT (cc)	—	200	—	250	ps	6
Cycle to cycle clock period jitter during DLL locking period	tJIT (cc, lck)	—	160	—	200	ps	6
Cumulative error across 2 cycles	tERR (2per)	−150	150	−175	175	ps	7
Cumulative error across 3 cycles	tERR (3per)	−175	175	−225	225	ps	7
Cumulative error across 4 cycles	tERR (4per)	−200	200	−250	250	ps	7
Cumulative error across 5 cycles	tERR (5per)	−200	200	−250	250	ps	7
Cumulative error across n=6,7,8,9,10 cycles	tERR (6-10per)	−300	300	−350	350	ps	7
Cumulative error across n=11, 12,…49,50 cycles	tERR (11-50per)	−450	450	−450	450	ps	7
Average high pulse width	tCH (avg)	0.48	0.52	0.48	0.52	tCK (avg)	2
Average low pulse width	tCL (avg)	0.48	0.52	0.48	0.52	tCK (avg)	3
Duty cycle jitter	tJIT (duty)	−100	100	−125	125	ps	4

Notes: 1. tCK (avg) is calculated as the average clock period across any consecutive 200cycle window.

$$tCK(avg) = \left\{ \sum_{j=1}^{N} tCKj \right\} \Big/ N$$

N = 200

2. tCH (avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left\{ \sum_{j=1}^{N} tCHj \right\} \Big/ (N \times tCK(avg))$$

N = 200

3. tCL (avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left\{ \sum_{j=1}^{N} tCLj \right\} \Big/ (N \times tCK(avg))$$

N = 200

4. tJIT (duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH (avg). tCL jitter is the largest deviation of any single tCL from tCL (avg). tJIT (duty) is not subject to production test.

   tJIT (duty) = Min./Max. of {tJIT (CH), tJIT (CL)}, where:

   tJIT (CH) = {tCH_j- tCH (avg) where j = 1 to 200}

   tJIT (CL) = {tCL_j − tCL (avg) where j = 1 to 200}

5. tJIT (per) is defined as the largest deviation of any single tCK from tCK (avg).

   tJIT (per) = Min./Max. of { tCK_j − tCK (avg) where j = 1 to 200}

   tJIT (per) defines the single period jitter when the DLL is already locked. tJIT (per, lck) uses the same definition for single period jitter, during the DLL locking period only. tJIT (per) and tJIT (per, lck) are not subject to production test.

6. tJIT (cc) is defined as the absolute difference in clock period between two consecutive clock cycles:

tJIT (cc) = Max. of $|tCK_{j+1} - tCK_j|$

tJIT (cc) is defines the cycle to cycle jitter when the DLL is already locked. tJIT (cc, lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only. tJIT (cc) and tJIT (cc, lck) are not subject to production test.

7. tERR (nper) is defined as the cumulative error across multiple consecutive cycles from tCK (avg).

tERR (nper) is not subject to production test.

$$tERR(nper) = \left\{ \sum_{j=1}^{n} tCKj \right\} - n \times tCK(avg))$$

$2 \leq n \leq 50$ for tERR (nper)

8. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing hold at all times.

(minimum and maximum of spec values are to be used for calculations in the table below.)

Parameter	Symbol	min.	max.	Unit
Absolute clock period	tCK (abs)	tCK (avg) min. + tJIT (per) min.	tCK (avg) max. + tJIT (per) max.	ps
Absolute clock high pulse width	tCH (abs)	tCH (avg) min. $\times$ tCK (avg) min. + tJIT (duty) min.	tCH (avg) max. $\times$ tCK (avg) max. + tJIT (duty) max.	ps
Absolute clock low pulse width	tCL (abs)	tCL (avg) min. $\times$ tCK (avg) min. + tJIT (duty) min.	tCL (avg) max. $\times$ tCK (avg) max. + tJIT (duty) max.	ps

Example: For DDR2-667, tCH(abs) min. = (0.48 $\times$ 3000 ps) - 125ps = 1315ps

Pin Functions

CK, /CK (input pin)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the VREF level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CK and the /CK.

/CS (input pin)

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A13 (input pins)

Row address (AX0 to AX13) is determined by the A0 to the A13 level at the cross point of the CK rising edge and the VREF level in a bank active command cycle. Column address (AY0 to AY9) is loaded via the A0 to the A9 at the cross point of the CK rising edge and the VREF level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = high when a precharge command is issued, all banks are precharged. If A10 = low when a precharge command is issued, only the bank that is selected by BA0, BA1 and BA2 is precharged. If A10 = high when read or write command, auto-precharge function is enabled. While A10 = low, auto-precharge function is disabled.

BA0, BA1, BA2 (input pin)

BA0, BA1 and BA2 are bank select signals (BA). The memory array is divided into 8 banks: bank 0 to bank 7. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1	BA2
Bank 0	L	L	L
Bank 1	H	L	L
Bank 2	L	H	L
Bank 3	H	H	L
Bank 4	L	L	H
Bank 5	H	L	H
Bank 6	L	H	H
Bank 7	H	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven low and exited when it resumes to high.

The CKE level must be kept for 1 CK cycle at least, that is, if CKE changes at the cross point of the CK rising edge and the VREF level with proper setup time tIS, at the next CK rising edge CKE level must be kept with proper hold time tIH.

DQ (input and output pins)

Data are input to and output from these pins.

DQS and /DQS (input and output pin)

DQS and /DQS provide the read data strobes (as output) and the write data strobes (as input).

DM (input pins)

DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and /DQS.

VDD (power supply pins)

1.8V is applied. (VDD is for the internal circuit.)

VDDSPD (power supply pin)

1.8V is applied (For serial EEPROM).

VSS (power supply pin)

Ground is connected.

Detailed Operation Part and Timing Waveforms

Refer to the EDE1104AFSE, EDE1108AFSE datasheet (E1390E).

Physical Outline

Unit: mm

Front side
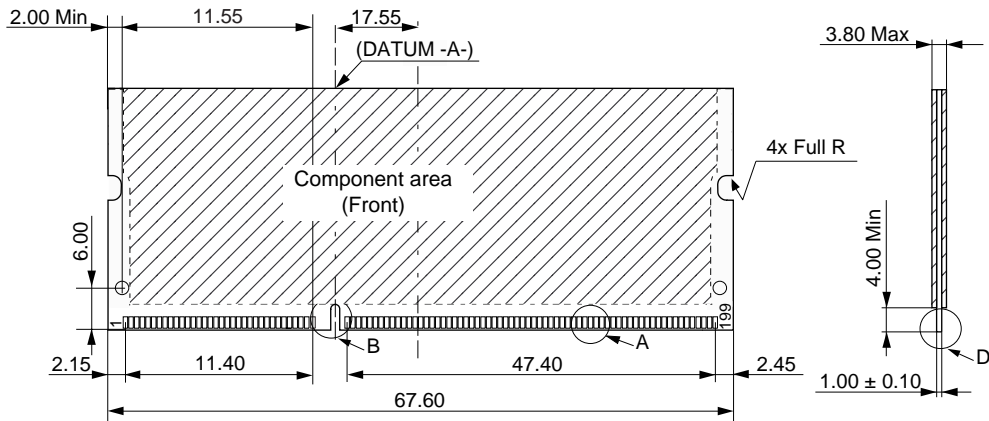
Back side
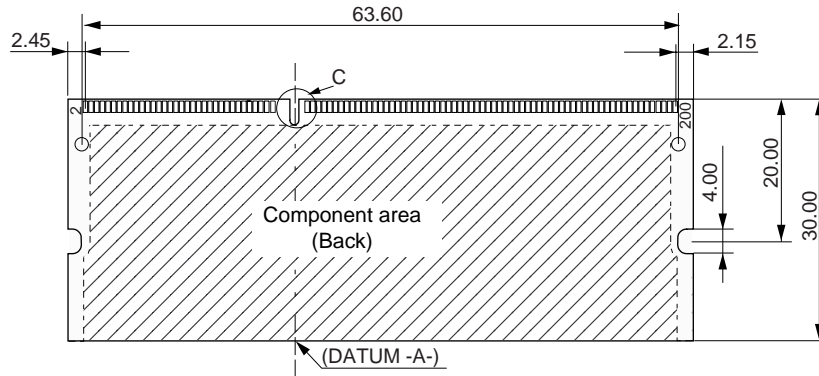
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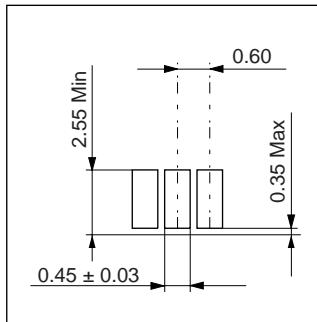
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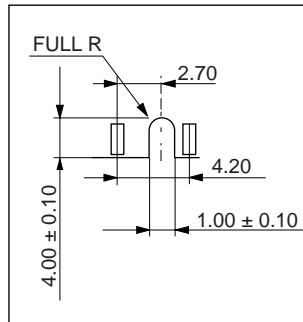
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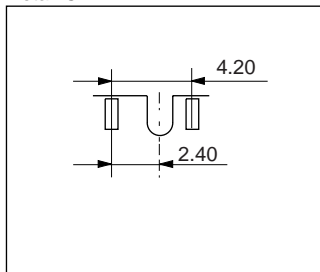
Detail D
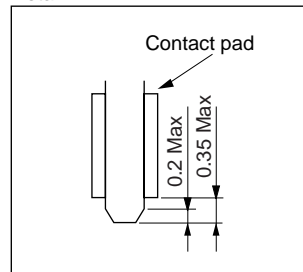
ECA-TS2-0209-01

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NO_X.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

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