

## Features

- 4 configurable IOs supporting
  - CapSense™ buttons
  - LED drive
  - Interrupt outputs
  - WAKE on interrupt input
  - Bi-directional sleep control pin
  - User defined input or output
- 2.4V to 2.9V, 3.10V to 3.6V, and 4.75V to 5.25V operating voltage
- Industrial temperature range: -40°C to +85°C
- I<sup>2</sup>C slave interface for configuration
  - I<sup>2</sup>C data transfer rate up to 400 kbps
- Reduce BOM cost
  - Internal oscillator - no external oscillators or crystal
  - Free development tool - no external tuning components
- Low operating current
  - Active current: 1.5 mA
  - Deep sleep current: 2.6 uA
- Available in 16-pin COL and 16-pin SOIC packages

## Overview

The CapSense Express™ controller allows the control of four IOs configurable as capacitive sensing buttons or as GPIOs for driving LEDs or interrupt signals based on various button conditions. The GPIOs are also configurable for waking up the device from sleep based on an interrupt input.

The user has the ability to configure buttons, outputs, and parameters, through specific commands sent to the I<sup>2</sup>C port. The IOs have the flexibility of mapping to capacitive buttons and as standard GPIO functions such as interrupt output or input, LED drive, and digital mapping of input to output using simple logical operations. This enables easy PCB trace routing and reduces the PCB size and stack up. CapSense Express products are designed for easy integration into complex products.

## Architecture

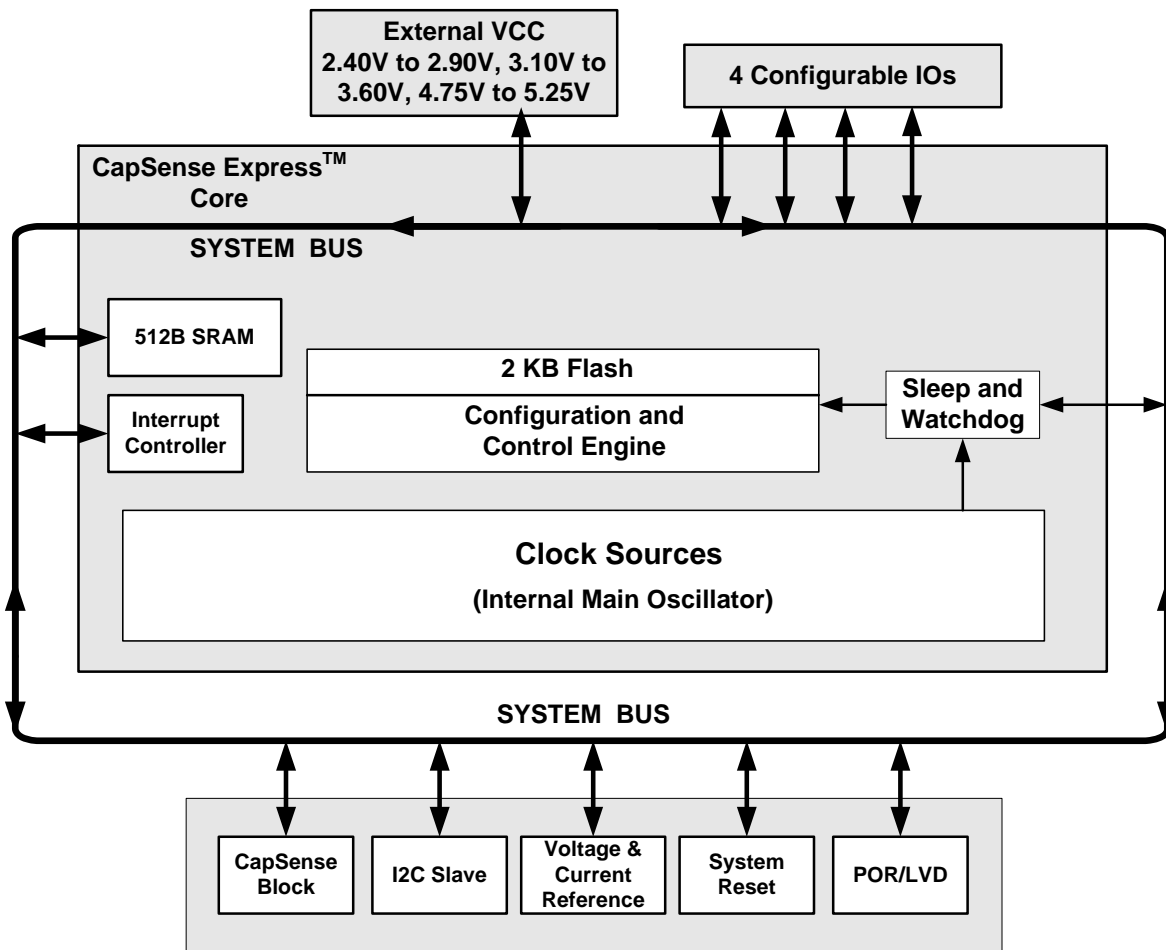
The logic block diagram shows the internal architecture of CY8C20140.

The user can configure registers with parameters needed to adjust the operation and sensitivity of the CapSense system. CY8C20140 supports a standard I<sup>2</sup>C serial communication interface that allows the host to configure the device and to read sensor information in real time through easy register access.

## The CapSense Express Core

The CapSense Express core has a powerful configuration and control block. It encompasses SRAM for data storage, an interrupt controller, and sleep and watchdog timers. System resources provide additional capability, such as a configurable I<sup>2</sup>C slave communication interface and various system resets. The analog system contains the CapSense PSoC® block, which supports capacitive sensing of up to four inputs.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 16 COL

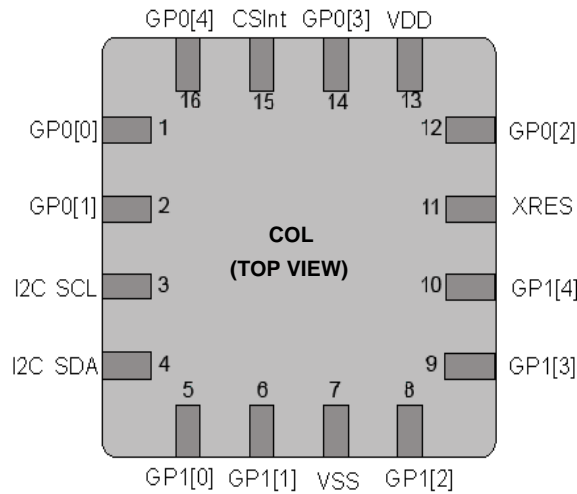


Table 1. Pin Definitions - 16 COL<sup>[1]</sup>

| Pin Number | Name                 | Description                                                                                                                            |
|------------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 1          | GP0[0]               | Configurable as CapSense or GPIO                                                                                                       |
| 2          | GP0[1]               | Configurable as CapSense or GPIO                                                                                                       |
| 3          | I <sup>2</sup> C SCL | I <sup>2</sup> C clock                                                                                                                 |
| 4          | I <sup>2</sup> C SDA | I <sup>2</sup> C data                                                                                                                  |
| 5          | GP1[0]               | Configurable as CapSense or GPIO                                                                                                       |
| 6          | GP1[1]               | Configurable as CapSense or GPIO                                                                                                       |
| 7          | VSS                  | Ground connection                                                                                                                      |
| 8          | GP1[2]               | Configurable as CapSense or GPIO                                                                                                       |
| 9          | GP1[3]               | Configurable as CapSense or GPIO                                                                                                       |
| 10         | GP1[4]               | Configurable as CapSense or GPIO                                                                                                       |
| 11         | XRES                 | Active HIGH external reset with internal pull down                                                                                     |
| 12         | GP0[2]               | Configurable as CapSense or GPIO                                                                                                       |
| 13         | V <sub>DD</sub>      | Supply voltage                                                                                                                         |
| 14         | GP0[3]               | Configurable as CapSense or GPIO                                                                                                       |
| 15         | CSInt                | Integrating capacitor input. The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 10 nF to 100 nF |
| 16         | GP0[4]               | Configurable as CapSense or GPIO                                                                                                       |

Note

1. 4 available configurable IOs can be configured to any of the 10 IOs of the package. After any of the 4 IOs are chosen, the remaining 6 IOs of the package get locked and is not available for any functionality

Figure 2. Pin Diagram - 16 SOIC

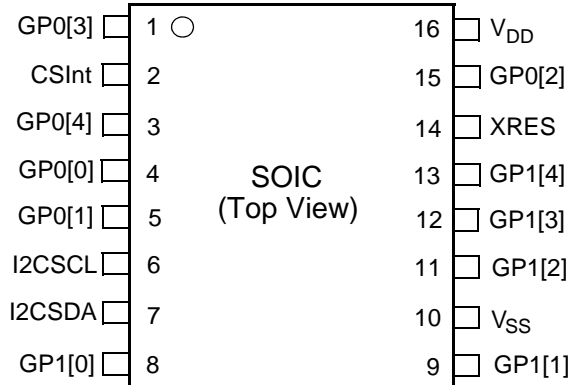


Table 2. Pin Definitions - 16 SOIC<sup>[1]</sup>

| Pin Number | Name                 | Description                                                                                                                            |
|------------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 1          | GP0[3]               | Configurable as CapSense or GPIO                                                                                                       |
| 2          | CSInt                | Integrating capacitor input. The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 10 nF to 100 nF |
| 3          | GP0[4]               | Configurable as CapSense or GPIO                                                                                                       |
| 4          | GP0[0]               | Configurable as CapSense or GPIO                                                                                                       |
| 5          | GP0[1]               | Configurable as CapSense or GPIO                                                                                                       |
| 6          | I <sup>2</sup> C SCL | I <sup>2</sup> C clock                                                                                                                 |
| 7          | I <sup>2</sup> C SDA | I <sup>2</sup> C data                                                                                                                  |
| 8          | GP1[0]               | Configurable as CapSense or GPIO                                                                                                       |
| 9          | GP1[1]               | Configurable as CapSense or GPIO                                                                                                       |
| 10         | VSS                  | Ground connection                                                                                                                      |
| 11         | GP1[2]               | Configurable as CapSense or GPIO                                                                                                       |
| 12         | GP1[3]               | Configurable as CapSense or GPIO                                                                                                       |
| 13         | GP1[4]               | Configurable as CapSense or GPIO                                                                                                       |
| 14         | XRES                 | Active HIGH external reset with internal pull down                                                                                     |
| 15         | GP0[2]               | Configurable as CapSense or GPIO                                                                                                       |
| 16         | V <sub>DD</sub>      | Supply voltage                                                                                                                         |

## The CapSense Analog System

The CapSense analog system contains the capacitive sensing hardware which supports CapSense Successive Approximation (CSA) algorithm. This hardware performs capacitive sensing and scanning without external components. Capacitive sensing is configurable on each pin.

### Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources are low voltage detection and power on reset.

- The I<sup>2</sup>C slave provides 50, 100, or 400 kHz communication over two wires.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels and the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.

An internal 1.8V reference provides an absolute reference for capacitive sensing. By this we are telling we have a stable internal reference, so that minor V<sub>DD</sub> changes does not alter the functionality of CapSense.

Table 3. Examples of I<sup>2</sup>C Addressing

| Slave Address Defined | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0   | Address to be sent (in Hex) by Master |
|-----------------------|----|----|----|----|----|----|----|------|---------------------------------------|
| 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0(W) | 00                                    |
| 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1(R) | 01                                    |
| 1                     | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0(W) | 02                                    |
| 1                     | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1(R) | 03                                    |
| 10                    | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0(W) | 14                                    |
| 10                    | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 1(R) | 15                                    |
| 75                    | 1  | 0  | 0  | 1  | 0  | 1  | 1  | 0(W) | 96                                    |
| 75                    | 1  | 0  | 0  | 1  | 0  | 1  | 1  | 1(R) | 97                                    |
| 127                   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0(W) | FE                                    |
| 127                   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1(R) | FF                                    |

### CapSense Express Software Tool

An easy to use software tool integrated with PSoC Express is available for configuring and tuning CapSense Express devices. Refer to the application note ["CapSense™ Express Software Tool - AN42137"](#) for details of the software tool.

## I<sup>2</sup>C Interface

The two modes of operation for the I<sup>2</sup>C interface are:

- Device register configuration and status read or write for controller
- Command execution

The I<sup>2</sup>C address is programmable during configuration. It can be locked to prevent accidental change by setting a flag in a configuration register.

### I<sup>2</sup>C Device Addressing

I<sup>2</sup>C device address is contained in the upper seven bits of the first byte of a read or write transaction. The first byte of the transaction is used by the I<sup>2</sup>C master to address the slave. The LSB of the byte contains the R/W bit. If this bit is 0, the master performs write operation to the addressed slave. If this bit is 1, the master performs read operation from the addressed slave. The LSB(B0) is eliminated when fixing the device address. For example, if the slave address is 02h, then the required address is 0000010 (7 bit) excluding LSB. If write operation is performed, the LSB is 0 and the address is 00000100(04h). If read operation is performed, the LSB is 1 and the address is 00000101(05h). [Table 3](#) provides examples of I<sup>2</sup>C addressing.

### CapSense Express Register Map

CapSense Express supports user configurable registers through which the device functionality and parameters are configured. For details, refer to the [CY8C201xx Register Reference Guide](#).

## Modes of Operation

CapSense Express devices are configured to operate in any of the following three modes to meet different power consumption requirements:

- Active Mode
- Sleep Mode
- Deep Sleep Mode

### Active Mode

In the active mode, all the device blocks including the CapSense sub system are powered. Typical active current consumption of the device across the operating voltage range is 1.5 mA

### Sleep Mode

Sleep mode provides an intermediate power operation mode. It is enabled by configuring the corresponding device register. When enabled, the device enters sleep mode and wakes up after a specified sleep interval. It scans the capacitive sensors before going back to sleep again. The device can also wake up from sleep mode with a GPIO interrupt. The following sleep intervals are supported in CapSense Express. The sleep interval is configured through registers.

- 1.95 ms (512 Hz)
- 15.6 ms (64 Hz)
- 125 ms (8 Hz)
- 1s (1 Hz)

## Deep Sleep Mode

Deep sleep mode provides the lowest power consumption because there is no operation running. In this mode, the device is woken up only using an external GPIO interrupt. A sleep timer interrupt cannot wake up a device from deep sleep mode. This can be treated as a continuous sleep mode without periodic wakeups. Refer to the application note [“CapSense Express Power and Sleep Considerations - AN44209”](#) for details on different sleep modes.

## Bi-Directional Sleep Control Pin

The CY8C20140 requires a dedicated sleep control pin to allow reliable I<sup>2</sup>C communication in case any sleep mode is enabled. This is achieved by pulling the sleep control pin LOW to wake up the device and start I<sup>2</sup>C communication. The sleep control pin can be configured on any of the GPIO. If sleep control feature is enabled, the device has one less GPIO available for CapSense and GPIO functions. The sleep control pin can also be configured as interrupt output pin from CY8C20140 to the host to acknowledge finger press on any button. To enable bi-directional feature, user must use I2C-USB bridge program.

## Electrical Specifications

### Absolute Maximum Ratings

| Parameter        | Description                                                   | Min                   | Typ | Max                   | Unit | Notes                                                                                                                                                                                        |
|------------------|---------------------------------------------------------------|-----------------------|-----|-----------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| T <sub>STG</sub> | Storage temperature                                           | -55                   | 25  | +100                  | °C   | Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C (0°C to 50°C). Extended duration storage temperatures above 65°C degrade reliability |
| T <sub>A</sub>   | Ambient temperature with power applied                        | -40                   | -   | +85                   | °C   |                                                                                                                                                                                              |
| V <sub>DD</sub>  | Supply voltage on V <sub>DD</sub> relative to V <sub>SS</sub> | -0.5                  | -   | +6.0                  | V    |                                                                                                                                                                                              |
| V <sub>IO</sub>  | DC input voltage                                              | V <sub>SS</sub> - 0.5 | -   | V <sub>DD</sub> + 0.5 | V    |                                                                                                                                                                                              |
| V <sub>IOZ</sub> | DC voltage applied to tri-state                               | V <sub>SS</sub> - 0.5 | -   | V <sub>DD</sub> + 0.5 | V    |                                                                                                                                                                                              |
| I <sub>MIO</sub> | Maximum current into any GPIO pin                             | -25                   | -   | +50                   | mA   |                                                                                                                                                                                              |
| ESD              | Electro static discharge voltage                              | 2000                  | -   | -                     | V    | Human body model ESD                                                                                                                                                                         |
| LU               | Latch up current                                              | -                     | -   | 200                   | mA   |                                                                                                                                                                                              |

### Operating Temperature

| Parameter      | Description          | Min | Typ | Max  | Unit | Notes |
|----------------|----------------------|-----|-----|------|------|-------|
| T <sub>A</sub> | Ambient temperature  | -40 | -   | +85  | °C   |       |
| T <sub>J</sub> | Junction temperature | -40 | -   | +100 | °C   |       |

## DC Electrical Characteristics

### DC Chip Level Specifications

| Parameter       | Description                                                            | Min  | Typ | Max  | Unit | Notes                                                         |
|-----------------|------------------------------------------------------------------------|------|-----|------|------|---------------------------------------------------------------|
| V <sub>DD</sub> | Supply voltage                                                         | 2.40 | -   | 5.25 | V    |                                                               |
| I <sub>DD</sub> | Supply current                                                         | -    | 1.5 | 2.5  | mA   | Conditions are V <sub>DD</sub> = 3.10V, T <sub>A</sub> = 25°C |
| I <sub>SB</sub> | Deep sleep mode current with POR and LVD active. Mid temperature range | -    | 2.6 | 4    | μA   | V <sub>DD</sub> = 2.55V, 0°C ≤ T <sub>A</sub> ≤ 40°C          |
| I <sub>SB</sub> | Deep sleep mode current with POR and LVD active                        | -    | 2.8 | 5    | μA   | V <sub>DD</sub> = 3.3V, -40°C ≤ T <sub>A</sub> ≤ 85°C         |
| I <sub>SB</sub> | Deep sleep mode current with POR and LVD active                        | -    | 5.2 | 6.4  | μA   | V <sub>DD</sub> = 5.25V, -40°C ≤ T <sub>A</sub> ≤ 85°C        |

### 5V and 3.3V DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.10V to 3.6V  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ . Typical parameters apply to 5v and 3V at 25°C and are for design guidance only.

| Parameter        | Description                        | Min                   | Typ | Max  | Unit | Notes                                                                                                                                      |
|------------------|------------------------------------|-----------------------|-----|------|------|--------------------------------------------------------------------------------------------------------------------------------------------|
| R <sub>PU</sub>  | Pull up resistor                   | 4                     | 5.6 | 8    | kΩ   |                                                                                                                                            |
| V <sub>OH1</sub> | High output voltage<br>Port 0 pins | V <sub>DD</sub> - 0.2 | -   | -    | V    | I <sub>OH</sub> ≤ 10 μA, V <sub>DD</sub> ≥ 3.10V, maximum of 20 mA source current in all IOs.                                              |
| V <sub>OH2</sub> | High output voltage<br>Port 0 pins | V <sub>DD</sub> - 0.9 | -   | -    | V    | I <sub>OH</sub> = 1 mA, V <sub>DD</sub> ≥ 3.10V, maximum of 20 mA source current in all IOs.                                               |
| V <sub>OH3</sub> | High output voltage<br>Port 1 pins | V <sub>DD</sub> - 0.2 | -   | -    | V    | I <sub>OH</sub> < 10 μA, V <sub>DD</sub> ≥ 3.10V, maximum of 10 mA source current in all IOs.                                              |
| V <sub>OH4</sub> | High output voltage<br>Port 1 pins | V <sub>DD</sub> - 0.9 | -   | -    | V    | I <sub>OH</sub> = 5 mA, V <sub>DD</sub> ≥ 3.10V, maximum of 20 mA source current in all IOs.                                               |
| V <sub>OL</sub>  | Low output voltage                 | -                     | -   | 0.75 | V    | I <sub>OL</sub> = 20 mA, V <sub>DD</sub> > 3.10V, maximum of 60 mA sink current on even port pins and 60 mA sink current on odd port pins. |
| V <sub>IL</sub>  | Input low voltage                  | -                     | -   | 0.75 | V    | V <sub>DD</sub> = 3.10V to 3.6V.                                                                                                           |
| V <sub>IH</sub>  | Input high voltage                 | 1.6                   | -   | -    | V    | V <sub>DD</sub> = 3.10V to 3.6V.                                                                                                           |
| V <sub>IL</sub>  | Input low voltage                  | -                     | -   | 0.8  | V    | V <sub>DD</sub> = 4.75V to 5.25V.                                                                                                          |
| V <sub>IH</sub>  | Input high voltage                 | 2.0                   | -   | -    | V    | V <sub>DD</sub> = 4.75V to 5.25V.                                                                                                          |
| V <sub>H</sub>   | Input hysteresis voltage           | -                     | 140 | -    | mV   |                                                                                                                                            |
| I <sub>IL</sub>  | Input leakage                      | -                     | 1   | -    | nA   | Gross tested to 1 μA.                                                                                                                      |
| C <sub>IN</sub>  | Capacitive load on pins as input   | 0.5                   | 1.7 | 5    | pF   | Package and pin dependent.<br>Temp = 25°C.                                                                                                 |
| C <sub>OUT</sub> | Capacitive load on pins as output  | 0.5                   | 1.7 | 5    | pF   | Package and pin dependent.<br>Temp = 25°C.                                                                                                 |

### 2.7V DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 2.90V and  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 2.7V at 25°C and are for design guidance only.

| Parameter        | Description                        | Min                   | Typ | Max  | Unit | Notes                                                                                                                                                                           |
|------------------|------------------------------------|-----------------------|-----|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R <sub>PU</sub>  | Pull up resistor                   | 4                     | 5.6 | 8    | kΩ   |                                                                                                                                                                                 |
| V <sub>OH1</sub> | High output voltage<br>Port 0 pins | V <sub>DD</sub> - 0.2 | -   | -    | V    | I <sub>OH</sub> ≤ 10 μA, maximum of 10 mA source current in all IOs.                                                                                                            |
| V <sub>OH2</sub> | High output voltage<br>Port 0 pins | V <sub>DD</sub> - 0.5 | -   | -    | V    | I <sub>OH</sub> = 0.2 mA, maximum of 10 mA source current in all IOs.                                                                                                           |
| V <sub>OH3</sub> | High output voltage<br>Port 1 pins | V <sub>DD</sub> - 0.2 | -   | -    | V    | I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all IOs.                                                                                                            |
| V <sub>OH4</sub> | High output voltage<br>Port 1 pins | V <sub>DD</sub> - 0.5 | -   | -    | V    | I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all IOs.                                                                                                             |
| V <sub>OL</sub>  | Low output voltage                 | -                     | -   | 0.75 | V    | I <sub>OL</sub> = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[3]). |



**2.7V DC General Purpose IO Specifications** (continued)

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 2.90V and  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 2.7V at 25°C and are for design guidance only.

| Parameter         | Description                       | Min | Typ | Max  | Unit | Notes                                                                                                                                                                                                                                                     |
|-------------------|-----------------------------------|-----|-----|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>OLP1</sub> | Low output voltage port 1 pins    | –   | –   | 0.4  | V    | I <sub>OL</sub> =5 mA, maximum of 50 mA sink current on even port pins (for example, P0[2] and P1[4]) and 50 mA sink current on odd port pins (for example, P0[1] and P1[3]). $2.4 \leq V_{DD} \leq 2.9\text{V}$ and $3.1 \leq V_{DD} \leq 3.6\text{V}$ . |
| V <sub>IL</sub>   | Input low voltage                 | –   | –   | 0.75 | V    | $V_{DD} = 2.4$ to 2.90V and 3.10V to 3.6V.                                                                                                                                                                                                                |
| V <sub>IH</sub>   | Input high voltage                | 1.6 | –   | –    | V    | $V_{DD} = 3.1$ to 3.6V.                                                                                                                                                                                                                                   |
| V <sub>IL</sub>   | Input low voltage                 | –   | –   | 0.75 | V    | $V_{DD} = 2.4$ to 3.6V.                                                                                                                                                                                                                                   |
| V <sub>IH1</sub>  | Input high voltage                | 1.4 | –   | –    | V    | $V_{DD} = 2.4$ to 2.9V and 3.1V to 3.6V.                                                                                                                                                                                                                  |
| V <sub>IH2</sub>  | Input high voltage                | 1.6 | –   | –    | V    | $V_{DD} = 2.7$ to 2.9V and 3.1V to 3.6V.                                                                                                                                                                                                                  |
| V <sub>H</sub>    | Input hysteresis voltage          | –   | 60  | –    | mV   |                                                                                                                                                                                                                                                           |
| I <sub>IL</sub>   | Input leakage                     | –   | 1   | –    | nA   | Gross tested to 1 $\mu\text{A}$ .                                                                                                                                                                                                                         |
| C <sub>IN</sub>   | Capacitive load on pins as input  | 0.5 | 1.7 | 5    | pF   | Package and pin dependent.<br>Temp = 25°C.                                                                                                                                                                                                                |
| C <sub>OUT</sub>  | Capacitive load on pins as output | 0.5 | 1.7 | 5    | pF   | Package and pin dependent.<br>Temp = 25°C.                                                                                                                                                                                                                |

**2.7V DC Spec for I<sup>2</sup>C Line with 1.8V External Pull-Up**

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 2.9V and 3.10V to 3.60V, and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 2.7V at 25°C. The I<sup>2</sup>C lines drive mode must be set to open drain and pulled up to 1.8V externally.

| Parameter         | Description                       | Min | Typ | Max  | Unit | Notes                                                                                                                                                                                          |
|-------------------|-----------------------------------|-----|-----|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>OLP1</sub> | Low output voltage port 1 pins    | –   | –   | 0.4  | V    | I <sub>OL</sub> =5 mA, maximum of 50 mA sink current on even port pins and 50 mA sink current on odd port pins.<br>$2.4 \leq V_{DD} \leq 2.9\text{V}$ and $3.1 \leq V_{DD} \leq 3.6\text{V}$ . |
| V <sub>IL</sub>   | Input low voltage                 | –   | –   | 0.75 | V    | $V_{DD} = 2.4$ to 2.90V and 3.10V to 3.6V.                                                                                                                                                     |
| V <sub>IH</sub>   | Input high voltage                | 1.4 | –   | –    | V    | $V_{DD} = 2.4$ to 2.7V.                                                                                                                                                                        |
| C <sub>IN</sub>   | Capacitive load on pins as input  | 0.5 | 1.7 | 5    | pF   | Package and pin dependent.<br>Temp = 25°C.                                                                                                                                                     |
| C <sub>OUT</sub>  | Capacitive load on pins as output | 0.5 | 1.7 | 5    | pF   | Package and pin dependent.<br>Temp = 25°C.                                                                                                                                                     |

**DC POR AND LVD Specifications**

| Parameter          | Description                                          | Min  | Typ  | Max  | Unit | Notes                                                                                                                  |
|--------------------|------------------------------------------------------|------|------|------|------|------------------------------------------------------------------------------------------------------------------------|
| V <sub>PPOR0</sub> | V <sub>DD</sub> Value for PPOR Trip                  | –    | 2.36 | 2.40 | V    | V <sub>DD</sub> must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from watchdog. |
| V <sub>PPOR1</sub> | V <sub>DD</sub> = 2.7V<br>V <sub>DD</sub> = 3.3V, 5V | –    | 2.60 | 2.65 | V    |                                                                                                                        |
| VLVD0              | V <sub>DD</sub> Value for LVD Trip                   | 2.39 | 2.45 | 2.51 | V    |                                                                                                                        |
| VLVD2              | V <sub>DD</sub> = 2.7V                               | 2.75 | 2.92 | 2.99 | V    |                                                                                                                        |
| VLVD6              | V <sub>DD</sub> = 3.3V<br>V <sub>DD</sub> = 5V       | 3.98 | 4.05 | 4.12 | V    |                                                                                                                        |

## DC Programming Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq \text{TA} \leq 85^{\circ}\text{C}$ , 3.10V to 3.6V and  $-40^{\circ}\text{C} \leq \text{TA} \leq 85^{\circ}\text{C}$ , or 2.4V to 2.90V and  $-40^{\circ}\text{C} \leq \text{TA} \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only. Flash Endurance and Retention specifications with the use of EEPROM user module are valid only within the range:  $25^{\circ}\text{C} \pm 20^{\circ}\text{C}$  during the Flash Write operation.

Refer to the EEPROM user module data sheet instructions for EEPROM Flash Write requirements outside the  $25^{\circ}\text{C} \pm 20^{\circ}\text{C}$  temperature window. Use of this User Module for Flash Writes outside this range must occur at a known die temperature ( $\pm 20^{\circ}\text{C}$ ) and requires the designer to configure the temperature as a variable rather than the default 25°C value hard coded into the API. All use of this UM API outside the range of  $25^{\circ}\text{C} \pm 20^{\circ}\text{C}$  is at the user's own risk. This risk includes overwriting the Flash cell (when above the allowable temperature range) thereby reducing the data sheet specified endurance performance or underwriting the Flash cell (when below the allowable temperature range) thereby reducing the data sheet specified retention.

| Symbol                | Description                                                                                 | Min                   | Typ | Max                    | Units | Notes                                |
|-----------------------|---------------------------------------------------------------------------------------------|-----------------------|-----|------------------------|-------|--------------------------------------|
| V <sub>DDWRITE</sub>  | Supply Voltage for Flash Write Operations <sup>[2]</sup>                                    | 2.7                   | –   | –                      | V     |                                      |
| I <sub>DDP</sub>      | Supply Current During Programming or Verify                                                 | –                     | 5   | 25                     | mA    |                                      |
| V <sub>ILP</sub>      | Input Low Voltage During Programming or Verify                                              | –                     | –   | 0.8                    | V     |                                      |
| V <sub>IHP</sub>      | Input High Voltage During Programming or Verify                                             | 2.2                   | –   | –                      | V     |                                      |
| I <sub>ILP</sub>      | Input Current when Applying V <sub>ilp</sub> to P1[0] or P1[1] During Programming or Verify | –                     | –   | 0.2                    | mA    | Driving internal pull down resistor. |
| I <sub>IHP</sub>      | Input Current when Applying V <sub>ihp</sub> to P1[0] or P1[1] During Programming or Verify | –                     | –   | 1.5                    | mA    | Driving internal pull down resistor. |
| V <sub>OLV</sub>      | Output Low Voltage During Programming or Verify                                             | –                     | –   | V <sub>SS</sub> + 0.75 | V     |                                      |
| V <sub>OHV</sub>      | Output High Voltage During Programming or Verify                                            | V <sub>DD</sub> – 1.0 | –   | V <sub>DD</sub>        | V     |                                      |
| Flash <sub>ENPB</sub> | Flash Endurance (per block)                                                                 | 50,000                | –   | –                      | –     | Erase/write cycles per block.        |
| Flash <sub>ENT</sub>  | Flash Endurance (total)                                                                     | 1,800,000             | –   | –                      | –     | Erase/write cycles.                  |
| Flash <sub>DR</sub>   | Flash Data Retention                                                                        | 10                    | –   | –                      | Years |                                      |

## CapSense Electrical Characteristics

| Max (V) | Typical (V) | Min (V) | Conditions for Supply Voltage | Result                                                                                                                                          |
|---------|-------------|---------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 3.6     | 3.3         | 3.10    | <2.9V                         | The device automatically reconfigures itself to work in 2.7V mode of operation.                                                                 |
| 3.10    | 2.7         | 2.45    | <2.45V                        | The scanning for CapSense parameters shuts down until the voltage returns to over 2.45V.                                                        |
|         |             |         | <2.4V                         | The device goes into reset.                                                                                                                     |
| 3.6     | 3.3         | 3.10    | >3.10V                        | The device automatically reconfigures itself to work in 3.3V mode of operation.                                                                 |
| 5.25    | 5.0         | 4.75    | <4.73V                        | The scanning for CapSense parameters shuts down until the voltage returns to over 4.73V.                                                        |
|         |             |         | 3.6 to 4.75V                  | This range is not supported by CapSense Express. The device will work, but CapSense scanning is not enabled until the voltage goes above 4.73V. |
|         |             |         | 2.9 to 3.1V                   | This range is not supported by CapSense Express.                                                                                                |

### Note

- Commands involving Flash Writes (0x01, 0x02, 0x03) must be executed only within the same VCC voltage range detected at POR (power on, XRES, or command 0x06) and above 2.7V. For register details, refer to CY8C201xx Register Reference Guide. If the user powers up the device in the 2.4V–3.6V range, Flash writes must be performed only in the range 2.7V to 2.9V and 3.10V to 3.6V. If the user powers up the device in the 4.75V to 5.25V range, Flash writes must be performed in that range only.

## AC Electrical Characteristics

### 5V and 3.3V AC General Purpose IO Specifications

| Parameter | Description                                         | Min | Max | Unit | Notes                                                         |
|-----------|-----------------------------------------------------|-----|-----|------|---------------------------------------------------------------|
| TRise0    | Rise time, strong mode,<br>Cload = 50 pF, Port 0    | 15  | 80  | ns   | V <sub>DD</sub> = 3.10V to 3.6V and 4.75V to 5.25V, 10% - 90% |
| TRise1    | Rise time, strong mode,<br>Cload = 50 pF, Port 1    | 10  | 50  | ns   | V <sub>DD</sub> = 3.10V to 3.6V, 10% - 90%                    |
| TFall     | Fall time, strong mode,<br>Cload = 50 pF, all ports | 10  | 50  | ns   | V <sub>DD</sub> = 3.10V to 3.6V and 4.75V to 5.25V, 10% - 90% |

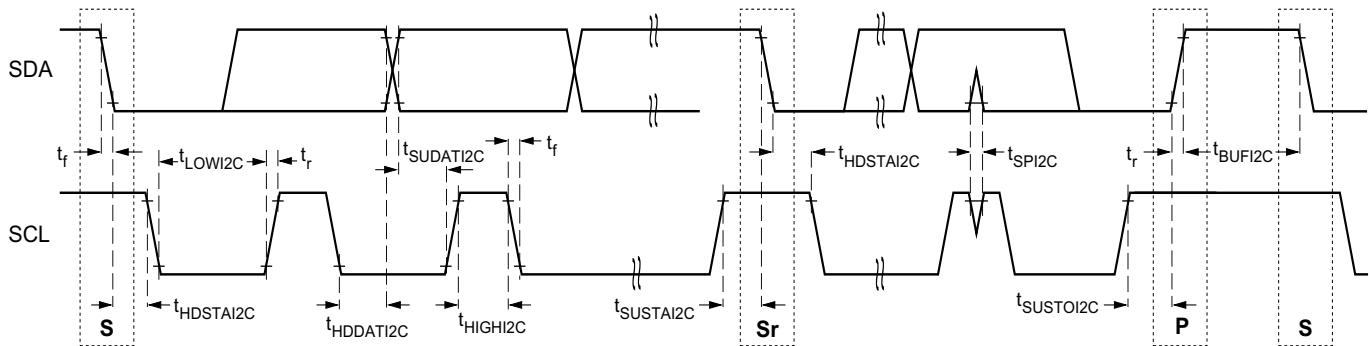
### 2.7V AC General Purpose IO Specifications

| Parameter | Description                                         | Min | Max | Unit | Notes                                      |
|-----------|-----------------------------------------------------|-----|-----|------|--------------------------------------------|
| TRise0    | Rise time, strong mode,<br>Cload = 50 pF, Port 0    | 15  | 100 | ns   | V <sub>DD</sub> = 2.4V to 2.90V, 10% - 90% |
| TRise1    | Rise time, strong mode,<br>Cload = 50 pF, Port 1    | 10  | 70  | ns   | V <sub>DD</sub> = 2.4V to 2.90V, 10% - 90% |
| TFall     | Fall time, strong mode,<br>Cload = 50 pF, all ports | 10  | 70  | ns   | V <sub>DD</sub> = 2.4V to 2.90V, 10% - 90% |

### AC I<sup>2</sup>C Specifications

| Parameter              | Description                                                                                 | Standard Mode |     | Fast Mode |     | Unit | Notes                                              |
|------------------------|---------------------------------------------------------------------------------------------|---------------|-----|-----------|-----|------|----------------------------------------------------|
|                        |                                                                                             | Min           | Max | Min       | Max |      |                                                    |
| F <sub>SCL</sub> I2C   | SCL clock frequency                                                                         | 0             | 100 | 0         | 400 | kHz  | Fast mode not supported for V <sub>DD</sub> < 3.0V |
| T <sub>HD</sub> STAI2C | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0           | -   | 0.6       | -   | μs   |                                                    |
| T <sub>LOW</sub> I2C   | LOW period of the SCL clock                                                                 | 4.7           | -   | 1.3       | -   | μs   |                                                    |
| T <sub>HIGH</sub> I2C  | HIGH period of the SCL clock                                                                | 4.0           | -   | 0.6       | -   | μs   |                                                    |
| T <sub>SU</sub> STAI2C | Setup time for a repeated START condition                                                   | 4.7           | -   | 0.6       | -   | μs   |                                                    |
| T <sub>HD</sub> DAI2C  | Data hold time                                                                              | 0             | -   | 0         | -   | μs   |                                                    |
| T <sub>SU</sub> DAI2C  | Data setup time                                                                             | 250           | -   | 100       | -   | ns   |                                                    |
| T <sub>SU</sub> STOI2C | Setup time for STOP condition                                                               | 4.0           | -   | 0.6       | -   | μs   |                                                    |
| T <sub>BU</sub> FI2C   | BUS free time between a STOP and START condition                                            | 4.7           | -   | 1.3       | -   | μs   |                                                    |
| T <sub>SPI</sub> I2C   | Pulse width of spikes suppressed by the input filter                                        | -             | -   | 0         | 50  | ns   |                                                    |

Figure 3. Definition of Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus



### Ordering Information

| Ordering Code   | Package Diagram | Package Type          | Operating Temperature |
|-----------------|-----------------|-----------------------|-----------------------|
| CY8C20140-LDX2I | 001-09116       | 16 COL <sup>[5]</sup> | Industrial            |
| CY8C20140-SX2I  | 51-85068        | 16 SOIC               | Industrial            |

### Thermal Impedances by Package

| Package               | Typical $\theta_{JA}$ <sup>[3]</sup> |
|-----------------------|--------------------------------------|
| 16 COL <sup>[5]</sup> | 46 °C                                |
| 16 SOIC               | 79.96 °C                             |

### Solder Reflow Peak Temperature

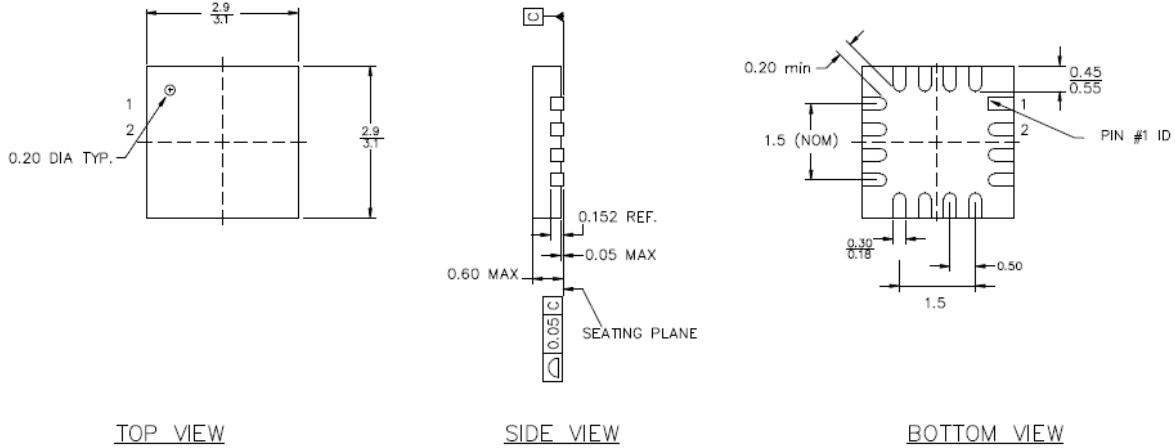
| Package               | Minimum Peak Temperature <sup>[4]</sup> | Maximum Peak Temperature |
|-----------------------|-----------------------------------------|--------------------------|
| 16 COL <sup>[5]</sup> | 240 °C                                  | 260 °C                   |
| 16 SOIC               | 240 °C                                  | 260 °C                   |

**Notes**

3.  $T_j = T_A + Power \times \theta_{JA}$ .
4. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are  $220 \pm 5^\circ\text{C}$  with Sn-Pb or  $245 \pm 5^\circ\text{C}$  with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.
5. Earlier termed as QFN package.

Package Diagrams

Figure 4. 16L Chip On Lead 3 X 3 mm Package Outline (SAWN) - 001-09116 - (Pb-Free)



TOP VIEW

SIDE VIEW

BOTTOM VIEW

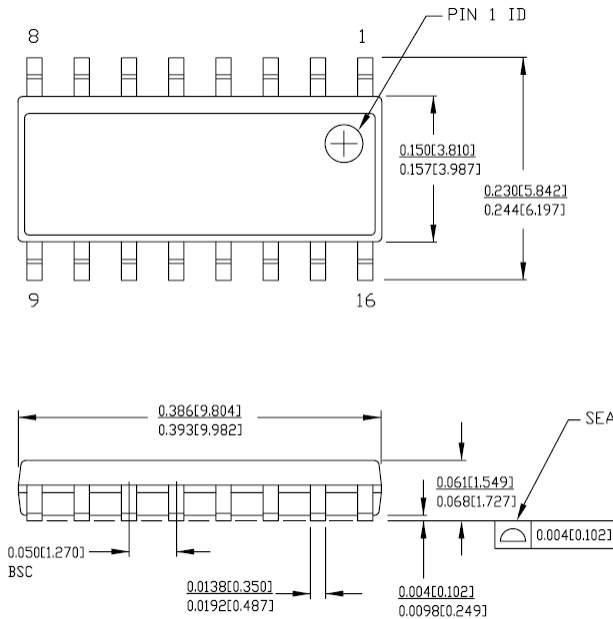
| PART NO. | DESCRIPTION |
|----------|-------------|
| LG16A    | LEAD-FREE   |
| LD16A    | STANDARD    |

NOTES:

1. JEDEC # MQ-220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM,  $\frac{\text{MIN}}{\text{MAX}}$

001-09116 \*D

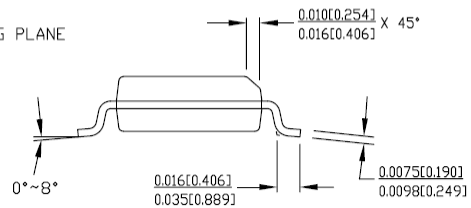
Figure 5. 16-Pin (150-Mil) SOIC (51-85068)



DIMENSIONS IN INCHES[MM]  $\frac{\text{MIN.}}{\text{MAX.}}$

REFERENCE JEDEC MS-012  
PACKAGE WEIGHT 0.15gms

| PART #  |                |
|---------|----------------|
| S16.15  | STANDARD PKG.  |
| SZ16.15 | LEAD FREE PKG. |



51-85068-\*B

Document History Page

| Document Title: CY8C20140 CapSense Express™ - 4 Configurable IOs<br>Document Number: 001-17348 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                           | ECN No. | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| **                                                                                             | 1341766 | TUP/VED         | See ECN         | New Datasheet                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| *A                                                                                             | 1494145 | TUP/AESA        | See ECN         | Changed to FINAL Datasheet<br>Removed table - 2.7V DC General Purpose IO Specifications - Open Drain with a pull up to 1.8V<br>Updated Logic Block Diagram<br>Removed Pinout and Package Diagram for 8-SOIC                                                                                                                                                                                                                                                                                                |
| *B                                                                                             | 1773608 | TUP/AESA        | See ECN         | Removed table - 3V DC General Purpose IO Specifications<br>Updated Logic Block Diagram<br>Updated table - DC POR and LVD Specifications<br>Updated table - DC Chip Level Specifications<br>Updated table - 5V and 3.3V DC General Purpose IO Specifications<br>Updated table - 2.7V DC General Purpose IO Specifications<br>Updated table - AC GPIO Specifications and split it into two tables for 5V/3.3V and 2.7V<br>Added section on CapSense Express™ Software tool<br>Updated 16-QFN Package Diagram |
| *C                                                                                             | 2091026 | DZU/MOHD /AESA  | See ECN         | Updated table-DC Chip Level Specifications<br>Updated table-Pin Definitions 16 pin COL<br>Updated table-Pin Definitions 16 pin SOIC<br>Updated table-5V and 3.3V DC General Purpose IO Specifications<br>Updated table - 2.7V DC General Purpose IO Specifications<br>Changed definition for Timing for Fast/Standard Mode on the I2C Bus diagram                                                                                                                                                          |
| *D                                                                                             | 2404731 | DZU/MOHD/P YRS  | See ECN         | Updated Logic Block Diagram<br>Added DC Programming Specifications Table<br>Updated Features<br>Added CapSense Electrical Specifications Table                                                                                                                                                                                                                                                                                                                                                             |
| *E                                                                                             | 2544918 | ZSK/AESA        | See ECN         | Different sleep modes explained<br>Bi-Directional Sleep Control Pin defined<br>Table added on "2.7V DC Spec for I2C Line with 1.8V External Pull-Up                                                                                                                                                                                                                                                                                                                                                        |
| *F                                                                                             | 2648811 | DZU/PYRS        | 01/28/09        | Included section on I2C Device Addressing<br>Updated CapSense Electrical Specifications table<br>Deleted VOH5, VOH6, VOH7, and VOH8 parameters                                                                                                                                                                                                                                                                                                                                                             |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [cypress.com/sales](http://cypress.com/sales).

#### Products

|                  |                                                                |
|------------------|----------------------------------------------------------------|
| PSoC             | <a href="http://psoc.cypress.com">psoc.cypress.com</a>         |
| Clocks & Buffers | <a href="http://clocks.cypress.com">clocks.cypress.com</a>     |
| Wireless         | <a href="http://wireless.cypress.com">wireless.cypress.com</a> |
| Memories         | <a href="http://memory.cypress.com">memory.cypress.com</a>     |
| Image Sensors    | <a href="http://image.cypress.com">image.cypress.com</a>       |

#### PSoC Solutions

|                       |                                                                                          |
|-----------------------|------------------------------------------------------------------------------------------|
| General               | <a href="http://psoc.cypress.com/solutions">psoc.cypress.com/solutions</a>               |
| Low Power/Low Voltage | <a href="http://psoc.cypress.com/low-power">psoc.cypress.com/low-power</a>               |
| Precision Analog      | <a href="http://psoc.cypress.com/precision-analog">psoc.cypress.com/precision-analog</a> |
| LCD Drive             | <a href="http://psoc.cypress.com/lcd-drive">psoc.cypress.com/lcd-drive</a>               |
| CAN 2.0b              | <a href="http://psoc.cypress.com/can">psoc.cypress.com/can</a>                           |
| USB                   | <a href="http://psoc.cypress.com/usb">psoc.cypress.com/usb</a>                           |

---

© Cypress Semiconductor Corporation, 2007-2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.