ACT8332

Rev0, 14-Mar-08

Three Channel Integrated Power Management IC for Handheld Portable Equipment

FEATURES

- **Multiple Patents Pending**
- **Three Integrated Regulators**
  - **350mA PWM Step-Down DC/DC**
  - **360mA Low Noise LDO**
  - **360mA Low Noise LDO**
- **Independent Enable/Disable Control**
- **Minimal External Components**
- **3×3mm, Thin-DFN (TDFN33-10) Package**
  - **Only 0.75mm Height**
  - **RoHS Compliant**

APPLICATIONS

- **Portable Devices and PDAs**
- **MP3/MP4 Players**
- **Wireless Handhelds**
- **GPS Receivers, etc.**

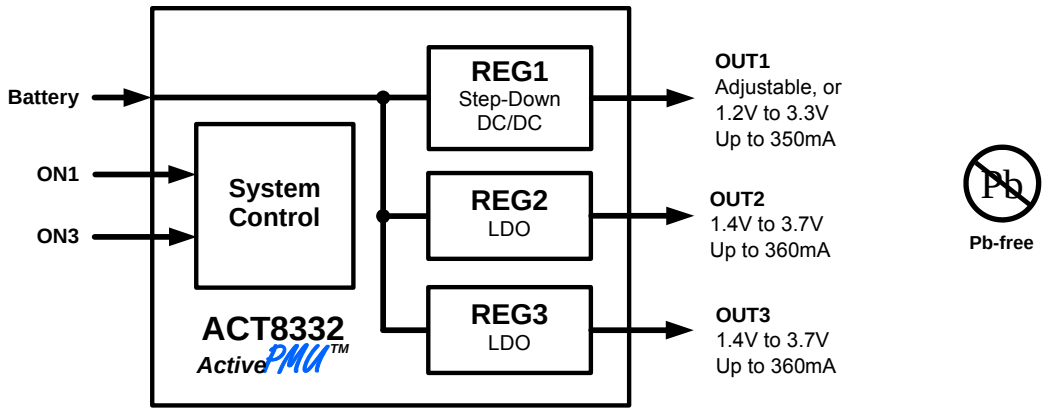
GENERAL DESCRIPTION

The patent-pending ACT8332 is a complete, cost effective, highly-efficient *ActivePMU*™ power management solution that is ideal for a wide range of portable handheld equipment. This device integrates one PWM step-down DC/DC converter and two low noise, low dropout linear regulators (LDOs) in a single, thin, space-saving package. This device is ideal for a wide range of portable handheld equipment that can benefit from the advantages of *ActivePMU* technology but does not require a high level of integration.

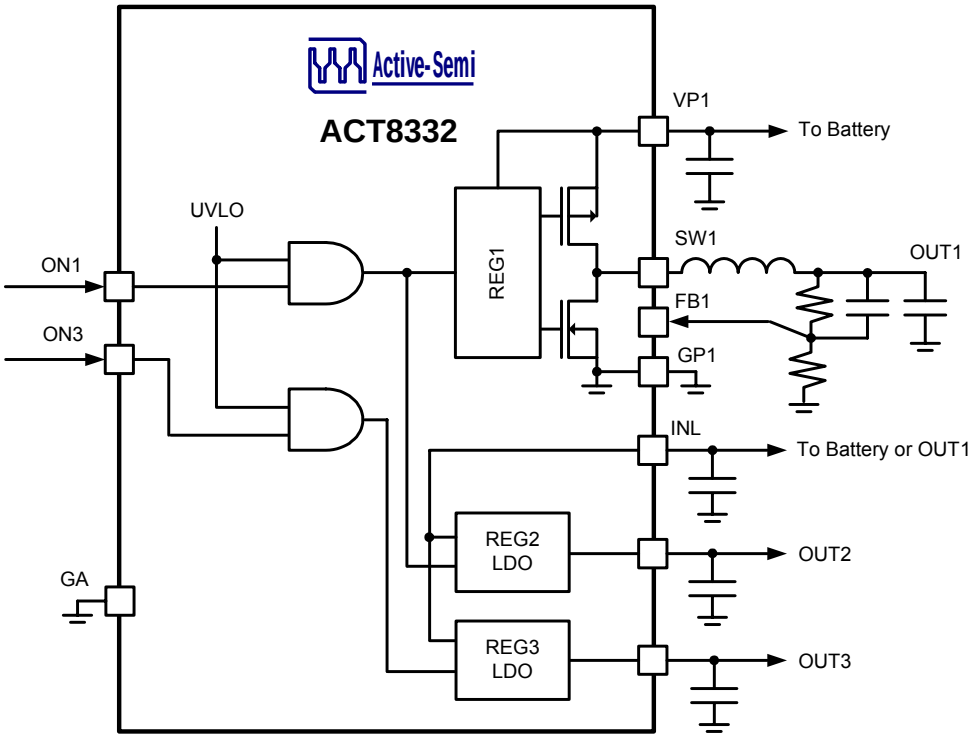
REG1 is a fixed-frequency, current-mode PWM step-down DC/DC converter that is optimized for high efficiency and is capable of supplying up to 350mA output current. REG1's output is available in a variety of factory-preset output voltage options, and an adjustable output voltage mode is also available. REG2, REG3 are low noise, high PSRR linear regulators that are capable of supplying up to 360mA, and 360mA, respectively.

The ACT8332 is available in a tiny 3mm × 3mm 10-pin Thin-DFN package that is just 0.75mm thin.

SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①②

PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8332NDAQB-T	Adjustable	2.85V	2.5V	TDFN33-10	10	-40°C to +85°C

REG1 OUTPUT VOLTAGE CODES										
A	C	P	J	D	E	F	I	Q	G	H
Adjustable	1.2V	1.3V	1.4V	1.5V	1.8V	2.5V	2.8V	2.85V	3.0V	3.3V

REG2 OUTPUT VOLTAGE CODES								
J	D	L	E	F	I	Q	G	H
1.4V	1.5V	1.7V	1.8V	2.5V	2.8V	2.85V	3.0V	3.3V

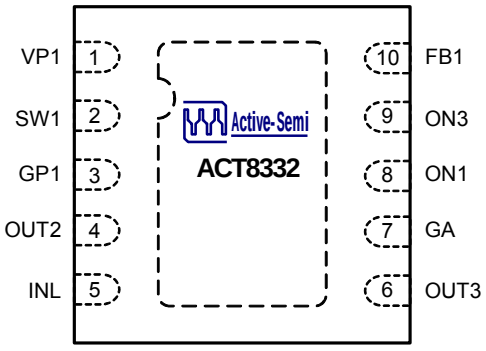
REG3 OUTPUT VOLTAGE CODES								
E	G	K	M	B	H	I	L	R
1.4V	1.5V	1.7V	1.8V	2.5V	2.8V	2.85V	3.0V	3.3V

①: Output voltage options detailed in this table represent standard voltage options, and are available for samples or production orders. Additional output voltage options, as detailed in the *Output Voltage Codes* table, are available for production subject to minimum order quantities. Contact Active-Semi for more information regarding semi-custom output voltage combinations.

②: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

PIN CONFIGURATION

TOP VIEW



Thin - DFN (TDFN 33-10)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	VP1	Power Input for REG1. Bypass to GP1 with a high quality ceramic capacitor placed as close as possible to the IC.
2	SW1	Switching node Output for REG1. Connect this pin to the switching end of the inductor.
3	GP1	Power Ground for REG1. Connect GA, GP1 together at a single point as close to the IC as possible.
4	OUT2	Output voltage for REG2. Capable of delivering up to 360mA of output current. Output has high impedance when disabled.
5	INL	Power input for REG2, REG3. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC.
6	OUT3	Output voltage for REG3. Capable of delivering up to 360mA of output current. Output has high impedance when disabled.
7	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP1 together at a single point as close to the IC as possible.
8	ON1	Enable control input for REG1, REG2. Drive ON1 to the VP1 or a logic high for normal operation, drive to GA or a logic low to disable REG1, REG2
9	ON3	Enable control input for REG3. Drive ON3 to the INL or a logic high for normal operation, drive to GA or a logic low to disable REG3
10	FB1	Output Feedback Sense. For fixed output voltage options REG1, connect this pin directly to the output node to connect the internal feedback network to the output voltage. For adjustable output voltage Options REG1. The voltage at this pin is regulated to 0.625V. Connect this pin to the center point of the output voltage feedback network between OUT1 and GA to set the output voltage.
EP	EP	Exposed Pad. Must be soldered to ground on PCB

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
SW1 to GP1, INL, VP1, FB1, OUT2, OUT3, ON1, ON3 to GA	-0.3 to +6	V
SW1 to VP1	-6 to +0.3	V
GP1 to GA	-0.3 to +0.3	V
Junction to Ambient Thermal Resistance (θ_{JA})	33	°C/W
Operating Temperature Range	-40 to 85	°C
Junction Temperature	125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (REG1)

(V_{VP1} = 3.6V, T_A = 25°C, unless otherwise specified.)

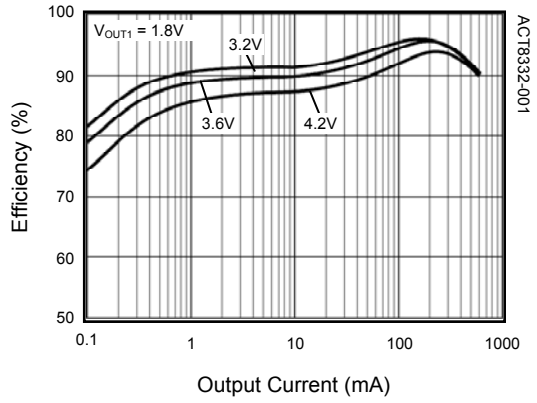
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP1 Operating Voltage Range		3.1		5.5	V
VP1 UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP1 UVLO Hysteresis	Input Voltage Falling		90		mV
Standby Supply Current			130	200	µA
Shutdown Supply Current	ON1 = GA, V_{VP1} = 4.2V		0.1	1	µA
Adjustable Output Option Regulation Voltage			0.625		V
Output Voltage Regulation Accuracy	V_{NOM1} < 1.3V, I_{OUT1} = 10mA	-2.4%	V_{NOM1}①	+1.8%	V
	V_{NOM1} ≥ 1.3V, I_{OUT1} = 10mA	-1.2%	V_{NOM1}	+1.8%	
Line Regulation	V_{VP1} = Max(V_{NOM1} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT1} = 10mA to 350mA		0.0017		%/mA
Current Limit		0.45	0.6		A
Oscillator Frequency	V_{OUT1} ≥ 20% of V_{NOM1}	1.35	1.6	1.85	MHz
	V_{OUT1} = 0V		530		kHz
ON1 Logic High Input Voltage	V_{INL} = 3.1V to 5.5V, V_{VP1} = 3.1V to 5.5V, T_A = -40°C to 85°C	1.4			V
ON1 Logic Low Input Voltage	V_{INL} = 3.1V to 5.5V, V_{VP1} = 3.1V to 5.5V, T_A = -40°C to 85°C			0.4	V
PMOS On-Resistance	I_{SW1} = -100mA		0.52	0.88	Ω
NMOS On-Resistance	I_{SW1} = 100mA		0.27	0.46	Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM1}
Minimum On-Time			70		ns
Thermal Shutdown Temperature	Temperature Rising		160		°C
Thermal Shutdown Hysteresis	Temperature Falling		20		°C

①: V_{NOM1} refers to the nominal output voltage level for V_{OUT1} as defined by the *Ordering Information* section.

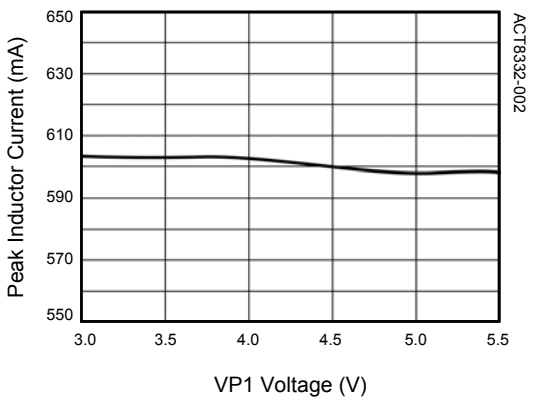
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8332NDAQB, V_{VP1} = 3.6V, L = 3.3µH, C_{VP1} = 2.2µF, C_{OUT1} = 10µF, T_A = 25°C, unless otherwise specified.)

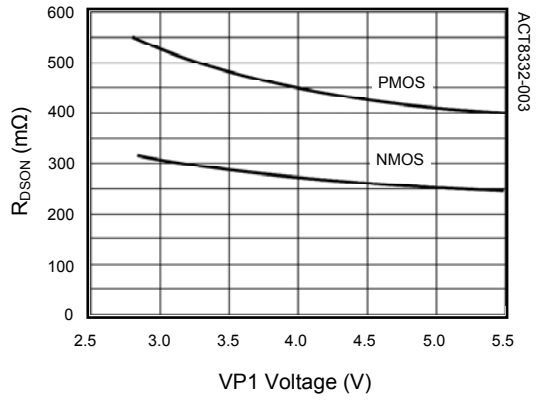
REG1 Efficiency vs. Load Current



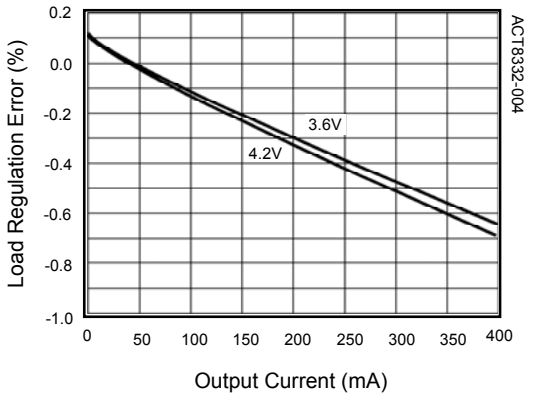
REG1 Transient Peak Inductor Current



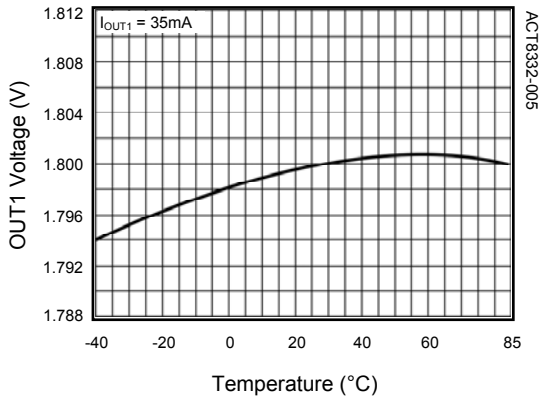
REG1 MOSFET Resistance



REG1 Load Regulation



OUT1 Regulation Voltage



FUNCTIONAL DESCRIPTION

General Description

REG1 is a fixed-frequency, current-mode, synchronous PWM step-down converters that achieves a peak efficiency of up to 97%. REG1 is capable of supplying up to 350mA of output current and operates with a fixed frequency of 1.6MHz, minimizing noise in sensitive applications and allowing the use of small external components. REG1 is available with a variety of standard and custom output voltages, as well as an adjustable output voltage option.

100% Duty Cycle Operation

REG1 is capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery-powered applications.

Synchronous Rectification

REG1 features an integrated n-channel synchronous rectifier, which maximizes efficiency and minimizes the total solution size and cost by eliminating the need for an external rectifier.

Enabling and Disabling REG1

REG1 is enabled or disabled using ON1. Drive ON1 to a logic-high to enable REG1. Drive ON1 to a logic-low to disable REG1, reducing supply current to less than 1μA

Soft-Start

REG1 includes internal soft-start circuitry, and enabled its output voltage tracks an internal 80μs soft-start ramp so that it powers up in a monotonic manner that is independent of loading.

Compensation

REG1 utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. No compensation design is required, simply follow a few simple guidelines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 2.2μF ceramic input capacitor is recommended for most applications.

Output Capacitor Selection

For most applications, a 10μF ceramic output capacitor is recommended. Although REG1 was designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR, low-ESR tantalum capacitors can provide acceptable results as well.

Inductor Selection

REG1 utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. REG1 was optimized for operation with a 3.3μH inductor, although inductors in the 2.2μH to 4.7μH range can be used. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current of the application by at least 30%.

Thermal Shutdown

The ACT8332 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions. This circuitry disables all regulators if the ACT8332 die temperature exceeds 160°C, and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

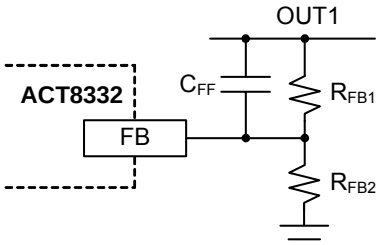
Output Voltage Programming

Figure 4 shows the feedback network necessary to set the output voltage when using the adjustable output voltage option. Select components as follows: Set R_{FB2} = 51KΩ, then calculate R_{FB1} using the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT1}}{V_{FB1}} - 1\right) \quad (1)$$

Where V_{FB1} is 0.625V

Figure 4:
Output Voltage Programming



Finally choose C_{FF} using the following equation:

$$C_{FF} = \frac{2.2 \times 10^{-6}}{R_{FB1}} \qquad (2)$$

where R_{FB1} = 47kΩ, use 47pF.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of vias if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loops should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple vias. For fixed output voltage options, connect the output node directly to the FB1 pin. For adjustable output voltage options, connect the feedback resistors and feed-forward capacitor to the FB1 pin through the shortest possible route. In both cases, the feedback path should be routed to maintain sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple vias to achieve low electrical and thermal resistance.

ELECTRICAL CHARACTERISTICS (REG2, REG3)

(V_{INL} = 3.6V, C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		3.1		5.5	V
INL UVLO Threshold	V_{INL} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{INL} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	V_{NOM}①	+2	%
	T_A = -40°C to 85°C	-2.5	V_{NOM}	+3	
Line Regulation Error	V_{INL} = Max(V_{OUT} + 0.5V, 3.6V) to 5.5V		0		mV
Load Regulation Error	I_{OUT} = 1mA to 360mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 360mA, C_{OUT} = 1μF		70		dB
	f = 10kHz, I_{OUT} = 360mA, C_{OUT} = 1μF		60		
Supply Current	REG2 or REG3 Enabled		85		μA
	REG2 and REG3 Enabled		125		
	REG2 and REG3 Disabled		1.5		
ON1, ON3 Logic High Input Voltage	V_{INL} = 3.1V to 5.5V, T_A = -40°C to 85°C	1.4			V
ON1, ON3 Logic Low Input Voltage	V_{INL} = 3.1V to 5.5V, T_A = -40°C to 85°C			0.4	V
Dropout Voltage②	I_{OUT} = 160mA, V_{OUT} > 3.1V		100	200	mV
Output Current				360	mA
Current Limit③	V_{OUT} = 95% of regulation voltage	400			mA
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT}, hysteresis = -4%		89		%
Output Noise	C_{OUT} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT} Range		1		20	μF
Discharge Resistor in Shutdown	LDO Disabled		1000		Ω
Thermal Shutdown Temperature	Temperature Rising		160		°C
Thermal Shutdown Hysteresis	Temperature Falling		20		°C

①: V_{NOM} refers to the nominal output voltage level for V_{OUT2} or V_{OUT3} as defined by the *Ordering Information* section.

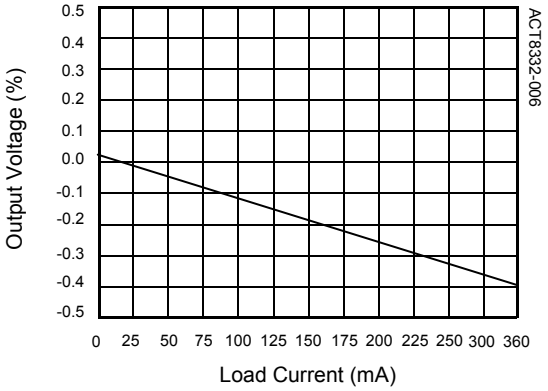
②: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

③: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 30% (typ)

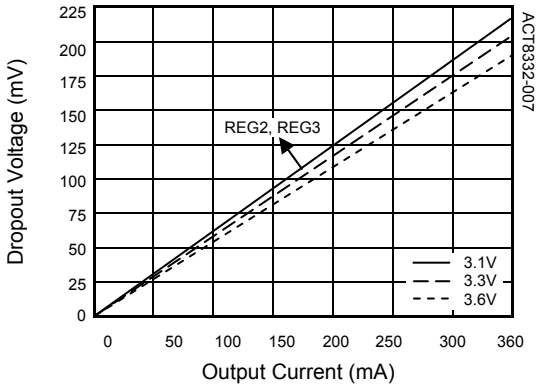
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8332NDAQB, V_{INL} = 5V, T_A = 25°C, unless otherwise specified.)

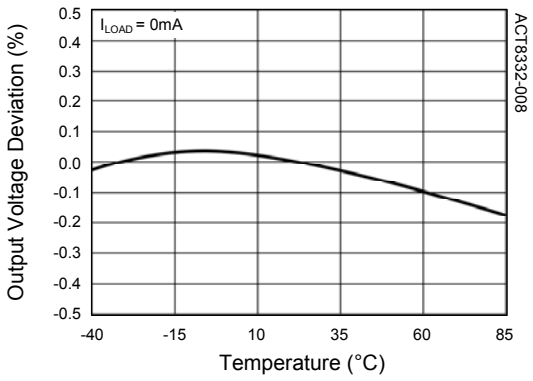
Load Regulation



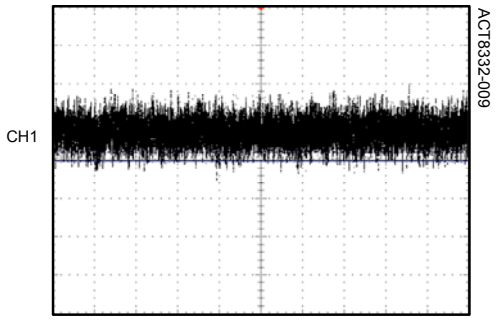
Dropout Voltage vs. Output Current



Output Voltage Deviation vs. Temperature

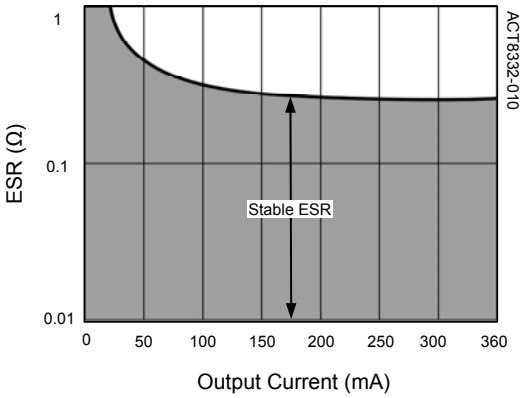


LDO Output Voltage Noise



CH1: V_{OUTx}, 200µV/div (AC COUPLED)
TIME: 200ms/div

Region of Stable C_{OUT} ESR vs. Output Current



FUNCTIONAL DESCRIPTION

General Description

REG2 and REG3 are low-noise, low-dropout linear regulators (LDOs) that are optimized for low-noise and high-PSRR operation, achieving more than 60dB PSRR at frequencies up to 10kHz.

Output Current Capability

REG2 and REG3 each supply 360mA of load current. Excellent performance is achieved over each regulator's entire load current ranges.

Output Current Limit

In order to ensure safe operation under over-load conditions, each LDO features current-limit circuitry with current fold-back. The current-limit circuitry limits the current that can be drawn from the output, providing protection in over-load conditions. For additional protection under extreme over current conditions, current-fold-back protection reduces the current-limit by approximately 30% under extreme overload conditions.

Enabling and Disabling the LDOs

REG2 and REG3 is enabled or disabled using ON1 and ON3. Drive ON1 and ON3 to a logic-high to enable REG2 and REG3. Drive ON1 and ON3 to a logic-low to disable REG2 and REG3, reducing supply current to less than 1μA.

Output Capacitor Selection

REG2 and REG3 each require only a small ceramic capacitor for stability. For best performance, each output capacitor should be connected directly between the OUT2 and OUT3 and G pins as possible, with a short and direct connection. To ensure best performance for the device, the output capacitor should have a minimum capacitance of 1μF, and ESR value between 10mΩ and 200mΩ. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

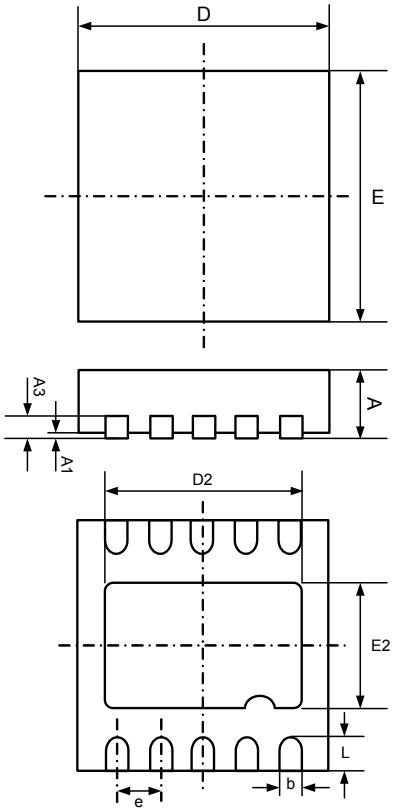
PCB Layout Considerations

The ACT8332's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance.

A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW nodes of the DC/DCs.

PACKAGE OUTLINE

TDFN33-10 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.0000	0.002
A3	0.153	0.253	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D2	2.350	2.450	0.093	0.096
E2	1.650	1.750	0.065	0.069
b	0.200	0.320	0.008	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

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