TEA1771

GreenChip PC primary control IC

Rev. 01 — 6 February 2009 Product data sheet

1. General description

The TEA1771 is a primary control IC for an active clamp forward converter. This converter enables higher duty cycles of up to 70 %. A higher maximum duty cycle lowers the required breakdown voltage of both the primary and secondary switches, reducing the total cost of the system.

The IC is optimized for (ATX) PC power supplies. Together with the TEA1781 and TEA1782 a unique system can be made that reduces costs by integrating the standby supply. It assures high output voltage accuracy and avoids cross regulation as the output voltages are regulated separately. This system exceeds the current and proposed efficiency standards such as 80 plus-gold, energy star and blue angel.

The TEA1771 is implemented in the high voltage EZ-HV SOI process. It enables direct start-up from the rectified mains voltage, excluding the need for a start-up resistor. The high voltage reset switch, required for the active clamp, is integrated in the IC. The IC has a feed-forward control regulation, avoiding high resonant voltage peaks as a result of output load or input voltage transients. This also assures proper regulation of the output voltages at input voltage variations.

2. Features

- Designed for ATX PC power supplies
- Universal mains operation, 90 V (AC) to 265 V (AC)
- Integrated start-up current source
- Integrated high-voltage, high-side active clamp reset switch
- Feed-forward regulation
- Enhanced efficiency in Standby mode and Normal mode
- OverVoltage Protection (OVP)
- OverCurrent Protection (OCP)
- Short-Winding Protection (SWP)
- Low external component count
- Soft (re)start
- High voltage ramp-up detection assuring Zero Voltage Switching (ZVS) of the reset switch
- Available in a 24-pin SO package

3. Applications

- PC desktop power supply

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltages						
V_{DM1}	voltage on pin DM1	continuous	–0.4	-	+570	V
		peak; Δt = 1 µs; non-repetitive	–0.4	-	+650	V
V_{DM2}	voltage on pin DM2	continuous	–0.4	-	+570	V
		peak; Δt = 1 µs; non-repetitive	–0.4	-	+650	V
V_{LVIN}	voltage on pin LVIN	continuous [1]	–0.4	-	+48	V
Currents						
$I_{ch(DM2)}$	charge current on pin DM2	V_{LVIN} = 0 V	2.3	2.9	3.5	mA
Reset switch						
R_{DSon}	drain-source on-state resistance	running mode; $V_{DD(float)}$ = 12 V				
		I_{DM2} = 0.1 A	20	25	30	Ω
		I_{DM2} = 0.3 A	11	15	22	Ω
Oscillator, opto control and secondary protection						
$f_{osc(max)}$	maximum oscillator frequency	$I_{OPTO(fmax)} > I_{OPTO} > I_{prot(OPTO)}$; I_{IREF} =				
		–200 µA	80	100 [2]	120	kHz
δ_{max}	maximum duty cycle	$I_{OPTO} < I_{OPTO(\delta max)}$; I_{IREF} = –100 mA; V_{LVIN} =				
		12 V	54.0	59.0	64.0	%
General						
T_{amb}	ambient temperature		–20	-	+85	°C

[1] Pin LVIN cannot be current driven.

[2] For the PSU, the recommended operating frequency is 75 kHz. The operating frequency can be raised to 100 kHz provided that the PSU input voltage, V_I, is above a minimum level which is typically 200 V. An application solution is available that automatically lowers the frequency when, during a mains dip, V_I drops below this minimum level. See the application note *Guidelines for applying the GreenChip PC chipset.*

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEA1771T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

6. Block diagram

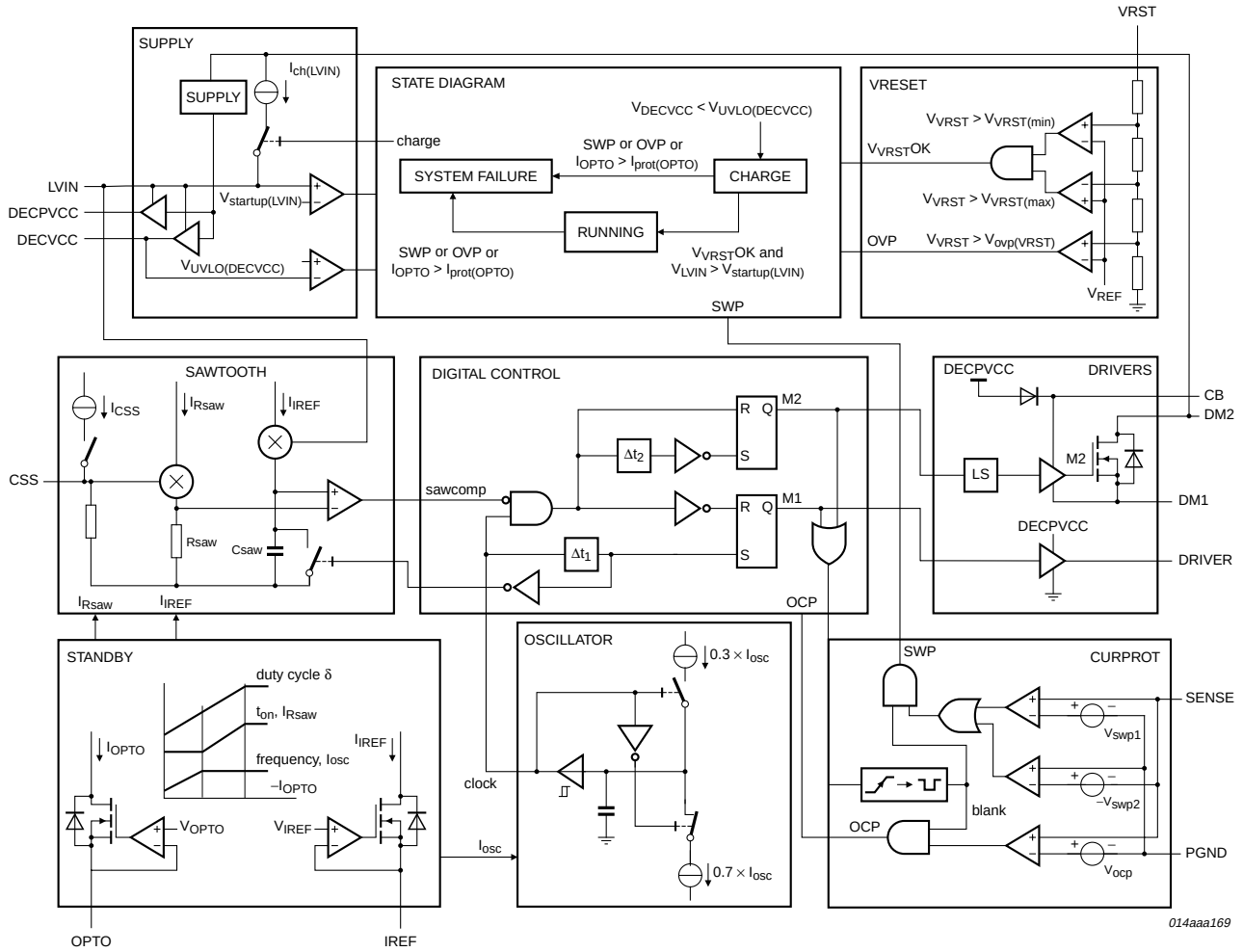


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

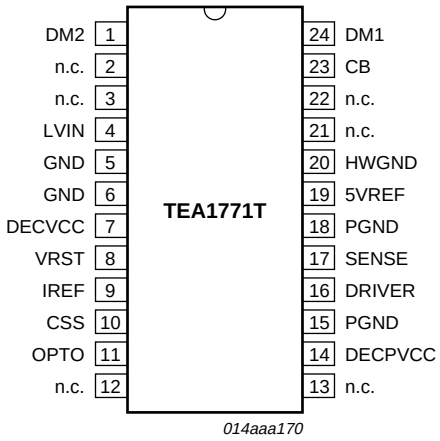


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
DM2	1	drain reset switch
n.c.	2	not connected
n.c.	3	not connected
LVIN	4	low voltage input (rectified auxiliary input)
GND	5	ground
GND	6	ground
DECVCC	7	decoupling supply voltage
VRST	8	reset capacitor voltage
IREF	9	oscillator reference current
CSS	10	capacitor soft start
OPTO	11	opto-coupler feedback input
n.c.	12	not connected
n.c.	13	not connected
DECPVCC	14	decoupling power supply
PGND	15	power ground
DRIVER	16	main switch gate driver
SENSE	17	overcurrent sensing
PGND	18	power ground
5VREF	19	5 V reference voltage
HWGND	20	handler wafer ground
n.c	21	not connected

Table 3. Pin description *...continued*

Symbol	Pin	Description
n.c	22	not connected
CB	23	boost capacitor
DM1	24	drain main switch (M1)

8. Functional description

8.1 Introduction

The TEA1771 is designed to cooperate with the TEA1781 and the TEA1782 secondary side controllers in a forward converter topology, see Figure 11. A typical application area of this converter is a power supply for a desktop PC.

The topology supported by the TEA1771 enables transformer resetting using an active reset mechanism. For this purpose a reset switch in the form of a lateral IGBT has been integrated into the IC. This reset switch can operate high-side using an external boost capacitor.

Advantage of this active reset mechanism is, compared to a third winding solution, that a higher maximum duty cycle (> 50%) can be achieved. Reducing dissipation by recovering energy is another advantage of the reset mechanism when compared to the standard R/C/D topology.

The TEA1771 has a feed-forward control regulation, avoiding high resonant voltage peaks as a result of output load or input voltage transients.

8.2 Supply

At power-up, the primary and secondary ICs are not yet supplied via the auxiliary windings as the main switch M1 is off, see Figure 11. Initially, before start-up, the primary IC is in Charge mode and supplies itself with a current $I_{ch(LVIN)}$ from the high voltage pin DM2, see the SUPPLY block in Figure 1. The voltage on pin DM2 is equal to the input voltage in this static situation. It is connected to the input via the transformer and the parallel diode of the reset switch, D_{rst}, see Figure 11. In Charge mode LVIN is charged from DM2 via an internal current source, $I_{ch(LVIN)}$. From LVIN the nodes DECVCC and DECPVCC are supplied by internal regulators. As a result, when LVIN is charged, the DECVCC and DECPVCC nodes, which are decoupled by external capacitors, are charged simultaneously. This is illustrated in the left part of Figure 3.

When the voltage at LVIN reaches its start level $V_{startup(LVIN)}$ and the voltage on pin VRST is in its start-up window, the IC enters Running mode and starts switching; see M1 signal in Figure 3. The voltage on pin VRST is in the start-up window when the voltage on pin VRST is between the minimum start voltage, $V_{start(VRST)(min)}$, and the maximum start voltage, $V_{start(VRST)(max)}$. These start-up conditions are pointed out in the STATE DIAGRAM block in Figure 1. If the logic signal V_{VRST}OK is high, the voltage V_{VRST} is in the start-up window.

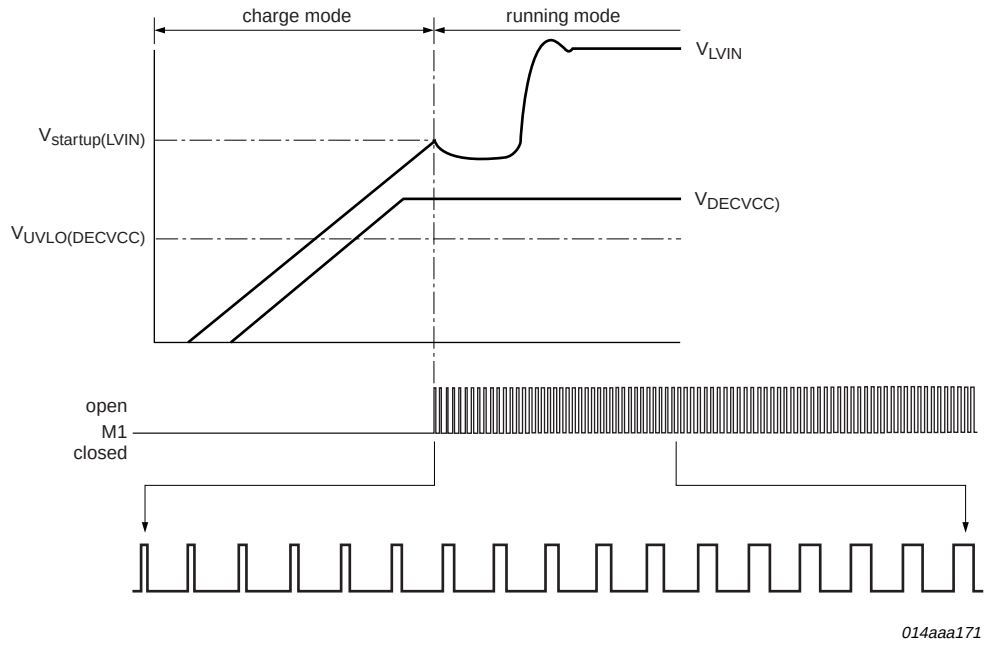


Fig 3. Start-up sequence TEA1771

Figure 11 shows the primary windings on the transformer. The main switch M1 directly powers up the primary winding. All remaining windings are also powered up via the transformer. The primary auxiliary winding is used to supply LVIN. Thus, when in Running mode, the primary IC is supplied externally by the primary auxiliary winding. The voltage on this winding reflects the input voltage scaled by a turn ratio. The internal current source between pin DM2 and pin LVIN is switched off in Running mode and System failure mode.

The secondary ICs are supplied via a rectified secondary winding. Because of this they start up after the primary side has started switching.

The voltage on pin VRST has to be in the start-up window to enable the controller to enter Running mode. Figure 11 shows that the pin VRST is connected to a resistive divider that is connected to DM2 (R1 and R2 in Figure 11). In Charge mode the voltage on DM2 is equal to the input voltage V_I. This implies that V_I must be in a specific window to start up the PSU. The IC parameters $V_{start(VRST)(min)}$ and $V_{start(VRST)(max)}$ are scaled by the divider ratio to a certain input voltage range. In a typical application setting the input voltage range is from 90 V (AC) to 264 V (AC).

8.3 Modes of operation

The TEA1771 features three operation modes: Charge mode, Running mode and System failure mode as shown in Figure 4.

When the DECVCC voltage is below the UVLO level the IC is in Charge mode. After sufficient charging of the external capacitor on pin LVIN, the IC enters Running mode and the system starts switching, see Figure 3.

When a system failure is detected, the IC enters System failure mode and the main switch and reset switch are turned off.

The switch that is in series with the current source, charging LVIN via DM2, is opened when the IC is in System failure mode (see the SUPPLY block in Figure 1). The IC consumption slowly discharges the LVIN capacitor. When V_{LVIN} has been discharged to the level of V_{DECVCC} and $V_{DECPVCC}$, these nodes are also discharged. Eventually the DECVCC voltage will drop below the UVLO level and the IC enters Charge mode. This is called a safe restart cycle. The period of this cycle depends on the capacitors at pins LVIN, DECVCC, and DECPVCC.

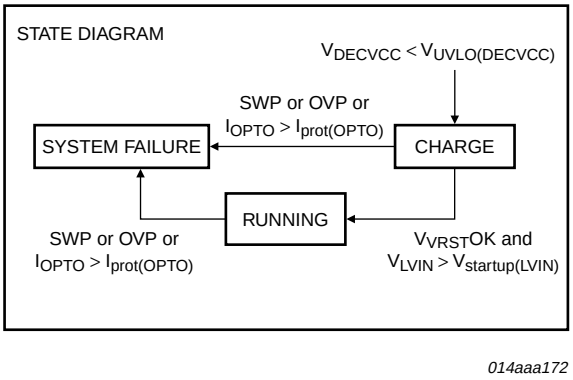


Fig 4. State diagram

8.4 Oscillator

In Figure 5 the OSCILLATOR block is shown together with the STANDBY block. The OSCILLATOR block shows the internal capacitor that is subsequently charged and discharged with the currents $0.3 \times I_{osc}$ and $0.7 \times I_{osc}$. The lower part of Figure 5 shows the oscillator signals. It points out that the I_{ch}/I_{dch} current ratio determines an internal clock with a duty cycle of 0.7. In Section 8.5 will be made clear that the clock duty cycle determines the max duty cycle that can be regulated.

Together with the capacitor value the I_{osc} current level determines the frequency. The I_{osc} is not fixed and therefore the frequency varies also.

Figure 5 shows that I_{osc} is generated by the STANDBY block and fed to the OSCILLATOR block. The curves in the STANDBY block show that I_{osc} is regulated by the current on pin OPTO, I_{OPTO}. For $I_{OPTO} > 2I_{IREF}$ the I_{osc} current is set to the maximum level, $I_{osc} = I_{IREF}$. As a result the frequency is set to the maximum level by putting $I_{OPTO} > 2I_{IREF}$.

$$f_{osc(max)} = \frac{I_{IREF}}{2} \quad (1)$$

- $f_{osc(max)}$ (kHz)
- I_{IREF} (µA)

I_{IREF} is regulated by the external resistor to pin IREF. The voltage on this pin is set to 3.6 V. The current I_{IREF} is set by choosing the resistor value.

$$I_{IREF} = \frac{V_{IREF}}{R_{IREF}} = \frac{3.6}{R_{IREF}} \quad (2)$$

Example:

A resistor of 36 kΩ sets I_{IREF} to 100 μA. This results in a frequency of 50 kHz.

If the Power Supply Unit (PSU) is in Normal mode I_{OPTO} is put at a high level, $I_{OPTO} > 2I_{IREF}$. This sets the TEA1771 frequency to the maximum level. If the PSU is in Standby mode, the frequency may be regulated to a lower level by lowering I_{OPTO}. See Section 8.8.

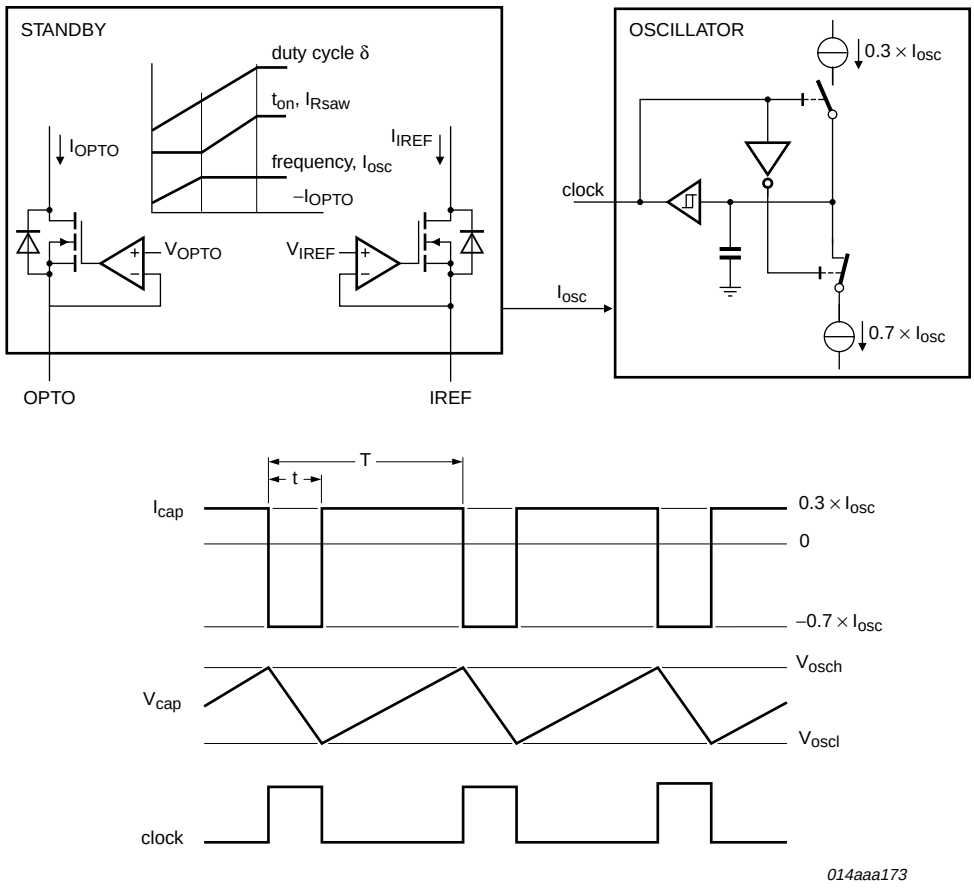


Fig 5. Oscillator

8.5 Feed-forward regulation

The output voltages of a GreenChip PC application are regulated at the secondary side by the TEA1781 (3.3 V and 5 V) and the TEA1782 (12 V and 5 V standby). The duty cycle of the secondary control switches (SB and SR, see Figure 11) are defined by Equation 3:

$$\delta\_S_{B/R} = \frac{V_O}{V_I / N} \quad (3)$$

Where:

- V_O is either 3.3 V, 5 V or 12 V
- V_I is the PSU input voltage

- N is the transformer turn ratio: primary to secondary winding

The primary side has to ensure that a positive secondary voltage is available just before the secondary side switches on the control switches SB and SR. To make sure there is a positive secondary voltage, also during transients, the duty cycle of the primary control switch, M1, has to be larger than the duty cycle of SB/SR.

$$\delta\_M1 > \frac{V_O}{V_I/N} \approx 1.2 \cdot \frac{V_O}{V_I/N} \quad (4)$$

As the transformer turn ratio and the output voltage of a PC power supply are constant values, it implies that the primary duty cycle has to be inverse proportional to the input voltage:

$$V_I \times \delta = constant \quad (5)$$

This relation is implemented in the TEA1771. The primary duty cycle is only defined by the input voltage, which is called feed-forward regulation. V_I is hereby measured via LVIN, which reflects the input voltage.

The sawtooth, the oscillator, and the digital control circuitry define the feed-forward regulation. The frequency is defined in the oscillator and the on-time in the sawtooth circuitry. The SAWTOOTH block, the DIGITAL CONTROL block, and their signals are shown in Figure 6. The outputs of the DIGITAL CONTROL block define the states of the output switches, the main switch (M1), and the reset switch (M2).

The oscillator generates a clock signal (see Section 8.4). When the clock becomes positive, the reset switch is turned off. A short time (Δt1) after this the main switch M1 is turned on. At the same time the charging of the capacitor C_{saw} is initiated.

As soon as the C_{saw} capacitor voltage exceeds an internal reference voltage, $V_{ref(saw)}$, the sawcomp signal becomes a logic '1', turning off the main switch via digital control. After a short delay (Δt2) the reset switch is turned on.

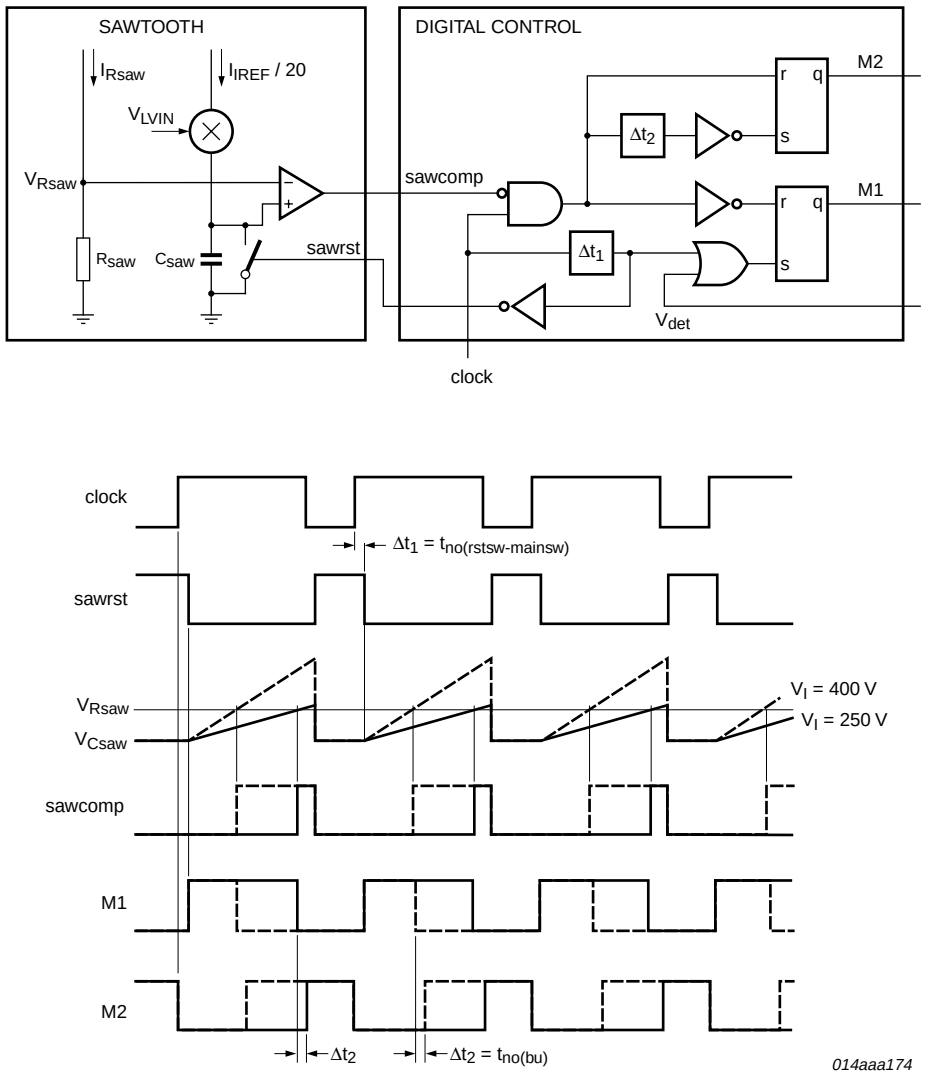


Fig 6. Feed-forward regulation

The current that charges the C_{saw} capacitor is proportional to the LVIN voltage, which reflects the input voltage. Figure 6 shows the signals for V_I = 250 V and for V_I = 400 V. A higher input voltage results in a higher charge current, which consequently results in a lower duty cycle. Thus, the duty cycle is made inverse proportional to the input voltage, which is the feed-forward regulation of the GreenChip PC converter.

So far the assumption has been that V_{Rsaw} is fixed. This does hold when the PSU is in Normal mode. In Standby mode this reference voltage may be lower causing a lower on-time, t_{on}. It is defined by I_{Rsaw} and the resistor R_{saw}. Figure 1 shows that I_{Rsaw} is generated by the STANDBY block. I_{Rsaw}, like I_{osc}, is regulated by I_{OPTO}. This on-time regulation is relevant when the PSU is in Standby mode. See Section 8.8. In Normal mode I_{OPTO} is set to a high level causing I_{Rsaw} to reach the maximum level, the assumed fixed level.

When the PSU is in Normal mode the duty cycle is independent of the operating frequency. The frequency is set to the maximum level and is proportional to I_{IREF}. See Section 8.4.

$$f_{osc(max)} = \frac{I_{IREF}}{2} \quad (6)$$

- $f_{osc(max)}$ (kHz)
- I_{IREF} (µA)

Figure 6 shows the sawtooth circuit. It also shows that the charge current of the C_{saw} capacitor is proportional to I_{IREF}. Thus both the oscillation period, t_{osc}, and the on-time, t_{on}, are inverse proportional to I_{IREF}. As a result the duty cycle, δ, is constant for varying operating frequencies.

8.6 Non-overlap times

In the previous section the non overlap times Δt1 and Δt2 are introduced. In Figure 7 these times are illustrated. The delays, Δt1 and Δt2 avoid overlap in the on-time of the main switch and the reset switch. The delay Δt1 is listed in the characteristics table: $\Delta t1 = t_{no(rstsw-mainsw)}$. The value slightly differs for Standby mode and Normal mode. In the characteristics table this is reflected by different delay values for a high and a low $-I_{OPTO}$ value that hold in Normal mode and Standby mode, respectively.

The delay Δt2 is less straightforward. It depends on the V_{DM1} signal. Figure 7 illustrates the mechanism showing stylized signals. When M1 is turned off the DM1 node is charged by the magnetizing current until it is clamped to the reset voltage. The primary controller waits for DM1 to be charged to the reset voltage before M2 is turned on. In fact, when this ramp has finished the controller waits an additional time, t_{wait} after which M2 is turned on. The DM1 voltage signal varies strongly as the PSU load is varied. By sensing the V_{DM1} ramp-up, hard switching of the reset switch is avoided in all load conditions.

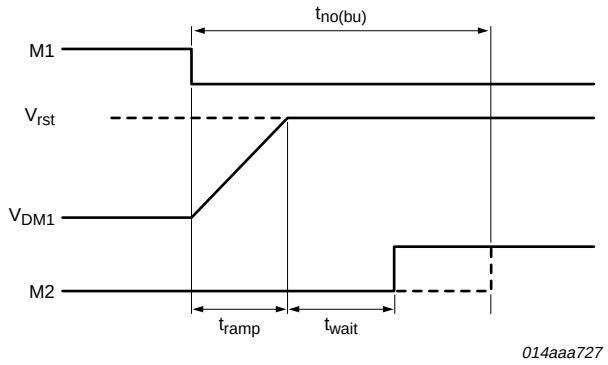


Fig 7. Δt2 non-overlap time between the main switch (mainsw) being turned off and the reset switch (rstw) being turned on.

If $(dV/dt)_r$ is below detection level the V_{DM1} ramp-up is not sensed at all. In that case a delay is applied which, like Δt1, is determined by the IC itself. This delay is called $t_{no(bu)}$, the backup delay. In Figure 7 this delay is illustrated by the dashed variant of M2. Counting time from the moment M1 is turned off M2 is turned after a delay of $t_{no(bu)}$ has passed.

8.7 Soft start

When entering Running mode, the IC starts switching at a minimum frequency set by an external resistor on pin OPTO, typically about 20 kHz. To avoid overshoot on the reset capacitor, C_{rst}, when the system starts switching, the primary control IC has an integrated soft start function. During this soft start period the on-time of the main switch slowly rises from zero to the required value; see Figure 3.

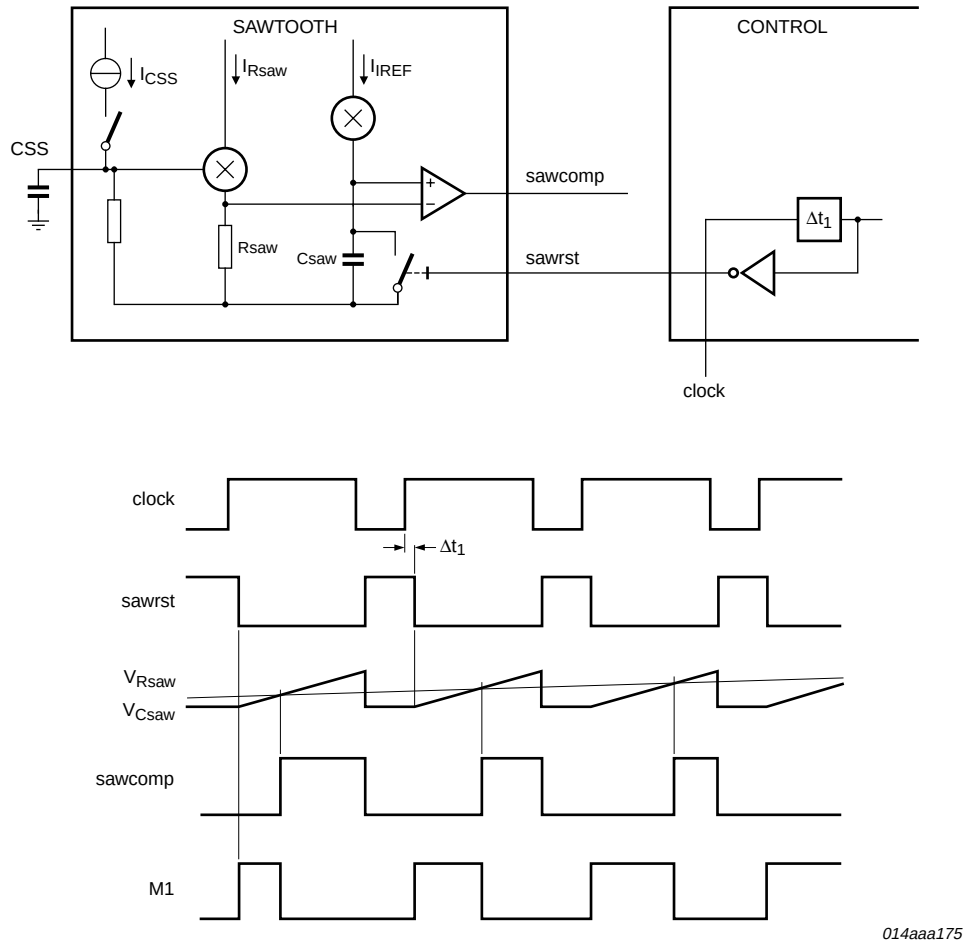


Fig 8. Implementation of the soft start period

During the soft start period, the external capacitor connected to pin CSS is charged via the current source I_{CSS}. See Figure 8. This current slowly charges the capacitor from 0 V to 4.1 V. The SAWTOOTH block in Figure 8 shows two multipliers. The left one points out that V_{CSS} modulates I_{Rsaw}. I_{Rsaw} in turn determines the reference voltage that is used to make the on-time. The slow ramp from 0 V to 4.1 V causes the duty cycle to grow slowly in time. This is called a soft start.

The duty cycle reaches the maximum level when the voltage on pin CSS pin is about 3.5 V. Eventually the voltage on pin CSS will be charged to the V_{CSS} parameter that is listed in Table 6, V_{CSS} = 4.1 V.

The time constant for the soft start period equals, see Equation 7:

$$\tau_{softstart} = \frac{C_{ss} \cdot 3.5}{I_{CSS(softstart)}} \quad (7)$$

Example:

With an external capacitor of 33 nF a time constant of about 2.8 ms is realized.

8.8 Standby regulation

In Section 8.4 and Section 8.5 it has already been explained that I_{OPTO} regulates both the oscillator frequency and the on-time. This section gives an overview of these regulations. Figure 9 shows both regulations.

The whole PSU can be either in Standby mode or in Normal mode. In Normal mode all outputs are active: 3.3 V, 5 V, 12 V, and 5 V standby. In Standby mode only the 5 V standby is active. In the PSU, I_{OPTO} is determined by the controller ICs on the secondary side of the transformer. Via an OPTO-coupler this current is transferred from the secondary side to the primary side. The secondary control regulates the primary duty cycle in Standby mode through I_{OPTO} in such a way that the primary duty cycle follows the duty cycle required on secondary side.

In Normal mode the I_{OPTO} current is set to a high level where both the frequency and the on-time are regulated to the maximum level.

When the PSU is in Normal mode I_{OPTO} is in range (1) (Figure 9). This range is characterized by the parameter $I_{OPTO(\delta max)}$. The primary controller is in range (1) (Figure 9) when $-I_{OPTO} > -I_{OPTO(\delta max)}$.

Remark: a current drawn from a pin is called a negative current by general convention.

In range (1) in Figure 9 the frequency is determined by the current I_{IREF} (see Section 8.4). The duty cycle, and therefore the on-time that goes with the duty cycle, is additionally determined by V_{LVIN} that reflects the input voltage (see Section 8.5).

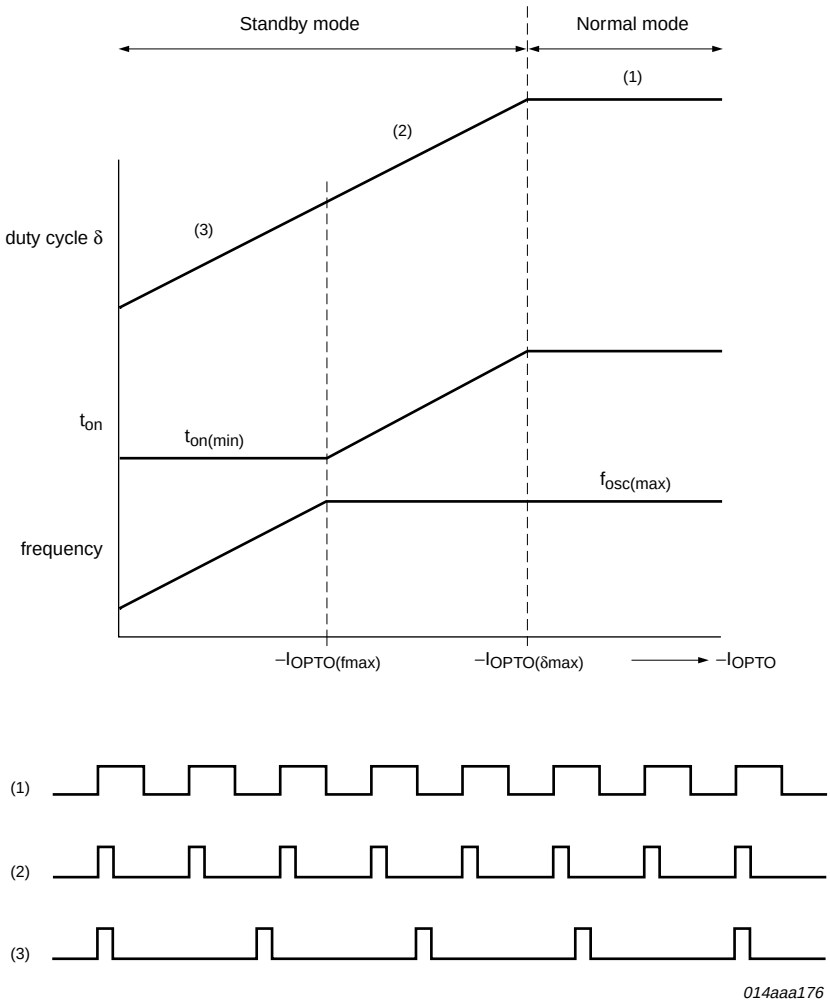


Fig 9. Duty cycle regulation via the I_{OPTO} output current

To optimize the efficiency, the duty cycle of the primary controller is reduced when the PSU enters Standby mode. In Standby mode the duty cycle is regulated via the current I_{OPTO}. The duty cycle can be reduced by lowering the current I_{OPTO}. Starting from the high duty cycle in Normal mode the on-time is reduced first. This is shown in range (2) (Figure 9). In this range the on-time can be reduced to a minimum level, $t_{on(min)}$. When the duty cycle is reduced further the frequency will be decreased, while the on-time stays at its minimum level. The transition between ranges (2) and (3) (Figure 9) is $2I_{IREF}$. When $-I_{OPTO} < -2I_{IREF}$ the primary controller operates in range (3) (Figure 9). Here the on-time is at the minimum level and the duty cycle is regulated via the frequency.

The duty cycle regulation has been made to obtain a good efficiency in Standby mode. By reducing the duty cycle magnetizing losses are reduced in the transformer. The minimum on-time is needed to obtain a minimum magnetizing current that makes sure the ZVS of both the main switch and the reset switch.

The opto coupler current is regulated by the secondary control. At start-up this current may be zero. To arrange a minimum I_{OPTO} level a resistor is placed at the OPTO pin, in parallel to the opto coupler (see R3 in Figure 11). In this way a minimum operating frequency is set. A 56 kΩ resistor on the OPTO pin sets the minimum frequency to approximately 20 kHz.

8.9 Reset circuitry

The TEA1771 has an integrated reset switch (see M2 in the DRIVERS block in Figure 1). The high side circuitry driving the high side reset switch is supplied from an external boost capacitor at pin CB. This capacitor is charged via an internal diode from DECPVCC when DM1 is low. This occurs when the primary main switch M1 is turned on.

8.10 Protections

To protect the controller ICs and the application against malfunction, the System failure mode is entered at a fault condition. In this mode, the switching of the main switch and reset switch is stopped.

The following protections are available in the TEA1771:

- Overcurrent protection
- Short-winding protection (swp1 and swp2)
- Overvoltage protection
- External protection via I_{OPTO}

When the primary controller enters System failure mode the charge current from DM2 to LVIN stays turned off. Because the switching is stopped, the auxiliary supply to LVIN is stopped as well. The LVIN capacitor is slowly discharged by the IC. Eventually V_{DECVCC} drops below $V_{UVLO(DECVCC)}$. At this point the IC enters Charge mode and the current source from DM2 to LVIN is turned on. This is called the system safe restart. The power up sequence is explained in Section 8.2.

How long the IC is in System failure mode depends on the external capacitance at DECVCC, DECPVCC and LVIN, and on the discharge current of the IC. As soon as $V_{UVLO(DECVCC)}$ is reached, the IC enters Charge mode and restarts.

To avoid false triggering of overcurrent protection or short-winding protection, a blanking period is activated when either M1 or M2 is turned on. During this blanking period the overcurrent protection and short-winding protection detection are disabled. In the characteristics table this period is called the leading edge blanking time t_{leb}.

8.10.1 Overcurrent protection

Figure 10 shows the current sense circuit that is involved with the OCP and SWP protections.

When switch M1 is on, (and the reset switch M2 is off), the voltage at the SENSE pin equals the voltage across R_{sense1}, This voltage is a used as a measure of the current through M1. See Figure 10. When the voltage on pin SENSE exceeds the OCP voltage level, V_{OCP} (typically 250 mV), M1 is turned off and then turned on again at the next cycle. The primary controller remains in Running mode. Here the overvoltage protection differs from other protections where the IC enters System failure mode.

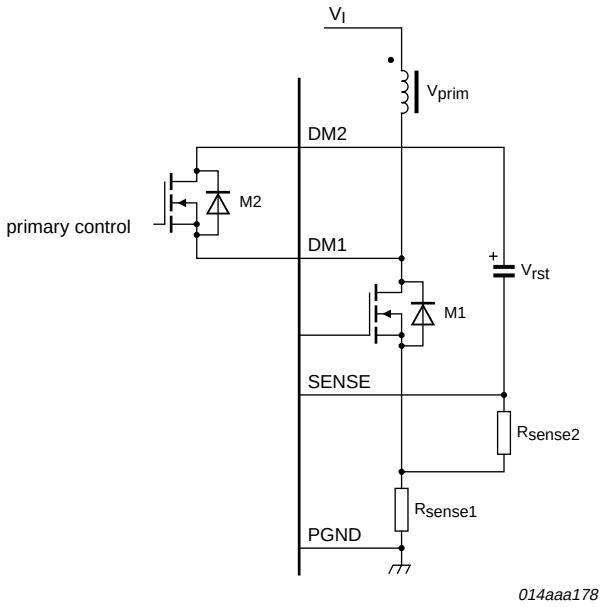


Fig 10. Current sense circuit

8.10.2 Short-winding protection

A shorted transformer winding can occur when either the primary main switch is on (positive secondary winding voltage) or when the system is in the reset phase (negative secondary winding voltage). In the first situation, a high positive current occurs through R_{sense1}. In the latter situation, a high negative current occurs through R_{sense2}. Therefore, the system has both a positive (V_{swp1}) and negative (V_{swp2}) SWP.

If the voltage on pin SENSE exceeds the voltage level V_{swp1} (300 mV) or V_{swp2} (–255 mV), the system enters System failure mode, disabling both switches. A safe restart will follow.

8.10.3 System failure mode externally activated

The primary side control IC can also be forced to enter System failure mode externally by pulling a current of $I_{prot(OPTO)}$ from the pin OPTO.

The secondary side activates this function if all secondary protections fail, e.g. when the bidirectional switch is shorted. The secondary side then increases the current drawn from the pin OPTO via the opto coupler.

Entering System failure mode is followed by a safe restart.

8.10.4 Reset capacitor voltage

The voltage across the reset capacitor (DM2) is sensed on pin VRST by using an external high ohmic resistive divider. System failure mode is activated when the voltage on pin VRST reaches the $V_{ovp(VRST)}$ level. A safe restart will follow.

As the voltage at DM2 equals the maximum drain voltage of the main switch M1 this switch is protected from breaking down.

8.11 Ground

The IC has a separate Power Ground (PGND) for sinking the driver currents. This prevents signal noise on the signal, Ground (GND).

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{LVIN}	voltage on pin LVIN	continuous [1]	–0.4	+48	V
V_{DM1}	voltage on pin DM1	continuous	–0.4	+570	V
		peak; Δt = 1 µs; non-repetitive	–0.4	+650	V
V_{DM2}	voltage on pin DM2	continuous	–0.4	+570	V
		peak; Δt = 1 ms; non-repetitive	–0.4	+650	V
Currents					
I_{IREF}	current on pin IREF		–300	-	µA
I_{OPTO}	current on pin OPTO	low power and normal mode	–13	0	mA
I_{DM1}	current on pin DM1		–300	+300	mA
I_{DM2}	current on pin DM2		–300	+300	mA
General					
P_{tot}	total power dissipation	T_{amb} < 45 °C	-	1.0	Ω
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–20	+85	°C
T_j	junction temperature		–20	+145	°C
V_{esd}	electrostatic discharge voltage	human body model [2]			
		pins DM2, DM1, and CB	–1500	+1500	V
		all other pins	–2000	+2000	V
		machine model [3]			
		all pins	–200	+200	V
		charged device model	-	500	V

[1] Pin LVIN cannot to be current driven.

[2] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[3] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω series resistor.

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	75	K/W

[1] Thermal resistance $R_{th(j-a)}$ can be lower when pin GND is connected to sufficient copper area on the printed-circuit board. See the TEA1771 application notes for details.

11. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up and supply management						
$V_{startup(LVIN)}$	start-up voltage on pin LVIN		14.4	15.2	16.0	V
$V_{UVLO(DECVCC)}$	undervoltage lockout voltage on pin DECVCC		8.25	9.0	9.75	V
V_{DECVCC}	voltage on pin DECVCC	running mode; V_{LVIN} = 25 V; I_{IREF} = –200 µA; I_{OPTO} = –2 mA	10.9	12.0	12.7	V
$V_{hys(DECVCC)}$	hysteresis voltage on pin DECVCC		1.7	3.1	4.5	V
$V_{DECPVCC}$	voltage on pin DECPVCC	running mode; V_{LVIN} = 25 V; I_{IREF} = –200 µA; I_{OPTO} = –2 mA; C_{DRIVER} = 100 pF	12.4	13.0	13.6	V
$I_{ch(DM2)}$	charge current on pin DM2	charge mode; V_{DM2} = 100 V; V_{LVIN} =				
		0.0 V	2.3	2.9	3.5	mA
		13.7 V	2.1	2.7	3.3	mA
$I_{ch(LVIN)}$	charge current on pin LVIN	charge mode; V_{DM2} = 100 V; I_{OPTO} = 0 mA; I_{IREF} = 0 mA; V_{LVIN} =				
		0.0 V	–3.2	–2.6	–2.0	mA
		13.7 V	–1.3	–0.7	–0.1	mA
I_{LVIN}	current on pin LVIN	running mode; I_{OPTO} = –2 mA; I_{IREF} = –200 µA; C_{DRIVER} = 100 pF	3.0	4.0	5.0	mA
5 V reference						
V_{5VREF}	voltage on pin 5VREF		4.75	5.00	5.25	V

Table 6. Characteristics *...continued*

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Soft start						
V_{CSS}	voltage on pin CSS	running mode; after soft start has completed	3.7	4.1	4.5	V
I_{CSS}	current on pin CSS	running mode; during soft start; V_{CSS} = 0 V	25	45	55	µA
$R_{int(CSS)}$	internal resistance on pin CSS	charge mode or system failure mode; V_{CSS} = 4 V	4.5	5.5	7.0	kΩ
Oscillator, opto control and secondary protection						
V_{IREF}	voltage on pin IREF	charge mode; I_{IREF} = –1 mA	0.40	0.55	0.70	V
		running mode; I_{IREF} = –1 mA	3.2	3.6	4.0	V
V_{OPTO}	voltage on pin OPTO	running mode; I_{OPTO} = –1 mA	3.2	3.6	4.0	V
		system failure mode; I_{OPTO} = –1 mA	-	0.0	-	V
$I_{OPTO(fmax)}$	current on pin OPTO (maximum frequency)	I_{IREF} = –100 mA; V_{LVIN} = 25 V	–250	–200	–170	µA
$I_{OPTO(\delta max)}$	current on pin OPTO (maximum duty cycle)	I_{IREF} = –100 mA; V_{LVIN} = 25 V	–1.8	–1.4	–1.0	mA
$I_{prot(OPTO)}$	protection current on pin OPTO	charge/running mode	–11	–9	–7	mA
δ_{max}	maximum duty cycle	$I_{OPTO} < I_{OPTO(\delta max)}$; I_{IREF} = –100 mA; V_{LVIN} =				
		12 V	54.0	59.0	64.0	%
		25 V	36.4	41.9	47.3	%
		40 V	23.2	26.6	30.0	%
$f_{osc(max)}$	maximum oscillator frequency	$I_{OPTO(fmax)} > I_{OPTO} > I_{prot(OPTO)}$; I_{IREF} =				
		–100 µA	40	50	60	kHz
		–200 µA	80	100[1]	120	kHz
$t_{on(min)}$	minimum on-time	$I_{OPTO} > I_{OPTO(fmax)}$; V_{LVIN} =				
		12 V	0.7	1.1	1.5	µs
		25 V	0.5	0.7	0.9	µs
		40 V	0.3	0.5	0.7	µs
Non-overlap times of main switch and reset switch						
$t_{no(rstsw-mainsw)}$	non-overlap time from reset switch to main switch	I_{OPTO} =				
		I_{OPTO} = –0.5 mA	0.91	1.15	1.39	µs
		I_{OPTO} = –1.5 mA	0.68	0.87	1.06	µs

Table 6. Characteristics *...continued*

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{no(bu)}$	backup non-overlap time	I_{OPTO} = –0.5 mA	3.14	4.16	5.18	µs
		I_{OPTO} = –1.5 mA	1.51	1.85	2.19	µs
Ramp detection						
t_{wait}	wait time	after ramp-up	1.48	1.80	2.12	µs
$(dV/dt)_r$	rise rate of change of voltage		-	50	-	V/µs
Driver						
R_{DSon}	drain-source on-state resistance	I = 50 mA	30	40	50	Ω
		I = 150 mA	2.5	5.0	8.0	Ω
Reset capacitor measurement: pin VRST						
$V_{start(VRST)(min)}$	minimum start voltage on pin VRST	charge mode	0.57	0.61	0.66	V
$V_{start(VRST)(max)}$	maximum start voltage on pin VRST	charge mode	2.52	2.62	2.71	V
$V_{ovp(VRST)}$	overvoltage protection voltage on pin VRST	running mode	3.49	3.62	3.74	V
$I_{sink(VRST)}$	sink current on pin VRST	voltage on pin > 0.5 V	-	-	520	nA
Overcurrent protection and short-winding protection: pin SENSE						
V_{ocp}	overcurrent protection voltage	running mode	-	250	-	mV
V_{swp1}	short-winding protection voltage 1	running mode	250	300	350	mV
V_{swp2}	short-winding protection voltage 2	running mode	–290	–250	–210	mV
t_{leb}	leading edge blanking time		-	400	-	ns
Floating supply on pins CB and DM1 ($V_{DD(float)} = V_{CB} - V_{DM1}$)						
$V_{DD(float)}$	float supply voltage		-	8.0	-	V
$V_{DD(float)UVLO}$	undervoltage lockout float supply voltage		4.25	4.75	5	V
Reset switch						
R_{DSon}	drain-source on-state resistance	running mode; $V_{CB} - V_{DM1}$ = 12 V				
		I_{DM2} = 0.1 A	20	25	30	Ω
		I_{DM2} = 0.3 A	11	15	22	Ω

[1] For the PSU, the recommended operating frequency is 75 kHz. The operating frequency can be raised to 100 kHz provided that the PSU input voltage, V_I, is above a minimum level which is typically 200 V. An application solution is available that automatically lowers the frequency when, during a mains dip, V_I drops below this minimum level. See application note.

12. Application information

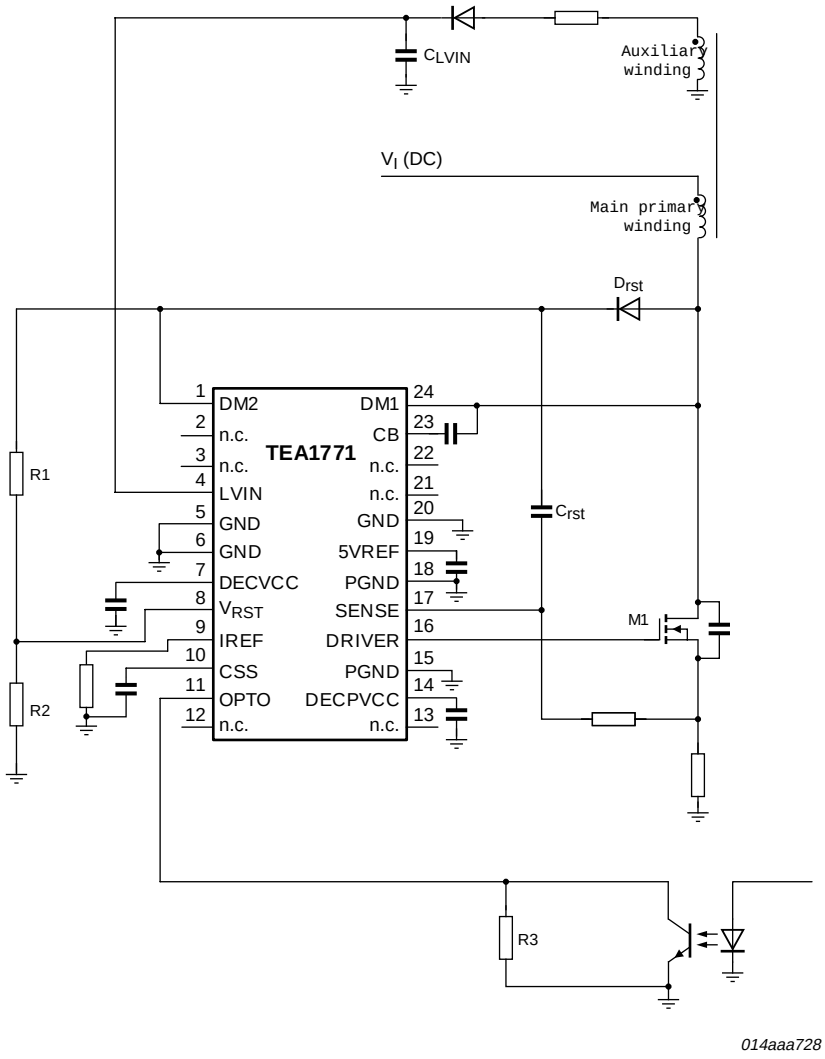
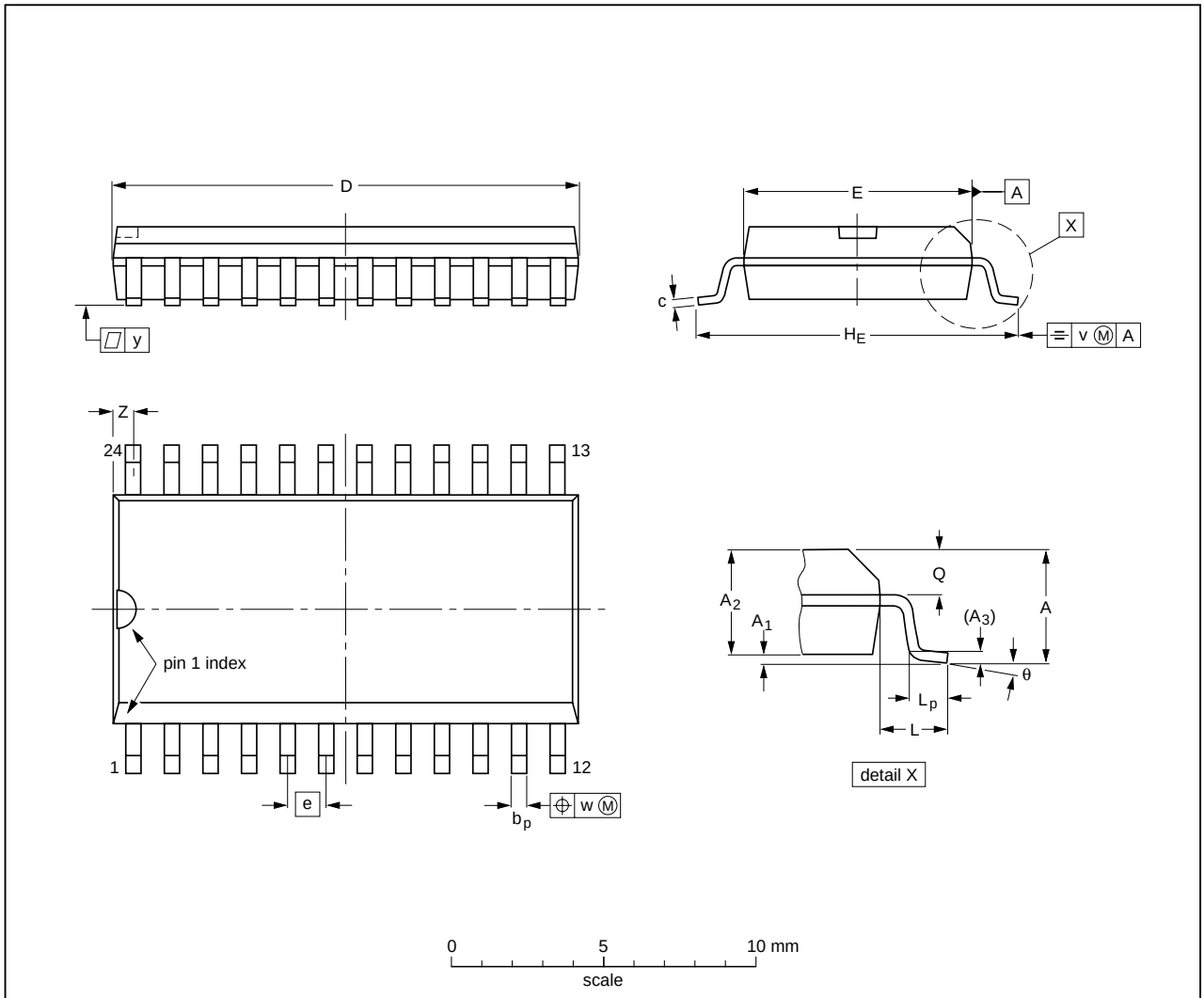


Fig 11. TEA1771 application diagram

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT137-1 (SO24)

14. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1771_1	20090206	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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