Expandable Four-Rail Tracking Manager

Preliminary Information[1] *(See Last Page)*

FEATURES & APPLICATIONS

- **Programmable Tracking Function**
- **Programmable Voltage Monitoring of 4 or more Independent Supplies**
- **Programmable Under-Voltage Thresholds**
- **Provides Soft Start, Reset, IRQ and Force Shutdown functions**
- **Minimizes Supply Differential During Power-on and Power-off**
- **Operates From Any One of Four Supply Voltages**
- **Easily Expandable to Control up to 32 Supplies**
- **Packaged in a 28 Lead SSOP**

Applications

- **Multi-voltage supply rail manager for**
  - **Telecom Infrastructure**
  - **Compact PCI**
  - **Servers**
- **Multi-voltage Network Processors, DSPs, ASICs**

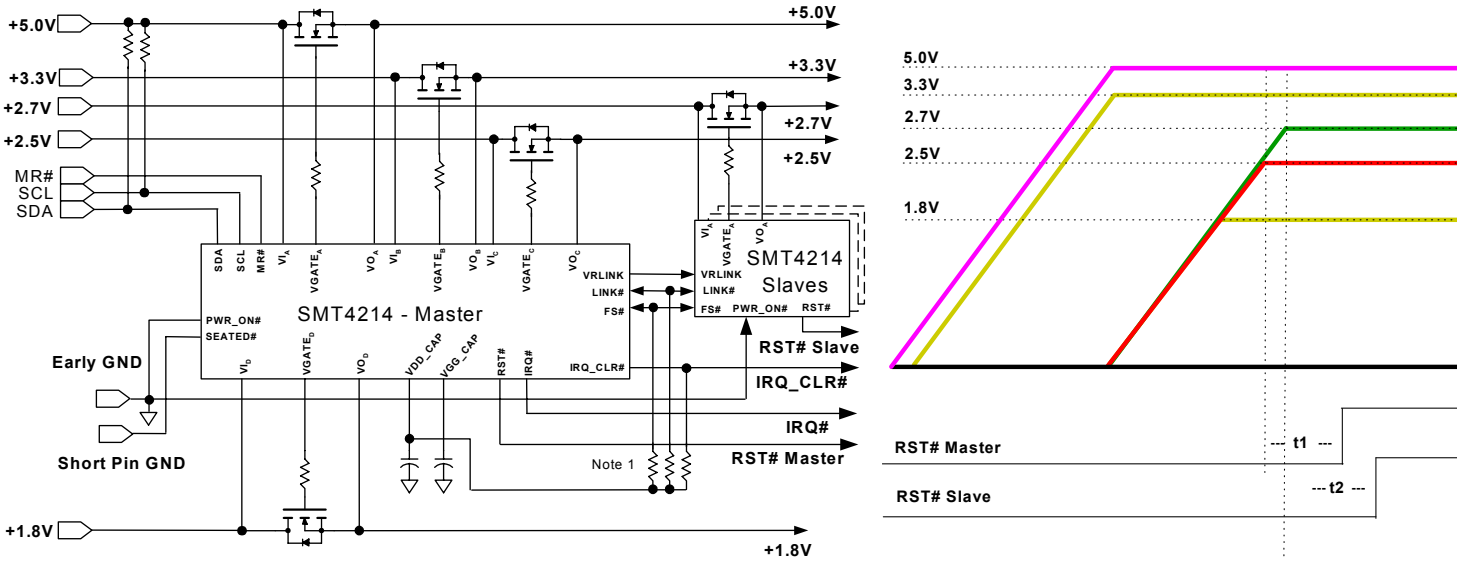
INTRODUCTION

The SMT4214 is a fully integrated programmable voltage manager IC, providing supervisory functions and tracking control for up to four independent power supplies. The four internal managers perform the following functions: Monitor source (bus-side) voltages for under-voltage conditions, monitor back end (card-side) voltages for under-voltage conditions, insure voltage of the card-side tracks within the specified parametric limits, and provides supply status information to a host processor.

The SMT4214 incorporates nonvolatile programmable circuits for setting all of the monitored thresholds for each manager. Individual functions are also programmable allowing interrupts or reset conditions to be generated by user-defined combinations of events.

Programming of configuration and control values by the user can be simplified with the interface adapter (SMX3200) and Windows GUI software obtainable from Summit Microelectronics.

SIMPLIFIED APPLICATIONS DRAWING



Power supply and system start-up initialization using multiple SMT4214s. Two power supply channels are set to 'softstart' and three are set to track.

The above drawing illustrates the use of the SMT4214 in a multi-device application. It should be noted this is just an example and the specific component values are purposely not shown. Note 1 - Several pins have internal resistors so external resistors are optional (see the Internal Functional Block Diagram). If external resistors are used they should be tied to VDD_CAP on the Master.

GENERAL DESCRIPTION

The SMT4214 is a fully integrated power supply manager designed for use on a distributed power or multi-supply rail circuit card. The supplies can be resident on the circuit card in the form of LDO's or DC-to-DC converters or the supplied voltages can be present on the backplane of the system. In either configuration, the SMT4214 will monitor both the raw voltages at their source and also on the circuit side of the power MOSFETs it is controlling.

A key function of the SMT4214 is the MOSFET control. The device can be programmed to turn on the MOSFET's with a controlled MOSFET gate slew rate in a soft start mode. Alternatively it can be programmed so that the MOSFETs are turned on so that the voltages being applied to the circuitry are 'tracked.'

Each supply on the card is assigned its own manager on the SMT4214. If there are more than four supplies, the SMT4214 can be linked with other SMT4214's through the use of the PWR_ON#, LINK#, VRLINK and FS# pins.

The individual managers are programmed to monitor their respective voltage supplies. The under-voltage threshold is programmable in 20mV increments to monitor voltages within the range of 0.9V to 6.0V. Under-voltage conditions can be programmed to assert IRQ#, RST# or FS#.

DETAILED DEVICE OPERATION

SUPPLY MANAGERS

The electrical placement of the SMT4214, and the associated MOSFET's, on a printed circuit card effectively divides the board into two electrical domains; the bus-side and the card-side. The bus-side constitutes the power supply sources either from the backplane or on-board LDOs or DC-to-DC converters. The card-side is comprised of the components that are powered by the voltage sources on the output side of the MOSFET's.

The SMT4214 has four identical supply managers each comprised of a programmable bus-side voltage threshold comparator and a secondary comparator for monitoring card-side voltages and programmable logic to determine device reactions to changes in the detected thresholds.

Figure 1 illustrates the functional segments of the individual managers. The curved resistive element is a symbolic representation of a non-volatile DAC. When using the SMX3200 (dongle) and GUI software the selected threshold level is programmed into the SMT4214, effectively adjusting the output of the DAC to the requested threshold detection level. Two different voltage potentials for each supply are measured, the pre-MOSFET threshold VI (bus-side voltage) and the post-MOSFET threshold VO (card-side voltage). The VI threshold is set by a non-volatile DAC. The VO threshold is set to 200mV below the VI threshold or VI-200mV.

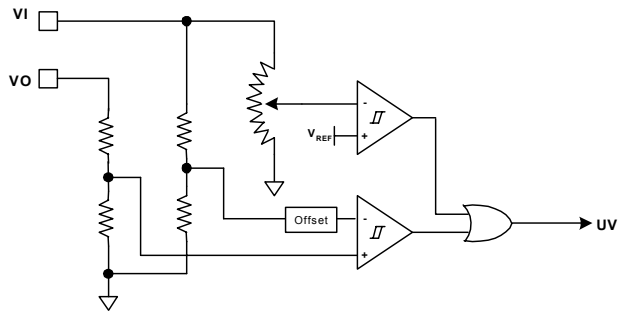


Figure 1. Supply Manager

An under-voltage condition is defined as either VI or VO dropping below its programmed threshold. A programmable under-voltage filter requires that, after the soft start and tracking are complete, an under-voltage condition must remain for a filter interval, t_{FILTER}, before any action is taken.

SOFT START

If a channel is set to soft start, its VGATE output will ramp at a constant slew rate of 500V/s until it reaches its maximum value. This type of operation would commonly be used where a bus voltage (e.g., 5V) is first switched to a DC-to-DC converter or group of LDOs; and then their outputs would be switched in a tracking mode to the card-side logic.

All unused channels must be programmed to soft-start mode. The thresholds for unused channels should be set to minimum, and the VO and VI inputs should be tied to VDD_CAP.

TRACKING

The tracking operation normally requires that at least two channels are programmed to track. However, a single channel can be set to track and is compared against an internally set tracking model. During tracking, the card-side voltages are monitored to minimize the differential voltage between any of these voltages until they reach their respective thresholds.

In the tracking mode, the ramp rates are inherently adaptive with a maximum of 500V/s. That is, if there is any difference between the VO inputs in the linear region, the VGATE outputs are adjusted to minimize the differential.

POWER-ON

The power-on operation is initiated by taking the PWR_ON# pin low. This pin can either be hardwired low for an automatic power-on or it can be pulled low after the device receives power. This pin can also be pulled low using an I^2C power-on command.

Two conditions must be met before the part begins the power-on operation. FS# must be high; if FS# is low, the SMT4214 will not power on. The SEATED# pin must also be low for the seated delay interval, t_{SEATED}, before the device will power on.

Once the power-on operation is initiated the SMT4214 will wait until all of the VI's for the designated soft start channels have reached their programmed thresholds and VGG_CAP is at the programmed output voltage (P_{VGG} = 10.5V or 14V). At this point the VGATE outputs of the soft start channels will ramp up and turn on their corresponding card-side voltages. When the VGATE outputs of the soft start channels have ramped above their programmed output voltage levels (P_{VVG} = 10.5V or 14V) and the respective card-side voltages are above their programmed and fixed offset thresholds, soft start is complete.

Once the soft start is complete the SMT4214 will wait until all of the VI's of the tracking channels are above their programmed thresholds and then begin tracking. The tracking operation ends when the VGATE outputs of the tracking channels ramp up to their maximum voltage. If the tracking time limit is enabled and if power-on is not completed (all VGATE outputs above their minimum programmed output voltage) within a power-on limit interval (t_{PWRON}), the soft start and tracking operations will cease and FS# will be asserted, shutting down all VGATE outputs. After this shutdown, the device will not perform a power-on operation until the PWR_ON# pin is toggled.

POWER-OFF

Once the SMT4214 has completed the power-on operation, the power-off operation can be initiated by bringing the PWR_ON# pin high. This pin can be toggled high either externally or internally with an IIC power-off command.

Once the power-off operation is initiated there is a delay of t_{TRKDN} = VDD/(500V/s). At this point the SMT4214 will begin the discharging of the VGATE output of the highest tracked channel. Once the VO inputs of all tracked channels are within 100mV of ground, all VGATE outputs will be clamped to ground.

RESET OPERATION (See Figure 2)

During power-on the RST# output will be low until all selected managers detect their respective VO's are at or above the programmed threshold and the tracking function is complete. RST# will remain active for the reset timeout period (t_{PRTO}) after the last VO reaches its programmed threshold and the tracking function is complete. RST# will also be held low from the beginning of a power-off operation until the end of a power-on operation.

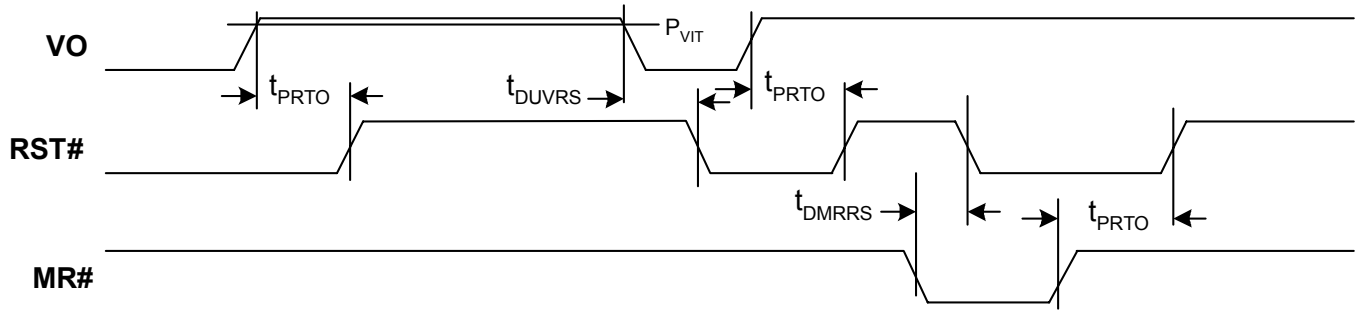


Figure 2. Timing relation between VO, RST# and MR#

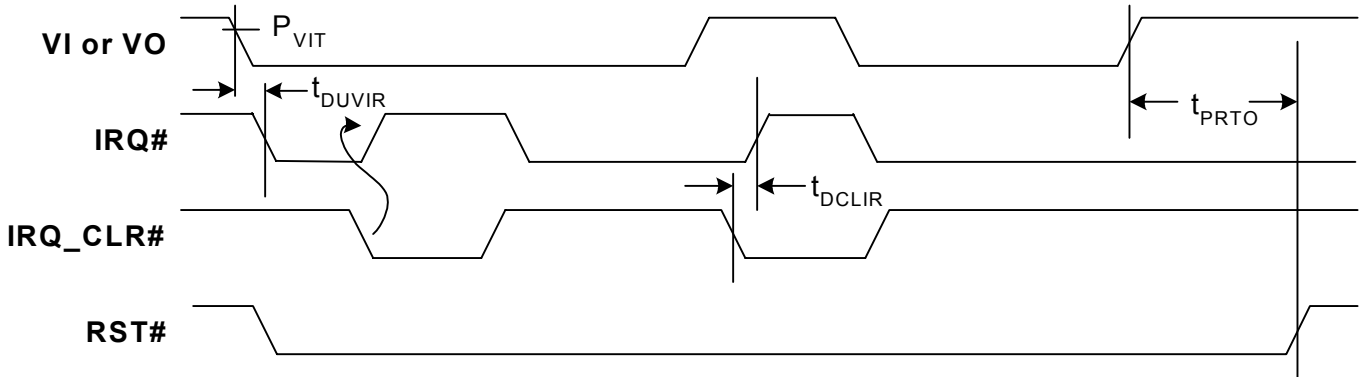


Figure 3. Timing relation between VI/VO, IRQ#, IRQ_CLR# and RST#

If enabled in the configuration register, RST# will be driven low by any under-voltage condition. RST# will remain asserted for a reset timeout period, t_{PRTO}, after the under-voltage condition has cleared.

RST# can be forced low by driving the manual reset input (MR#) low. RST# will remain low so long as the MR# input is active and stay low for t_{PRTO} after MR# returns high. The manual reset input is used to drive the RST# output low and to enable write operations to the configuration registers. It has no affect on any other outputs or device operations.

IRQ OPERATION (See Figure 3)

The IRQ# output is disabled throughout the power-on and power-off operations; from when power is first applied until the VI inputs and VO inputs are above their programmed thresholds and from the beginning of a power-off until the end of a power-on operation. If enabled in the configuration register, IRQ# will be driven low by any under-voltage condition. Once asserted, the IRQ output is latched until cleared by removing the under-voltage condition and asserting IRQ_CLR#. Refer to Figure 3 for an illustration of the relationship of these conditions and signals.

FORCE SHUTDOWN (See Figure 4)

The force shutdown function can be initiated either externally or internally. The FS# pin is always configured as an I/O and will always be enabled. If the FS# pin is taken low the VGATE outputs will immediately be clamped to ground.

The force shutdown function can be configured as an internally initiated function when an under-voltage condition is detected. The force shutdown can be initiated internally when an under-voltage condition is sampled at the end of tracking or on an under-voltage condition after tracking is complete. In either case, the FS# pin will be driven low and latched until either the power is cycled or the PWR_ON# pin is toggled. Refer to Figure 4,for an illustration of the basic relation between VI, VO, FS# and VGATE.

MULTI-DEVICE OPERATION

Multiple SMT4214's can be used on the same board if more than four supplies need to be monitored and controlled. One SMT4214 must be configured as the master and the others must be configured as slaves. The device configured as the master must have a supply voltage that is greater than or equal to the supply voltages of its slave devices. The SMT4214 provides four signals for easy interfacing; PWR_ON#, FS#, VRLINK and LINK#.

PWR_ON# is an I/O. This pin should be connected together on each of the SMT4214s to coordinate the power-on and power-off operation. PWR_ON# can be toggled by an external host or by the master SMT4214 in response to a command received on the I^2C bus.

FS# is an I/O, therefore, all FS# pins in a multi-device application must be tied together. One or more of the SMT4214's could be configured to generate a force shutdown if an under-voltage condition is detected.

When a device is configured as a master its VRLINK pin will be configured as an output; all other devices in the system are slaves with VRLINK pins configured as inputs. As an output, the VRLINK provides an analog signal that is the ramp reference used to track the card-side voltages. The slave devices will use this input as their own ramp reference. In this manner, tracking is coordinated between all of the devices.

The LINK# pin is an I/O that is used only during a power-on or power-off operation and all the devices will have their LINK# pins connected together. It is through this pin that the tracking function is coordinated. As an example: device 1 is the master and is supplying the ramp reference to devices 2 and 3. If Channel A of device 3 falls behind the ramp reference, device 3 will assert its LINK# output thus halting the ramp on the card-side voltages of devices 1, 2 and 3 until channel A of device 3 can catch-up. The master and slave devices must have at least one of their four channels configured to track.

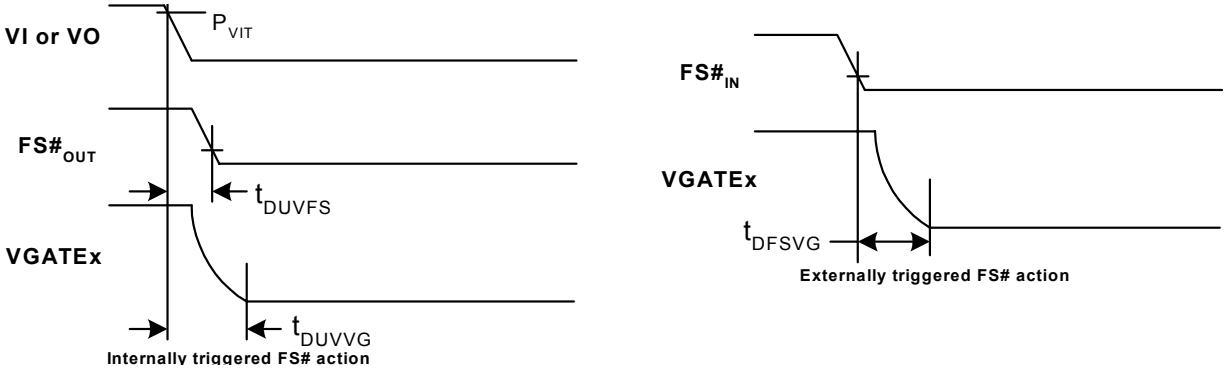


Figure 4. Timing relation between VI/VO, FS# out and VGATE and the relation between FS# in and VGATE

FAULT STATUS REGISTERS

The SMT4214 has one volatile fault status register. When an IRQ# is generated the cause of the interrupt is recorded in the fault register. The fault source is indicated as a '1' in the assigned bit location (Figure 5). The fault status register is overwritten each time an IRQ# is generated. The fault status register is always available for reading except for when a volatile write is in progress. The conditions for overwriting (clearing) the fault condition is dependent upon the device configuration with regard to the programmable 'active writing state' of the MR# input. Clearing the fault status registers is not necessary as the last fault condition overwrites any information previously stored. If clearing the registers is desired, it is accomplished by forcing a write to those registers while no fault conditions exist.

Fault recording is disabled when the PWR_ON# input is high.

Fault Status Register Address 06							
7	6	5	4	3	2	1	0
PWR_ON# State	RST# Pin State	IRQ# Pin State	VGATE Pin State	VO_D State	VO_C State	VO_B State	VO_A State

Figure 5. Fault Status register bit allocation

SERIAL INTERFACE

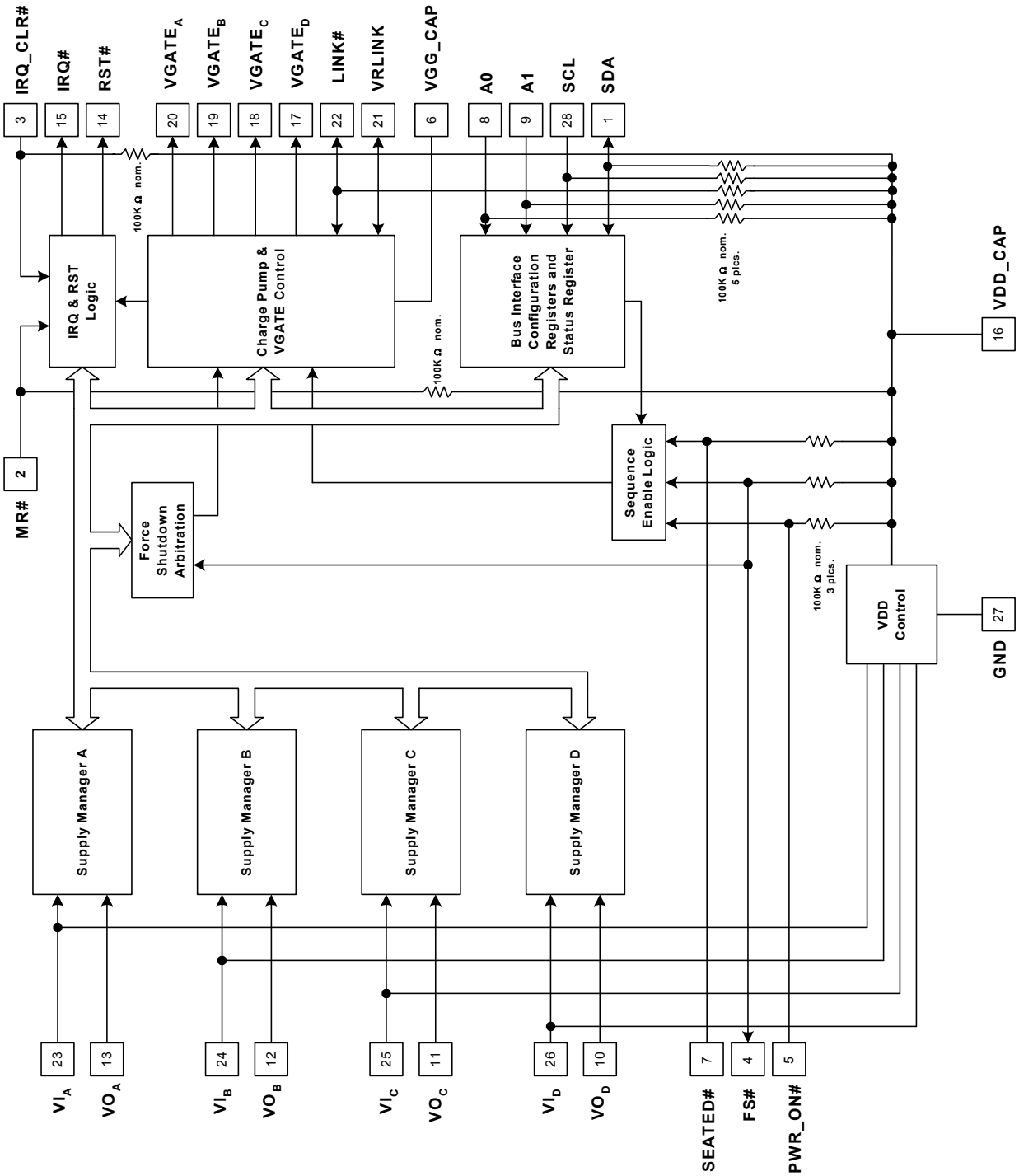
The SMT4214 uses the industry standard I^2C, 2-wire serial data interface. This interface provides access to the configuration registers, the volatile fault registers and I^2C Power-On/Off command. The interface has three address inputs (A0, A1, A2) allowing up to eight devices on the same bus. This allows multiple devices on the same board or multiple boards in a system to be controlled with two signals; SDA and SCL.

The configuration and volatile fault registers share the same fixed device type identifier, $1001_{[bin]}$.

The configuration and fault registers may be read regardless of the state of MR#. MR# input has to be low and the PWR_ON# pin high in order to write to the configuration registers.

Device configuration utilizing the Windows based SMT4214 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (www.summitmicro.com). Using the GUI in conjunction with this datasheet and Application Note 28, simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMT4214. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I^2C bus protocol.

INTERNAL FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

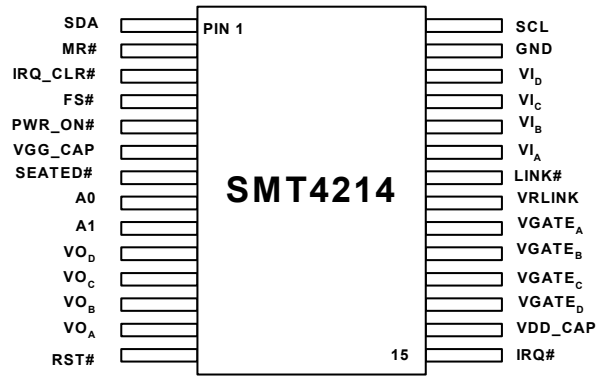
Pin Number	Pin Type	Pin Name	Pin Description
1	I/O	SDA	SDA is the bi-directional serial data pin. It is configured as an open drain output. SDA is internally connected to VDD_CAP through a 100kΩ pull-up resistor. In multiple device systems, an external pull-up should be connected to the highest supply
2	I	MR#	The Manual Reset input is an active low input, internally connected to VDD_CAP through a 100kΩ pull-up resistor. Taking MR# low will force the RST# output low. MR# must be forced low when writing to the configuration registers.
3	I	IRQ_CLR#	Interrupt Clear is an active low input. Forcing IRQ_CLR# low will clear the IRQ# output provided that it is not being driven by an under-voltage condition. IRQ_CLR# is internally connected to VDD_CAP through a 100kΩ pull-up resistor.
4	I/O	FS#	Force Shutdown is an active low open-drain I/O internally connected to VDD_CAP through a 100kΩ pull-up resistor. FS# can be asserted either by an outside signal or by a programmable under-voltage condition. If FS# is brought low, the SMT4214 will immediately take the VGATE outputs to 0V. If multiple SMT4214's are used on a single board, the FS# outputs can be tied together. In this configuration it is possible for a fault condition on one SMT4214 to shutdown all of the SMT4214's on a system.
5	I/O	PWR_ON#	The Power-On input must be low for the SMT4214 to begin turning on the VGATE outputs. PWR_ON# is internally connected to VDD_CAP through a 100kΩ pull-up resistor, therefore its normal state is not active. PWR_ON# must be held in its inactive state while writing to the configuration registers. Once the power-on operation has completed, de-asserting the PWR_ON# input will force the 'tracked' channels to power down and then clamp all VGATE outputs to ground.
6	PWR	VGG_CAP	VGG_CAP is a charge storage connection for the charge pump. This capacitor provides current to the VGATE outputs under varying load conditions. VGG_CAP should nominally be 1μF.
7	I	SEATED#	The SEATED# is an active low input, internally connected to VDD_CAP through a 100kΩ pull-up resistor. The SEATED# input is effectively an enable input that must be low for t_{SEATED} before the power-on operation can proceed. It is generally tied to the 'short pin' in a staggered pin connector. When the card is removed, SEATED# will go high and will initiate a power-off operation.
8	I	A0	The address pins are biased either to VDD_CAP or GND and provide a mechanism for assigning a unique bus address to the SMT4214. AO and A1 are internally connected to VDD_CAP through a 100kΩ pull-up resistor
9	I	A1	
10	I	VOD	The Voltage Output monitor inputs are used to monitor the 'card-side' voltages for the individual managers. See Figure 8 for additional external component recommendations.
11	I	VOC	
12	I	VOB	
13	I	VOA	
14	O	RST#	Reset is an active low open-drain output. It will be driven low whenever the MR# input is low. RST# can be programmed so that it is asserted on an under-voltage condition.

PIN DESCRIPTIONS CONT'D

Pin Number	Pin Type	Pin Name	Pin Description
15	O	IRQ#	Interrupt is an active low open-drain output. It can be programmed so that it is driven low on an under-voltage condition. It is cleared by removing any under-voltage conditions and asserting IRQ_CLR#.
16	PWR	VDD_CAP	VDD_CAP is a charge storage connection to the SMT4214's internal power supply. For most applications this is tied to a 10µF capacitor. A smaller 0.1µF can be added in parallel for additional noise decoupling
17	O	VGATED	The VGATE outputs are used to control the "turn-on" of the card-side voltages by providing a high side voltage to a power MOSFET. The VGATE output voltages are programmable as either 10.5V or 14.5V depending on the type of MOSFET gate drive needed to fully enhance the device. See Figure 8 for additional external component recommendations.
18	O	VGATEC	
19	O	VGATEB	
20	O	VGATEA	
21	I/O	VRLINK	Voltage Ramp Link is an I/O and is used in a multi-SMT4214 application. If the SMT4214 is designated as the master its VRLINK will become an output providing the ramp reference of the card-side voltages for the slave SMT4214's. If the SMT4214 is designated as a slave its VRLINK will become the input for the VRLINK of the master.
22	I/O	LINK#	Link is an active low open-drain I/O internally connected to VDD_CAP through a 100kΩ pull-up resistor. In a multi-SMT4214 application the LINK# pin of all the devices can be tied together to synchronize tracking. The LINK# I/O is active only during a power-on or power-off operation. If one of the devices is falling behind in tracking of the card-side voltages, it will assert its LINK# output and temporarily halt the ramping of the VGATE voltages of the other devices.
23	I	VI_A	The Voltage Inputs provide two functions. Internally they are diode-OR'ed; therefore, the input with the highest voltage will act as the device's VDD supply. They are also the bus-side (unswitched) voltage monitoring inputs to the individual supply managers. See Figure 8 for additional external component recommendations.
24	I	VI_B	
25	I	VI_C	
26	I	VI_D	
27	PWR	GND	GND is the ground for both the analog and digital portions of the internal circuitry.
28	I	SCL	SCL is the serial clock input, used for clocking data into or out of the SMT4214. SCL is internally connected to VDD through a 100kΩ pull-up resistor. In multiple device systems, an external pull-up should be connected to the highest supply.

PACKAGE PIN CONFIGURATION

28 Lead SSOP



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature..... -65°C to +150°C
Terminal Voltage with Respect to GND:
VI & VO Inputs ……..…..-0.3V to 7.0V
VGATE Outputs……..……...16V
All Others .....……..-0.3V to 7.0V
Output Short Circuit Current .....……100mA
Lead Solder Temperature (10 secs)....……300°C
Junction Temperature.....…….....…...150°C
ESD Rating per JEDEC……..2000V
Latch-Up testing per JEDEC…….....+/- 100mA

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Industrial).....–40°C to +85°C
(Commercial).....0°C to +70°C

Supply Voltage…….……2.7V to 6.0V 1/

Package Thermal Resistance (θ JA)
28 Lead SSOP……80°C/W
Moisture Classification Level 1 (MSL 1) per J-STD- 020

Notes: 1/ For reliable operation the VDD_CAP node voltage must be equal to or greater than 2.7V (voltage level measured on pin 16).

RELIABILITY CHARACTERISTICS

Data Retention……..…..100 Years
Endurance……..……100,000 Cycles

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
VI	Supply Voltage VI_A, VI_B, VI_C or VI_D	Device supply voltage defined by the highest of the four VI inputs. Note 1/	2.7		6.0	V
I_{DD} (ON)	Power Supply Current	Active Current VGATE Outputs enabled			2	mA
P_{VIT}	Programmable VI Threshold	8-bit resolution 20mV/bit	0.9		6.0	V
P_{VOT}	VO Threshold	VI_X-VO_X	180	200	220	mV
P_{VVG}	Programmable VGATE Output	Option 1 (MOSFETs on)	13	14		V
		Option 2 (MOSFETs on)	10	10.5		V
V_{VG} OFF	VGATE Output	VGATE sinking 2mA	0		0.4	V
I_{VG}	VGATE Drive Current	MOSFET switches enabled		20	80	µA
SR_{VG}	VGATE Slew Rate			500		V/s
V_{TRKR}	Tracking Differential Voltage	Allowable differential between VO pins programmed for tracking		100	250	mV
V_{IH}	Input High Voltage	VI = 2.7V	0.9xVI		VI	V
		VI = 5.0V	0.7xVI		VI	V
V_{IL}	Input Low Voltage	VI = 2.7V	-0.1		0.1xVI	V
		VI = 5.0V	-0.1		0.3xVI	V
V_{OL}	Output Low Voltage	Open Drain Outputs, I_{SINK} = 2mA	0		0.4	V
$R_{Pull-Up}$	Input Pullup Resistors	See Pin Descriptions	50	100	165	kΩ

Notes: 1/ - At least one of the VI inputs needs to be at or above 2.7V for proper device operation.

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.) See Figure 2, 3, 4 and 5 Timing diagrams.

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{PRTO}	Programmable Reset Time-Out Period	t_{PRTO} = 25ms	-25	t_{PRTO}	+25	%
		t_{PRTO} = 50ms				
		t_{PRTO} = 100ms				
		t_{PRTO} = 200ms				
t_{UVFILT}	Programmable UV Filter Time Interval	t_{UVFILT} = OFF	-25	t_{UVFILT}	+25	%
		t_{UVFILT} = 0.2ms				
		t_{UVFILT} = 1.6ms				
		t_{UVFILT} = 12.8ms				
t_{SEATED}	Seated Delay Interval	t_{SEATED} = 25ms	-25	t_{SEATED}	+25	%
t_{PWRON}	Power-On Limit Interval	t_{PWRON} = 200ms	-25	t_{PWRON}	+25	%
t_{DFIRQ}	Delay from fault detection to IRQ#			1		µs
t_{DFRST}	Delay from fault detection to RST#			1		µs
t_{DMRRST}	Delay from assertion of MR# to RST# Active			100		ns
t_{DVIVG}	Delay from VIX valid to VGATEX activated	VGG_CAP fully charged		10		µs
t_{DUVFS}	Delay UV to FS#			1		µs
t_{DUVVG}	Delay UV to VGATE low			1		µs
t_{DFSVG}	Delay from assertion of FS# to VGATE clamped to ground.	VGATE Capacitance = 10nF			100	µs
t_{TRKDN}	Delay from PWR_ON# deasserted to VGATEX deactivated.			VDD/(500V/s)		s

TIMING DIAGRAMS

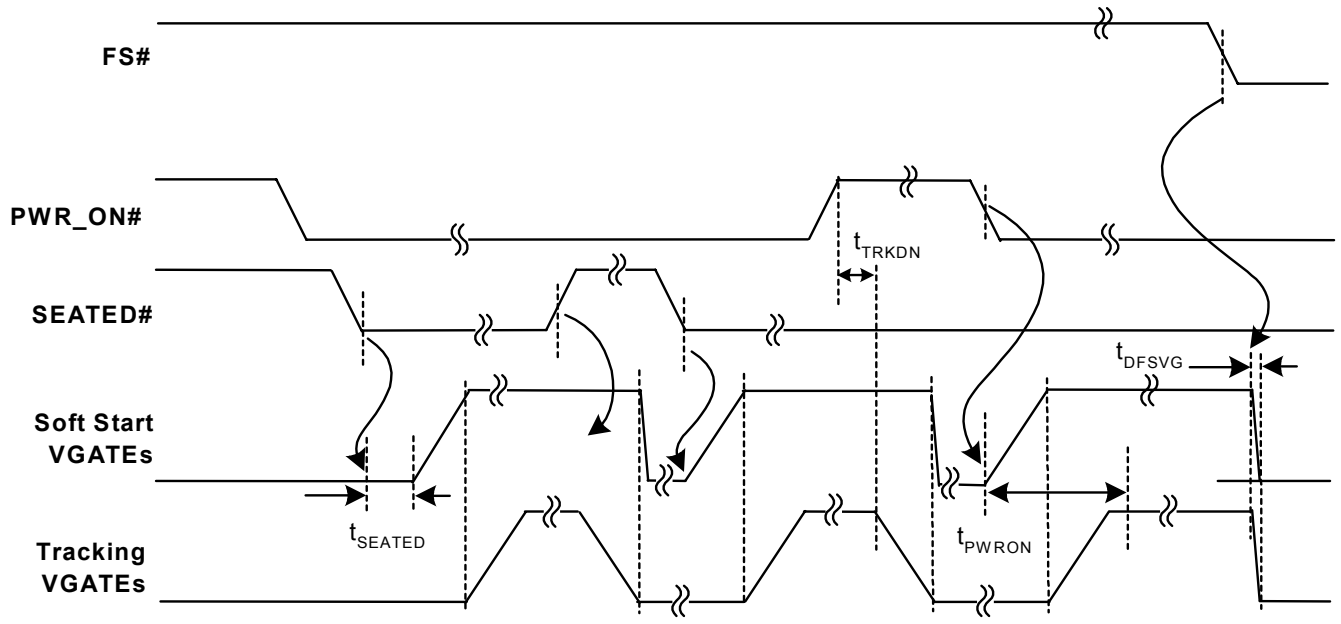


Figure 5 - Timing relationship of de-asserting the enabling inputs on the VGATE outputs.

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS - 100kHz

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.) See Figure 6 Timing diagram.

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency		0		100	KHz
t_{LOW}	Clock Low Period		4.7			µs
t_{HIGH}	Clock High Period		4.0			µs
t_{BUF}	Bus Free Time	Before New Transmission Note 1/	4.7			µs
$t_{SU:STA}$	Start Condition Setup Time		4.7			µs
$t_{HD:STA}$	Start Condition Hold Time		4.0			µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7			µs
t_{AA}	Clock Edge to Data Valid	SCL low to valid SDA (cycle n)	0.2		3.5	µs
t_{DH}	Data Output Hold Time	SCL low (cycle n+1) to SDA change	0.2			µs
t_R	SCL and SDA Rise Time	Note 1/			1000	ns
t_F	SCL and SDA Fall Time	Note 1/			300	ns
$t_{SU:DAT}$	Data In Setup Time		250			ns
$t_{HD:DAT}$	Data In Hold Time		0			ns
TI	Noise Filter SCL and SDA	Noise suppression		100		ns
t_{WR}	Write Cycle Time	VGG_CAP Capacitor =1uF, VGG_CAP=10.5V			100	ms

Note: 1/ - Guaranteed by Design.

TIMING DIAGRAMS

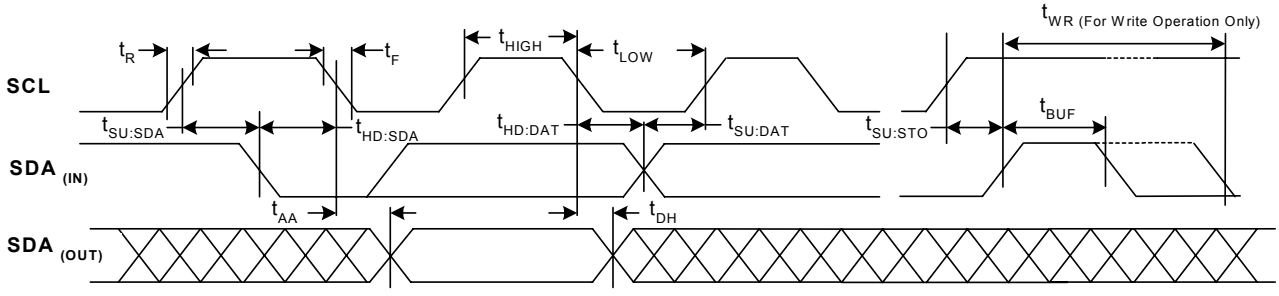


Figure 6 . Basic I²C Serial Interface Timing

PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers and memory array is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is the clock input. Data is clocked in on the rising edge of SCL and clocked out by the falling edge of SCL. All data transfers begin with the MSB. During data transfers SDA must remain stable while SCL is high. Data are transferred in 8-bit packets with an intervening clock period in which an acknowledge is provided by the device receiving data.

The SCL high period (t_{HIGH}) is used for generating start and stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA during t_{HIGH} is a start condition and a low-to-high transition of SDA during t_{HIGH} is a stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through the use of unique device addressing. The address byte is comprised of a 4-bit device type identifier, a 3-bit bus address and a single bit indicating that the operation is a read or a write. The configuration and fault status registers are accessible with a separate device type identifier of $1001_{[bin]}$. The bus address is defined by the state ('0' or '1') of the A0, A1 pins and A2 virtual address bit. The serial data stream must match the state of these pins.

WRITE

Writing to the configuration registers is illustrated in Figures 7. A start condition followed by the address byte is provided by the host; the SMT4214 responds with an acknowledge; the host then responds by sending the configuration register address pointer; the SMT4214 responds with an acknowledge; the host then clocks in the data. Only one configuration register can be written per data transfer. After the last byte is clocked in, a stop condition must be issued for the nonvolatile write operation to proceed. *The SMT4214 requires an I^2C read immediately after a successful write to prevent the generation of a high voltage pulse on the VGG_CAP pin. A start command will achieve the required result.*

READ

The address pointer for the registers can only be changed by a write command. If a read command is issued without address conditioning, the data that is clocked out will be from a location pointed to by the last written (or read) address incremented by 1.

In order to read data from a specific location a false write command is issued. The sequence is: issue a start and a device address with a write command; wait for an acknowledge; send the array or register address; wait for an acknowledge; issue a new start and device address with a read command; wait for an acknowledge then proceed to clock out data. For register reads, only a single location can be read with each command sequence. All read operations are concluded by issuing a stop condition. Refer to Figure 8 for an illustration of the read sequence.

MR#, PWR_ON# AND THE SERIAL INTERFACE

When reading the status registers, the state of the MR# input is ignored. When writing the configuration registers, MR# must be low and the PWR_ON# pin high.

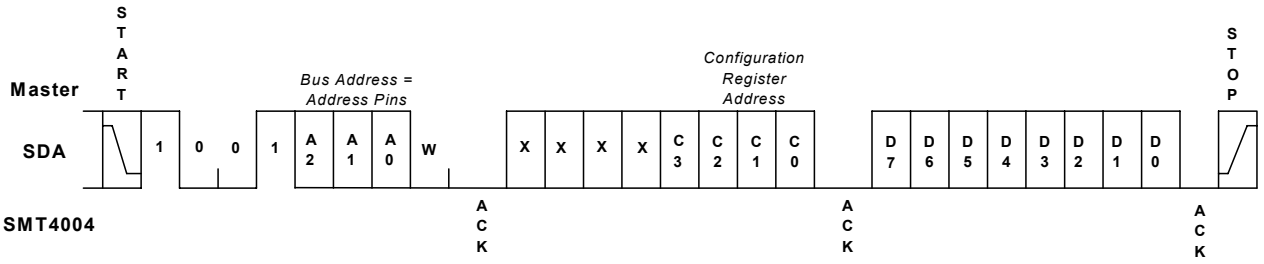


Figure 7. Write configuration register sequence.

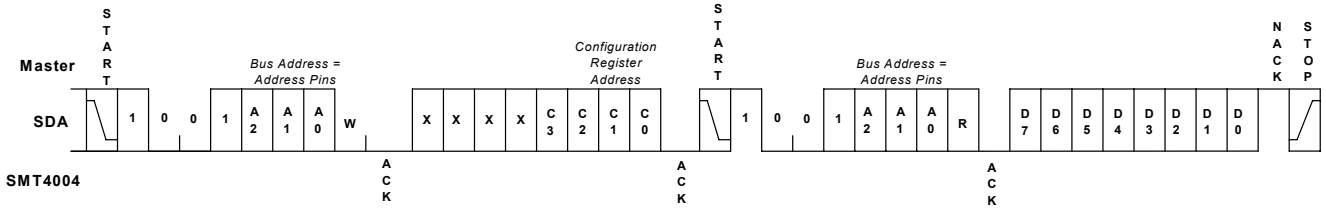


Figure 8. Read Configuration register or status register sequence.

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website (see below).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I2C serial bus format so that it can be directly downloaded to the SMT4214 via the programming Dongle and cable. An example of the connection interface is shown in Figure 9A and 9B.

When design prototyping is complete, the software can generate a HEX data file that should then be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

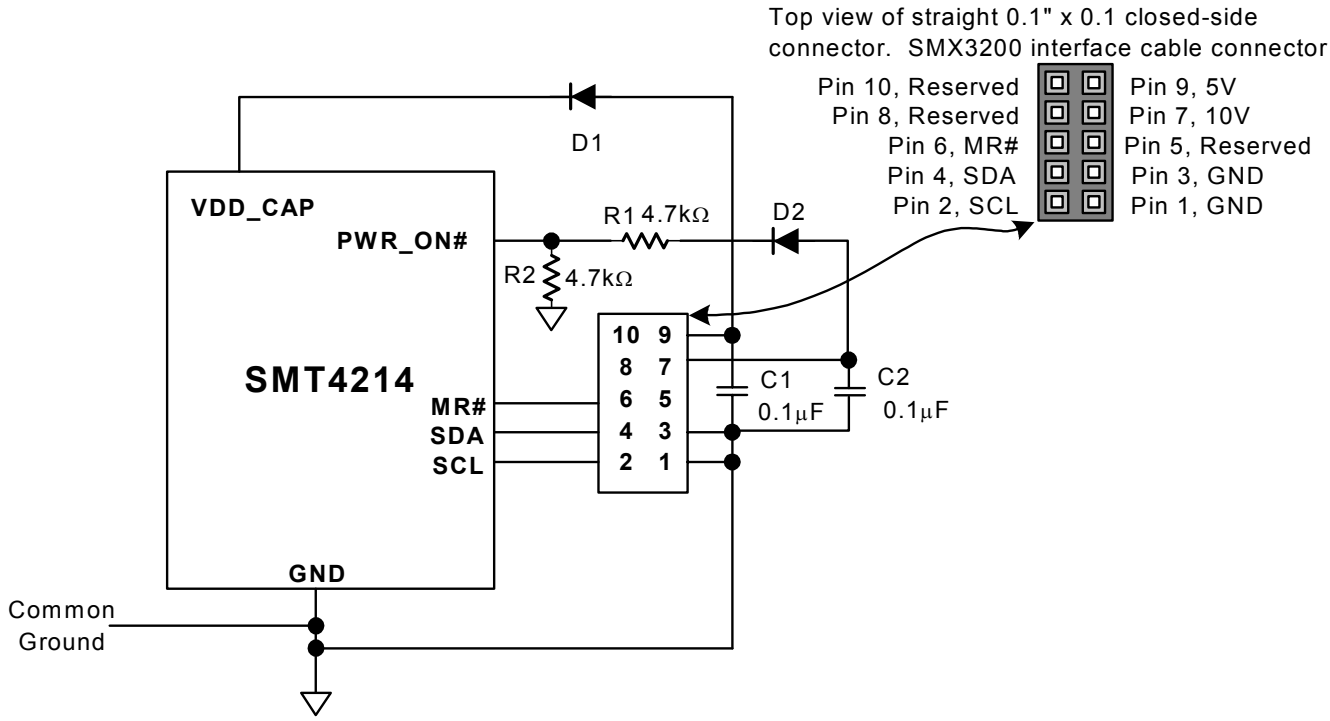


Figure 9A – SMX3200 Programmer and I²C serial bus connections to program the SMT4214. For the SMT4214, the PWR_ON# pin must be high in order to program the device. It can be done optionally through the SMX3200 programmer and R1/R2 or through an external control signal or switch. The SMX3200 should be disconnected after programming the part. If the PWR_ON# is hardwired to ground, this method will not work. Normally SDA and SCL signals require on board pull-up resistors, however, both the SMT4214 and the SMX3200 have internal pull-up resistors. D1 and D2 (1N4148) are needed between the Dongle Supplies and the VDD_CAP and PWR_ON# pins so that there will be no contention between the two supplies. C1 and C2 are for noise bypassing.

The latest revisions of all software and an application brief describing the SMX3200 is available from the website at:

http://www.summitmicro.com/tech_support/program_kit/SMX3200.htm

DEVELOPMENT HARDWARE & SOFTWARE (Cont.)

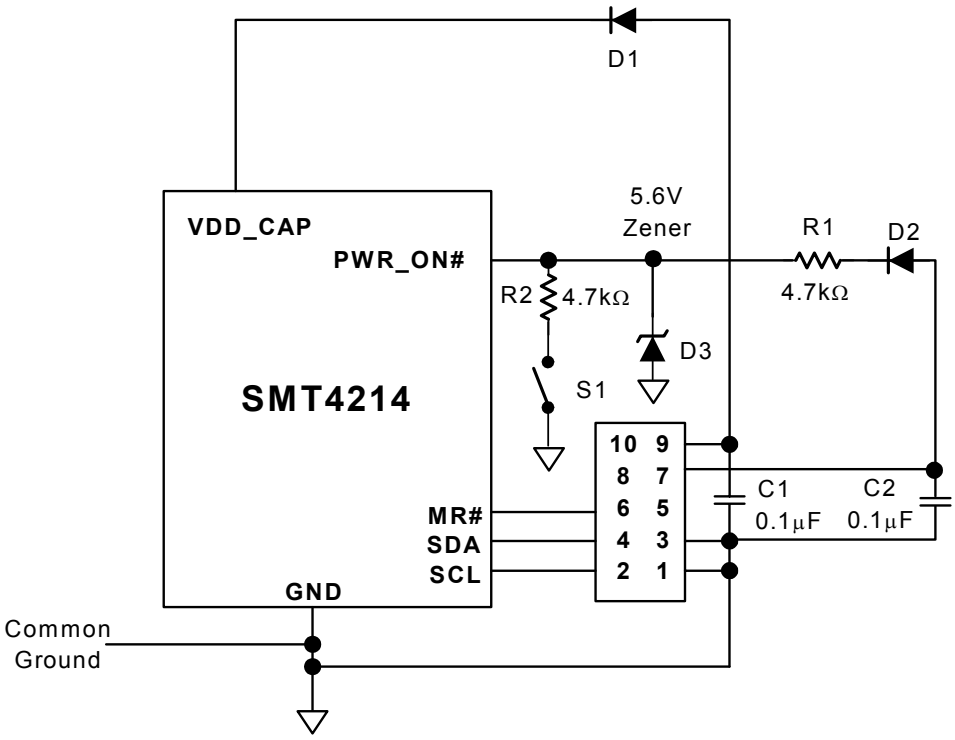


Figure 9B – An alternative connection between the SMX3200 Programmer and SMT4214 I^2C serial bus connections. Although this alternative requires additional components, it will work regardless of the position of the external PWR_ON# control signal or switch (S1). The zener diode (D3) provides further protection by clamping the output voltage at 5.6V.

APPLICATIONS INFORMATION

An example master/slave application circuit is shown in Figure 10A and 10B. Additional optional noise bypassing components are shown for the VIX and VOX pins. These components consist of ferrite bead inductors and capacitors. They may be necessary in very noisy systems where tight undervoltage tolerances are needed.

All unused channels must be programmed to soft-start mode. The thresholds for unused channels should be set to minimum, and the VO and VI inputs should be tied to the highest voltage VI input.

The VGATE output pins require series resistors to drive the gates of the power MOSFETs. Gate capacitors (C23 thru C30) are also recommended to prevent initial MOSFET turn-on during the SMT4214 power on sequence. To minimize transient power surges in hot-swappable line card designs, place a 0.01µF (10nF), 25V, ceramic capacitor on each VGATE output pin to ground.

The VGATE output level is programmable to either 10.5V or 14V depending on the type of MOSFET. To minimize the voltage drop across the MOSFET, it needs to be fully enhanced to minimize $RDS_{(ON)}$. However, some MOSFETs have maximum VGS specifications of 15V while others are 20V. For improved tracking performance with the SMT4214, it is recommended to use the lower rated VGS devices with the VGATE output levels set to 10.5V instead of 14V. The industry trend for power MOSFETs is toward lower VGS specs while also maintaining low $RDS_{(ON)}$ specifications.

APPLICATIONS INFORMATION (Cont.)

LAYOUT CONSIDERATIONS

When a power MOSFET is off, the trace from the supply to the VIX input of the SMT4214 carries very little current. As that MOSFET turns on the trace will carry more current possibly causing a voltage drop across the trace. If this voltage drop is severe, the VIX input will droop below the UV trip point and the supply will stay below the trip point even when the MOSFET is fully enhanced. Therefore, the internal ramp model of the SMT4214 will halt indefinitely. Subsequent higher voltage channels will also halt with the internal ramp model causing their corresponding VGATE outputs to halt. This leaves the MOSFETs on but not fully enhanced and therefore with higher rDS(ON) and more power dissipation. In order to prevent this situation it is recommended that the sense lines of the power supply be connected close to the power MOSFET as the power supply will then compensate for any voltage drop along the trace. The trace should also be designed to adequately handle the required current with minimal voltage drop.

The Tracking Time Limit feature in the Windows GUI should be enabled to prevent tracking from hanging-up and allowing the MOSFETs to get hot. Lowering the UV trip points will also solve the problem, but could leave the output voltages lower than expected.

APPLICATIONS INFORMATION (Cont.)

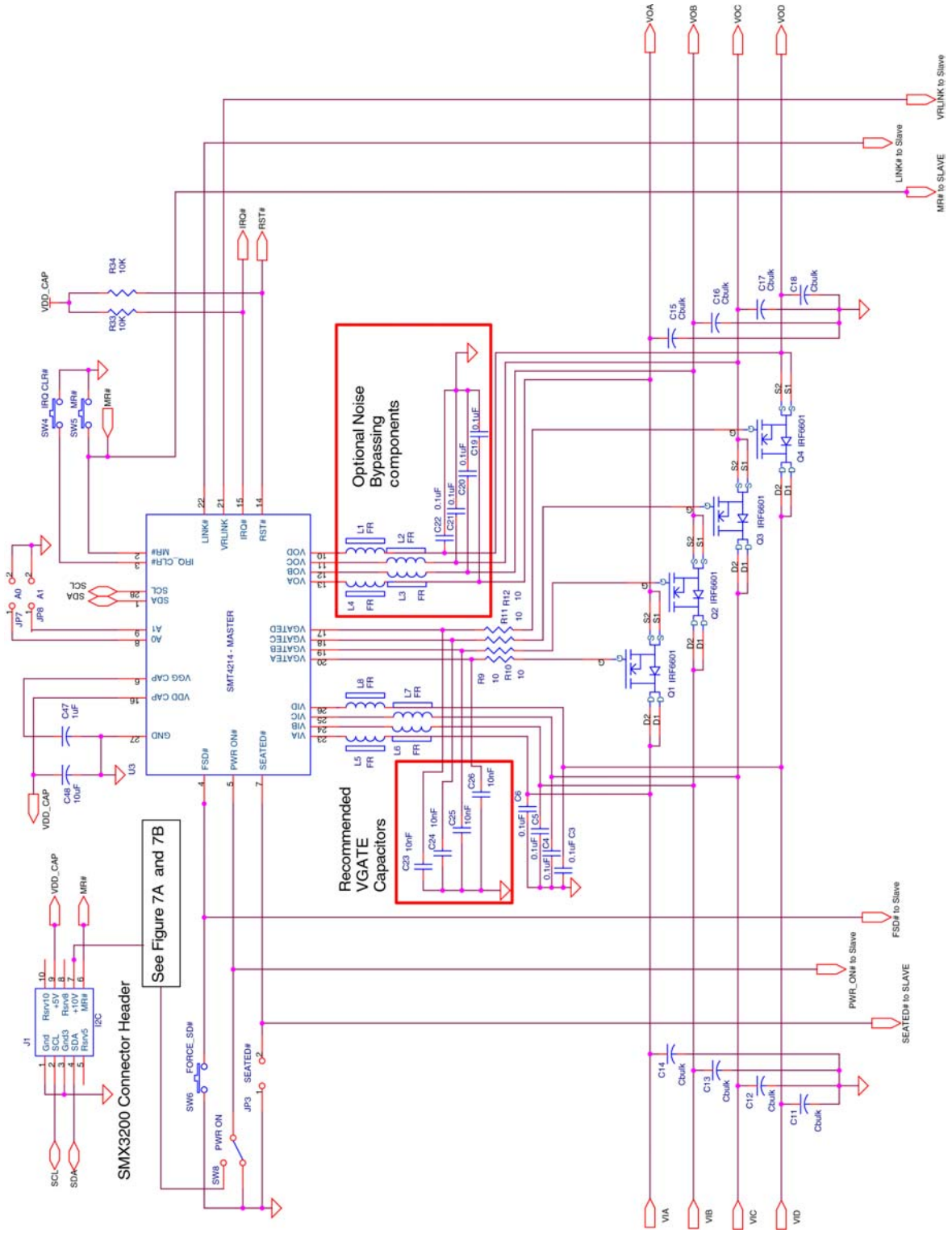


Figure 10A – Example application using two SMT4214s connected in a Master/Slave configuration. The Master is shown above, the Slave is shown in Figure 10B.

APPLICATIONS INFORMATION (cont.)

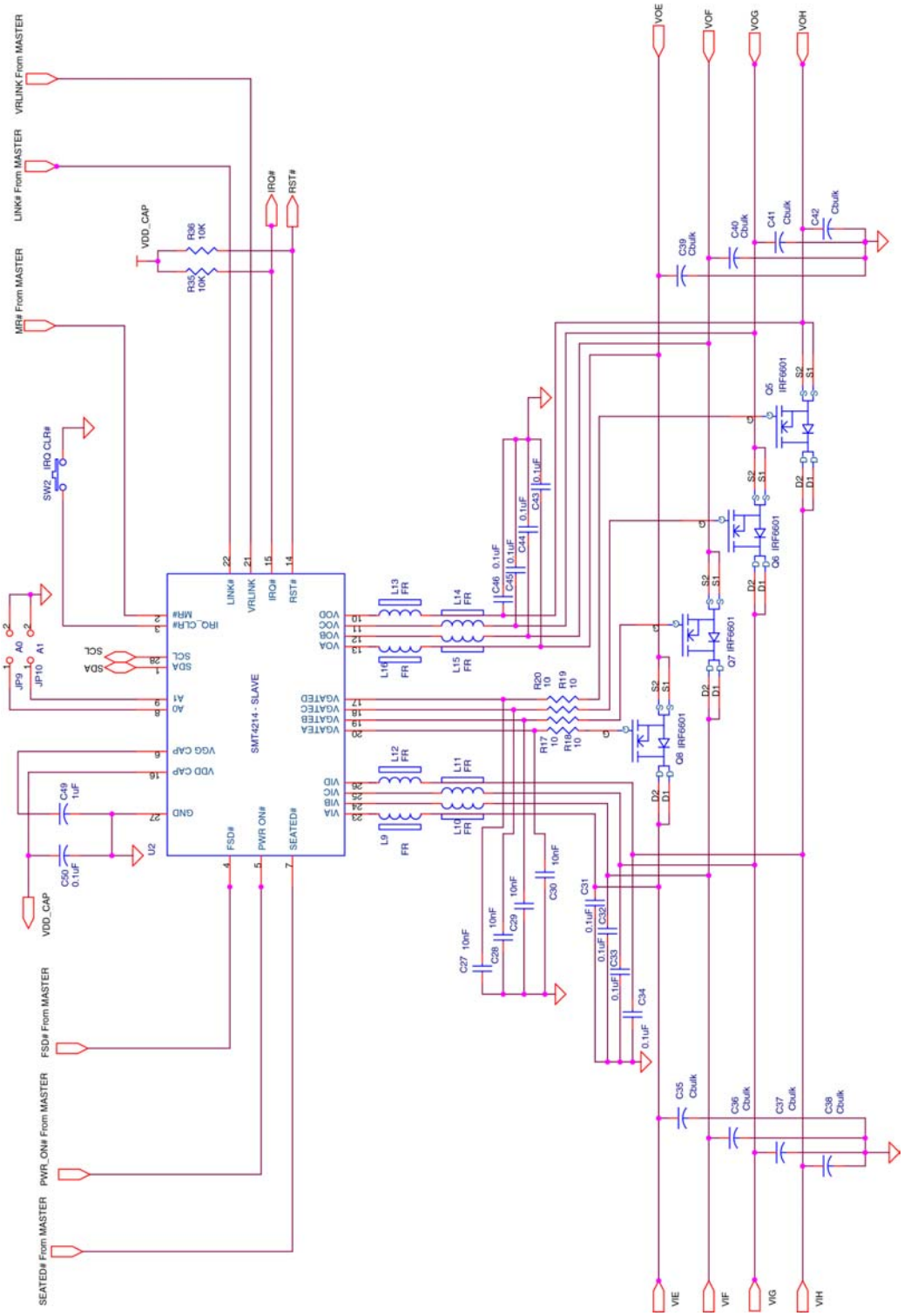


Figure 10B – Example application using two SMT4214s connected in a Master/Slave configuration. The Slave is shown above, the Master is shown in Figure 10A

DEFAULT CONFIGURATION REGISTER SETTINGS – SMT4214G-115

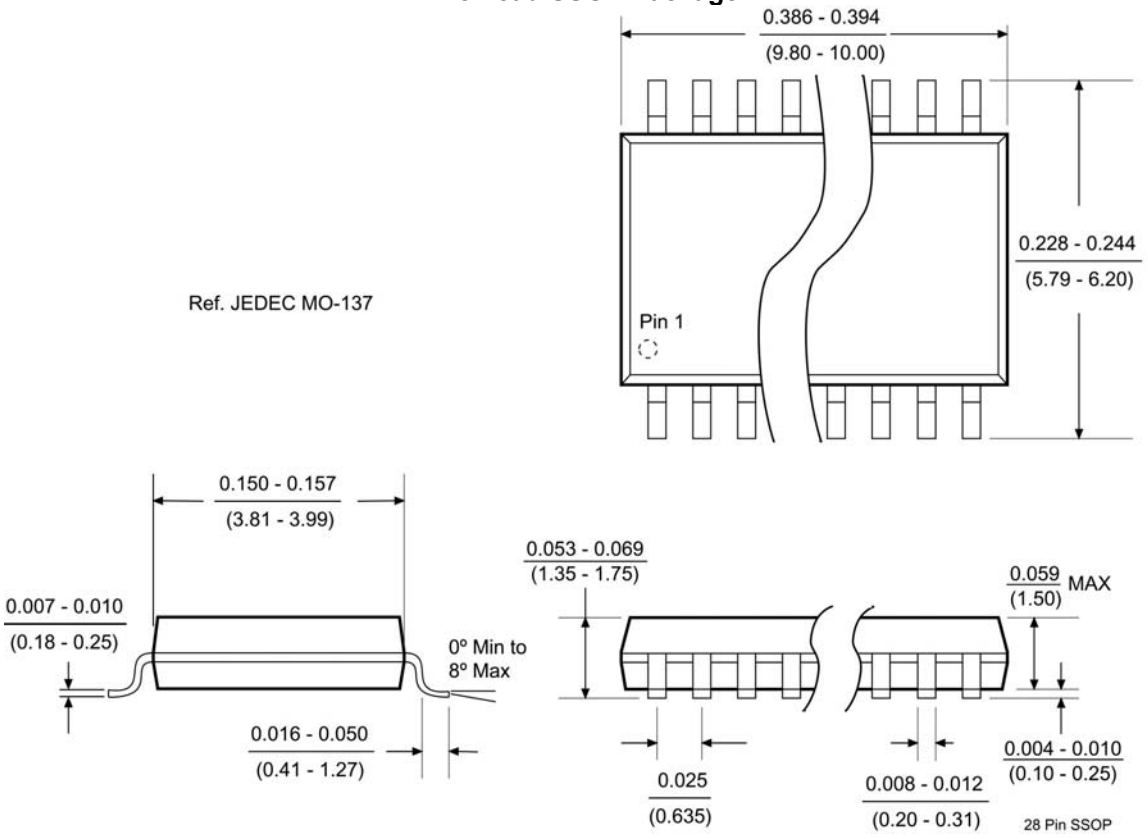
Register	Hex Contents	Configured as:
R00	B4	Channel A UV Trip Point = 4.5V
R01	69	Channel B UV Trip Point = 3.0V
R02	41	Channel C UV Trip Point = 2.2V
R03	28	Channel D UV Trip Point = 1.7V
R04	F1	Channel A,B,C, and D set to track Tracking time limit enabled RST# timeout interval set to 25ms Device set as Master
R05	21	VGATE output level = 10.5V UV cause RST# after tracking enabled UV cause IRQ# after tracking disabled Filter time = 0ms Virtual address A2 set to high UV does not cause a FS# after tracking is complete (steady state) UV does not cause a FS# at the end of tracking filter time interval
R06	00	Volatile register, all status bits are low

The default device ordering number is SMT4214G-115. It is programmed with the register contents as shown above and tested over the commercial temperature range.

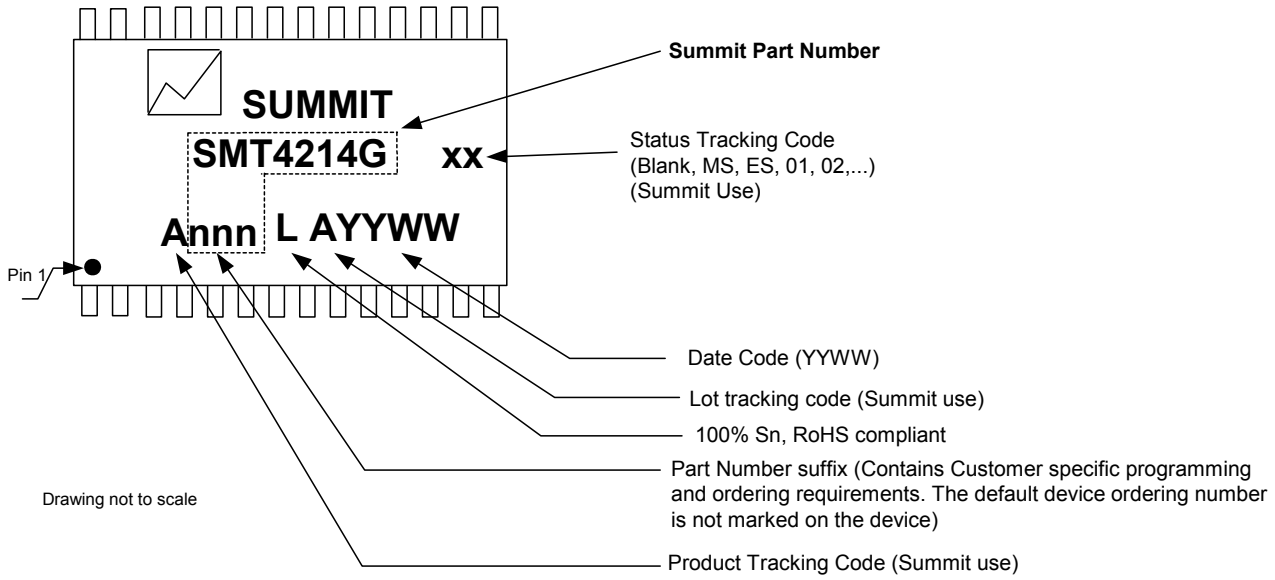
Application Note 28 contains a complete description of the Windows GUI and the default settings of each of the 6 individual Configuration Registers.

PACKAGE

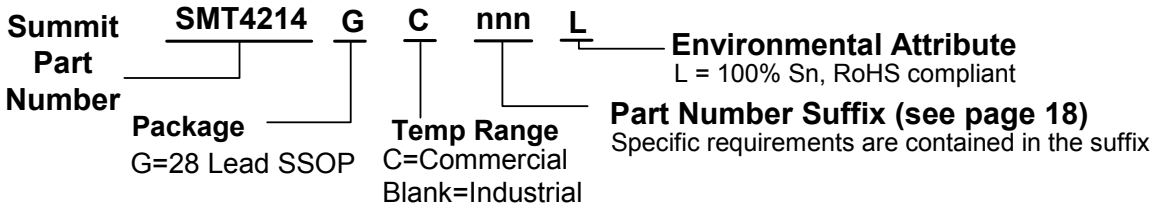
28 Lead SSOP Package



PART MARKING



ORDERING INFORMATION



NOTICE

NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

Revision 2.2 - This document supersedes all previous versions. . Data Sheet updates can be accessed by "right" or "left" mouse clicking on the link: http://www.summitmicro.com/prod_select/summary/smt4214.htm

Device Errata sheets can be accessed by "right" or "left" mouse clicking on the link: http://www.summitmicro.com/errata/SMT4214