SRS TruSurround HD/HD4 Decoder

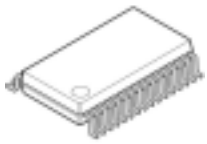
■ General Description

The NJU26040-09D is a digital audio signal processor that provides the function of TruSurround HD/HD4 + FOCUS and WOW HD.

The NJU26040-09D processes all sound sources, such as DVD multi channel signals, CD, AM/FM radio, and TV sound into spacious sound of natural virtual surround by TruSurround HD/HD4 + FOCUS and WOW HD.

The applications of NJU26040-09D are suitable for front multi-channel and stereo outputs products such as DVD Receivers, AV Amplifiers, TV, radio-cassettes player, Car Audio or ordinary audio products such as small speakers system.

■ Package



NJU26040V-09D

■ FEATURES

- Software

- Front Multi channel outputs by SRS TruSurround HD/HD4 technology
- WOW HD technology is offered to the stereo I/O product.
- LFE by SRS TruBass-II technology
- SRS FOCUS technology (FOCUS is possible to use with TruSurround HD/HD4.)
- SRS Definition technology improves the perception of clarity and acoustic space
- Dialog Clarity technology
- Support mono ~ 5.1ch input, 2.0 ~ 5.1ch output.

- Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency : 38MHz Max.
- Digital Audio Interface : 3 Input ports / 3 Output ports
- Power Supply : 3.3V (Input : 5V tolerant)
- Package : SSOP32 (Pb-Free)
- Micro computer interface : I^2C bus (standard-mode/100kbps, fast-mode/400kbps), 4-Wire Serial Bus (4-Wire: clock, enable, input data, output data)

The detail hardware specification is described in the “NJU26040 Series Hardware Data Sheet”.

■ DSP Block Diagram

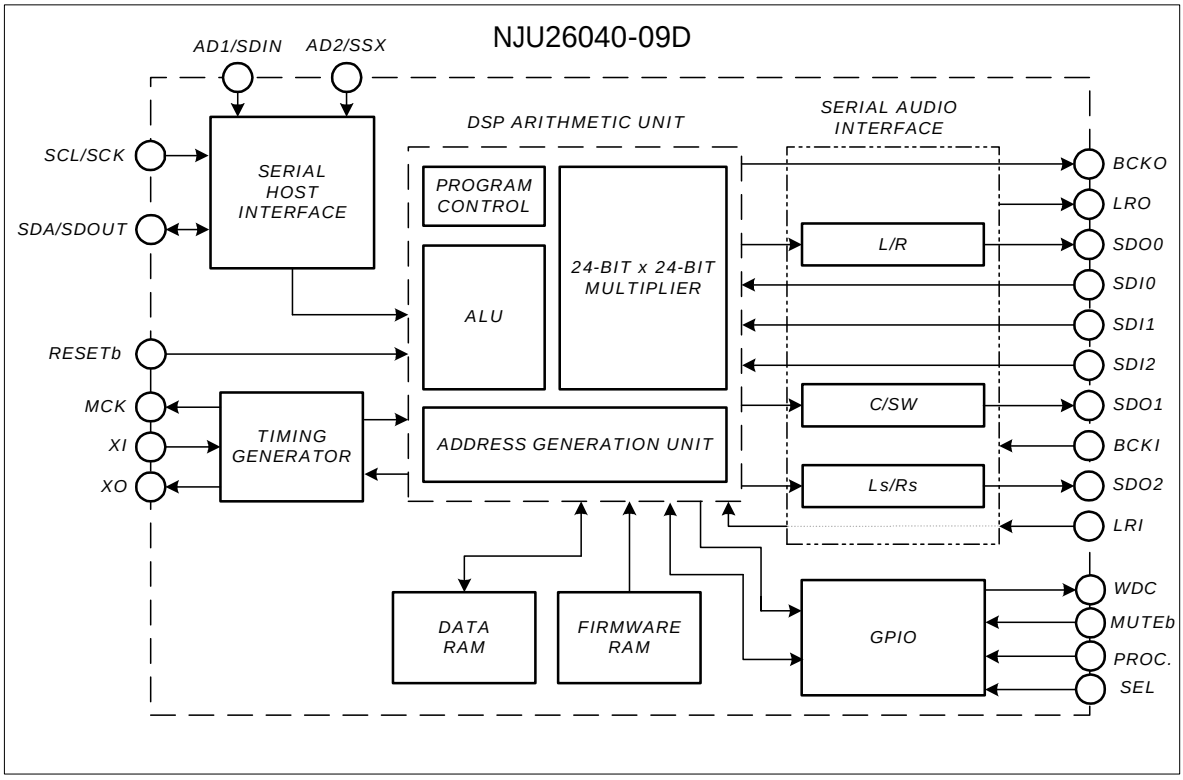


Fig.1-1 NJU26040-09D Block Diagram

■ TruSurround HD/HD4 Decoder

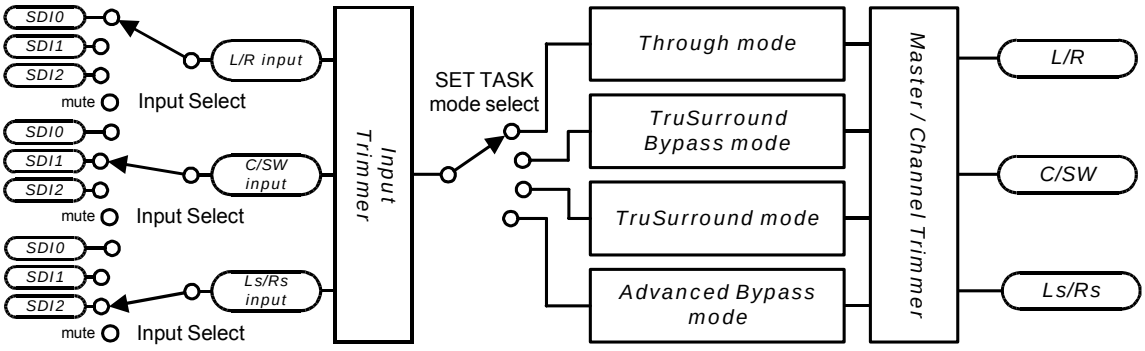
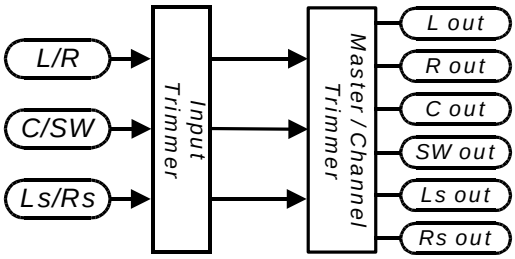
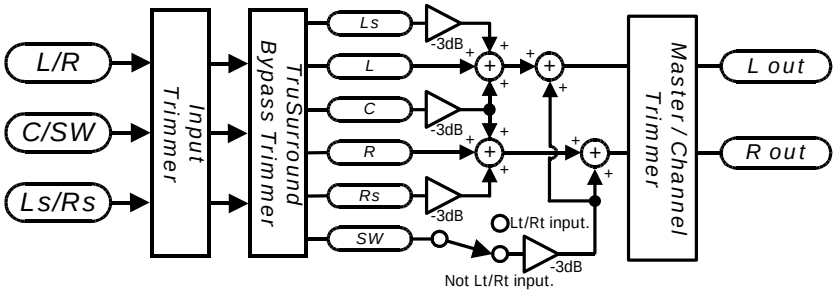


Fig.1-2 NJU26040-09D Top Level Function Diagram



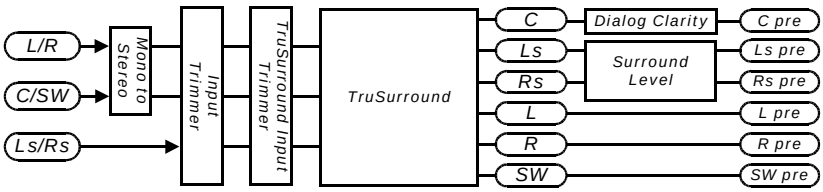
Through mode Block Diagram

Fig.1-3a NJU26040-09D Function Diagram

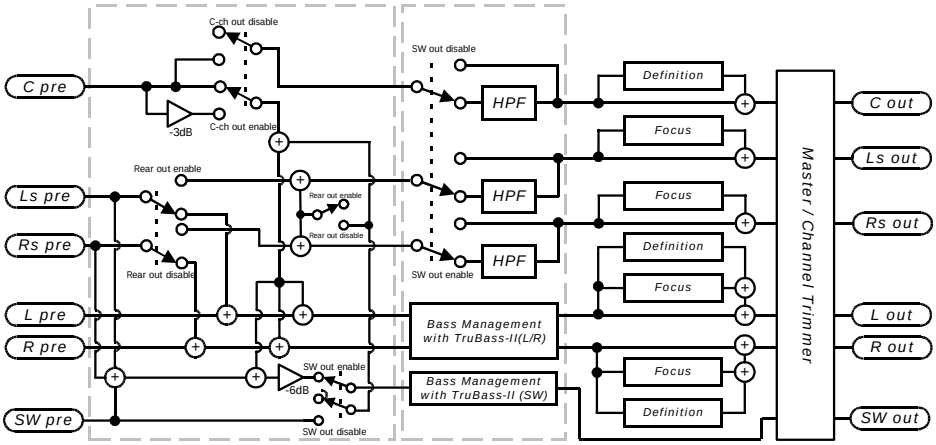


TruSurround Bypass mode Block Diagram

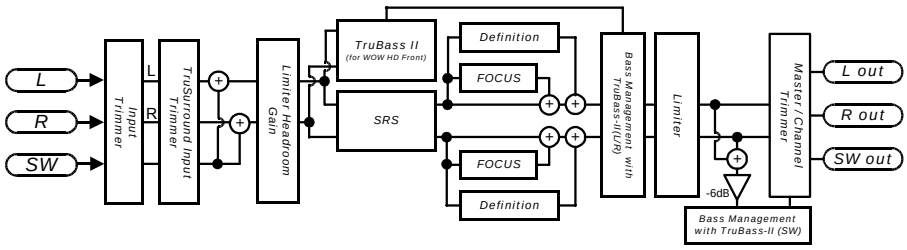
Fig.1-3b NJU26040-09D Function Diagram



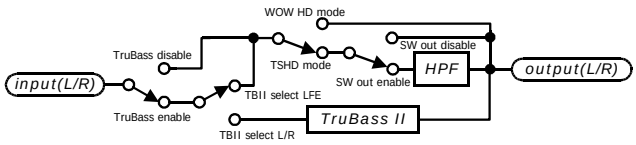
TruSurround mode Block Diagram (TruSurround mode)



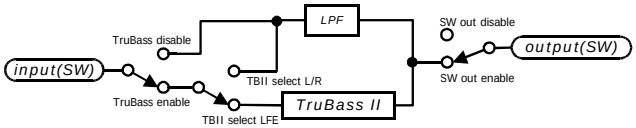
TruSurround mode Block Diagram (TruSurround mode)



TruSurround mode Block Diagram (WOW HD mode)

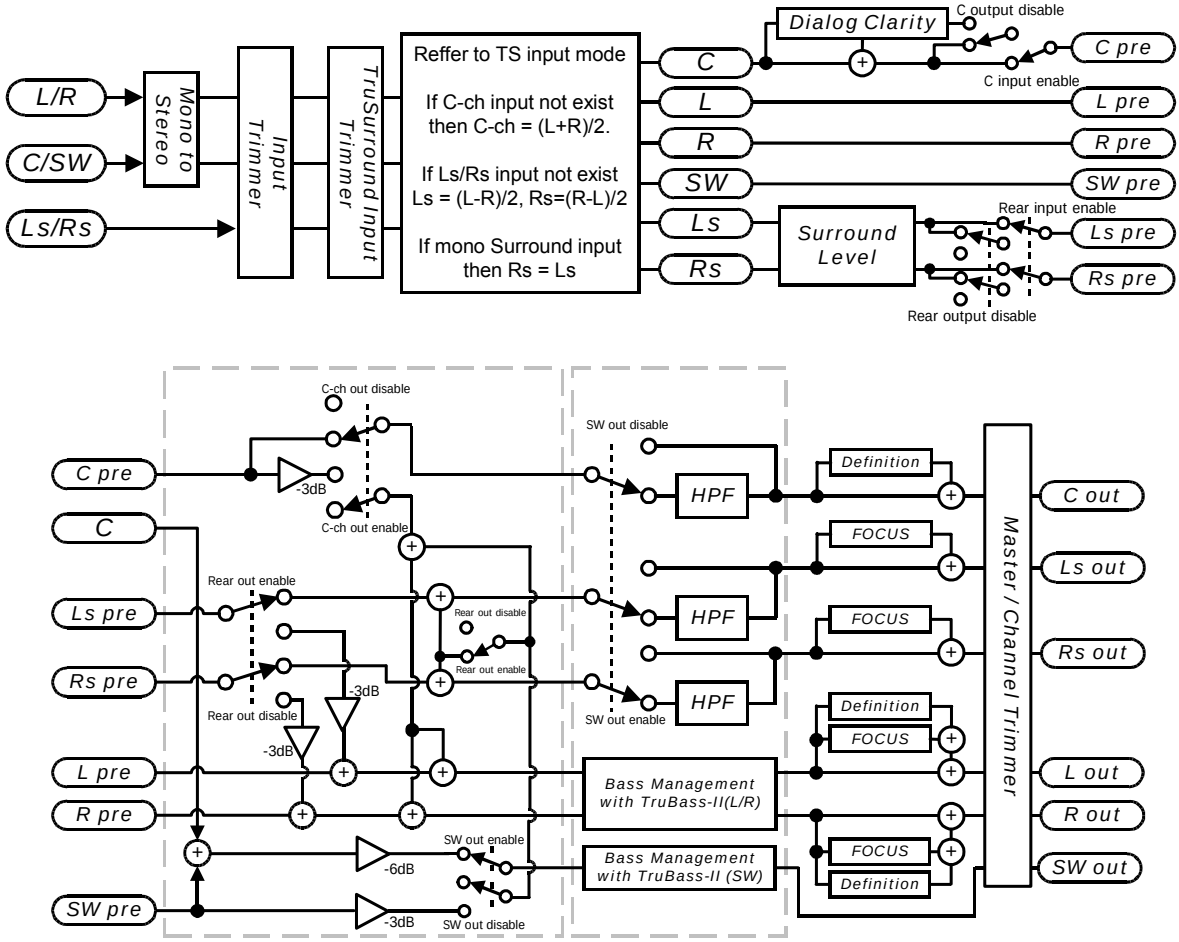


Front(L/R) Bass Management



LFE(SW) Bass Management

Fig.1-3c NJU26040-09D Function Diagram



Advanced Bypass mode Block Diagram

Fig.1-3d NJU26040-09D Function Diagram

■ Pin Configuration

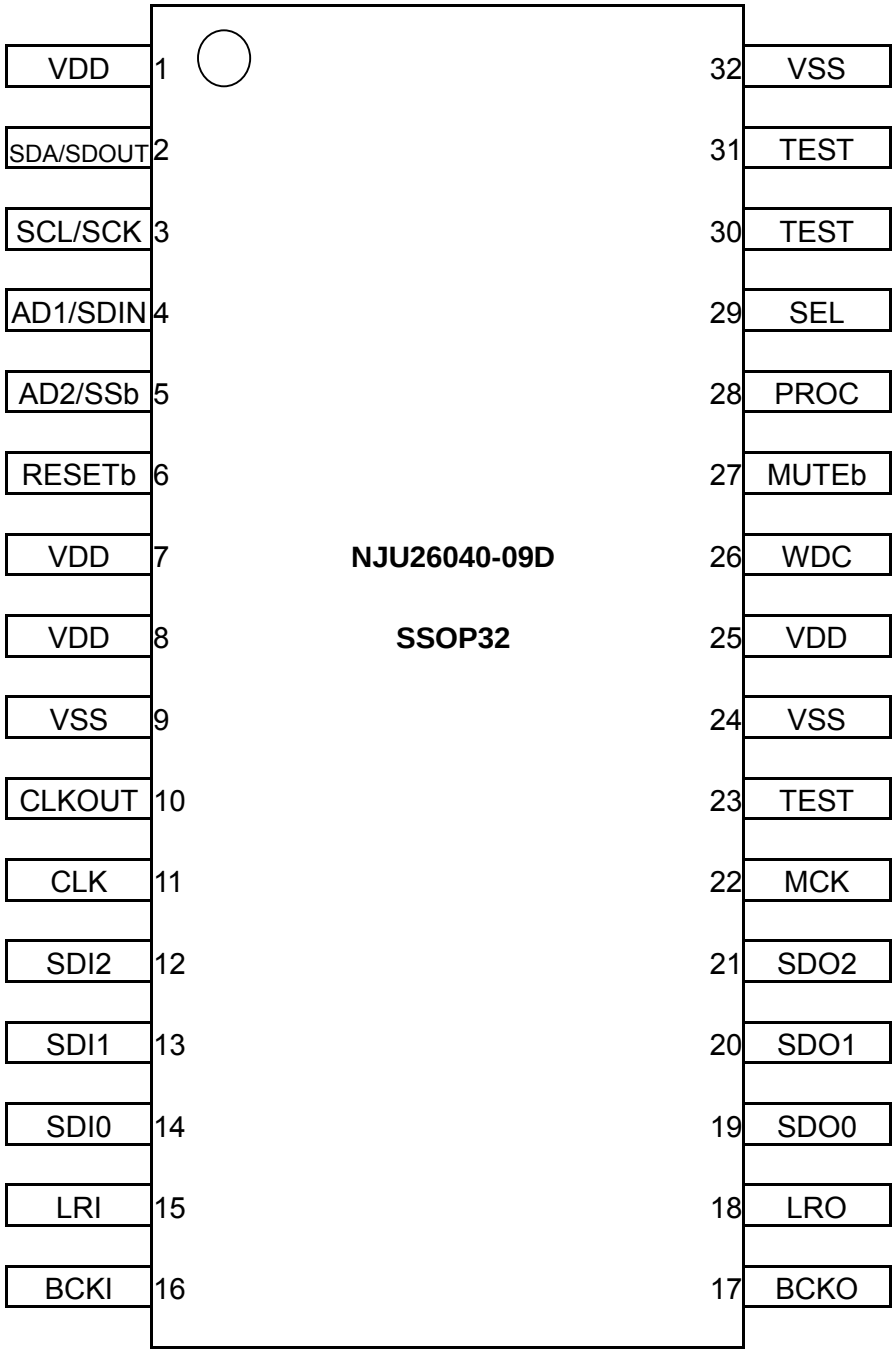


Fig.1-4 NJU26040-09D Pin Configuration

■ Pin Description

Table 1. Pin Description

Pin No.	Symbol	I/O	Description
1, 7, 8, 25	VDD	-	Power Supply +3.3V
2	SDA/SDOUT	OD	I^2C I/O / 4-Wire Serial Output This pin requires a pull-up resistance in both I^2C bus and 4-Wire serial mode.
3	SCL/SCK	I	I^2C clock / Serial clock
4	AD1/SDIN	I	I^2C Address / Serial In
5	AD2/SSb	I	I^2C Address / Serial Enable
6	RESETb	I	Reset (RESETb='Low' : DSP Reset)
9, 24, 32	VSS	-	GND
10	CLKOUT	O	OSC Output
11	CLK	I	OSC Clock Input
12	SDI2	I	Audio Data Input 2
13	SDI1	I	Audio Data Input 1
14	SDI0	I	Audio Data Input 0
15	LRI	I	LR Clock Input
16	BCKI	I	Bit Clock Input
17	BCKO	O	Bit clock Output
18	LRO	O	LR clock Output
19	SDO0	O	Audio Data Output 0 (L/R)
20	SDO1	O	Audio Data Output 1 (C/SW)
21	SDO2	O	Audio Data Output 2 (Ls/Rs)
22	MCK	O	Master Clock Output for A/D, D/A
23, 30, 31	TEST	I-	for Test (connected to VSS)
26	WDC	OD	Watchdog clock output (open drain output)
27	MUTEb	I	Master Volume level, After Reset DSP ("1" : 0dB "0" : Mute)
28	PROC	I	After Reset DSP. ("1" : Normal "0" : Wait from Command)
29	SEL	I	Select I^2C or Serial bus ('1' : Serial / '0' : I^2C-Bus)

Note : I : Input
I - : Input (Pull-down)
O : Output
OD : Bi-directional (Open Drain) This pin requires a pull-up resistance.
I/O+ : Bi-directional (with Pull-up resistance)
I/O - : Bi-directional (with Pull-down resistance)

■ Digital Audio Interface

The NJU26040-09D audio interface provides industry standard serial data formats of I^2S, MSB-first left-justified or MSB-first right-justified. The NJU26040-09D audio interface provides three data input, SDI0, SDI1, SDI2 and three data outputs, SDO0, SDO1, SDO2 as shown in table 2, table 3 and Fig.2. An audio interface input and output data format become the same data format.

Table 2. Serial Audio Input Pin

Pin No.	Symbol	Description
14	SDI0	Audio Data Input 0 (L/R, C/SW, Ls/Rs are selected by the command.)
13	SDI1	Audio Data Input 1 (L/R, C/SW, Ls/Rs are selected by the command.)
12	SDI2	Audio Data Input 2 (L/R, C/SW, Ls/Rs are selected by the command.)

Table 3. Serial Audio Output Pin

Pin No.	Symbol	Description
19	SDO0	Audio Data Output 0 L / R
20	SDO1	Audio Data Output 1 C / SW
21	SDO2	Audio Data Output 2 Ls / Rs

■ Host Interface

The NJU26040-09D can be controlled via Serial Host Interface (SHI) using either of two serial bus formats: I^2C bus or 4-Wire serial bus.(Table 4) Data transfers are in 8 bit packets (1 byte) when using either format.

Serial Host Interface Pin Description.(Table 5)

Table 4. Serial Host Interface Pin Description

Pin No.	Symbol	Setting	Host Interface
29	SEL	"Low"	I^2C bus
		"High"	4-Wire serial bus

Table 5. Serial Host Interface Pin Description

Pin No.	Symbol (I^2C bus / Serial)	I^2C bus Format	4-Wire Serial bus Format
2	SDA / SDOUT *	Serial Data Input/Output (Open Drain Input/Output)	Serial Data Output (Open-Drain Output)
3	SCL / SCK *	Serial Clock	Serial Clock
4	AD1 / SDIN *	I^2C bus address Bit1	Serial Data Input
5	AD2 / SSb *	I^2C bus address Bit2	Serial enable

Note : SDA /SDOUT pin is a bi-directional open drain.
This pin requires a pull-up resistance in both I^2C bus and 4-Wire serial mode.
* When the power supply (V_{DD}= +3.3V) is supplied to NJU26040, these pins become +5.0V Input tolerant.

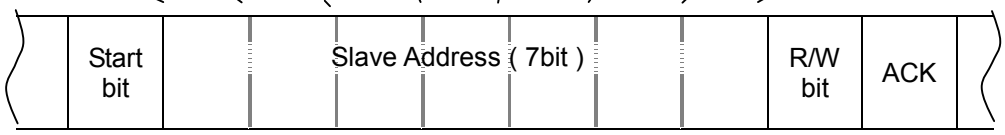
■ I²C bus

When the NJU26040-09D is configured for I²C bus communication during the Reset initialization sequence. I²C bus interface transfers data to the SDA pin and clocks data to the SCL pin.

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26040-09A. The AD1 and AD2 pins can arbitrarily set up an address. The I²C address of AD1/AD2 is decided by connection of AD1/AD2 pins.

Table 6. I²C bus SLAVE Address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	



* SLAVE address is 0 when AD1/2 is “Low”. SLAVE address is 1 when AD1/2 is “High”.

Note : In case of the NJU26040-09D only single-byte transmission is available. The serial host interface supports “Standard-Mode (100kbps)” and “Fast-Mode (400kbps)” I²C bus data transfer.

■ 4-Wire Serial Interface

SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the Slave Select pin Low (SSb=0). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSb.

SDOUT is Hi-Z in case of SSb = “High”. SDOUT is Open-drain output in case of SSb = “Low”. SDOUT needs a pull-up resistor when SDOUT is Hi-Z.

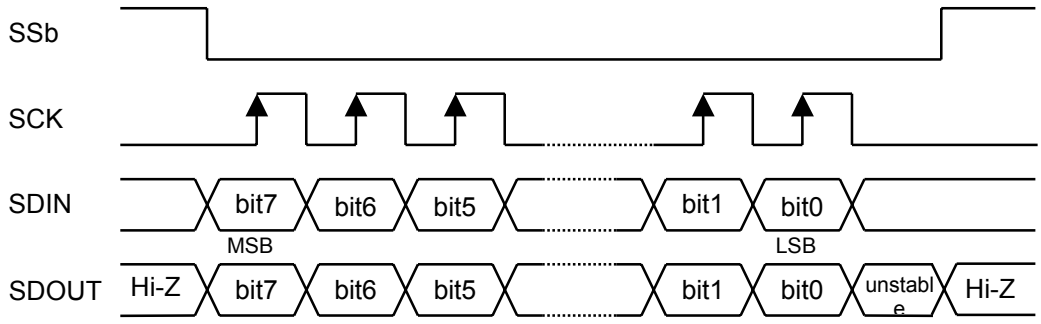


Fig. 4 4-Wire Serial Interface Timing

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb=”High”. When the data-clock is more than 8 clocks, the last 8 bit data becomes valid. After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes “High”.

■ Pin setting

The NJU26040-09D operates default command setting after resetting the NJU26040-09D. In addition, the NJU26040-09D restricts operation at power on by setting PROC pin and MUTEb pin (Table 7). These pins are input pin. However, these pins operate as bi-directional pins. Connect with VDD or VSS through 3.3kΩ resistance.

Table 7. Pin setting

Pin No.	Symbol	Setting	Function
28	PROC	"High"	The NJU26040-09D operates default setting after reset.
		"Low"	The NJU26040-09D does not operate after reset. Sending start command is required for starting operation.
27	MUTEb	"High"	Master volume is set 0dB after reset.
		"Low"	Master volume is set mute after reset.

■ WatchDog Clock

The NJU26040-09D outputs clock pulse through WDC (No.26) pin during normal operation. (Table 8)

Table 8. WatchDog Clock Output Cycle

WDC Output Cycle (Low/High) Time
85ms

The NJU26040-09D generates a clock pulse through the WDC terminal after resetting the NJU26040-09D. The WDC clock is useful to check the status of the NJU26040-09D operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26040-09D. When the WDC clock pulse is lost or not normal clock cycle, the NJU26040-09D does not operate correctly. Then reset the NJU26040-09D and set up the NJU26040-09D again.

Note : If input and output of an audio signal stop and an audio interface stops, WDC can't output. That is because it has controlled based on the signal of an audio interface.

■ NJU26040-09D Command Table

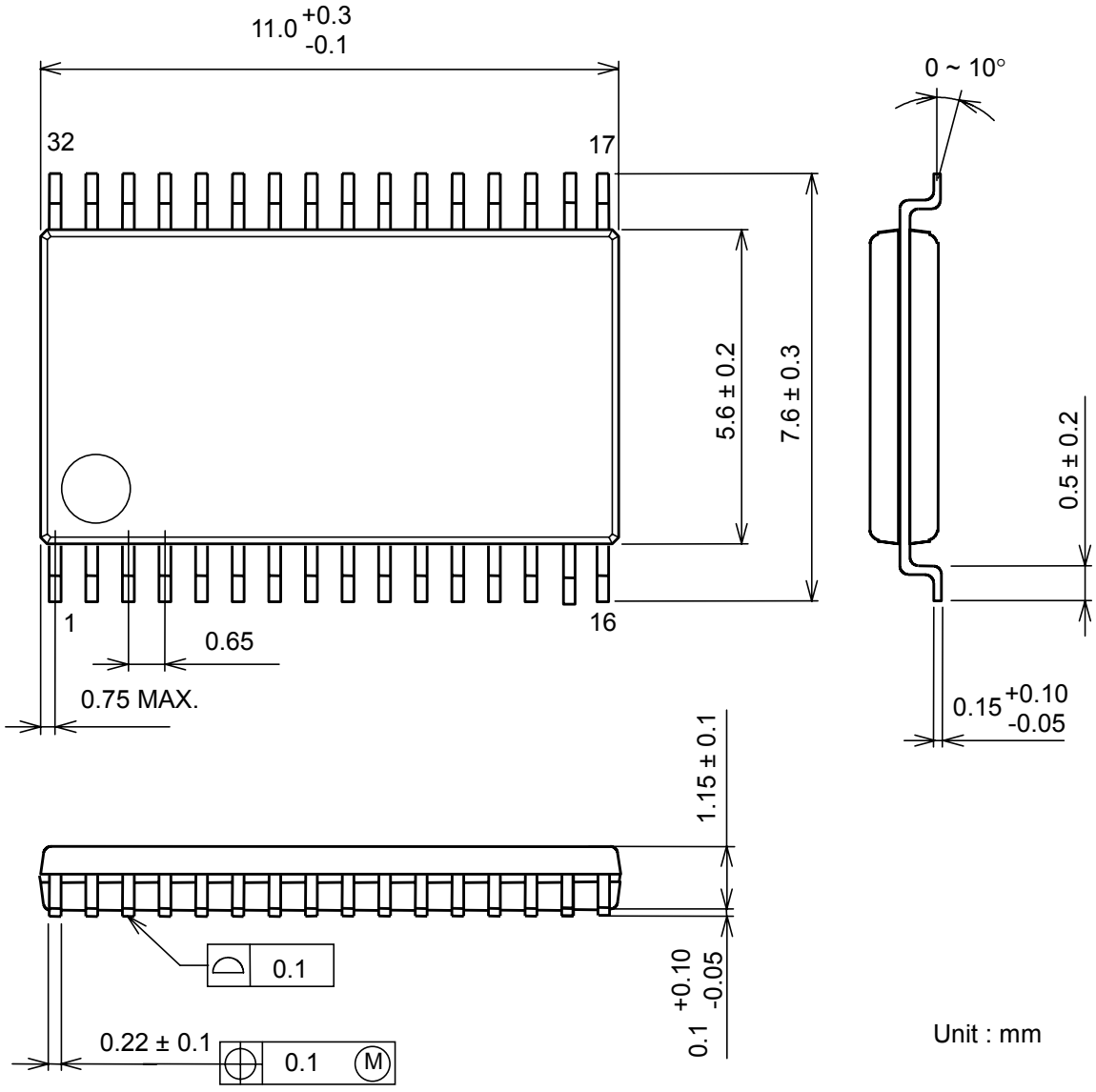
Table 9. NJU26040-09D Command

No.	Command
1	SET_TASK_CMD
2	AUDIO_FORMAT_CMD
3	SYSTEM_STATE_CMD
4	SAMPRATE_CMD
5	INPUT_SELECT_CMD
6	TSHD_INPUT_MODE_CMD
7	TSHD_OUTPUT_MODE_CMD
8	DF_SELECT_CMD
9	TB2_SETUP_CMD
10	SW_CROSSOVER_FREQ_CMD
11	SRS3D_SETUP_CMD
12	INPUT_TRIM_CMD
13	MASTER_TRIM_CMD
14	LEFT_TRIM_CMD
15	RIGHT_TRIM_CMD
16	CENTER_TRIM_CMD
17	SUBWOOFER_TRIM_CMD
18	LEFT_SRND_TRIM_CMD

No.	Command
19	RIGHT_SRND_TRIM_CMD
20	TSHD_INPUT_TRIM_CMD
21	TSHD_BYPASS_TRIM_CMD
22	TSHD_SRND_LEVEL_CMD
23	DC_CNTRL_CMD
24	FC_FRONT_CNTRL_CMD
25	FC_REAR_CNTRL_CMD
26	TB2_FRONT_CNTRL_CMD
27	TB2_LFE_CNTRL_CMD
28	DF_FRONT_CNTRL_CMD
29	DF_CENTER_CNTRL_CMD
30	SRS3D_SPACE_CNTRL_CMD
31	SRS3D_CENTER_CNTRL_CMD
32	LIMITER_CMD
33	SOFT_RESET_CMD
34	WDC_TEST_CMD
35	START_CMD

Notes : In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (SRS Labs. Inc.) is required.

■ **NJU26040-09D Package Dimensions (SSOP32, Pb-Free)**



Unit : mm

■ License Information

The "TruSurround HD", "TruSurround HD4", “WOW HD”, "Dialog Clarity", "FOCUS" and "TruBass" technology rights incorporated in the NJU26040-09D are owned by SRS Labs, a U.S. Corporation and licensed to New Japan Radio Co., Ltd.. Purchaser of NJU26040-09D must sign a license for use of the chip and display of the SRS Labs trademarks. Any products incorporating the NJU26040-09D must be sent to SRS Labs for review. "TruSurround HD", "TruSurround HD4", “WOW HD”, "Dialog Clarity", "FOCUS" and "TruBass" is protected under US and foreign patents issued and/or pending. "TruSurround HD", "TruSurround HD4", “WOW HD”, "Dialog Clarity", "FOCUS", "TruBass", SRS and  symbol are trademarks of SRS Labs, Inc. in the United States and selected foreign countries. Neither the purchase of the NJU26040-09D, nor the corresponding sale of audio enhancement equipment conveys the right to sell commercialized recordings made with any SRS technology. SRS Labs requires all set makers to comply with all rules and regulations as outlined in the SRS Trademark Usage Manual separately provided.

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